Physics 311 Sequential Logic

1. Design and build an RS latch using NAND Gates.
    a. Draw the circuit diagram.
    b. Create the truth table and verify the output for different inputs by measuring the output voltage with the digital DMM.

2. Now add two more NAND Gates and create a "gated" RS latch. The circuit should display the following behavior: If "Enable" is "HIGH" it should work as RS latch. If "ENABLE" is "LOW" it should ignore the inputs. Measure the output voltage.

3. Using the SN7490 counter build the circuit as shown below. On the input, add a signal by connecting the function generator or the oscillator that you built in 3. Make sure the voltage is not more than 5 V. Observe the output waveform and compare input and output signal. What type of counter is this circuit? A divide by 5 counter or divide by eight counter or divide by 10 counter? Record the waveform with open choice desktop and put it into your report.