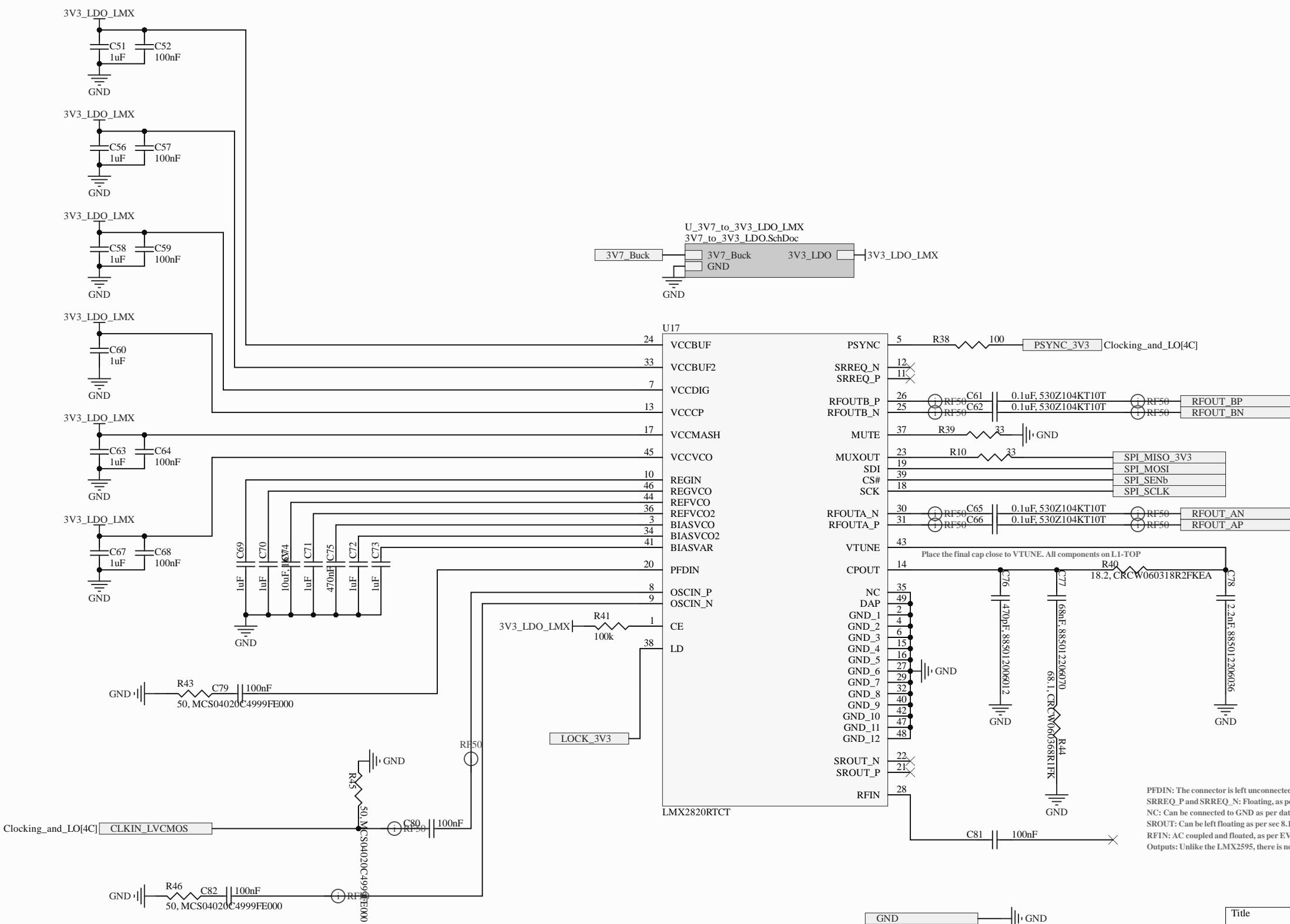


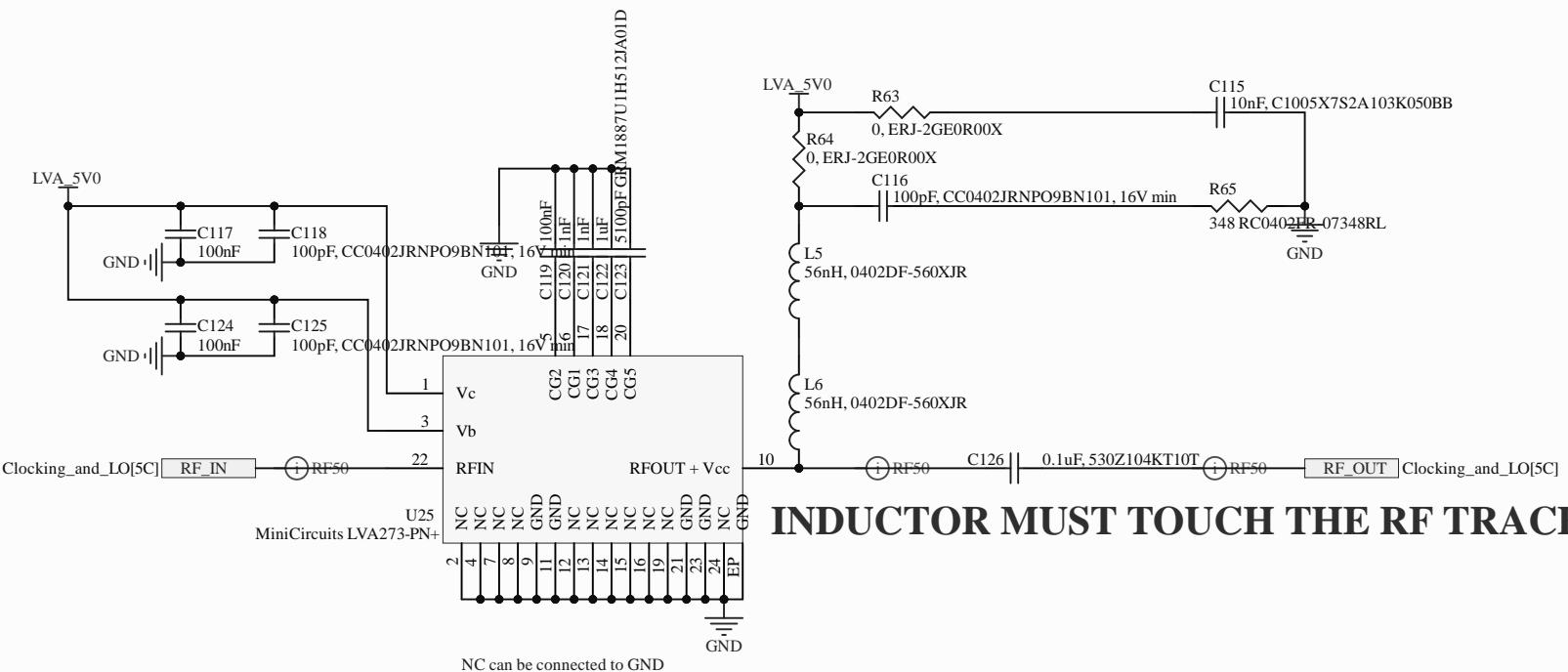
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File:	C:\Users\.\Clocking_and_LO.SchDoc	Drawn By:



PFDIN: The connector is left unconnected in the EVM general use-case. Use the 0.1uF cap and 50ohm Res as per EVM schematic
SRREQ_P and SRREQ_N: Floating, as per sec 8.1.1 of the datasheet
NC: Can be connected to GND as per datasheet and EVM schematic
SROUT: Can be left floating as per sec 8.1.1 of the datasheet
RFIN: AC coupled and floated, as per EVM schematic
Outputs: Unlike the LMX2595, there is no external pullup required

Title		
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Date:	2/18/2025	Sheet of
File:	C:\Users\.\LMX2820.SchDoc	Drawn By:

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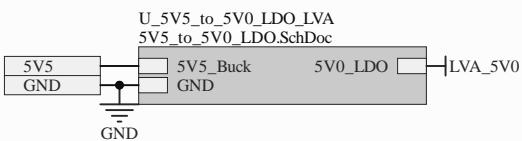
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Revision

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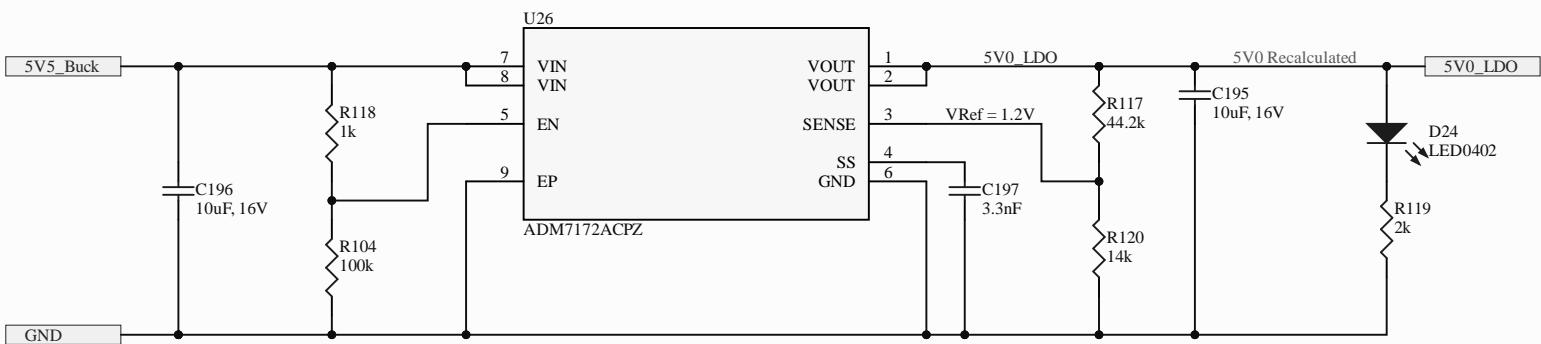
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Date: 2/18/2025 Sheet of

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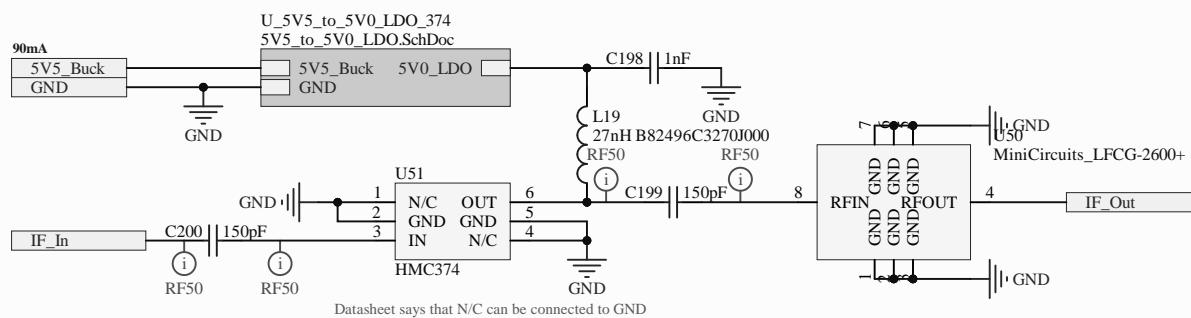
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Date: 2/18/2025

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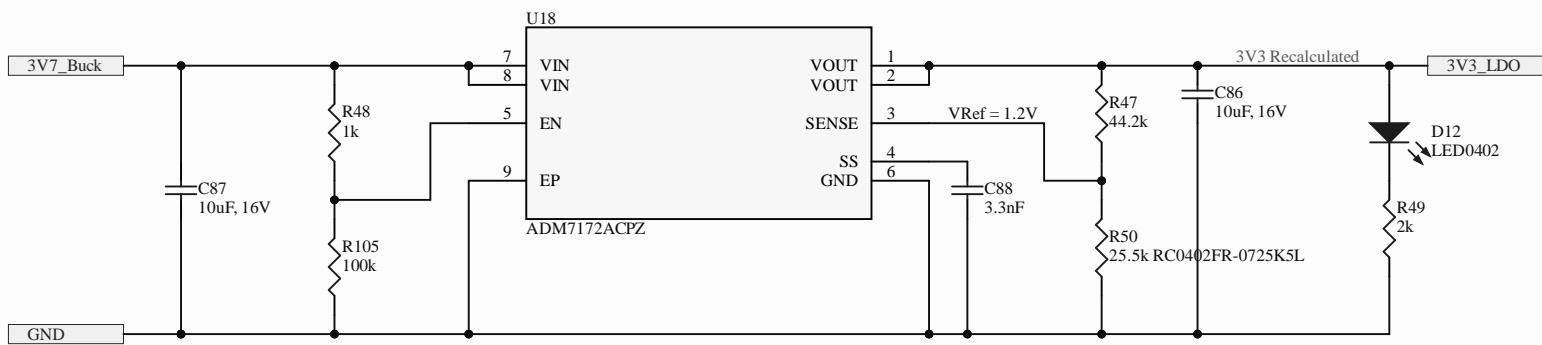
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Title

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A

Number

Revision

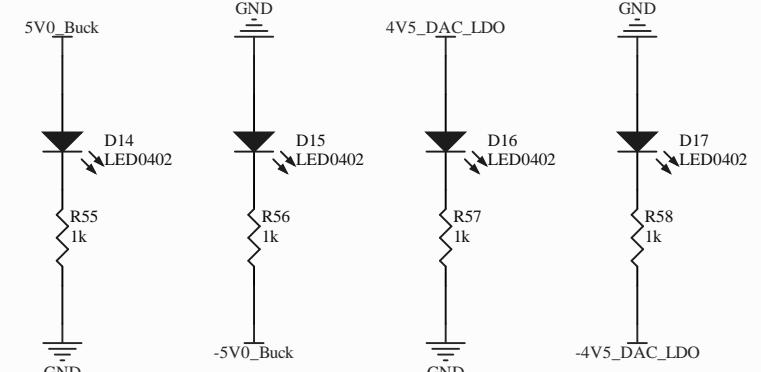
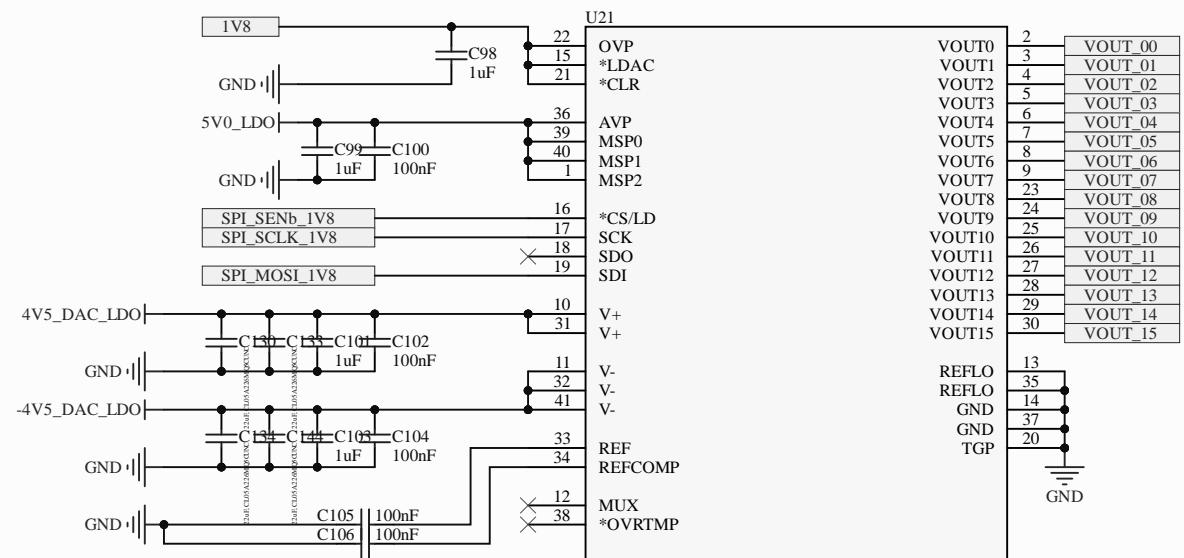
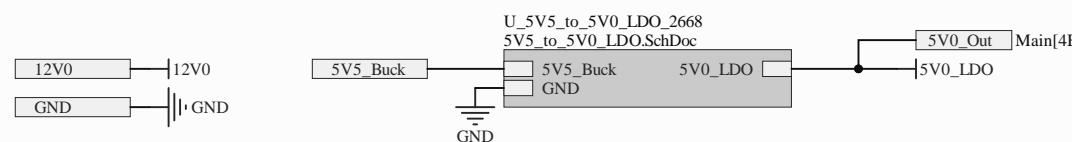
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2/18/2025

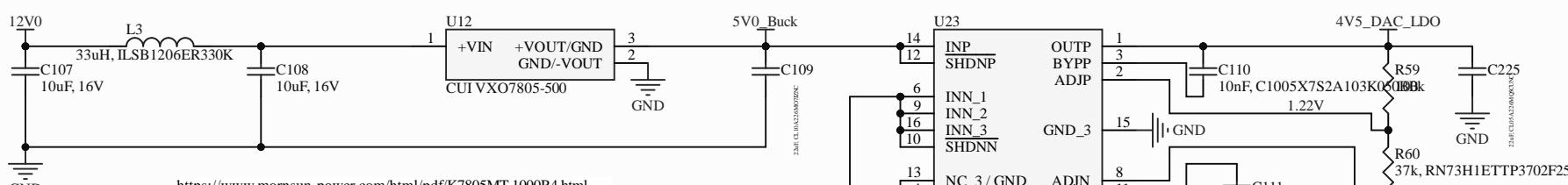
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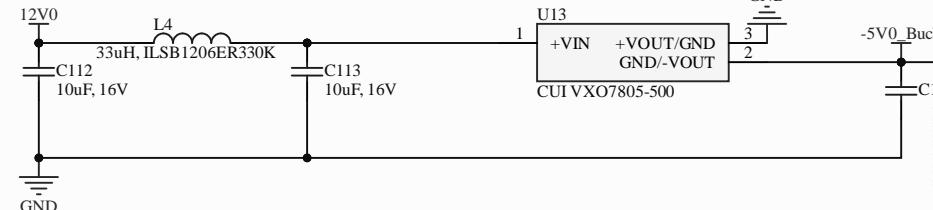
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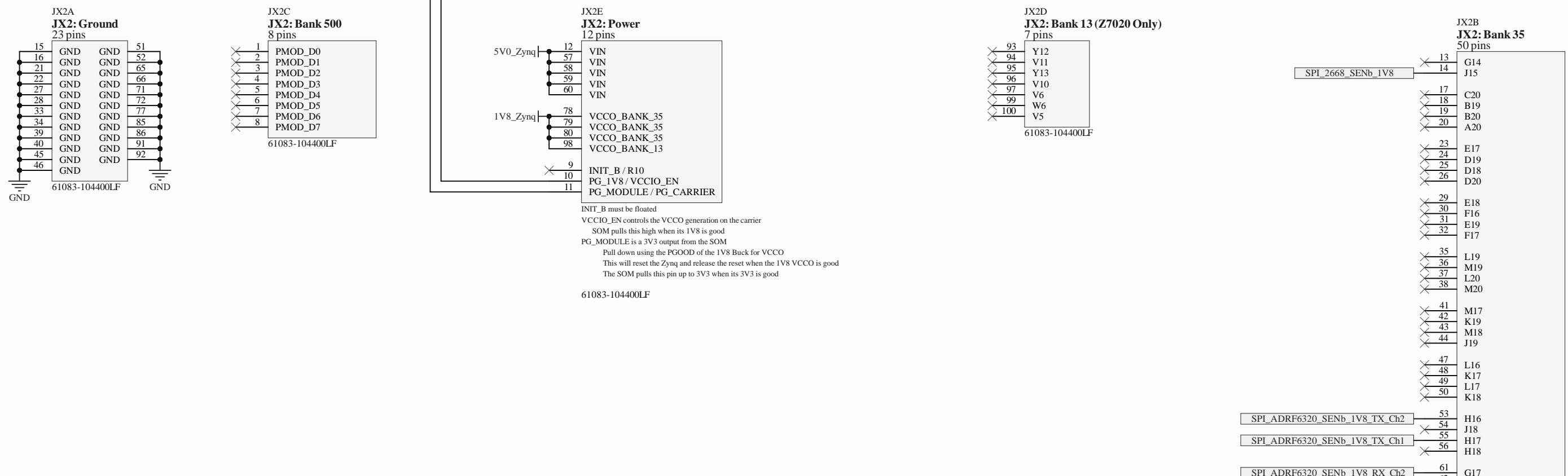
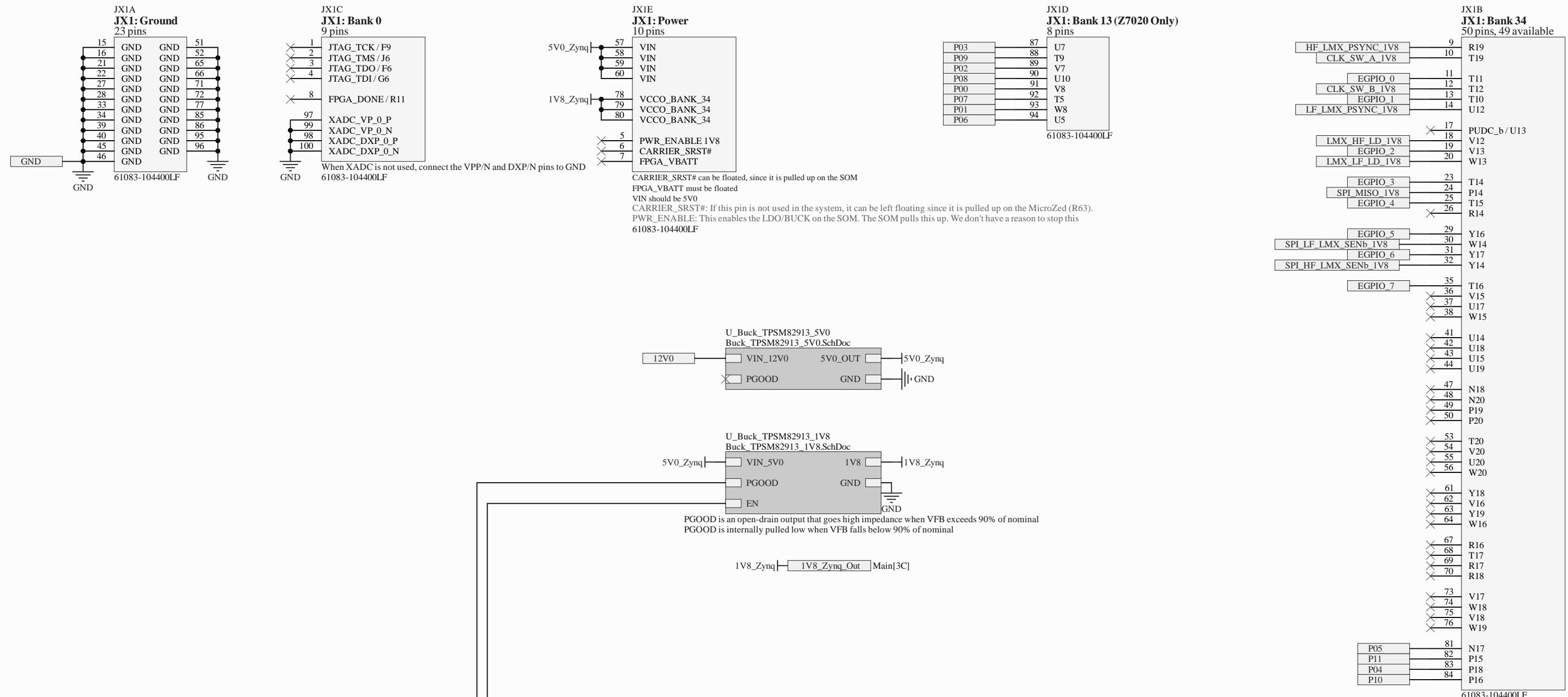
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<https://www.analog.com/media/en/technical-documentation/data-sheets/3032ff.pdf>

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Date: 2/18/2025	Sheet of	
File: C:\Users\..\LTC2668HUJ-16_VDAC.SchDoc	Drawn By:	

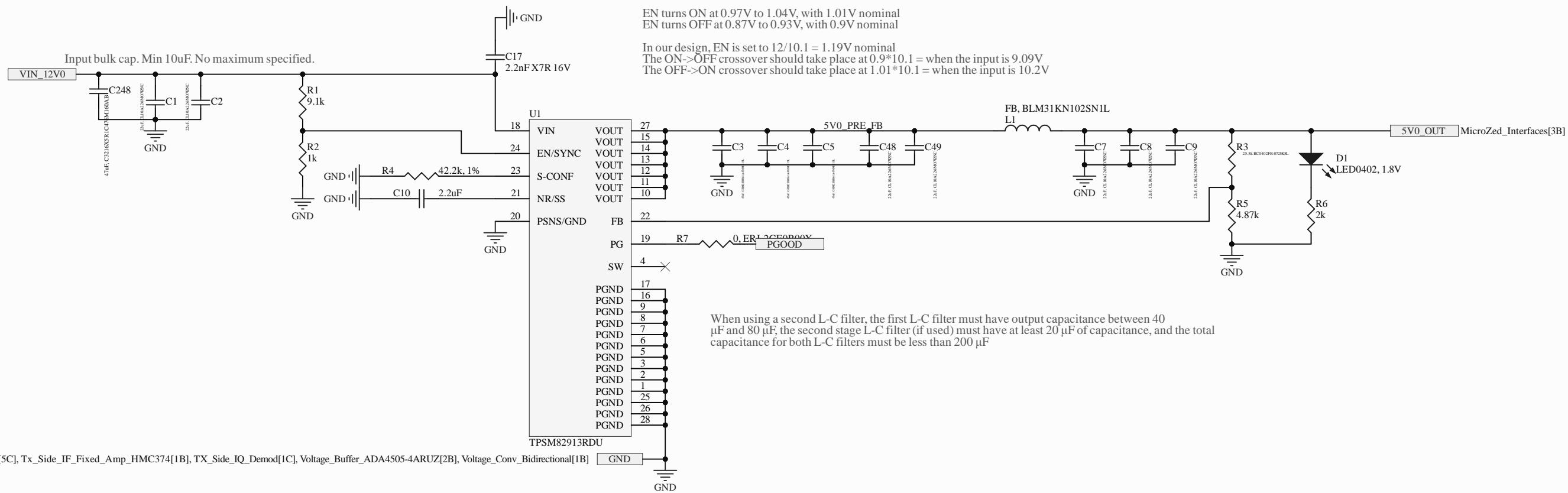


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C		
Date: 2/18/2025	Sheet of:	
File: C:/Users/..MicroZed Interfaces.SchDoc	Drawn By:	

A

In addition to the bulk input cap, a smaller cap must be placed directly from the VIN pin to the PGND pin to minimize input loop parasitic inductance, thereby minimizing the high frequency noise of the device.
Recommended: 2.2nF X7R

B



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Title		
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File: C:\Users..\Buck_TPSM82913_5V0.SchD	Drawn By:	

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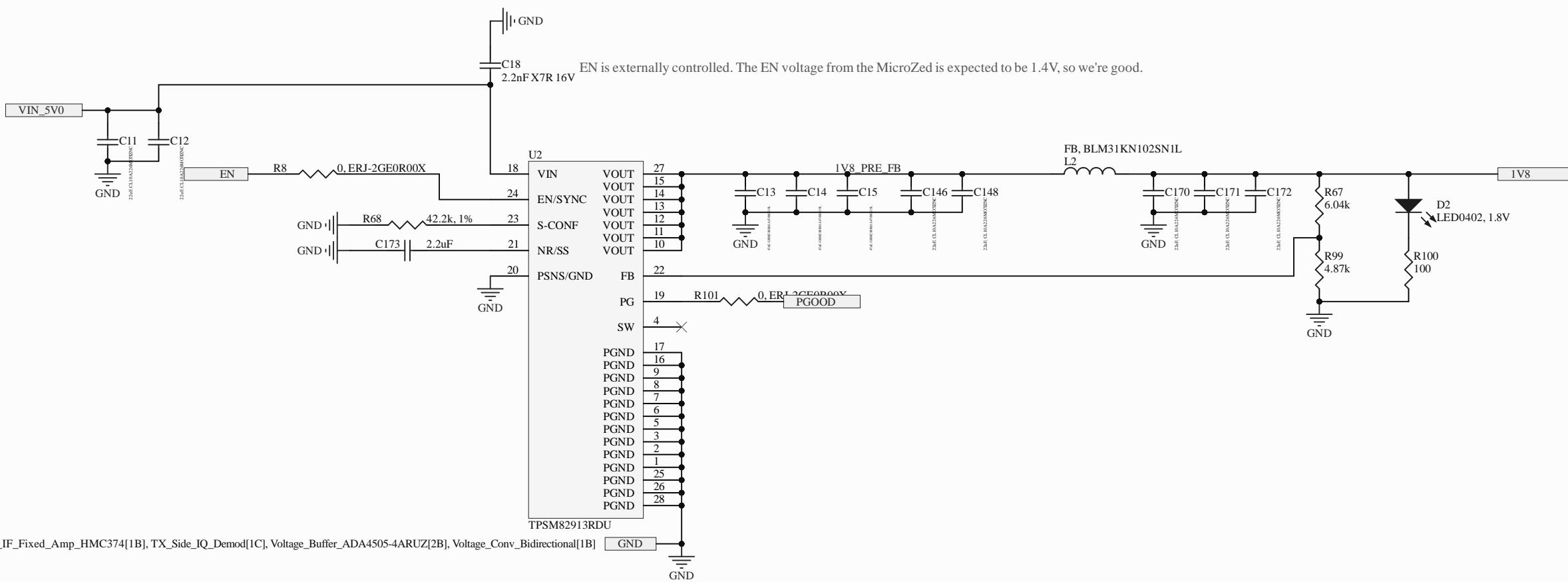
D

A

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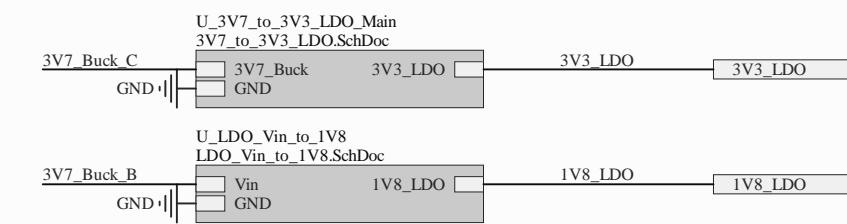
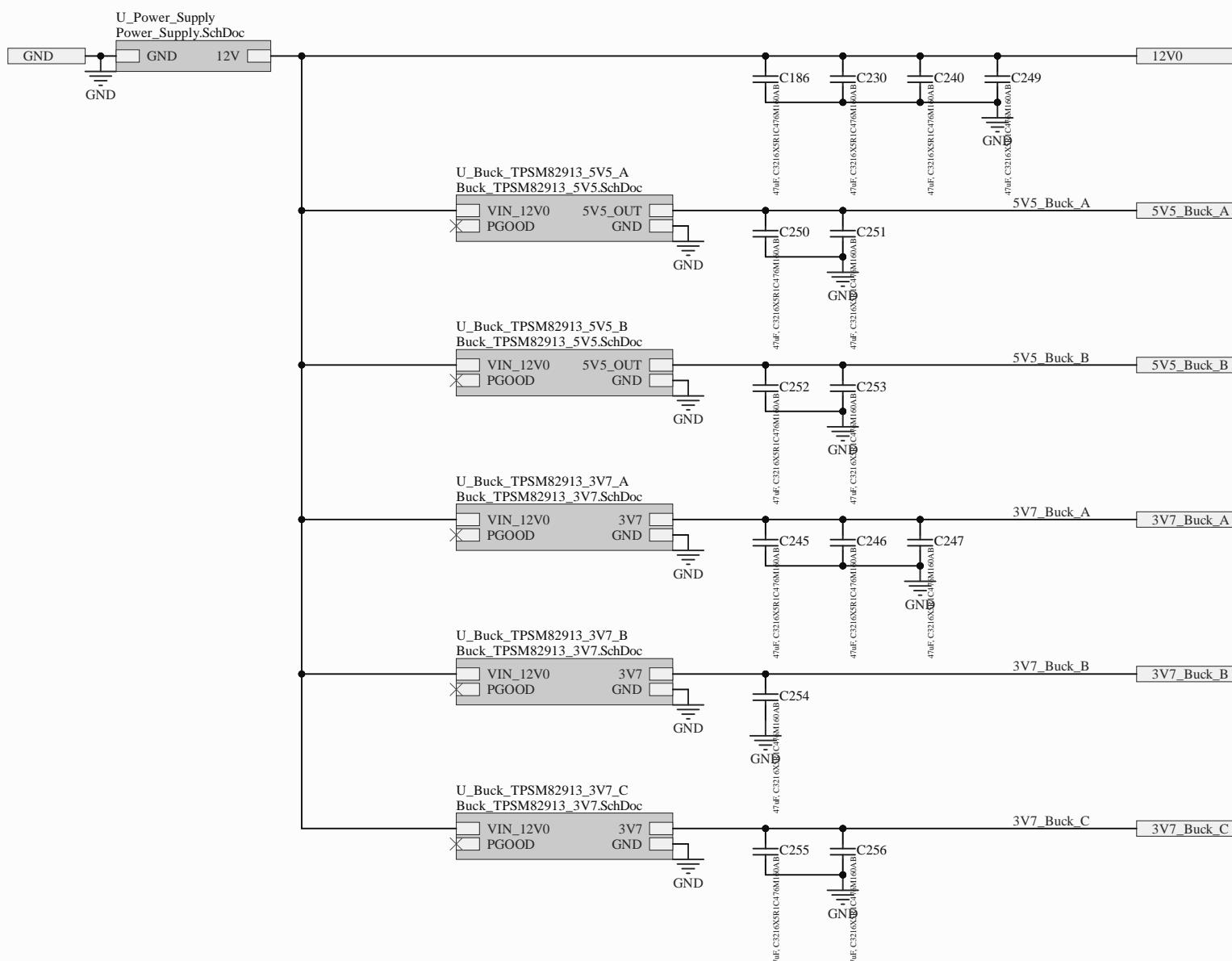
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DL9006[5C], Tx_Side_IF_Fixed_Amp_HMC374[1B], TX_Side_IQ_Demod[1C], Voltage_Buffer ADA4505-4ARUZ[2B], Voltage_Conv_Bidirectional[1B]

Title		
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File: C:\Users\..\Buck_TPSM82913_1V8.SchD	Drawn By:	

A



Added bulk capacitance to certain polygons to suppress resonances

Title

Size
B

Number

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File: C:\Users\.\Power_Tree.SchDoc

Drawn By:

A

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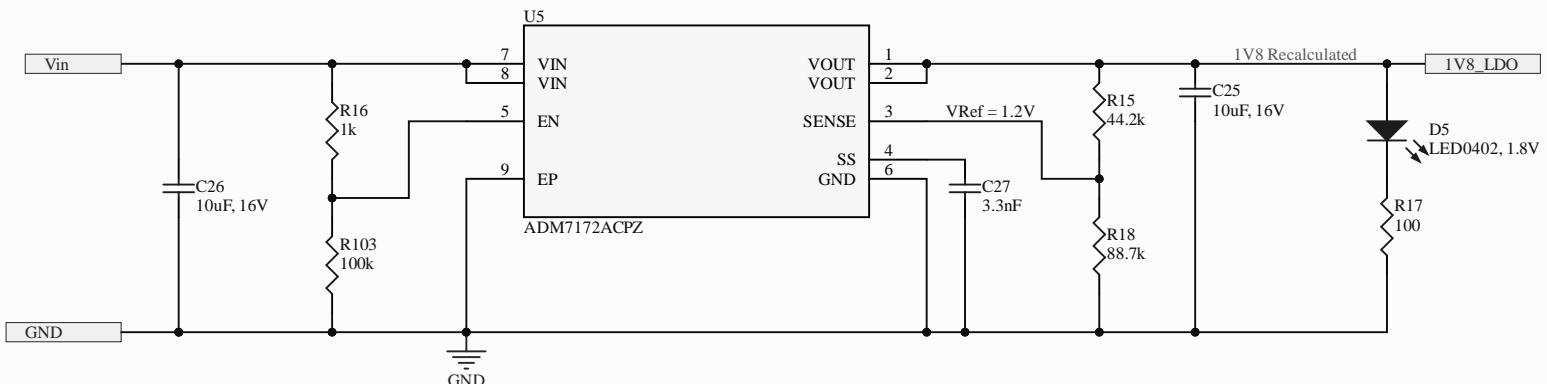
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Title

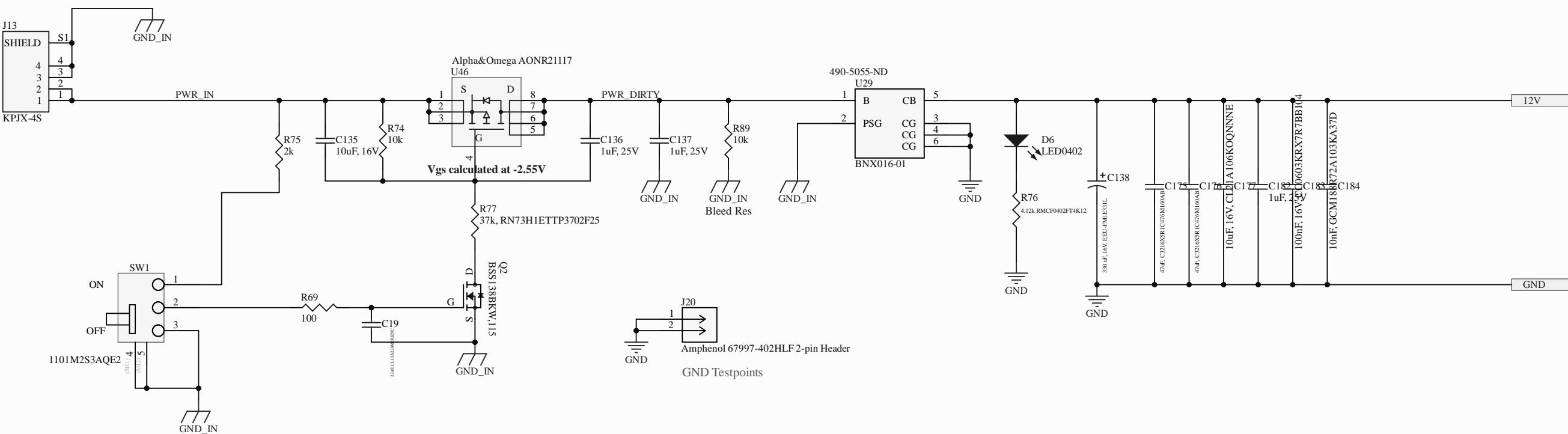
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Number

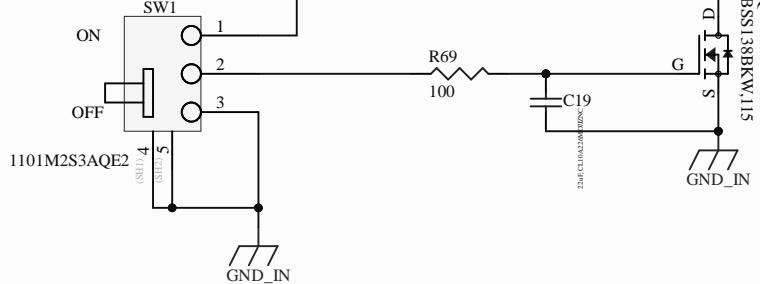
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C:\Users\...\LDO_Vin_to_1V8.SchDoc Drawn By:

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Title		
Size	Number	Revision
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Date: 2/18/2025	Sheet of	
File: C:\Users\..\Power_Supply.SchDoc		Drawn By:

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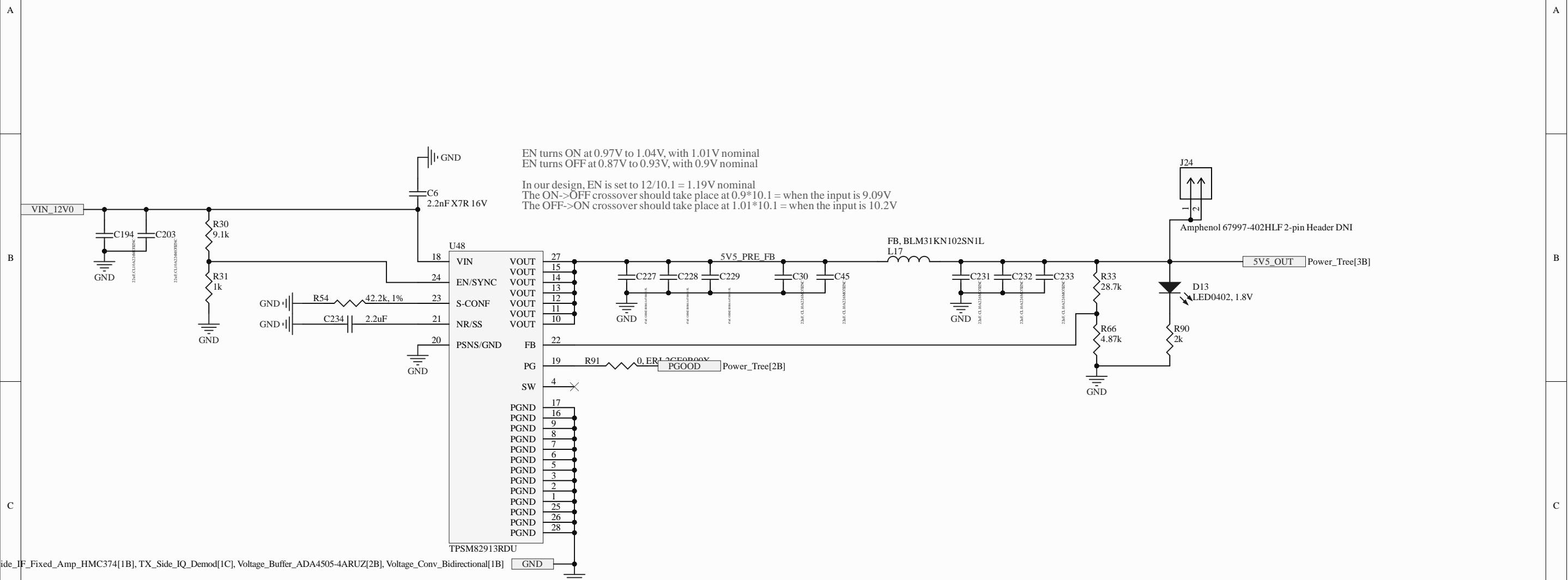
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ide_IF_Fixed_Amp_HMC374[1B], TX_Side_IQ_Demod[1C], Voltage_Buffer ADA4505-4ARUZ[2B], Voltage_Conv_Bidirectional[1B]



Title

Size
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Number

Revision

Date: 2/18/2025

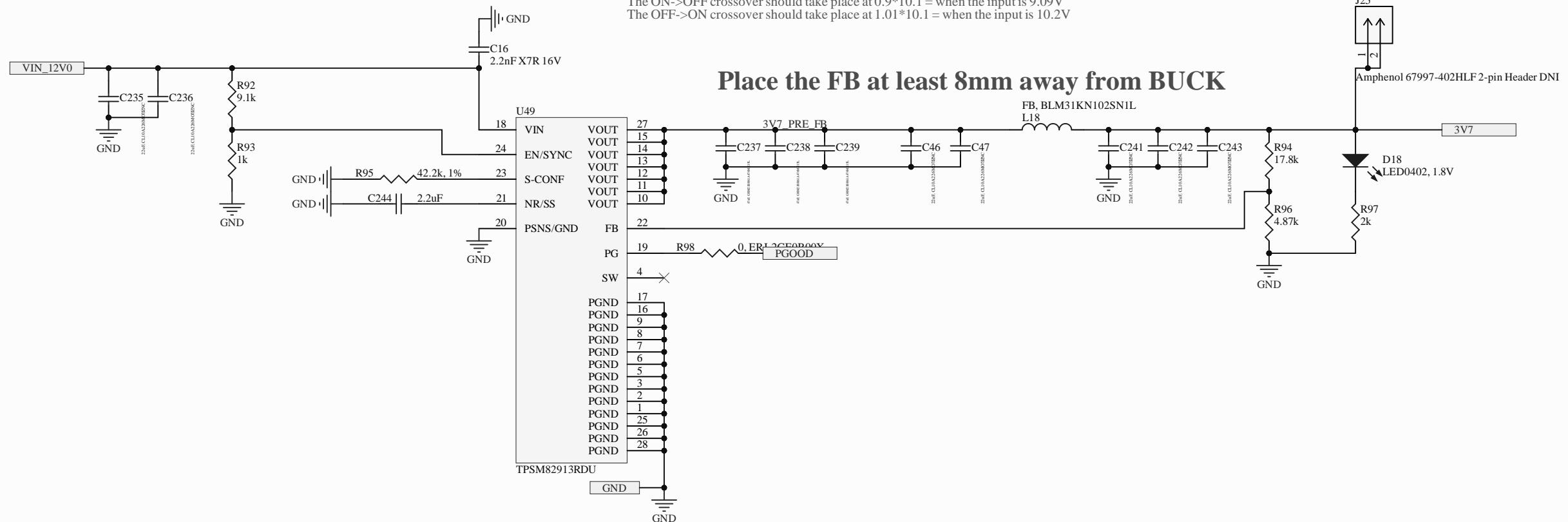
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EN turns ON at 0.97V to 1.04V, with 1.01V nominal
EN turns OFF at 0.87V to 0.93V, with 0.9V nominal

In our design, EN is set to 12/10.1 = 1.19V nominal
The ON->OFF crossover should take place at $0.9^*10.1$ = when the input is 9.09V
The OFF->ON crossover should take place at $1.01^*10.1$ = when the input is 10.2V

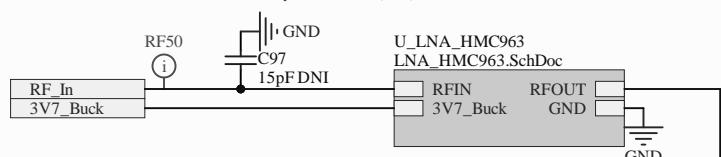


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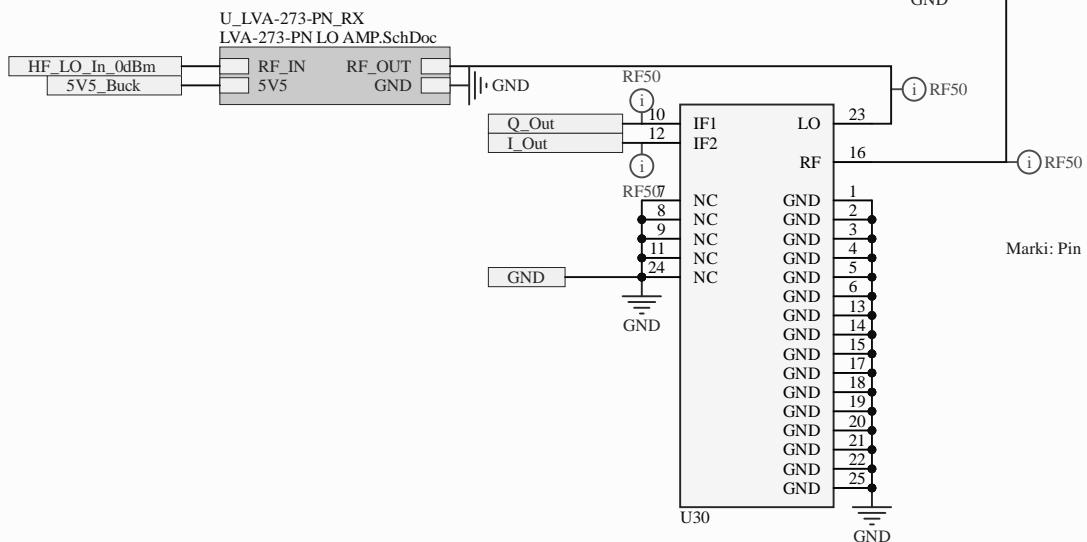
A

Placeholder for the ESD protection diode (0201)



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B



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Title

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File: C:\Users\...\RX_HMC963_MMIO626.Sch

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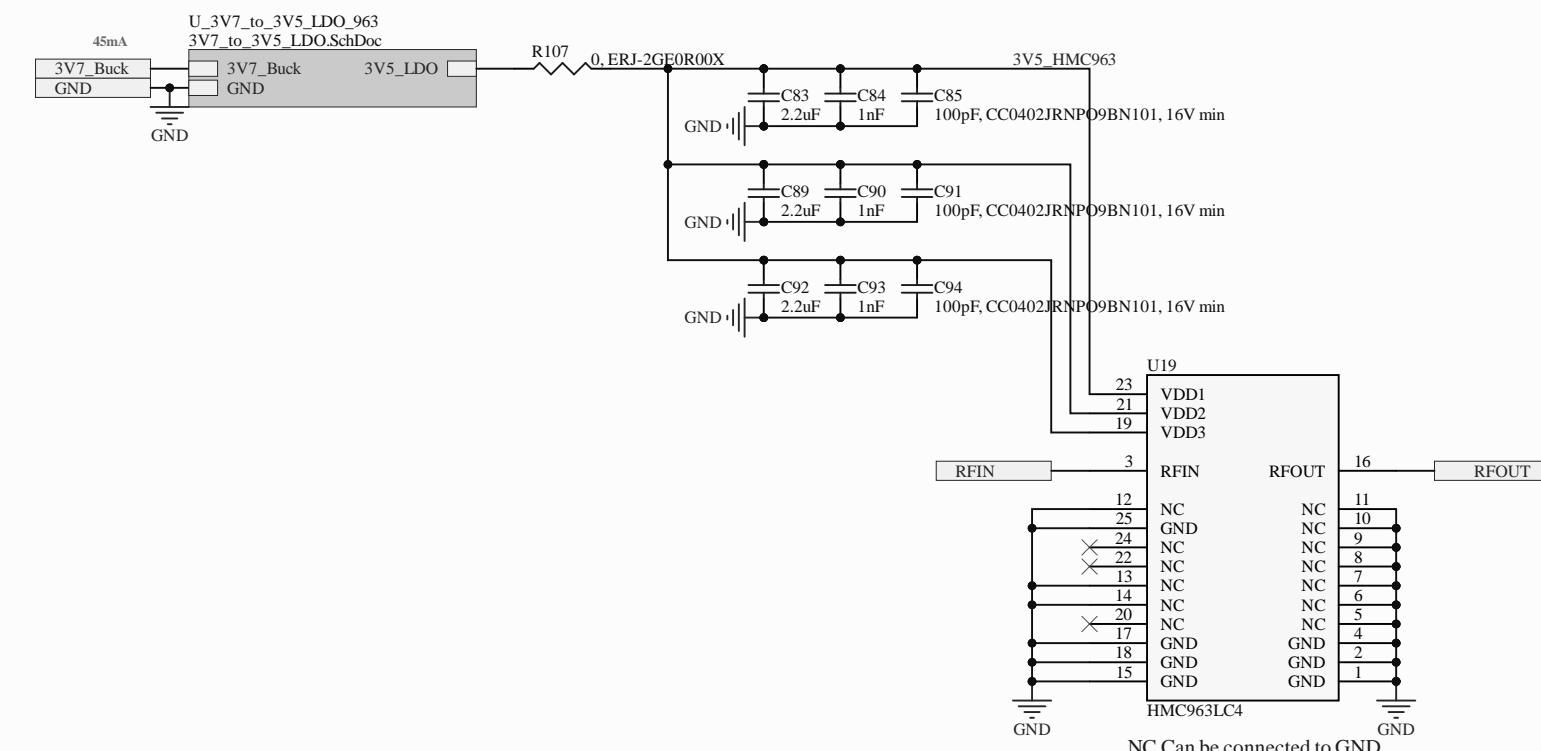
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File: C:\Users\.\LNA_HMC963.SchDoc	Drawn By:	

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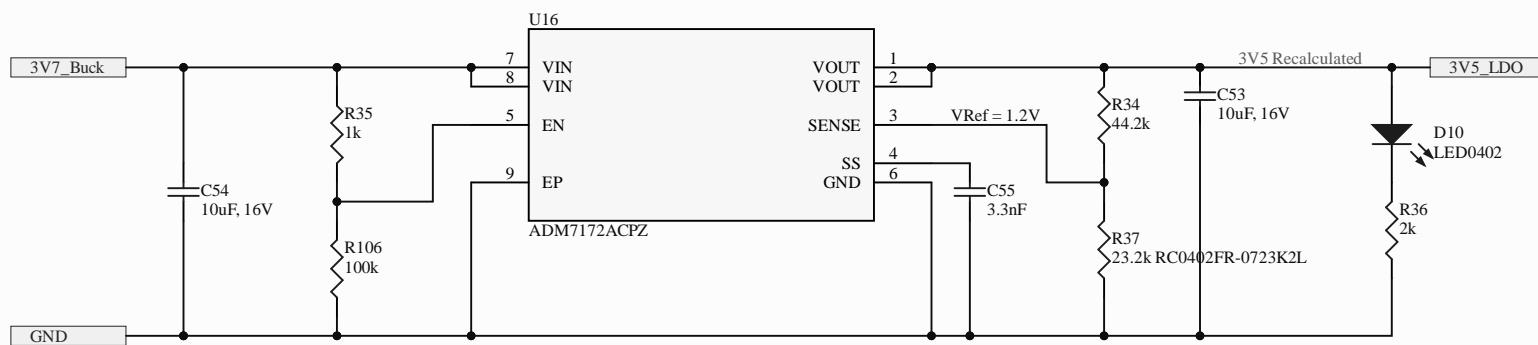
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Title

Size

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Number

Revision

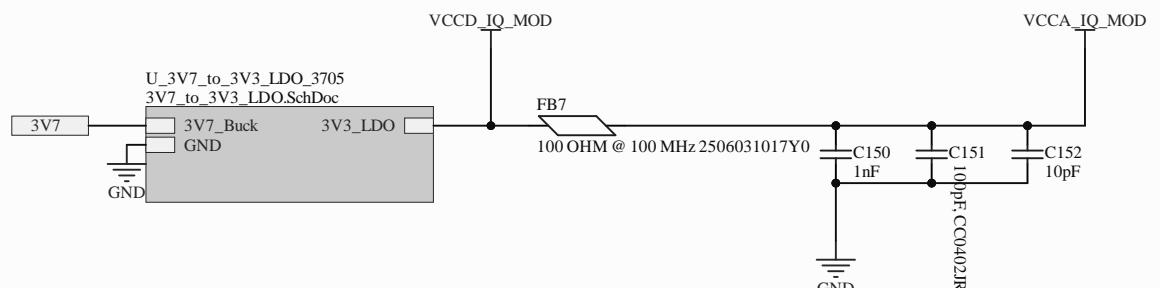
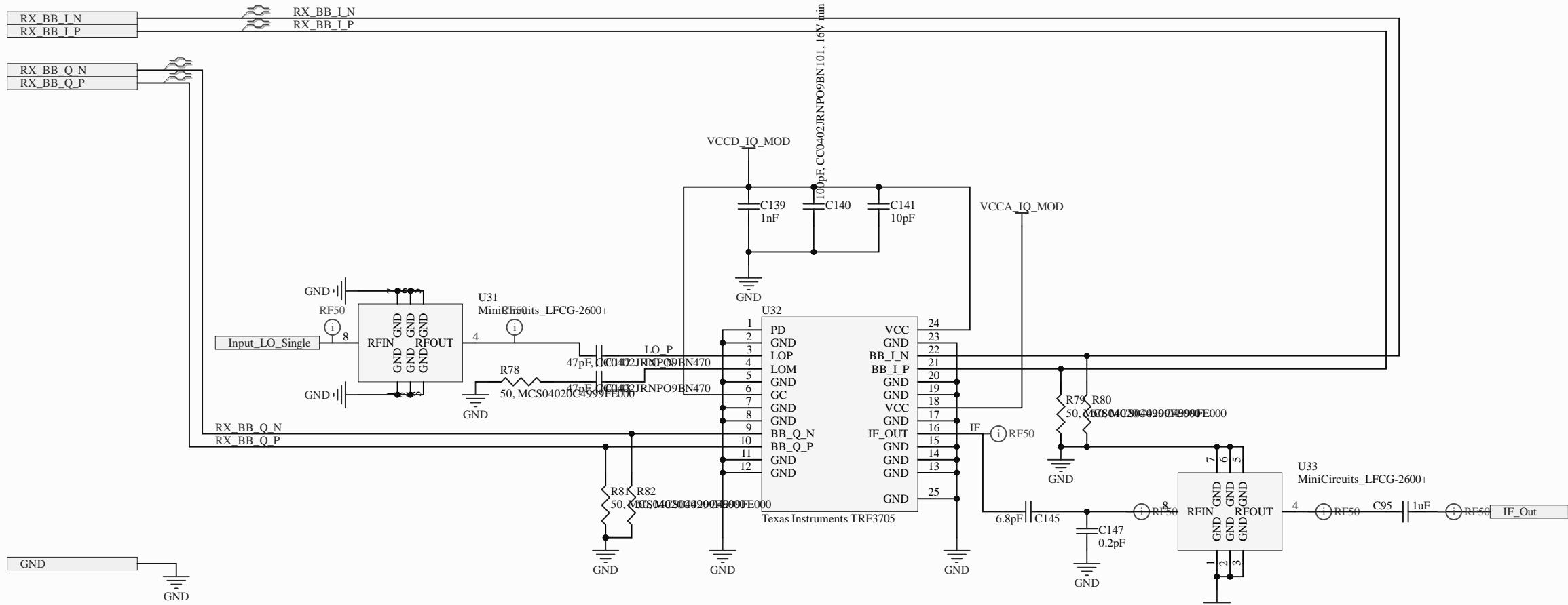
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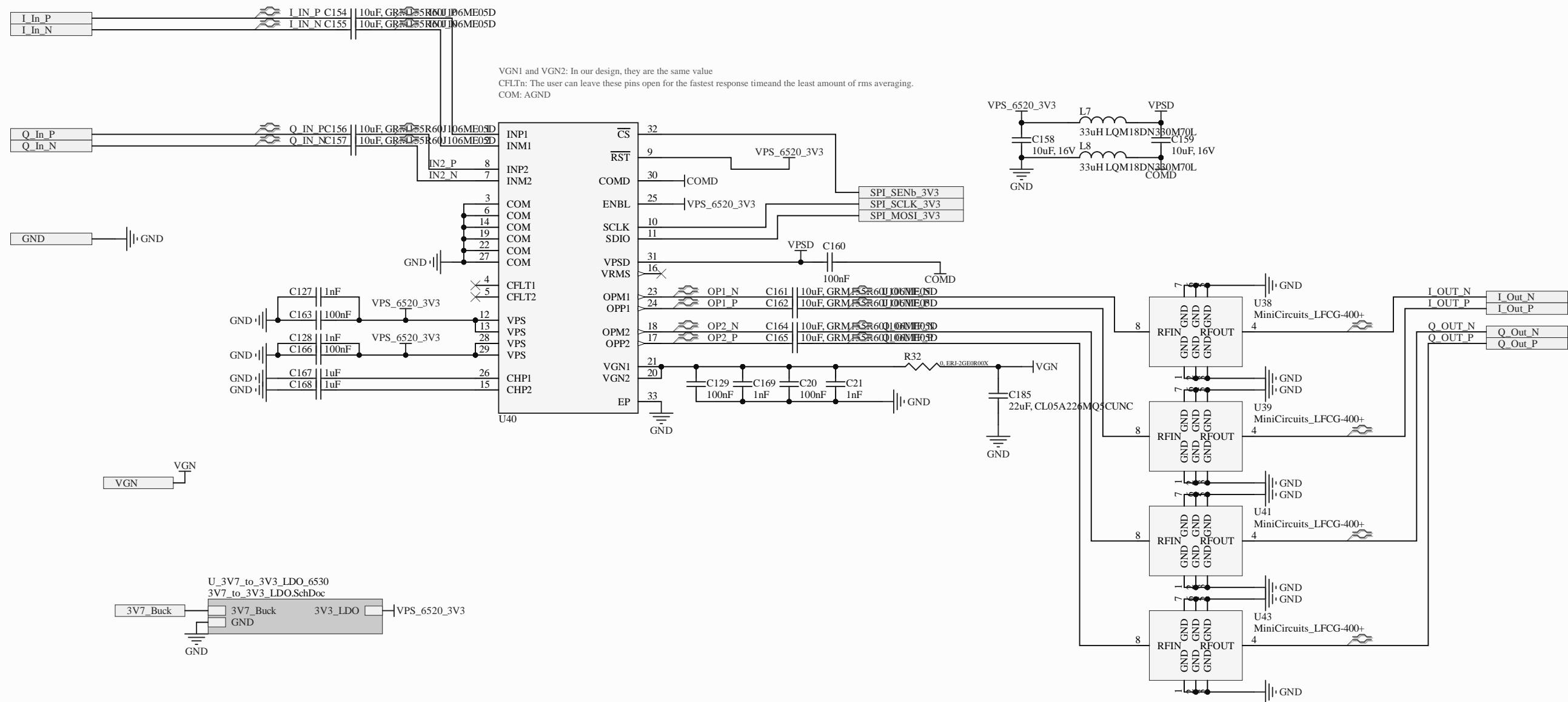
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Title			
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Date:	2/18/2025	Sheet of	
File:	C:\Users\...\RX_Side_IQ_Mod.SchDoc	Drawn By:	



Title		
Size B	Number	Revision
Date:	2/18/2025	Sheet of
File:	C:\Users\...\IO VGA ADRF6520.SchDoc	Drawn By:

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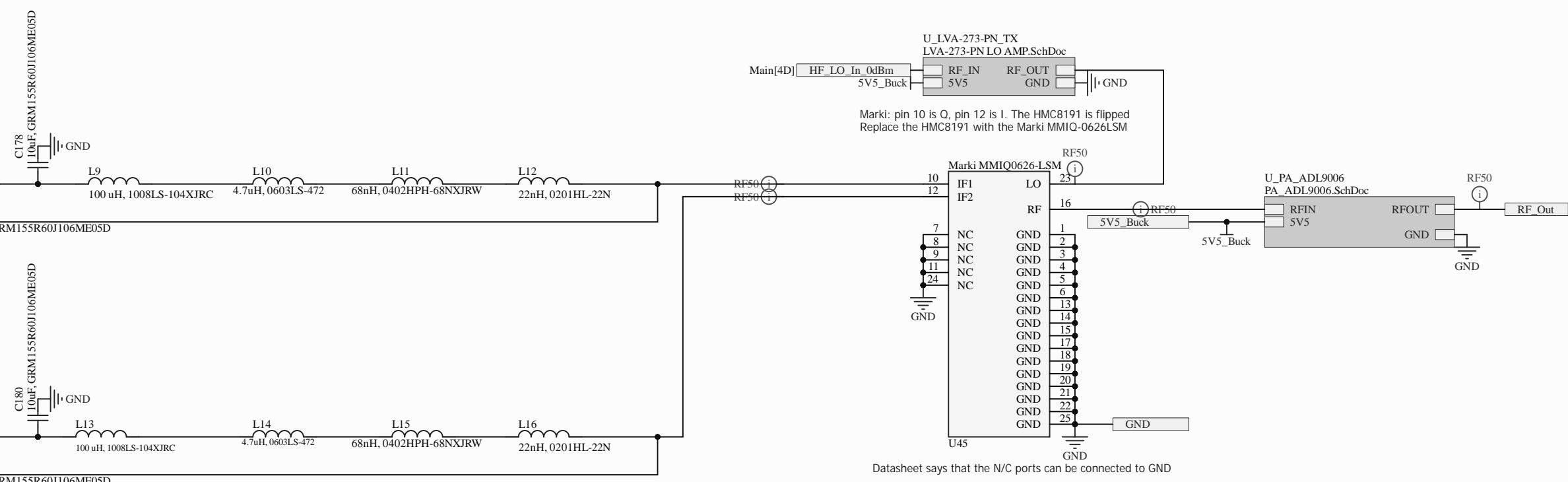
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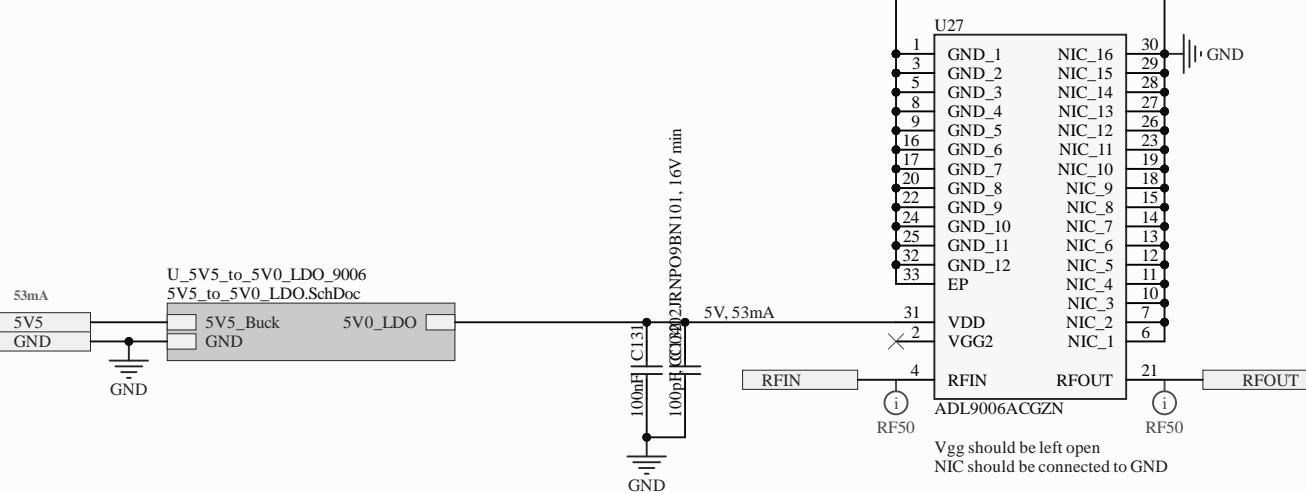
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Title		
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B		
Date: 2/18/2025	Sheet of	
File: C:\Users\.\TX_MMIQ0626_ADL9006.SchDoc	Down By:	



Title

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Revision

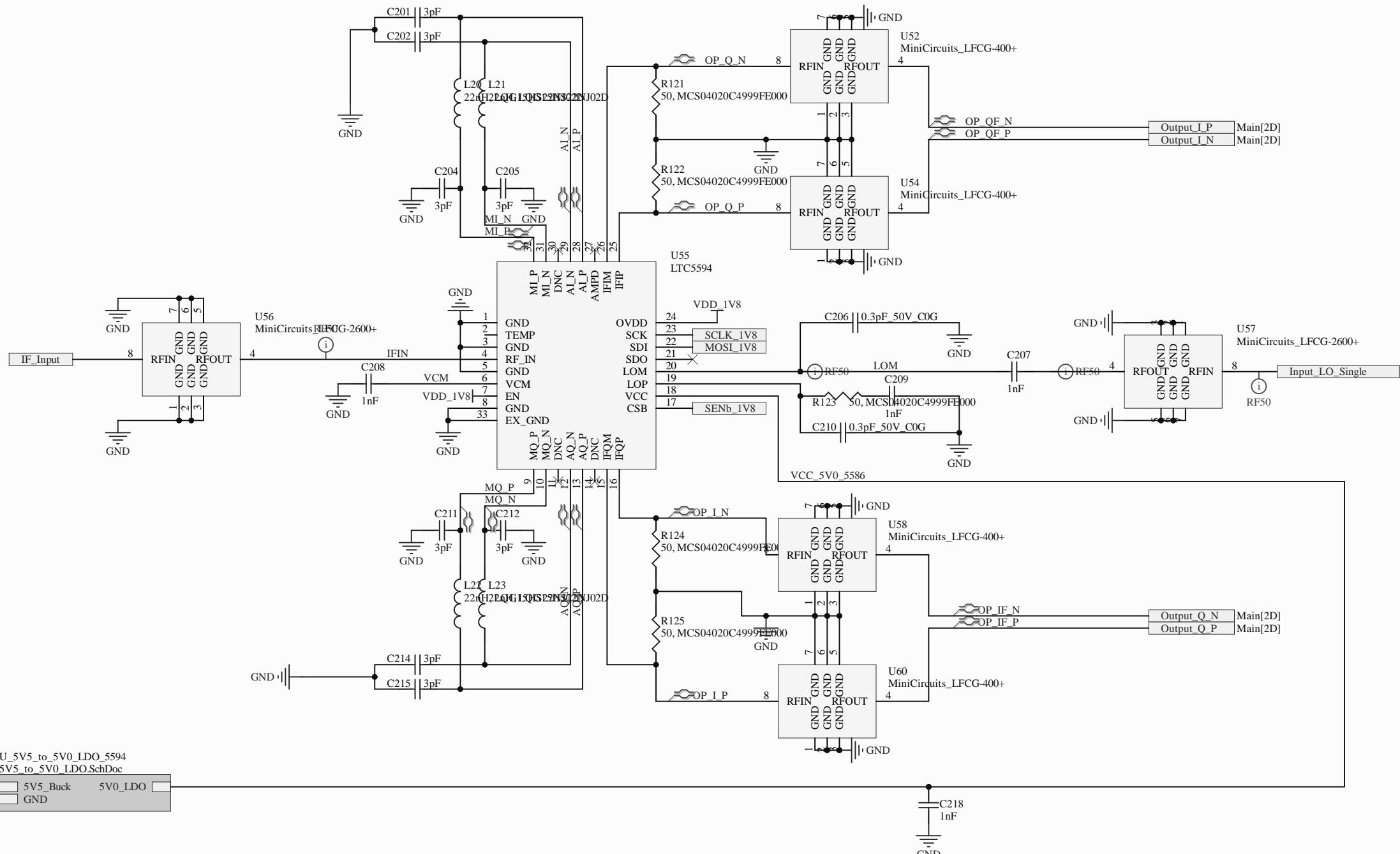
Date: 2/18/2025

File: C:\Users\PA\ADL9006.SchDoc

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Note: We have swapped I/Q, and changed the polarity of I. Functionally, this is identical to a perfect mapping.



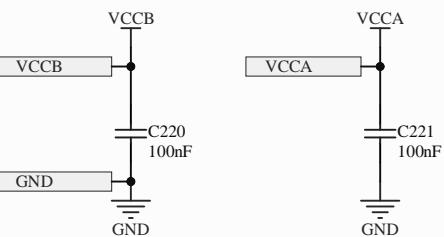
Analog Devices LTC5586
The output I/Q signals need to be filtered

The input IF signal needs to be filtered

Title		
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Date:	2/18/2025	Sheet of
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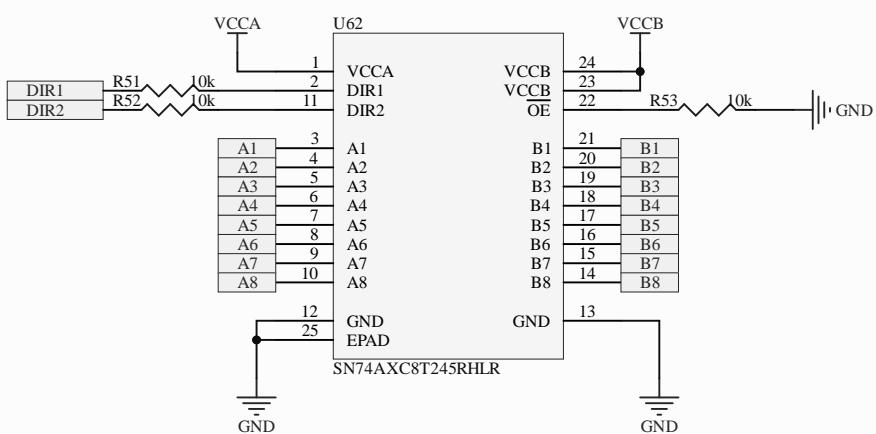
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A



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C

C

Table 1. Function Table⁽¹⁾

CONTROL INPUTS			Signal Direction	
OE	DIR1	DIR2	Bits 1:4	Bits 5:8
H	X	X		Disabled (Hi-Z)
L	L	L	B to A	A to B
L	L	H		
L	H	L	A to B	B to A
L	H	H	A to B	B to A

(1) Input circuits of the data I/Os are always active and must be driven to a valid logic level.

D

D

Title

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Number

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Date:

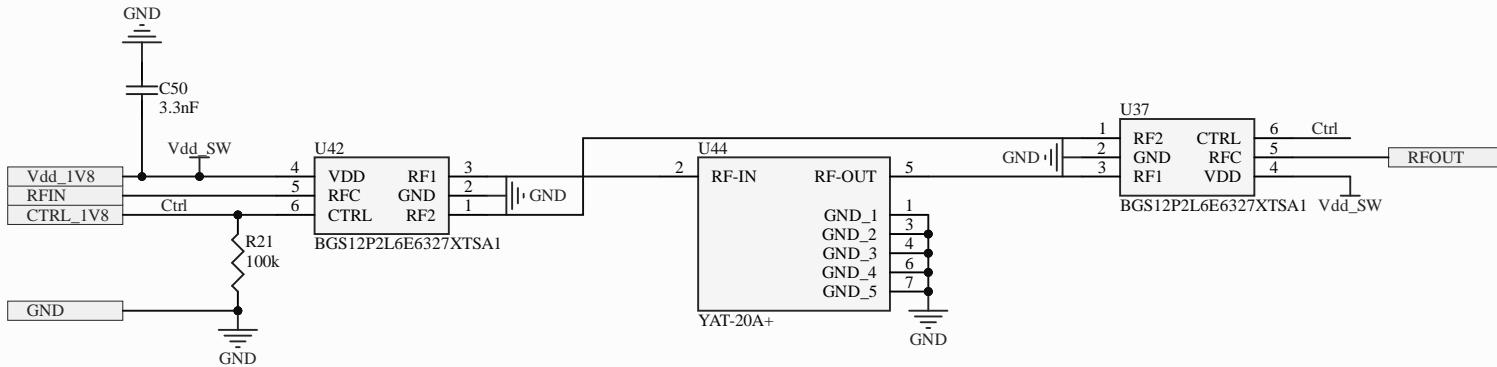
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Sheet of

File: C:\Users\...\Voltage_Conv_Bidirectional.vhd

1

A



We put a weak pulldown to GND. When CTRL is low, the RF1 path is activated.
This way, when the GPIO is in high-Z, then the signal always goes through the attenuator.

C

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C:\Users\...\IF_Power_Limiter.SchDoc

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<https://mm.digikey.com/Volume0/opasdata/d220001/medias/docus/2121/MF40101VX-1000U-A99.pdf>

A

The fans have a female 2-pin connector
We need a 2.54mm pitch 2-pin header for 12V0 and GND

A

B

B

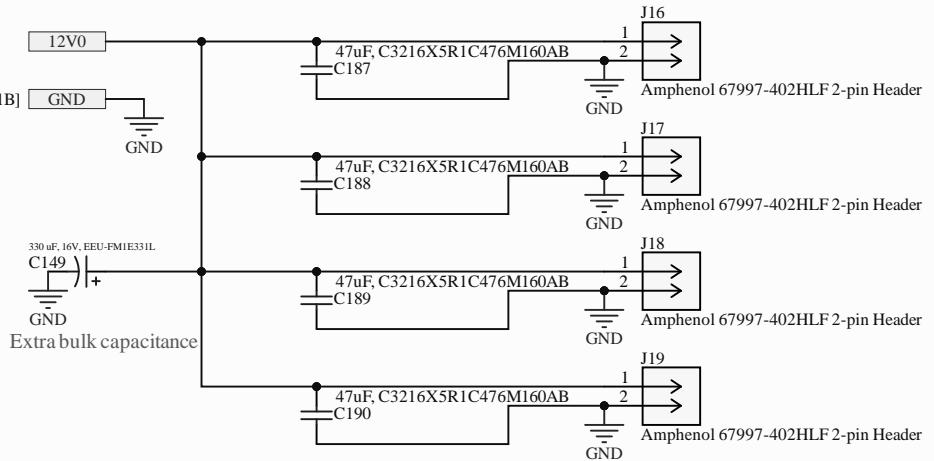
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File: C:\Users\...\Fan_Interfaces.SchDoc

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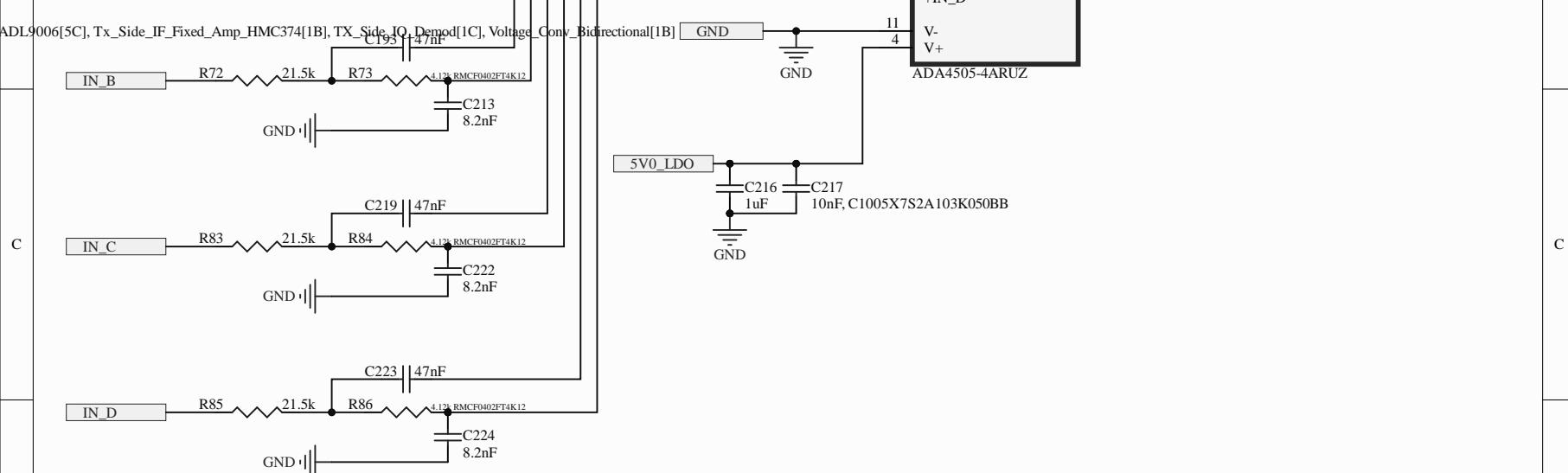
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Title

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Revision

Date: 2/18/2025
File: C:\Users\...\Voltage_Buffer_ADA4505-4ARUZ.Brd

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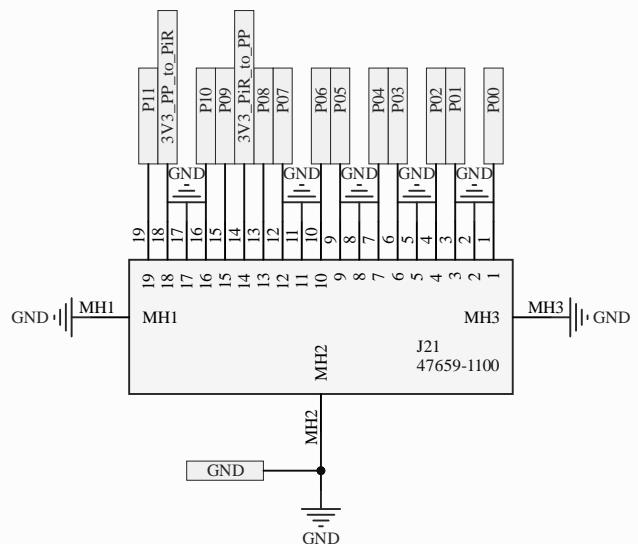
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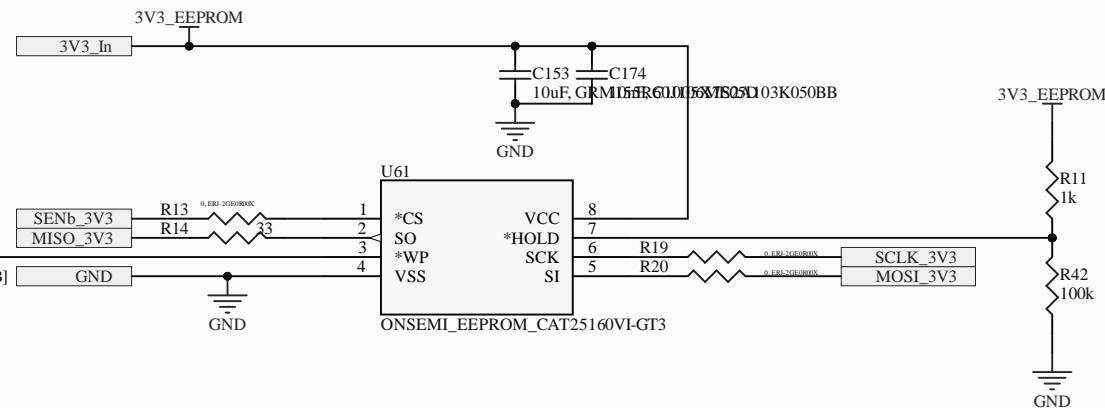
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Title		
Size	Number	Revision
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