FPGA PROTOTYPING
Lab2 Report

Team 11

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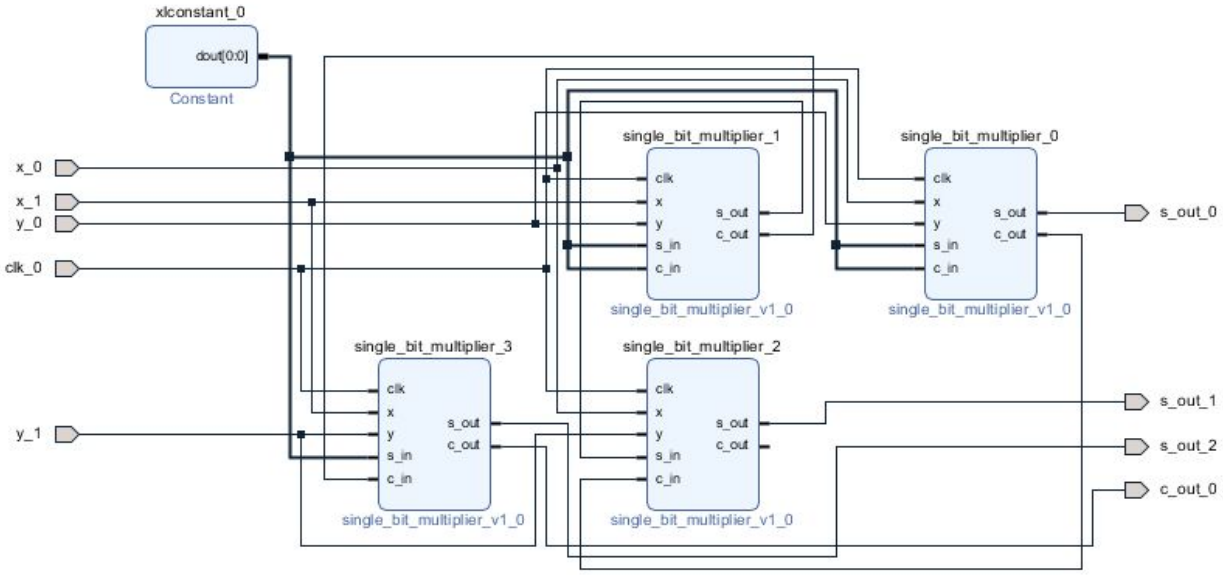
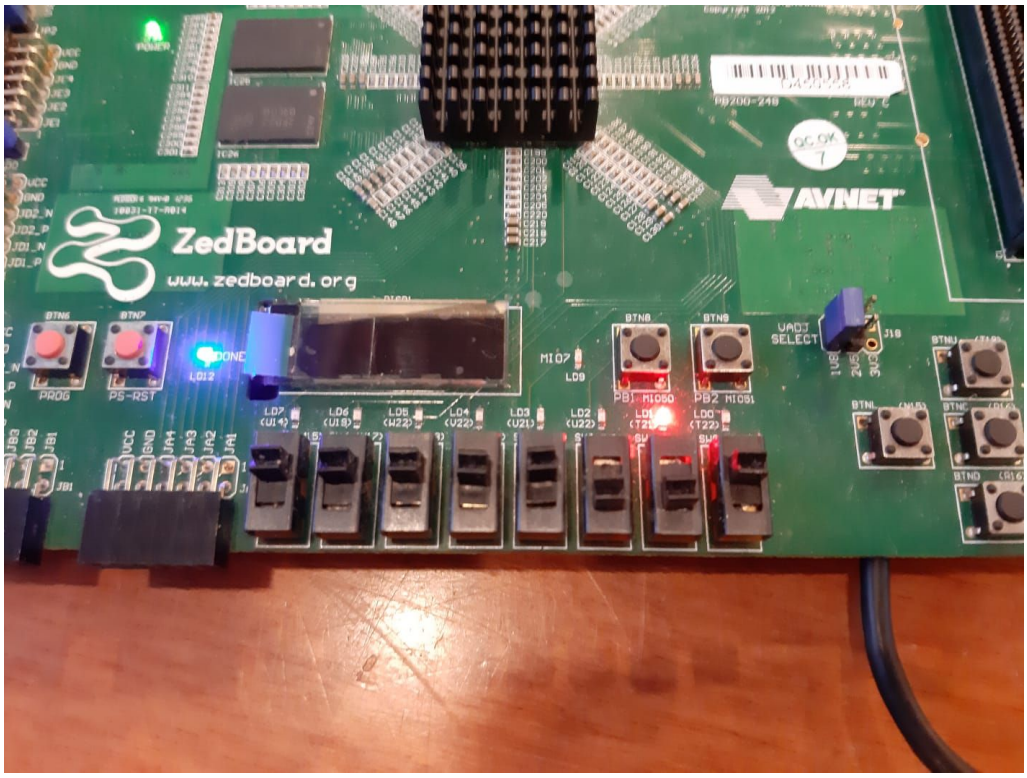
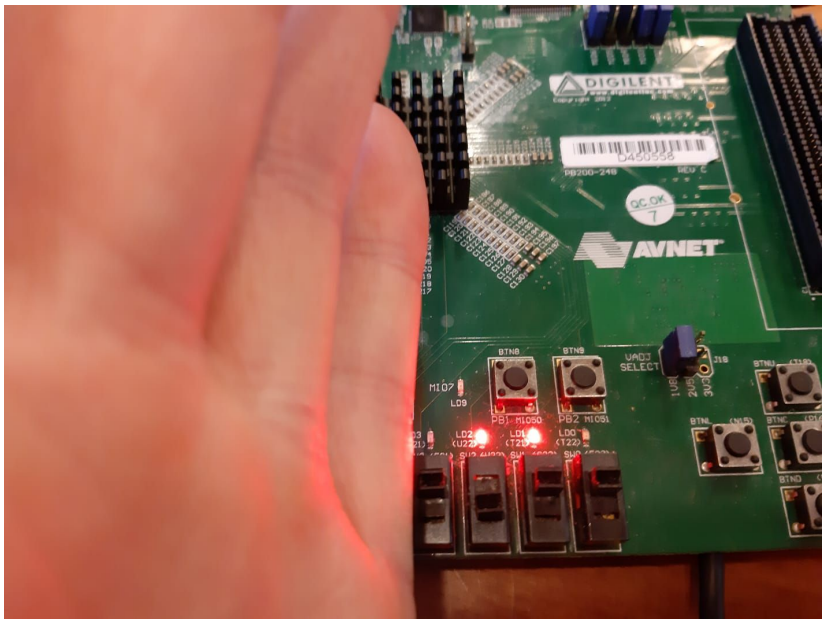
Task 1

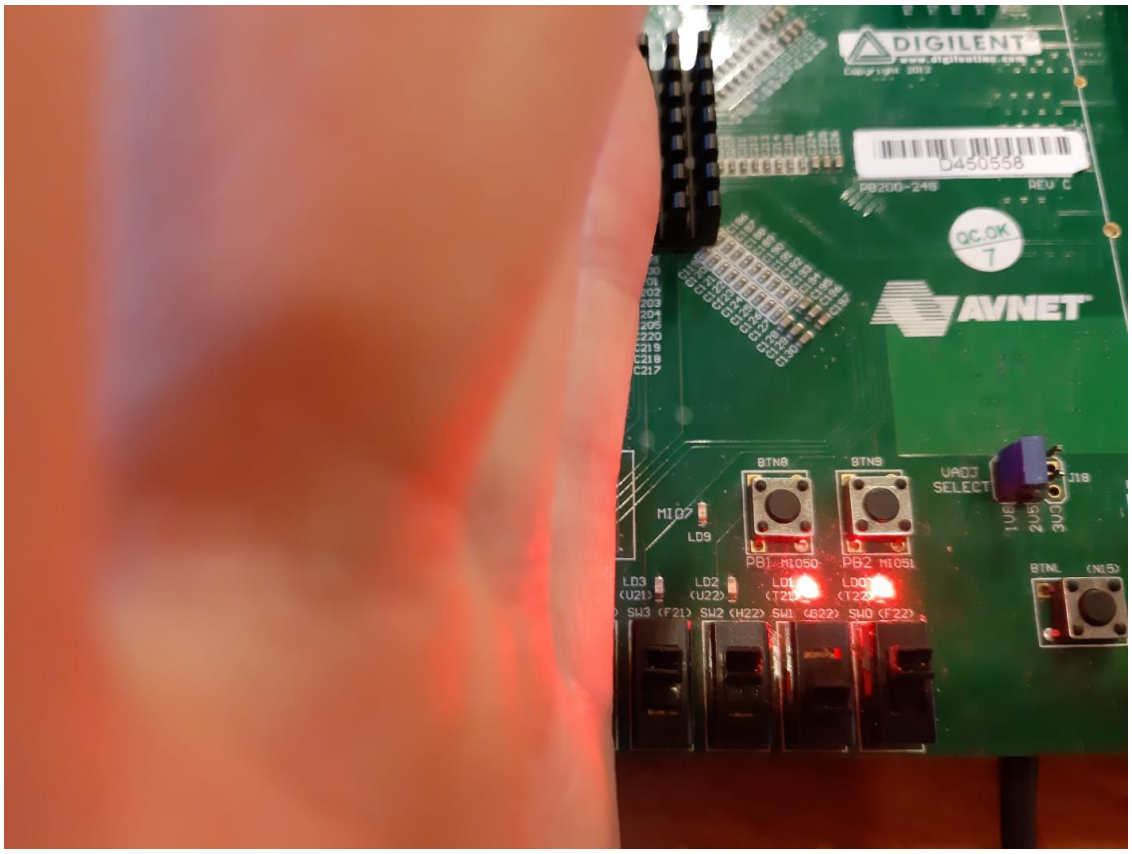
Create a 2x2 parallel bit multiplier without writing any HDL code (except a port map in the top file). In your block design, import 4 single_bit_multiplier IPs and connect them appropriately. To convert a port into an input or an output, right click into the port and choose “Make External”. In this task, connect the carry outputs in diagonal to reduce the multiplier’s latency

Attach to the report a screenshot of your block design and a photo of the board with a working example.



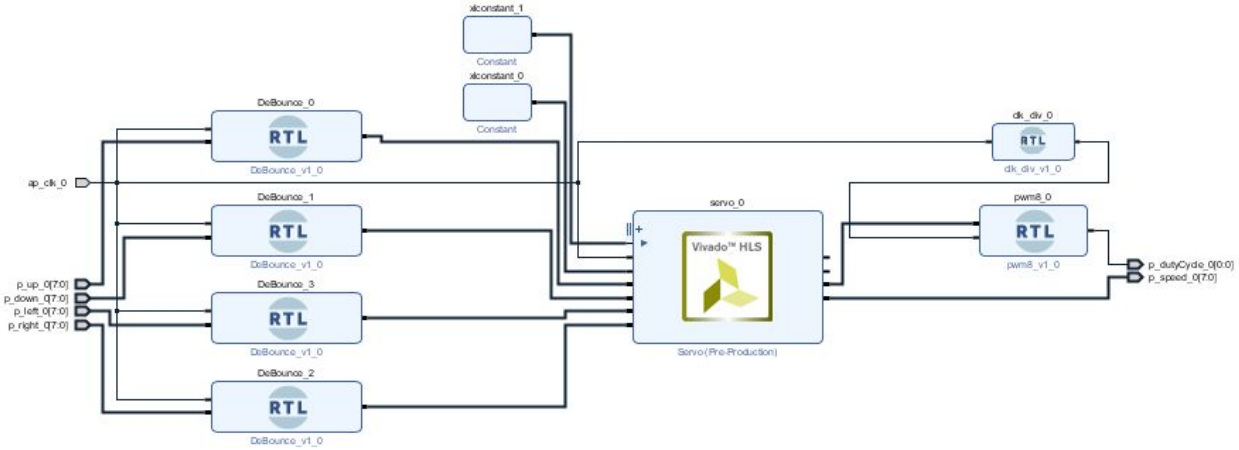

ZedBoard
www.zedboard.org
AVNET
PROG
PS-RST
DONE
LD12
VADJ SELECT
PB1 MIO50
PB2 MIO51
MIO7
LD9

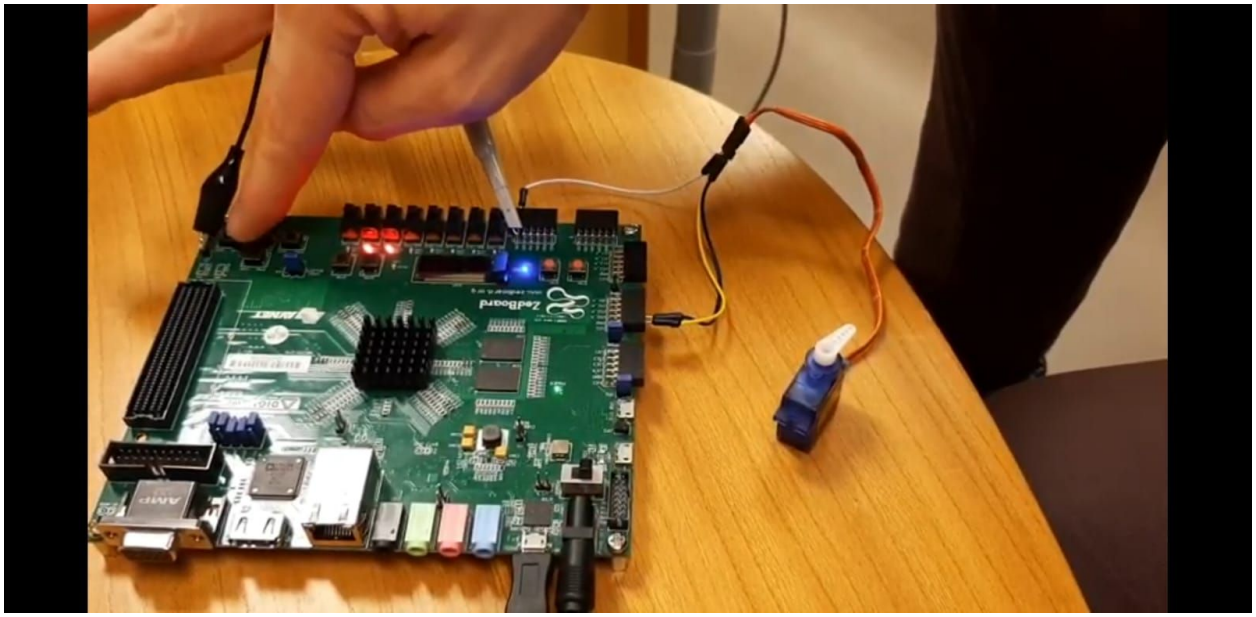

DIGILENT
AVNET
VADJ SELECT
PB1 MIO50
PB2 MIO51
MIO7
LD9


DIGILENT
D450558
PB200-248
REV C
QC.OK
7
AVNET
BTN0
BTN3
VADJ
SELECT
J18
MIO7
LD9
PB1 MIO50
PB2 MIO51
BTNL (N15)
LD3 (U21)
LD2 (U22)
SW3 (F21) SW2 (H22) SW1 (G22) SW0 (F22)

Task 2

Task 2 (3 points) Create a new Vivado project. Import the IP you created in Vivado HLS. Assign the speed output to the 8 LEDs and utilize the buttons BTNU and BTND. Add a debouncer and utilize the two buttons of the Zedboard and change your constraint file accordingly. Together with your report, send a video (max 10 seconds) where you show this function.



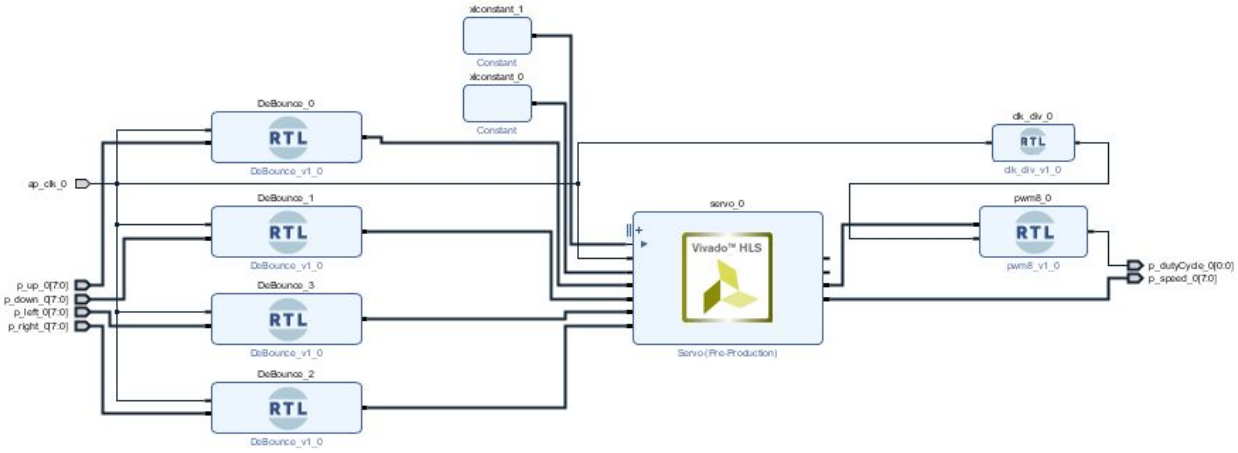


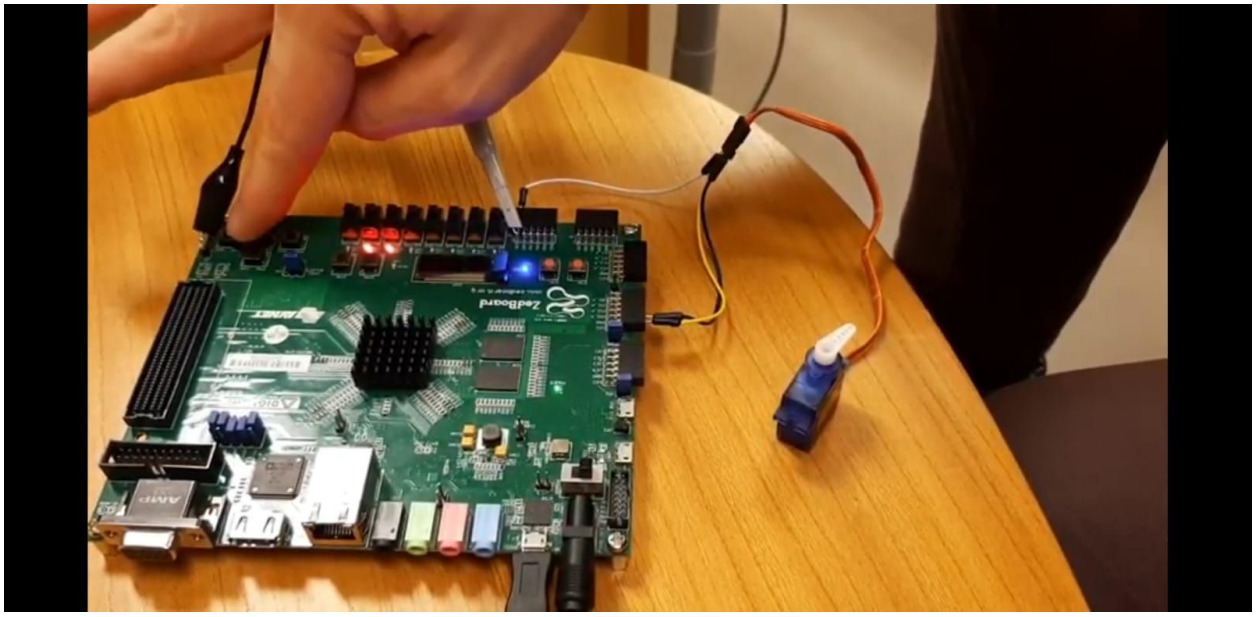
Videos:

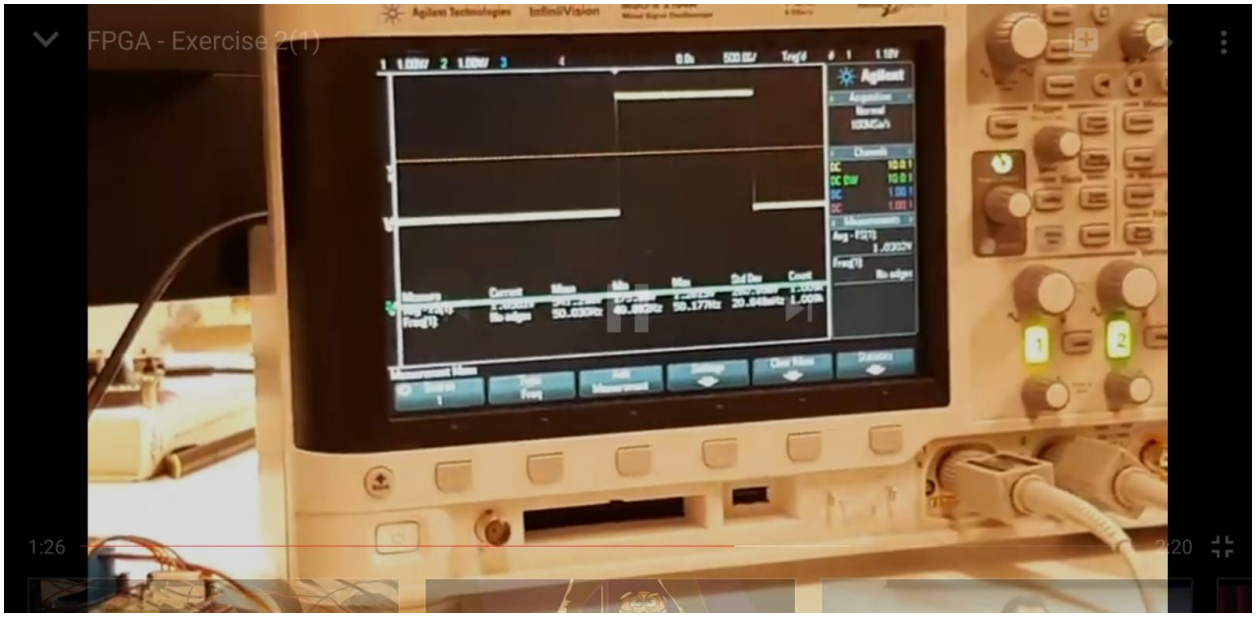
https://youtu.be/0d-x-3-rmsQ
https://youtu.be/-Y6_8efadyU
https://youtu.be/h0P1KcxcVD8

Task 3

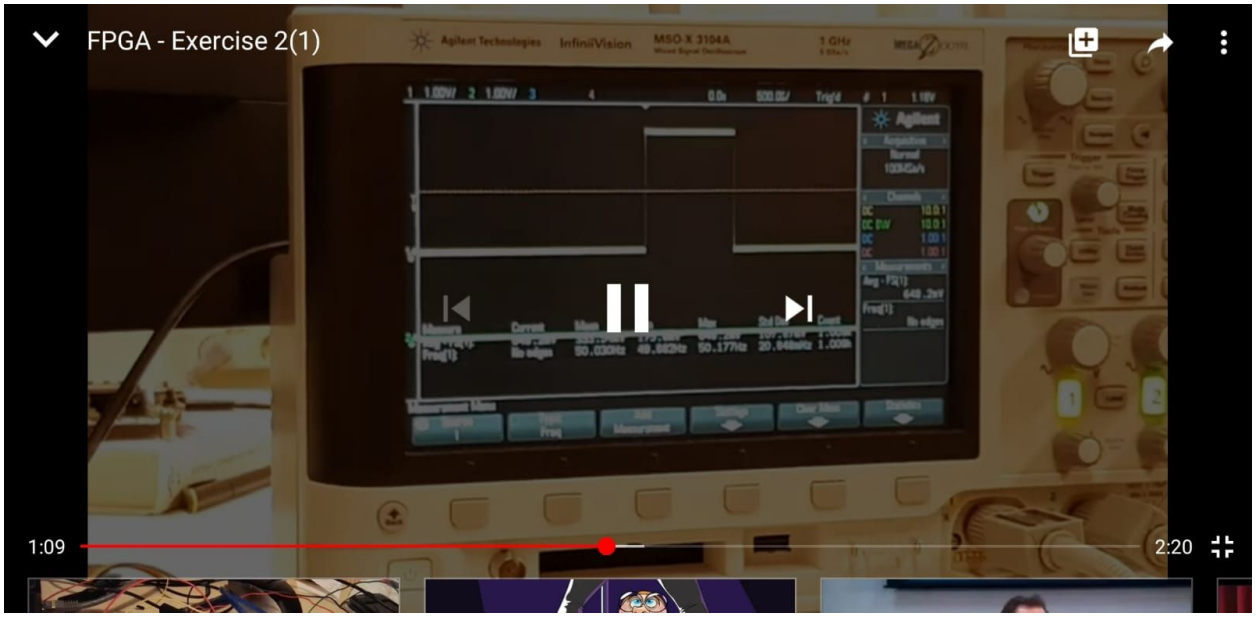
Task 3 (5 points) Create two new IPs using Vivado: one for a PWM signal generator and another one for a debouncer. The PWM works at a frequency of 50Hz (20ms period), and has a duty cycle of 1ms to 2ms. The input to the PWM is an 8-bit integer (std_logic_vector) that ranges from 100 (1ms) to 200 (2ms). This comes directly from your HLS module. Create an IP block and connect all the parts. Write a top module to do any last tweaks you need and set the inputs and outputs you need in the constraint file. To connect your servo motor, you can utilize any of the PMOD headers in the Zedboard. For example, this is the JA PMOD:







It is possible to see in the oscilloscope how the frequency is 50 Hz, and how the duty cycles changes when the buttons are pressed.



Videos:

https://youtu.be/0d-x-3-rmsQ
https://youtu.be/-Y6_8efadyU
https://youtu.be/h0P1KcxcVD8

Notes about the PWD

The frequency divider is 100e6/(N*2)=50*2048

2048 is our round for 2000

We need to have 100 counts of the pwm generator as 1 ms. Therefore, 20 ms of the period is 2000 counts. We used 2048 instead so that the pwm logic is simpler

50 Hz = 20ms
Our granule of the pulse width is 20/2048 ms