CSSE1000/CSSE7035 - Prac 3

Flip Flops & Sequential Circuits

Goals

- Understand the operation of D flip-flops
- Construct a ripple counter and examine its operation
- Construct a synchronous 3-bit counter and examine its operation
- Construct a 4-bit shift register and examine its operation
- Challenge: Construct a 3-bit synchronous counter with parallel load input

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See the following topics:

Back to Lab Experiment Index

Preparation - Complete the following questions in your Prac workbook

Note the you have enough switches (8), push buttons (4) and LEDs (16) to wire up all circuits simultaneously (except for part one you may dismantle this after you have competed it). Use different switches/buttons/LEDs for each circuit and indicate this in your circuit schematic diagrams.

Where Logisim models are required in preparation, make sure you paste a printout of your attempt into your workbook.

D Flip-flop operation

Prepare a circuit schematic diagram for the circuit in Figure 1. Assume the two inputs, *A* and *B* of the AND gate are connected to toggle switches, CK (clock) is connected to a push button and the output *Q* is connected to an LED. Use one of the flip-flops on a 74HCT74 chip and also connect the "set" and "reset" (or "clear") inputs of that flip-flop to push buttons. (Your circuit schematic should indicate this - you can use the flip-flop symbol shown in the pinout diagram).

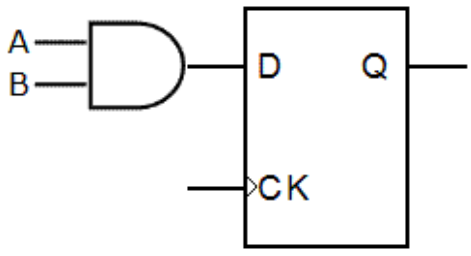

Figure 1. A simple D flip-flop circuit.

Ripple Counter

The circuit of a 3-stage ripple counter is shown in Figure 2. This counter uses D-type flip-flops. The state of each flip-flop is inverted when a 0 to 1 transition (rising edge) occurs at its clock input. Every time Qc goes

from 0 to 1, it inverts Qb. Every time Qb goes from 0 to 1, it inverts Qa. The flip-flops change in rapid succession, and the signal propagates through the counter in a ripple fashion. Ripple counters are also called asynchronous counters. The circuit is considered asynchronous as the clock edges for different flip-flops are able to arrive at different times.

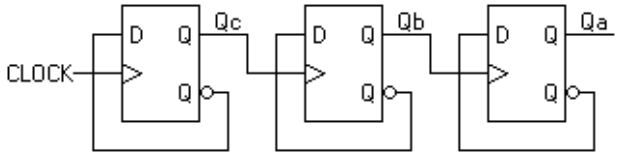

Figure 2. 3-stage ripple counter.

Determine the count sequence for this 3-stage ripple counter when Qc, Qb and Qa start at logic 0. (Note that not all counters are binary counters, i.e., the sequence may not follow a binary counting sequence.)

Prepare a circuit schematic diagram of the 3-stage ripple counter shown in Figure 2. Which of the two flip-flop chips (74HCT74 or 74HCT175 should you use? Hint: Consider how the flip-flops are clocked.) Represent the flip-flops in the circuit schematic diagram by their symbol (e.g. shown for the 74HCT74 & 74HCT175). If there are any flip-flops within a chip not being used in your circuit, connect its D input to GND. The clock input should connect to a toggle switch and reset input will connect to a pushbutton. The three outputs, Qc, Qb and Qa, will connect to a 7-segment display digit on the logic workstation.

Synchronous Counter

Synchronous counters are distinguished from ripple counters in that a single clock signal is wired to the clock inputs of all flip-flops. The common clock triggers all the flip-flops simultaneously on every clock edge. Remember that for each flip flop, the value of Q updates to become the value of D at the time of the rising clock edge. The circuit of a 3-bit synchronous counter is shown in Figure 3.

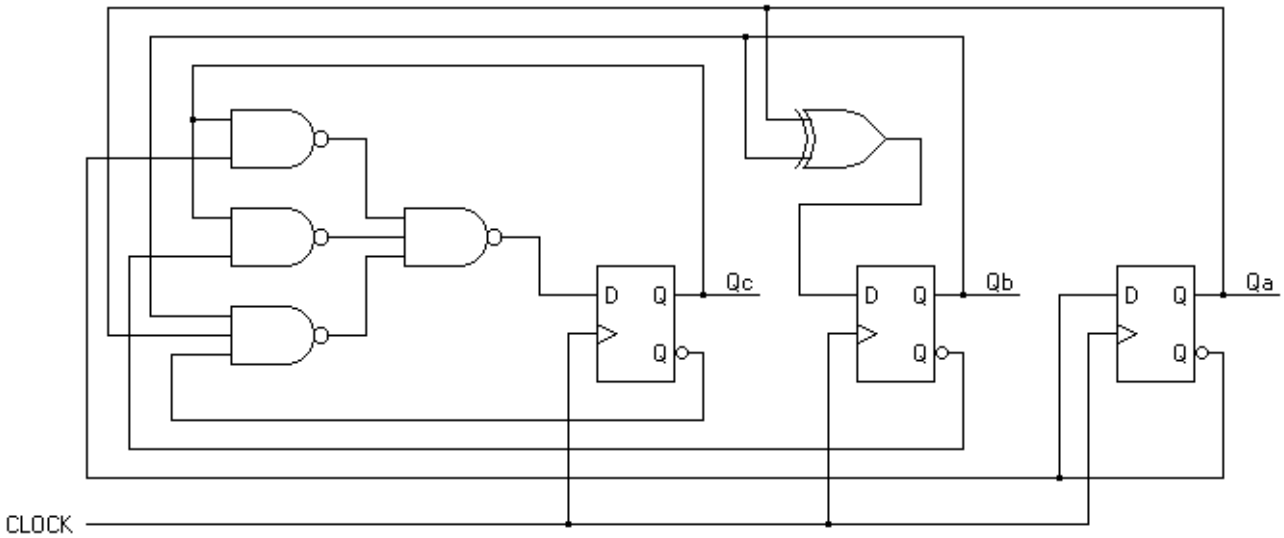

Figure 3. 3-bit synchronous counter.

Determine the count sequence for the 3-bit synchronous counter when Qc, Qb and Qa all start at logic 0.

Prepare a circuit schematic diagram and a LogiSim model of the 3-bit synchronous counter shown in Figure 3. Which of the two flip-flop chips should you use? Represent the flip-flops in the circuit schematic diagram by its symbol (e.g. shown for the 74HCT74 & 74HCT175). Again, if there are any flip-flops within a chip not being used in your circuit, connect its D input to GND. The clock input should connect to a toggle switch and reset input will connect to a pushbutton. The three outputs, Qc, Qb and Qa, will connect to a 7-segment display digit on the logic workstation.

Shift Register

A register capable of shifting its binary information either to the right or to the left is called a *shift register*. Note that again all flip flops are clocked from a single clock wire making this a synchronous circuit. The logical configuration of a shift register consists of a chain of flip-flops connected in cascade, with the output of one flip-flop connected to the input of the next flip-flop. All flip-flops receive a common clock pulse which causes the shift from one stage to the next. The diagram of a 4-bit shift register is shown in Figure 4.

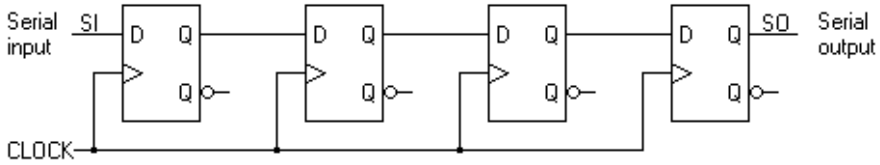

Figure 4. 4-bit shift register.

Prepare a circuit schematic diagram and a LogiSim model of the 4-bit shift register shown above. Which of the two flip-flop chips should you use? The clock(s) and reset input will connect to pushbuttons and the input and output will connect to a toggle switch and LED respectively.

(Optional - Challenge task) Bidirectional Shift Register

Some shift registers have both shift-right and shift-left capabilities. These are called *bidirectional shift registers*. The diagram of a 4-bit bidirectional shift register is shown in Figure 5. It consists of four flip-flops and four 2-input multiplexers. The four multiplexers have a common selection input S which controls the shift direction. When S is 0, the register shifts to the right. When S is 1, the register shifts to the left.

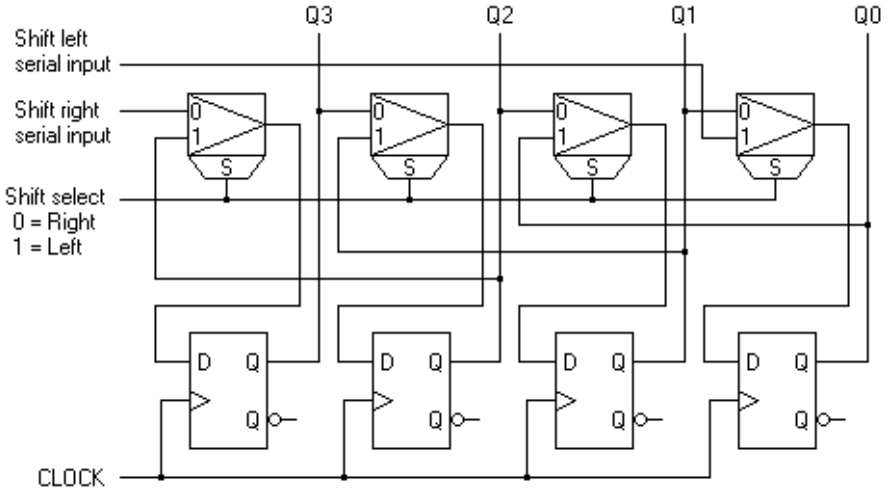

Figure 5. 4-bit bidirectional shift register.

Prepare a circuit schematic diagram of the 4-bit bidirectional shift register implemented using a 74HCT175 quad D-type flip-flop and 74HCT157 quad 2-input multiplexer. The clock and reset input will connect to pushbuttons on the logic workstation. The two shift serial inputs and the shift select input will connect to toggle switches. The four outputs, Q3, Q2, Q1 and Q0, will connect to LEDs (or 7-segment display if you wish).

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Procedure

Ask a tutor to check your preparation, and in particular, provide feedback on your circuit schematic diagrams. (You can start constructing your circuit(s) before this happens.)

Familiarisation with equipment (if necessary):

- Attempt to use the wire stripper to customise the length of a wire.
- If you haven't already, work out how to use the logic probe - the yellow pen shaped object attached to the logic workstation.

Standard Tasks - help will be provided by the tutor if required - don't hesitate to ask any questions. Keep all circuits wired up until the demonstration.

1. Construct and test the D flip-flop circuit shown in Figure 1 using the circuit schematic diagram that you have prepared. Demonstrate to yourself and your partner that the output (Q) can only change on the rising edge of the clock. Document your tests.
2. Construct and test the 3-stage ripple counter circuit using the circuit schematic diagram that you have prepared. Verify the circuit is functioning correctly. Document your tests.
3. Construct and test the 3-bit synchronous counter using the circuit schematic diagram that you have

prepared. Verify that the circuit is functioning correctly. Documents your tests.
4. Construct and test the 4-bit shift register using the circuit schematic diagram that you have prepared. Verify that the circuit is working by devising and inputting a set of interesting test cases. Document your tests.
5. Demonstrate the parts above to the tutor and complete the tutor assigned task. You will not be given the tutor task unless your circuit and simulation work and your workbook is complete to the satisfaction of the tutor.

*Important: **Do NOT use your fingers to remove chips from the breadboard.** Use two pens as levers on both side to "pop" it out. This will avoid the nasty (and painful) metal pins in fingernails problem, and also avoid damage to the chip.*

Challenge Task

Construct the 4 bit bidirectional shift register given in the preparation section.

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Assessment

This practical is marked out of 4 and worth 2% of your mark for CSSE1000:

- Preparation - All circuit schematic diagrams & Logisim schematics completed - ***1 Mark***
- Documentation - All testing results are documented in workbook - ***1 Mark***
- Demonstration - Required circuits demonstrated. - ***1 Mark***
- Tutor Task - Tutor task completed and documented in workbook - ***1 Mark***

Equipment

- Computer
- Logic Workstation
- Breadboard
- Hook up Wire
- Wire Strippers
- Components:

1 x 74HCT00	- Quad 2-input NAND Gate	Datasheet
1 x 74HCT08	- Quad 2-input AND Gate	Datasheet
1 x 74HCT10	- Triple 3-input NAND Gate	Datasheet
2 x 74HCT74	- Dual D-Type Positive Edge-Triggered Flip Flop	Datasheet
1 x 74HCT86	- Quad 2-input XOR Gate	Datasheet
1 x 74HCT157	- Quad 2-input Multiplexer	Datasheet
2 x 74HCT175	- Quad D-Type Flip Flop	Datasheet

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References

- Tanenbaum, Andrew S., *Structured Computer Organization*, 5th Ed., Prentice/Hall, 2006. ISBN: 0-13-148521-0
- Mano, M., *Digital Design*, Prentice/Hall, 1984. ISBN: 0-13-212325-8

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