Prac 2 4209453 Justin Mancinelli

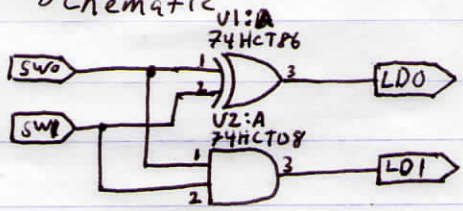
Preparation

Half-Adder

Logic Diagram

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Circuit Schematic

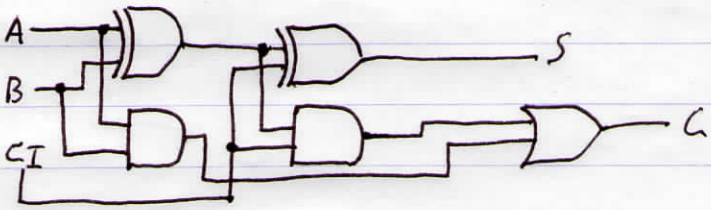


74HCT86: VCC = P14
GND = P7

74HCT08: VCC = P14
GND = P7

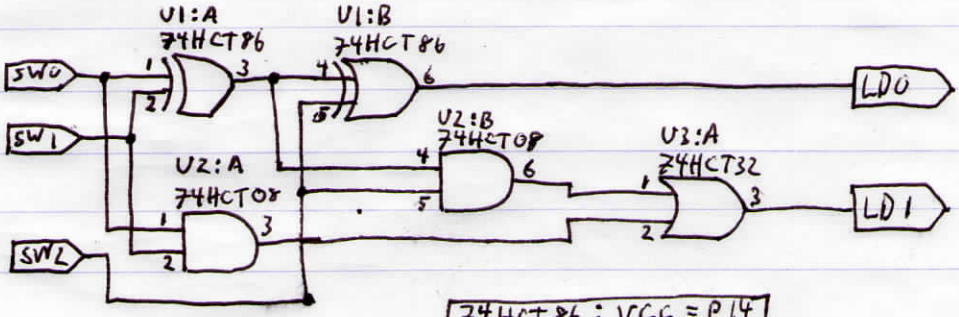
Full-Adder

Logic Diagram



A	B	CI	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Circuit Schematic



74HCT86 : VCC = P14
GND = P7

74HCT08 : VCC = P14
GND = P7

74HCT32 : VCC = P14
GND = P7

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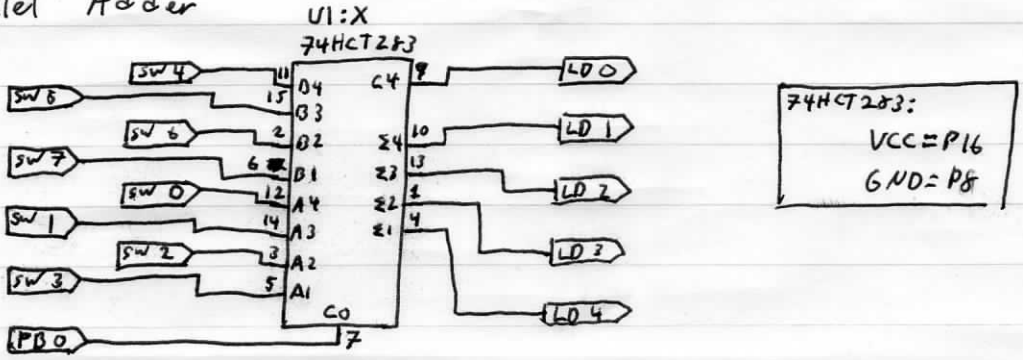
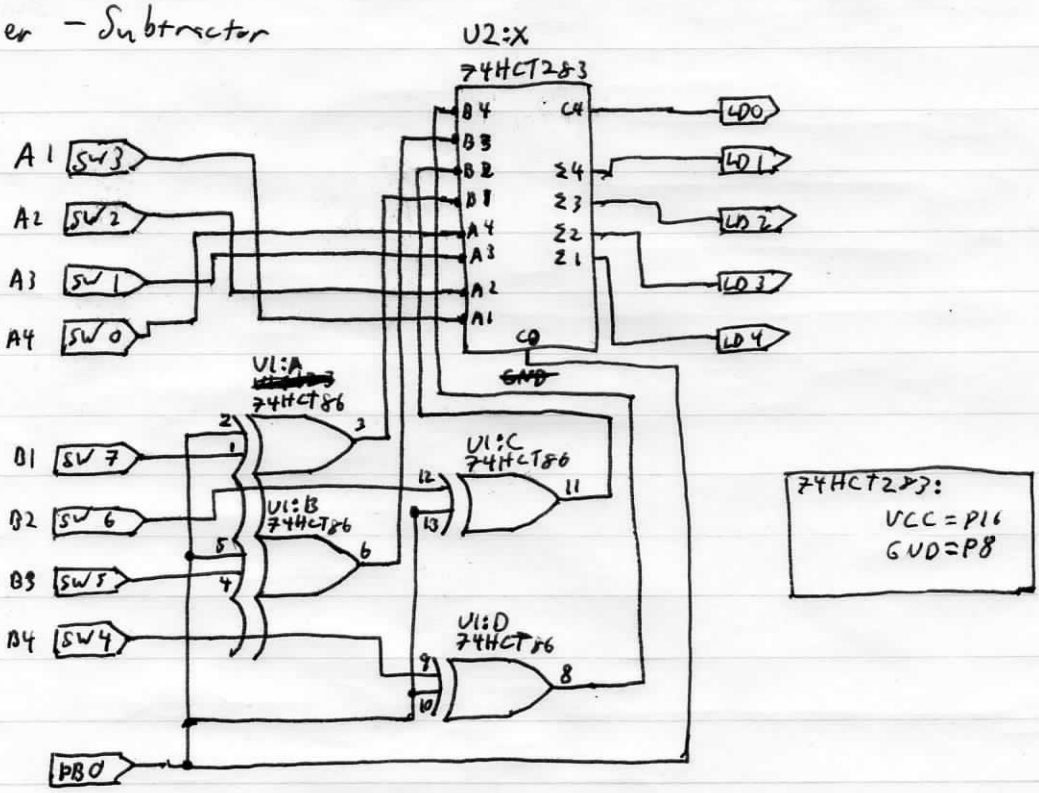
Prep Cont.

Parallel Adder



Adder - Subtractor



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Procedure

0) Initialize breadboard with V_{cc}, GND, and wire up to all chips.

1) Construct and test half-adder

A	B	S	C
1	1	0	1
1	0	1	0
0	1	1	0
0	0	0	0

} Consistant w/ prep

2) Construct full adder - Consistant with Prep and Logisim

3) Construct Adder-Subtractor - Consistant with Logisim

4) Investigate 7-seg display
Each digit in hex has 4 digits in binary
Don't use /LE or /RBI

Conclusion

It is very important to test along the way. Equipment may be faulty so debugging early will catch that early.

The 7-Seg display indicates hex digits which must be wired according to the binary LSB and MSB.

To implement subtraction we used XOR gates to take the one's complement of one set of inputs but two's complement must be used to implement subtraction with an adder. We used a Mode Switch to set one's complement when it is 1 so we wired the mode switch to the carry in of the adder which will give two's complement when the mode switch is high.

Tutor Task

A) $12 - 8 = C_x + (-1)8 = 4$, Tested → A B: C 8, S: (4)

B) $A_x + 2 = 10 + 2 = 12 = C_x$ Test → A 2 (C)

C) $6 - 10 = 6 - A_x = -4 = -1(4) = C_x$ Test → 6 8 (C)

D) $2 - (-2) = 0010 - (-1)0010 = 0010 - 1110 = 2 - 14 = 2 - E_x = 0$

Test → A 2, B E (0)