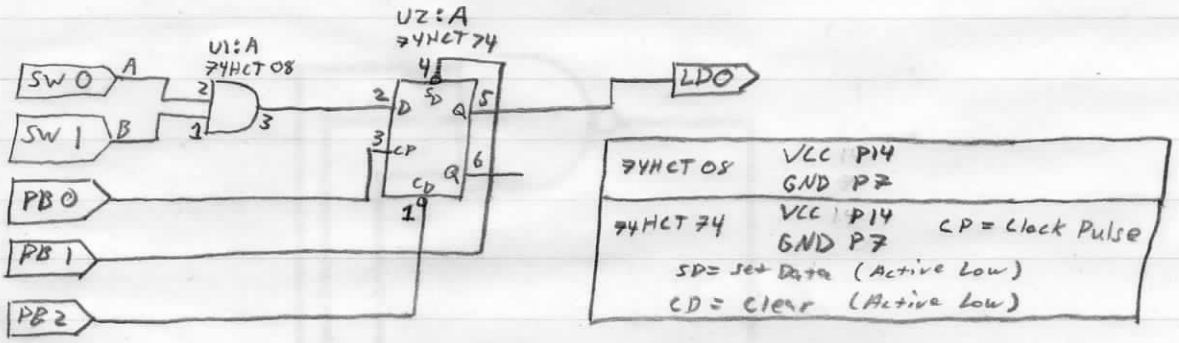
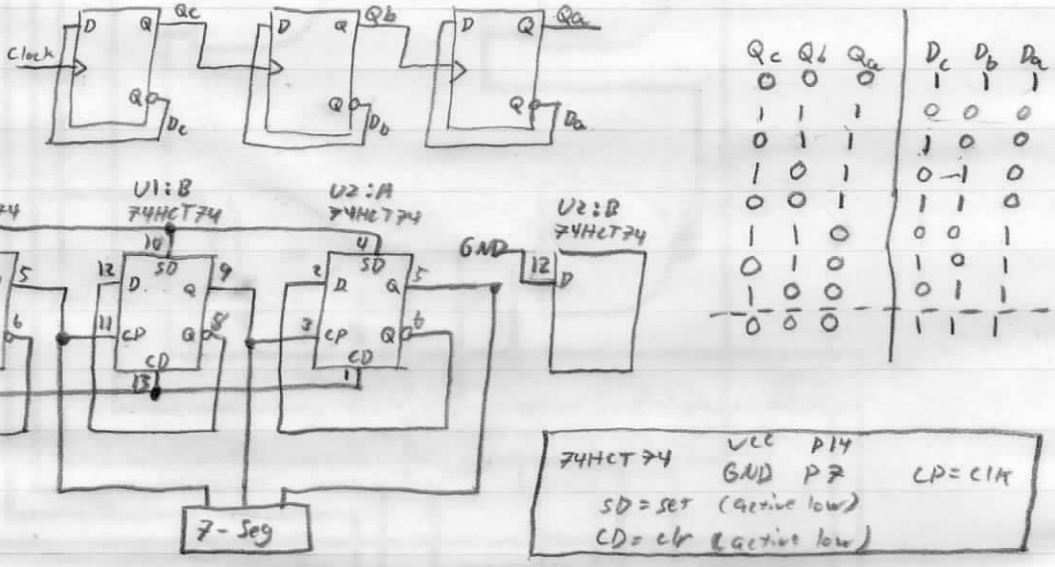
Prac 3 4209435 Justin Mancinelli

Preparation

D Flip-flop Operation



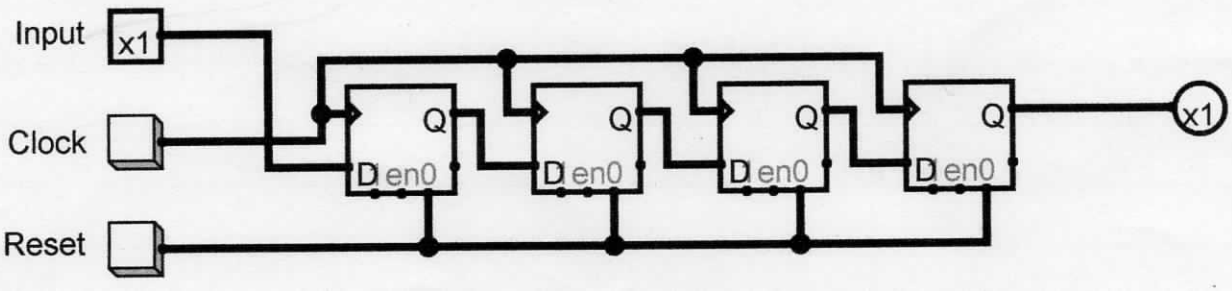
Ripple Counter



Use the 74HCT74 so that the clocks can be asynchronous.

4-bit Shift Register

main (1 of 1)



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Prep. Cont.

Synchronous Counter

P2	P7	P10			
Q_c	Q_b	Q_a	D_c	D_b	D_a
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

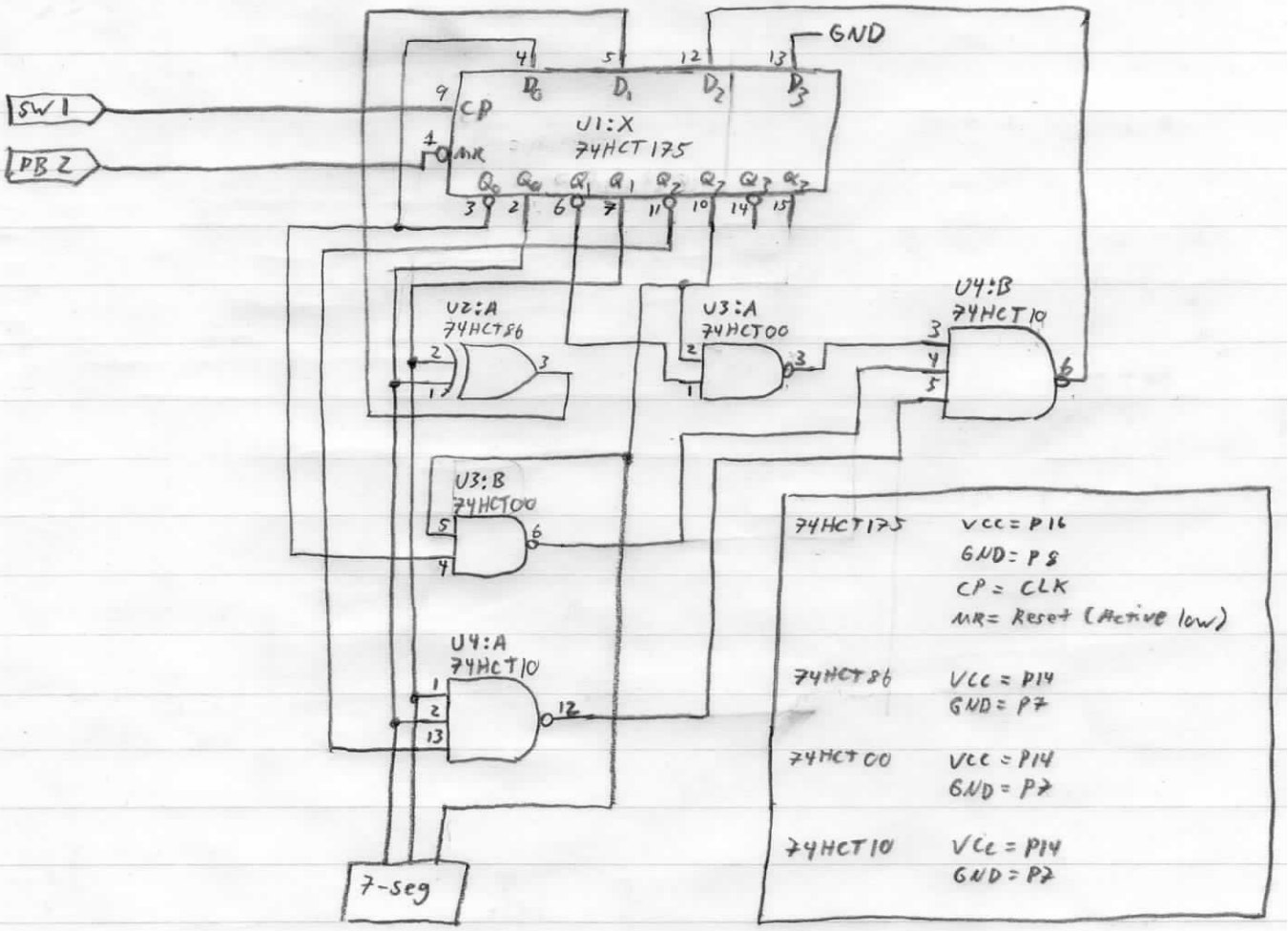
USB

$$D_a = \overline{Q_a}$$

$$D_b = Q_a \oplus Q_b$$

$$D_c = \overline{(\overline{Q_c Q_a})(\overline{Q_c Q_b})(\overline{Q_b Q_a Q_c})}$$

$$= Q_c\overline{Q_a} + Q_c\overline{Q_b} + Q_b Q_a \overline{Q_c}$$



$$D_0 = \overline{(\overline{Q0\ Q2})(\overline{Q0\ Q1})(\overline{Q1Q2\overline{Q0}})}$$

$$= (Q0\overline{Q_2}) + (Q0\overline{Q1}) + (Q1Q2\overline{Q0})$$

00 1110 1110 1110

09 1111 0000 1111 00

1 Prep min

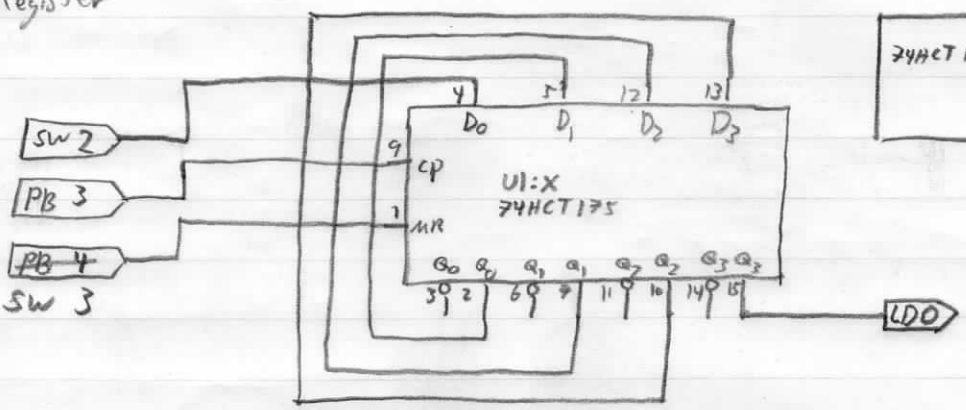
Proc 3

1 Dsc

1 Demo

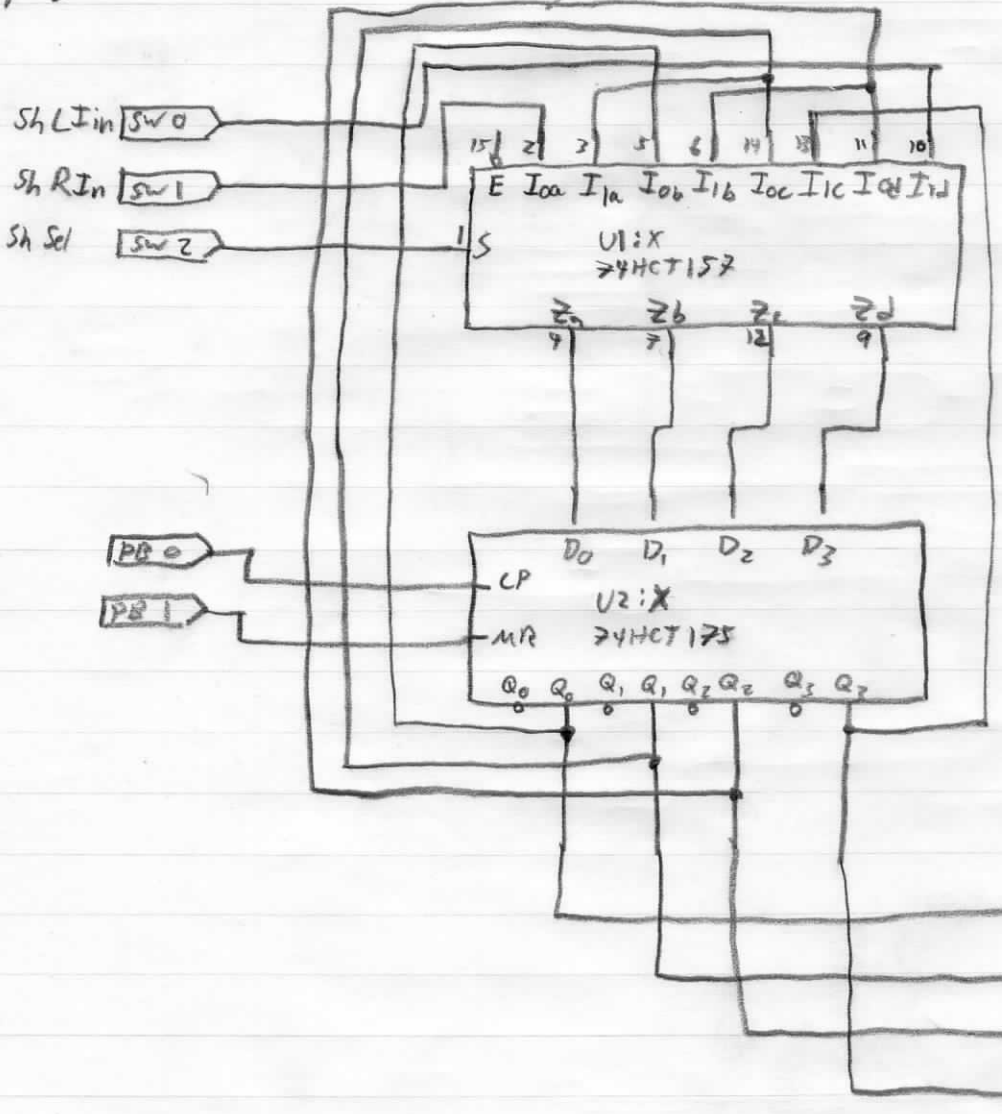
Prep Cont.

Shift Register



74HCT 175 VCC = P16 GND = P8

(Opt) Bidirectional Shift Register



Sh Sel = 0 → Sh Right

74HCT 175 VCC = P16 GND = P8

74HCT 157 VCC = P16 GND = 8

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Procedure

D Flip-Flop operation

Tests: ① push clear — led off
② push set — led on
③ set AND Low — no change
④ push clock — led off
⑤ set AND High — no change
⑥ push clock — led on

Ripple Counter

Test: ① pulse the clock → count = 0, 7, 3, ⋯, 0, ⋯
Note this count is opposite order of my prep count. This is because the flipflops were wired in the opposite sequence.

Synchronous Counter

Test ① pulse the clock → XOR output as expected
NAND output as expected
$\overline{Q} \rightarrow D$ Feedback as expected
② Check Hex Display → Count = C, 1, 2, ⋯, 7, 0,

Shift Register

Test ① clear → all outputs 0
② send 1 to D0 → all outputs 0
③ push clock → Q0 is high, all others 0
④ pulse clock → digit shifts as expected

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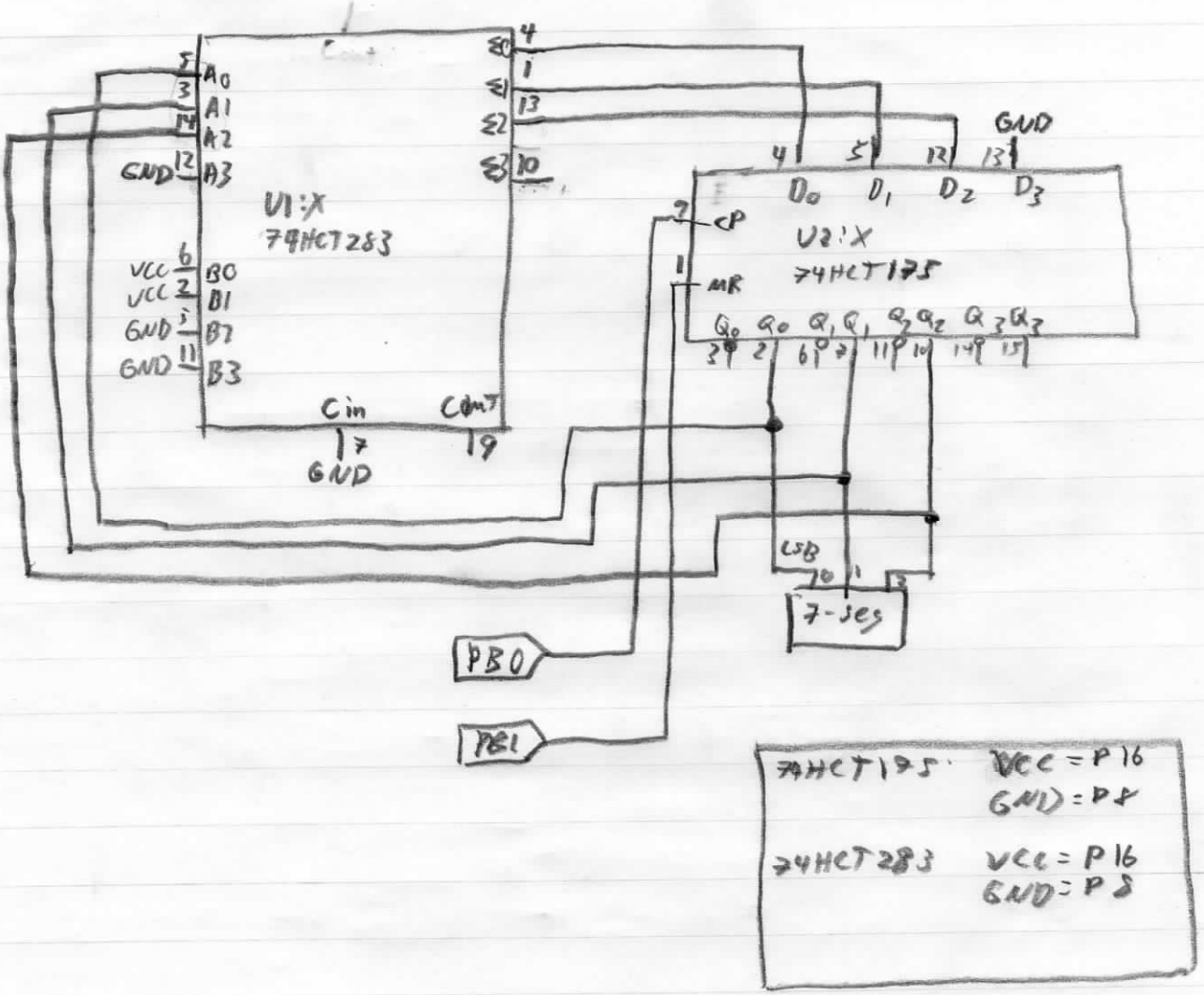
Tutor Task



The adder must always add 3 to the current number. so set $B0 = B1 = 1$ and $B2 = B3 = 0$ for $3_{10} = 0011_2$ S3 is not required because we only care about numbers less than or equal to 7.

This is a synchronous counter because the clock updates all flip-flops at the same time.

This approach is better than gates because it is simple to implement but it may be slower than gates.