

# Synthesis Report

Testbench	Pass
Clock Cycle	10 (ns)
Cell Area	41021.066203 (Please report <b>Total cell area</b> )
Total Time	9640 for p1 data ; 9650 for p2 data (ns)
Area*Time	395443078.2 for p1 data ; 395853288.3 for p2 data

## Synthesis No-latch (screenshot)

counter_reg	Flip-flop	10	Y	N	Y	N	N	N	N	N
Inferred memory devices in process in routine IOTDF line 48 in file '/home/raid7_2/userb10/b10151/ICD2024/HW3/02_SYN/IOTDF.v'.										
Register Name	Type	Width	Bus	MB	AR	AS	SR	SS	ST	
counter_delay1_reg	Flip-flop	4	Y	N	N	N	N	N	N	N
counter_delay2_reg	Flip-flop	4	Y	N	N	N	N	N	N	N
Inferred memory devices in process in routine IOTDF line 59 in file '/home/raid7_2/userb10/b10151/ICD2024/HW3/02_SYN/IOTDF.v'.										
Register Name	Type	Width	Bus	MB	AR	AS	SR	SS	ST	
wait_to_reg	Flip-flop	128	Y	N	N	N	N	N	N	N
iot_data_reg	Flip-flop	128	Y	N	Y	N	N	N	N	N
Inferred memory devices in process in routine IOTDF line 135 in file '/home/raid7_2/userb10/b10151/ICD2024/HW3/02_SYN/IOTDF.v'.										
Register Name	Type	Width	Bus	MB	AR	AS	SR	SS	ST	
valid_reg	Flip-flop	1	N	N	Y	N	N	N	N	N
Inferred memory devices in process in routine IOTDF line 162 in file '/home/raid7_2/userb10/b10151/ICD2024/HW3/02_SYN/IOTDF.v'.										
Register Name	Type	Width	Bus	MB	AR	AS	SR	SS	ST	
iot_out_reg	Flip-flop	128	Y	N	Y	N	N	N	N	N
Presto compilation completed successfully.										

## Synthesis slack (screenshot)

clock clk (rise edge)	10.00	10.00
clock network delay (ideal)	1.00	11.00
clock uncertainty	-0.10	10.90
iot_out_reg[0]/CK (DFFRX1)	0.00	10.90 r
library setup time	-0.13	10.77
data required time		10.77
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data required time		10.77
data arrival time		-10.72
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slack (MET)		0.06