Motor Driver IC Series for Printers

Bipolar Stepping Motor Drivers for Paper Feed or Carriage Use

BD6775EFV, BD6384EFV

●Description

The BD6775EFV and BD6384EFV are PWM constant-current drivers that are operable in full-step, half-step, and quarter-step mode. The BD6384EFV allows the selection of current decay modes, thus making it possible to realize optimum control under a variety of conditions.

●Features

1) Low on-resistance DMOS
2) Power-saving function
3) TSD (Thermal Shutdown) circuit
4) UVLO (Under Voltage Locked Out) circuit
5) Compact, thin-shape, and high heat dissipation package
6) Current decay mode selection (BD6384EFV)
7) OCP (Over Current Protection) circuit (BD6384EFV)

●Applications

Laser beam printer, PPC, scanner, photo printer, fax, ink-jet printer, and mini printer.

●Absolute maximum ratings (Ta=25℃)

	Symbol	BD6775EFV	BD6384EFV	Unit
Power supply voltage	VCC	7	7	V
Motor power supply voltage	VM	40	36	V
Power dissipation	Pd	1100(*1)	1600(*2)	mW
Operating temperature range	Topr	-20～+75	-25～+85	℃
Storage temperature range	Tstg	-55～+150	-55～+150	℃
Junction temperature	Tjmax	150	150	℃
Output current	IOUT	800(*3)	1500(*3)	mA
RNF voltage	VRNF	-	0.5	V

*1 Reduced by 8.8mW/°C over 25°C, when mounted on a glass epoxy board (70mm × 70mm × 1.6mm).
*2 Reduced by 12.8mW/°C over 25°C, when mounted on a glass epoxy board (70mm × 70mm × 1.6mm).
*3 Must not exceed Pd or ASO.

●Operating conditions

Parameter	Symbol	BD6775EFV	BD6384EFV	Unit
Power supply voltage	VCC	4.5～6.0	3.0～5.5	V
Motor power supply voltage	VM	10～37	16～28	V
Output current(max)	IOUT	500(*1)	1200(*1)	mA

*1 Must not exceed Pd or ASO.

●Electrical characteristics

1) BD6775EFV (Unless otherwise specified, Ta=25°C, VCC=5.0 V, VM=35V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Overall						
VCC circuit current during standby mode	ICCST	250	360	400	uA	PS=0V, VREF=2V
VCC circuit current	ICC	4.4	5.8	7.2	mA	PS=H, VREF=2V
VM circuit current during standby mode	IVMST	-	0	10	uA	PS=0V, VREF=2V
VM circuit current	IVM	2	3	4	mA	PS=H, VREF=2V
Power-saving						
High-level input voltage	VPSH	2.0	-	-	V	
Low-level input voltage	VPSL	-	-	0.8	V	
High-level input current	IINH	25	50	80	uA	VIN=5V
Low-level input current	IINL	5	10	16	uA	VIN=1V
Control input						
High-level input voltage	VINH	2.0	-	-	V	PHA1,PHA2,I01,I11,I02,I12
Low-level input voltage	VINL	-	-	0.8	V	PHA1,PHA2,I01,I11,I02,I12
Output						
Output on resistance	RON	-	3	3.6	Ω	IOUT=±300mA, on high and low sides in total
Output leak	ILEAK	-	0	10	uA	
Current control block						
RNFX inflow current	IRNF	-2	-0.6	-	uA	RNF=0V
VREFX inflow current	IVREF	-1	-0.1	-	uA	VREF=0V
VREFX voltage range	VREF	0	-	2.0	V	
Comparator threshold 100%	CTHLL	0.34	0.4	0.46	V	VREF=2V, I0x=L,I1x=L
Comparator threshold 67%	CTHHL	0.227	0.267	0.307	V	VREF=2V, I0x=H,I1x=L
Comparator threshold 33%	CTHLH	0.113	0.133	0.153	V	VREF=2V, I0x=L,I1x=H
Minimum on time	TMINON	0.3	0.5	1.0	us	R=39kΩ, C=1000pF, Output 100Ω load

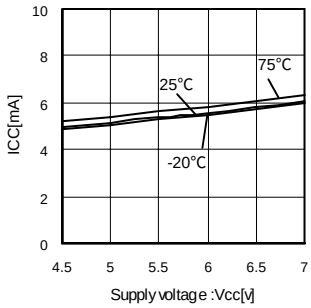


Fig.1 VCC Circuit Current (BD6775EFV)

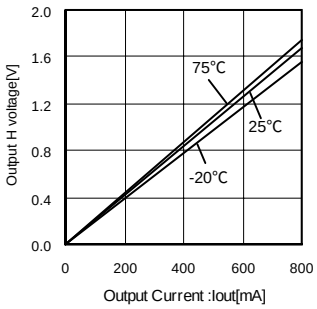


Fig.2 High Output Voltage (BD6775EFV)

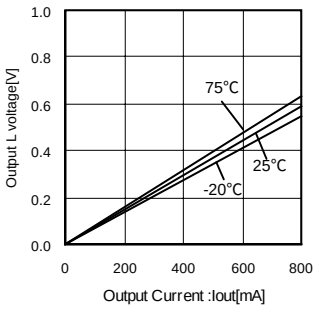


Fig.3 Low Output Voltage (BD6775EFV)

2) BD6384EFV (Unless otherwise specified, Ta=25°C, VCC=5.0V, VM=24V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Overall						
VCC circuit current at standby	ICCST	-	0	10	uA	PS=L
VCC circuit current	ICC	-	3	5	mA	PS=H, VREFX=2V
VM current at standby	IVMST	-	0	10	uA	PS=L
VM circuit current	IVM	-	1.5	3	mA	PS=H, VREFX=2V
Control input VCC = 3.3V						
H level input voltage	VINH1	2.0	-	3.3	V	
L level input voltage	VINL1	0	-	0.8	V	
Control input VCC = 5.0 V						
H level input voltage	VINH2	2.5	-	5.0	V	
L level input voltage	VINL2	0	-	0.8	V	
Output						
Output ON resistance	RON	-	1.2	1.44	Ω	IOUT=±1.0A, on high and low sides in total
Output leak current	ILEAK	-	-	10	uA	
Current control block						
RNFX_REF input current	IRNF_REF	-2	-0.6	-	uA	RNFX_REF=0V
RNFX input current	IRNF	-40	-20	-	uA	
VREFX input current	IVREF	-1	-0.1	-	uA	VREFX=0V
VREFX input voltage range	VREF	0	-	2	V	
MTHX input current	IMTH	-1	-0.1	-	uA	MTHX=0V
MTHX input voltage range	MTH	0	-	2	V	
Comparator threshold (100%)	CTHLL	0.34	0.4	0.46	V	VREFX=2V,I0x=L,I1x=L
Comparator threshold (67%)	CTHHL	0.227	0.267	0.307	V	VREFX=2V,I0x=H,I1x=L
Comparator threshold (33%)	CTHLH	0.113	0.133	0.153	V	VREFX=2V,I0x=L,I1x=H
Minimum on time	TMINON	0.3	0.7	1.2	usec	R=39kΩ,C=1000pF

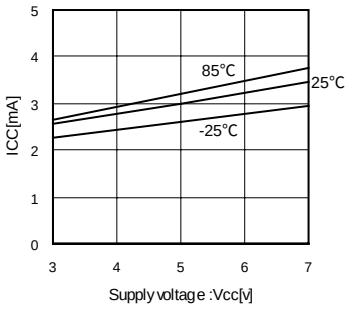


Fig.4 VCC Circuit Current
(BD6384EFV)

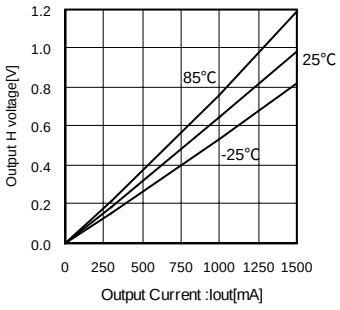


Fig.5 High Output Voltage
(BD6384EFV)

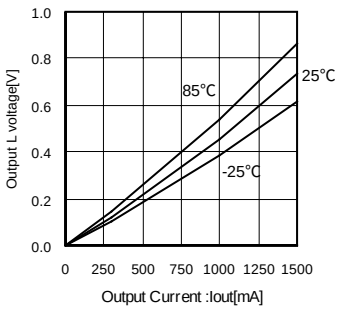


Fig.6 Low Output Voltage
(BD6384EFV)

●Block diagram, Application circuit diagram, and Pin function

1) BD6775EFV

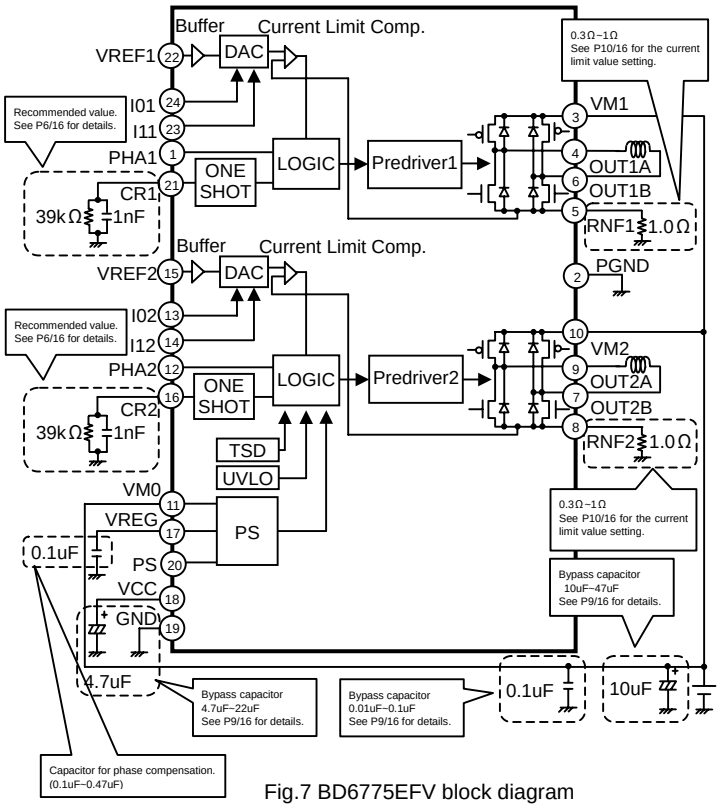
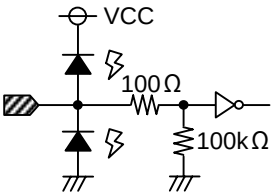


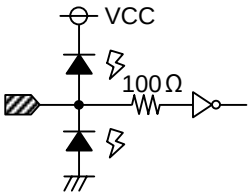
Fig.7 BD6775EFV block diagram

PIN No.	Pin name	Function
1	PHA1	Phase selection pin 1
2	PGND	GND
3	VM1	Motor power supply pin 1
4	OUT1A	H-bridge output pin 1A
5	RNF1	Output current detection pin 1
6	OUT1B	H-bridge output pin 1B
7	OUT2B	H-bridge output pin 2B
8	RNF2	Output current detection pin 2
9	OUT2A	H-bridge output pin 2A
10	VM2	Motor power supply pin 2
11	VM0	Power supply pin 0
12	PHA2	Phase selection pin 2
13	I02	VREF division ratio setting pin 02
14	I12	VREF division ratio setting pin 12
15	VREF2	Reference voltage input pin 2
16	CR2	CR pin 2
17	VREG	Regulating voltage output pin
18	VCC	Power supply pin
19	GND	GND
20	PS	Power-saving pin
21	CR1	CR pin 1
22	VREF1	Reference voltage input pin 1
23	I11	VREF division ratio setting pin 11
24	I01	VREF division ratio setting pin 01

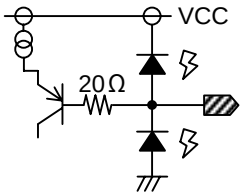
PS(20)



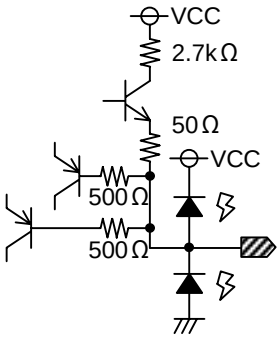
Logic input(1,12～14,23,24)



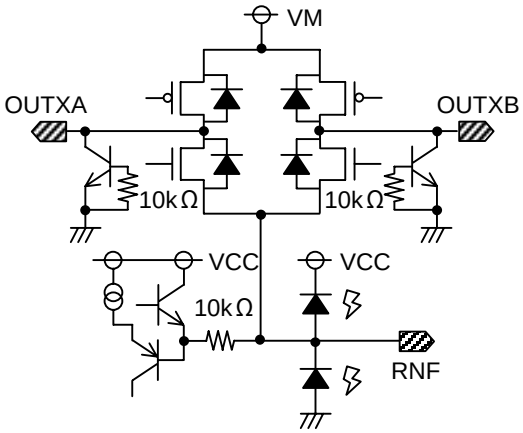
VREF1,2 (15,22)



CR1,2 (21,16)



OUT1A～2B、RNF1,2 (4～9)



VREG(17)

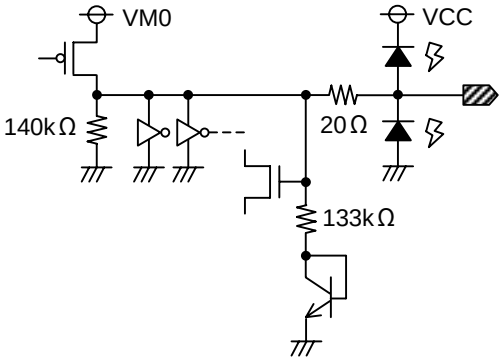


Fig.8 BD6775EFV I/O circuit diagram

3) BD6384EFV

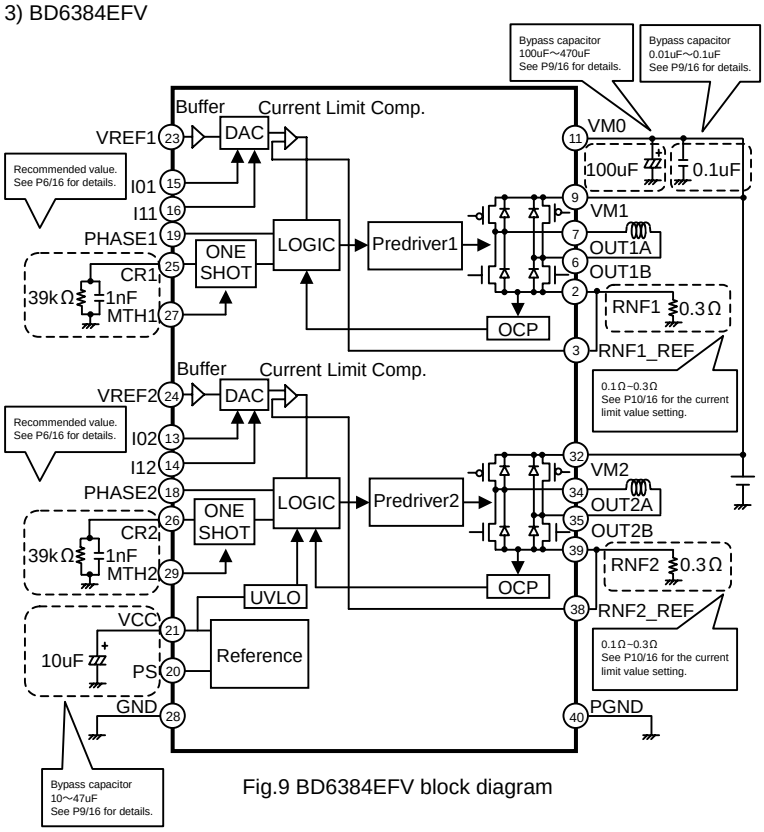
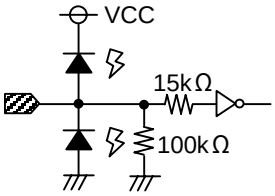
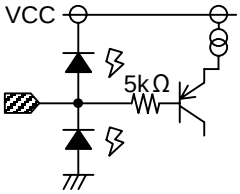


Fig.9 BD6384EFV block diagram

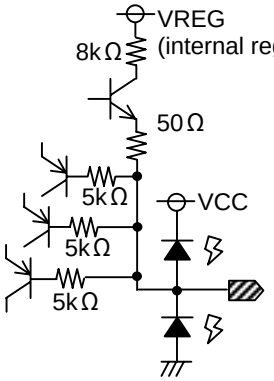
Logic input(13～16,18～19,20)



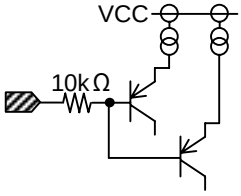
VREF1,2 MTH1,2(23,24,27,29)



CR1,2(25,26)



RNF1,2_REF(3,38)



OUT1A～2B(6,7,34,35), RNF1,2(2,39)

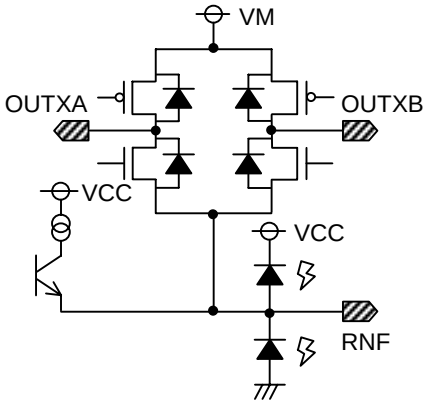


Fig.10 BD6384EFV I/O circuit diagram

PIN No.	Pin name	Function
1	N.C.	N.C.
2	RNF1	Output current detection pin
3	RNF1_REF	Current limit comp. input pin
4	N.C.	N.C.
5	N.C.	N.C.
6	OUT1B	H-bridge output pin
7	OUT1A	H-bridge output pin
8	N.C.	N.C.
9	VM1	Motor power supply pin
10	N.C.	N.C.
11	VM0	Motor power supply pin
12	N.C.	N.C.
13	I02	VREF division ratio setting pin 02
14	I12	VREF division ratio setting pin 12
15	I01	VREF division ratio setting pin 01
16	I11	VREF division ratio setting pin 11
17	N.C.	N.C.
18	PHASE2	Phase selection pin
19	PHASE1	Phase selection pin
20	PS	Power-saving pin
21	VCC	Power supply voltage pin
22	N.C.	N.C.
23	VREF1	Reference voltage input pin
24	VREF2	Reference voltage input pin
25	CR1	CR pin
26	CR2	CR pin
27	MTH1	Decay mode setting pin
28	GND	GND pin
29	MTH2	Decay mode setting pin
30	N.C.	N.C.
31	N.C.	N.C.
32	VM2	Motor power supply pin
33	N.C.	N.C.
34	OUT2A	H-bridge output pin
35	OUT2B	H-bridge output pin
36	N.C.	NC
37	N.C.	NC
38	RNF2_REF	Current limit comp. input pin
39	RNF2	Output current detection pin
40	PGND	GND pin

●PWM constant-current control

1) Current Control Operation

The output current increases when the output transistors turn on. When the RNF voltage (i.e., a voltage converted from the output current by the external resistance on the RNF pin) reaches a current limit value determined by the VREF voltage and VREF division ratio setting pin, the current limit comparator activates, and the current decay mode will turn on. After the off time (Toff), caused by the CR timer, the output will be turned on again. This cycle is repeated.

2) Noise Canceling Function

In order to avoid the incorrect detection of the current detection comparator, due to spike noise that occurs when the output is turned on, the noise canceling time (Tn) is provided. Current detection is disabled for the noise canceling time after the output is turned on. Noise canceling time is equal to minimum on time.

3) CR Timer

The voltage on the CR pin will be clamped at approximately 0.9V when the output is turned on. When the output current reaches the current limit value and the current decay mode is turned on, the CR pin will start discharging the electricity. When the electricity is discharged until the voltage reaches approximately 0.4V, the output will be turned on again and the CR pin will start charging electricity. The time required to discharge approximately 0.9V to 0.4V is the off time (Toff). Moreover, the time it takes to charge from about 0.4V to about 0.8V, after CR pin starts charging, is equal to the noise canceling time (Tn). Toff and Tn can be set by the constants of components attached externally to the CR pin in the following equation (typ.):

$$Toff(s) \quad C \times R \times 0.81$$

$$Tn(s) \quad C \times R' \times \ln [(VCR-0.4)/(VCR-0.8)]$$

But, $VCR = V \times R/(R'+R)$

V: VCC voltage (BD6775EFV), internal regulator voltage of 13 V (BD6384EFV)

R': CR pin internal impedance of approximately 5kΩ (BD6775EFV), approximately 15kΩ (BD6384EFV)

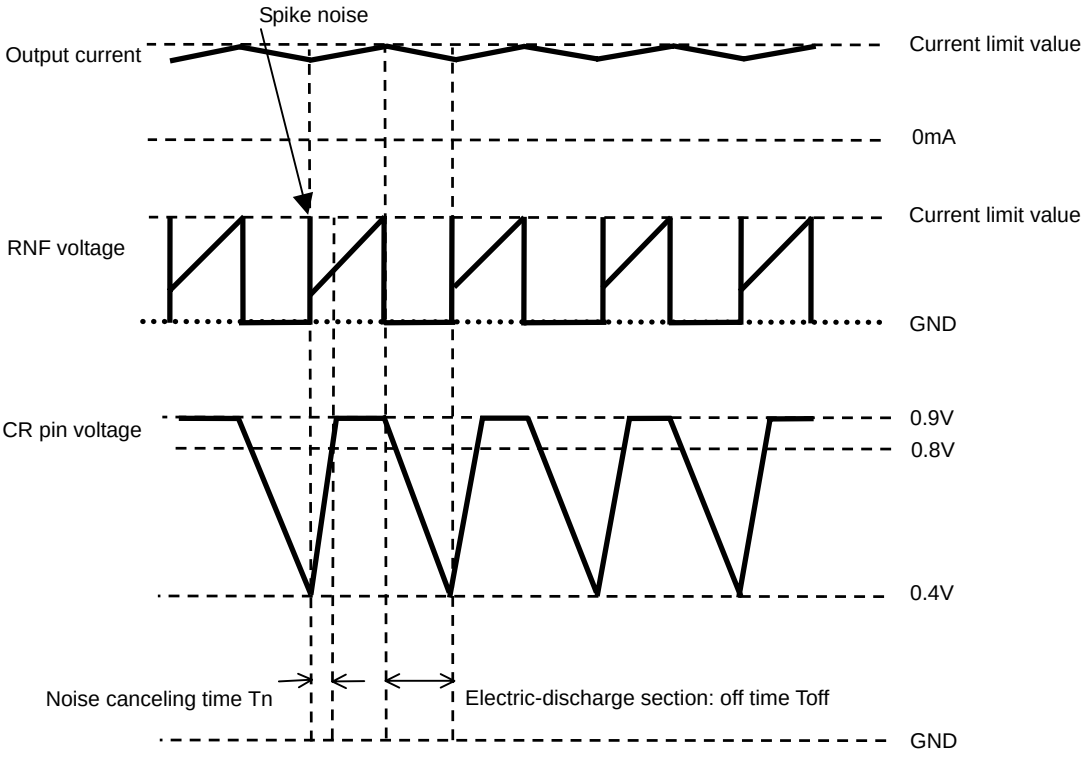


Fig.11 CR Voltage, RNF Voltage, Output Current Timing Chart

If the resistance on the CR pin is too low, the voltage on CR pin will not reach a clamp voltage of approximately 0.9V. Use a resistance of approximately 15kΩ or over. (The recommended resistance is 15kΩ to 100kΩ.) If a capacitor with a value of a few thousand pico farad is used (470pF to 3300pF is recommended), the noise canceling time (Tn) will become long, and the output current flowing may be higher than the current limit value, depending on the motor coil impedance. If off time (Toff) is set to a longer value, the ripple of the output current will increase. This may drop the average current which may reduce rotation efficiency. Select the optimum value so that motor drive sound and the distortion of the output current waveform will be minimized.

●**Control sequence of stepping motor**(2 phase stepping motor, 2 pole rotor,unit step angle=90 °)

Full-step (2-phase excitation), half-step (1-2-phase excitation), and quarter-step (W1-2-phase excitation) driving modes are enabled by control input pins, the phase selection pins (PHAx and PHASEx) and the VREF division ratio setting pins (I0x, I1x). Input pattern examples for respective excitation modes are shown below. The figure Torque Vector shows typically the relation of the minimum step angles and the levels and directions of currents flowing into motor coils in respective excitation modes. The vector will be in the OUTA direction when the current flows from OUTA to OUTB, and the scale of the vector is determined with the VREF division ratio setting pin. The position of the vector refers to the rotation position of the motor. While in half-step mode, the phase selection pins for phase 1 and phase 2 are both in high-level logic in timing chart ①. The VREF division ratio setting pins are both (I0x, I1x) = (H, L). Therefore, a vector with a scale of 67% will be located in the OUT1A direction and OUT2A direction. (See pages 11 and 12 for the phase selection pins and VREF division ratio setting pins in detail.) The vector in ① is synthesized from these two vectors. In ②, since (I01, I11) = (H, H) (I02, I12) = (L, L), no current flows to OUT1, and a 100% current flows to OUT2 only. It is possible to consider ③ to ⑧ in the same way. The minimum step angle is 90° in full-step mode, 45° in half-step mode, and 22.5° in quarter-step mode.

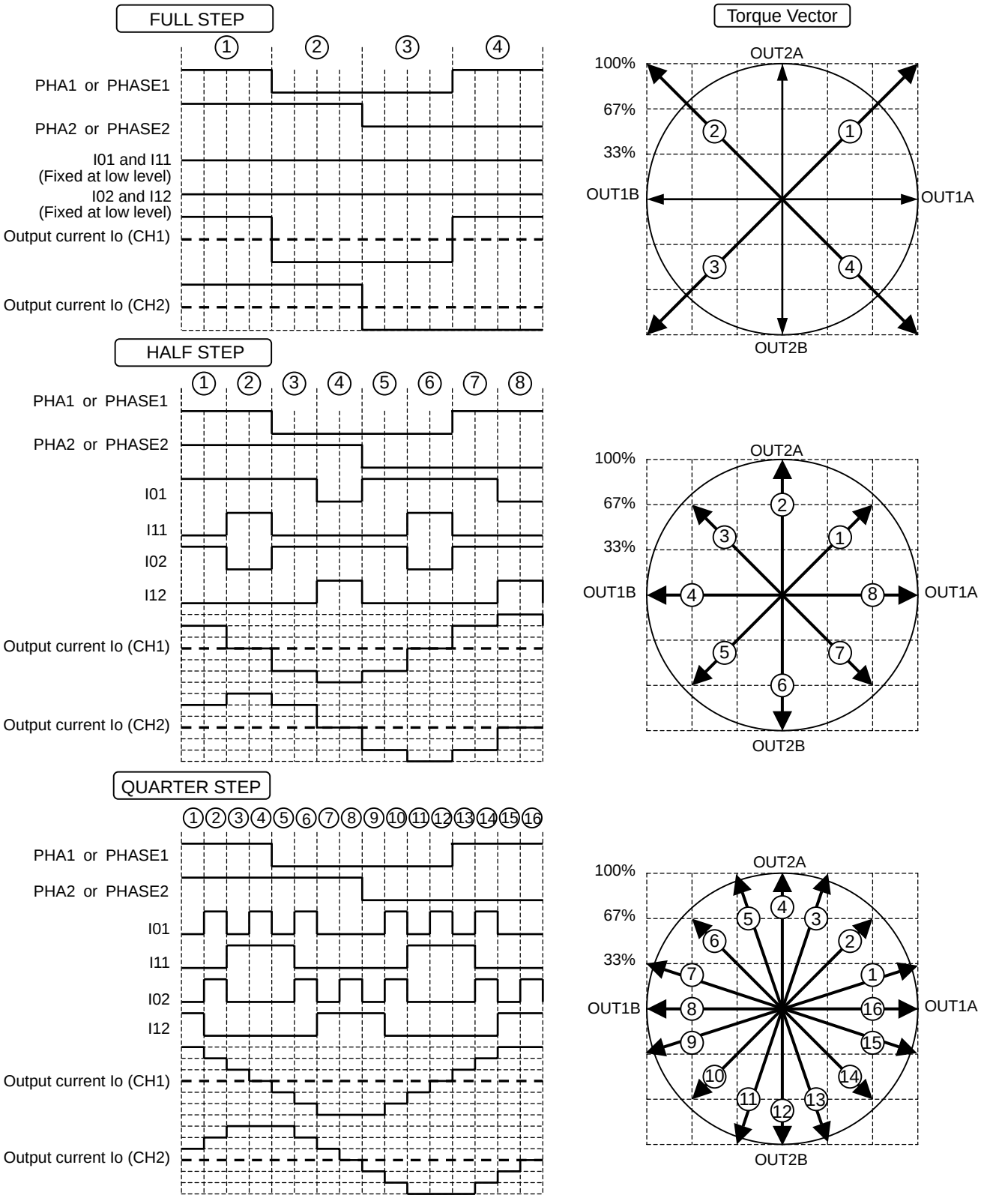
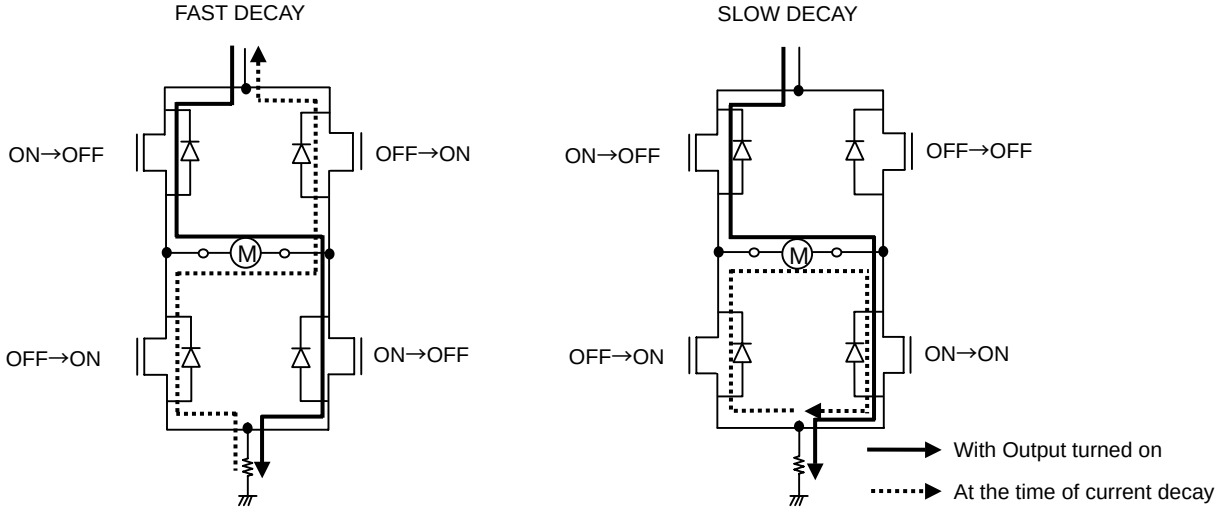


Fig.12 Control Sequence Example

●**Current decay mode**

The BD6775EFV performs current decay in SLOW DECAY mode. The BD6384EFV performs current decay in SLOW DECAY, FAST DECAY, or MIXE DECAY mode, through the decay mode setting pin MTH. Both SLOW DECAY and FAST DECAY occur in synchronous rectification mode. See below for the condition of the output transistors in each decay mode and the path of the regenerated currents.



FAST DECAY will be switched to SLOW DECAY if the current flows in the reverse direction.

Fig.13 Regenerated Current Path at the Time of Current Decay.

See below for the feature of each decay mode.

○SLOW DECAY

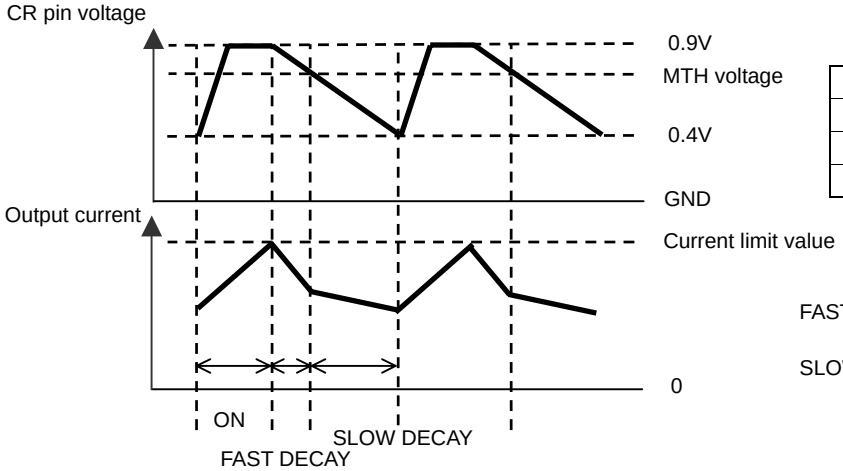
At the time of current decay, the voltage on each motor coil will be low and the regenerated current will be attenuated slowly with low current ripples. This is advantageous for motor torque to maintenance. There will be, however, an output current increase in the small current region, due to the degradation of current control performance. Furthermore, the output will be easily affected by counterelectromotive voltage of the motor driven at high pulse rates in half-step or quarter-step mode. Therefore, the output cannot catch up with the change of the current limit value, thus deforming the current waveform and resulting in an increase in motor vibration. The decay mode is suitable to the operation of the motor in full-step mode or the motor driven at low-pulse rates in half-step or quarter-step mode.

○FAST DECAY

The regenerated current decreases rapidly, thus mitigating the deformation of the current waveform while the motor is driven at high-pulse rates. The ripples of the output current, however, will become high, thus dropping the average current and the following items will result: (1) The motor torque will drop. A countermeasure can be taken by increasing the current limit value, but the output rated current must be taken into consideration. (2) Motor loss will become great with an increase in heat generation. The decay mode is suitable to the operation of the motor driven at high pulse rates in half-step or quarter-step mode.

●**MIXED DECAY** (BD6384EFV)

The MIXED DECAY mode is available for an improvement in the above problems that occur while in SLOW DECAY or FAST DECAY mode. By switching the FAST DECAY and SLOW DECAY of the current, current control performance can be improved if the current ripples are suppressed. Furthermore, the time ratio of SLOW DECAY and FAST DECAY can be changed by MTH input voltage, which realizes optimum control for a variety of conditions. While in MIXED DECAY mode, the point of changing FAST DECAY to SLOW DECAY will vary with the voltage on the CR pin at the time of current discharge and with the level of MTH voltage. The FAST DECAY time and SLOW DECAY time, while in MIXED DECAY mode, are expressed in the following equations (typ.):



MTH pin input voltage	DECAY MODE
0~0.3V	FAST DECAY
0.4~0.9V	MIXED DECAY
1.5~2V	SLOW DECAY

FAST DECAY time:Toff_f(s)　C×R×ln (0.9/MTH)

SLOW DECAY time:Toff_s(s)　Toff-Toff_f

Fig.14 Relation of CR Pin Voltage, MTH Voltage, and Output Current during MIXED DECAY

●Pin description and board layout precautions

○PHA, PHASE/Phase Selection Pin

The output logic is determined. BD6384EFV Supports 5.0/3.3V logic. System.

When this pin is open in BD6384EFV, input logic is L for 100 kΩ pull down resistor.

PHA、PHASE	OUTA	OUTB
L	L	H
H	H	L

	PHA,PHASE	VCC=5.0V	VCC=3.3V
BD6775EFV	High input voltage	2.0～5.0V	Not supported
	Low input voltage	0～0.8V	Not supported
BD6384EFV	High input voltage	2.5～5.0V	2.0～3.3V
	Low input voltage	0～0.8V	0～0.8V

○PGND/GND pin

The GND for output driving circuits. Switching noise is generated because the MOS circuit is driven. Perform low impedance wiring so that there will be no impedance in common with any other GND pattern.

○VCC pin/power supply pin

Perform low impedance wiring. Connect a bypass capacitor with a capacitance value of 4.7 μF to 22 μF to the BD6775EFV and 10 μF to 47 μF to the BD6384EFV as close to the pins as possible.

○VM0, VM1, and VM2/Motor Power Supply Pin

Perform low impedance wiring due to the motor drive current flows. The VM voltage may fluctuate due to the back electromotive force of the motor and PWM switching noise. Therefore, connect a bypass capacitor with a capacitance of 10 μF to 47 μF to the BD6775EFV and 100 μF to 470 μF to the BD6384EFV. The capacitors should be as close as possible to the pins for VM voltage stabilization. Also we recommend that ceramic capacitor of 0.01uF to 0.1uF is connected in parallel. Make sure that the VM voltage will not be in excess of the rated value for any length of time. Be sure to short the VM0, VM1, and VM2 pins.

○OUT1A,OUT1B,OUT2A,OUT2B/Motor Output Pin

These pins perform low impedance wiring due to the motor drive current flows.

○RNF1,RNF2/Output Current Detection Pin

Connect a current detection resistor 0.3 Ω to 1.0 Ω between this pin and the GND pin of the BD6775EFV and 0.1 Ω to 0.3 Ω to those of the BD6384EFV. Perform low impedance wiring because the motor drive current flows. Keep the permissible power of the resistor in mind. In the case of the BD6384EFV, select the resistance according to the output current so that the RNF voltage will not exceed the rated value.

○RNF1_REF,RNF2_REF/Current Detection Comparator Input Pin(BD6384EFV)

Use this pin shorted with the RNF pin. Design a board pattern that prevents external noise interference.

○VREG/VREG pin (BD6775EFV)

A pin for power supply generated in the IC. (Typ. = 13.5V)

Be sure to connect a capacitor (0.1 μF to 0.47 μF) between this pin and the GND.

○I01,I11,I02,I12/VREF Division Setting Pin

Though VREF voltage is input to 2 bit D/A converter internally, this pin sets division ratio of VREF in D/A converter.

BD6384EFV Supports 5.0/3.3V logic. System.

When this pin is open in BD6384EFV, input logic is L for 100 kΩ pull down resistor.

I01orI02	I11orI12	Current level(%)
L	L	100
H	L	67
L	H	33
H	H	0

	I01,I11,I02,I12	VCC=5.0V	VCC=3.3V
BD6775EFV	High input voltage	2.0～5.0V	Not supported
	Low input voltage	0～0.8V	Not supported
BD6384EFV	High input voltage	2.5～5.0V	2.0～3.3V
	Low input voltage	0～0.8V	0～0.8V

○VREF1,VREF2/Reference Voltage Input Pin

This pin determines the output current. The output current is determined by the VREF voltage input voltage and Ixx pin logic and RNF resistor value.

I01 or I02	I01 or I02	Set current value (A)
L	L	VREF1 or VREF2 (V)/5 × 1.00/RNF1 or 2 (Ω)
H	L	VREF1 or VREF2 (V)/5 × 0.67/RNF1 or 2 (Ω)
L	H	VREF1 or VREF2 (V)/5 × 0.33/RNF1 or 2 (Ω)
H	H	0※

※ If (I01, I11) = (H, H) or (I02, I12) = (H, H), the respective outputs will be turned off.

VREF input is PNP transistor input. When the VREF pin is open, the VREF voltage will rise and the set current will increase. Do not use the IC when the VREF pin is open. If the input is applied by divided voltage with resistance, select the resistance in consideration of the bias current (2μA maximum). The minimum current controllable by VREF voltage is determined by the motor coil impedance and minimum on time, since PWM driving requires the minimum on time.

○CR1,CR2/CR connection pin

A pin to connect C (470pF to 3300pF) and R (15kΩ to 100kΩ) for off time settings.

Off time is determined by Toff [s]=C×R×0.81. Perform low impedance wiring to the GND so that there will be no impedance in common with any other GND pattern and that external noise interference is prevented.

○PS/PS pin

A power saving pin. The power-saving mode will be turned on with the input voltage set to low level. The motor output will be off (open) at that time.

When this pin is open, input logic is L for 100 kΩ pull down resistor.

BD6384EFV Supports 5.0/3.3V logic. System.

PS	MODE
L	stand by
H	active

	PS	VCC=5.0V	VCC=3.3V
BD6775EFV	High input voltage	2.0～5.0V	Not supported
	Low input voltage	0～0.8V	Not supported
BD6384EFV	High input voltage	2.5～5.0V	2.0～3.3V
	Low input voltage	0～0.8V	0～0.8V

○MTH/Decay Mode Setting Pin (BD6384EFV)

A pin to make decay mode settings or to set the ratio of FAST DECAY and SLOW DECAY while in MIXED DECAY mode.

MTH input is PNP transistor input. Do not used the IC when the MTH pin is open. If the input is applied by divided voltage with resistance, select the resistance in consideration of the bias current (2μA maximum).

●Protection circuit

○UVLO(Under Voltage Locked Out)

When VCC voltage is low voltage, this protection circuit prevents IC from operating in the wrong. When VCC voltage is less than about 2.3V(typ.), the motor output will be open state. This threshold voltage has about 100mV(typ.) hysteresis voltage for noise margin.

○TSD(Thermal Shutdown)

When junction temperature Tj is more than 175℃(typ.), the motor output will be open state. If Tj decreases less than 150℃(typ.), the motor output return to normal operating state.

○OCP(Over Current Protection)

BD6384EFV is built-in over current protection circuit If an over current flows during about 5us as a result of a malfunction, such as the shorting of the motor output pins together or the shorting of motor output pins and other pins or ground, the output will be latched in an open state. The IC will be in a normal operating state with the latch mode canceled by turning the power on again or changing the PS pin from low level to high level.

●Heat loss

Consider the power consumption (W), package power (Pd), and ambient temperature (Ta) of the IC, and check that the chip temperature Tj is not in excess of 150°C. If the Tj is in excess of 150°C, the IC will not function as a semiconductor and parasitic operation or leakage will occur. If the IC is used under such conditions, the IC may deteriorate and IC damage may result. Must not exceed Tjmax.=150°C under any circumstance.

The rough power consumption of the IC can be computed from each power supply voltage(VCC,VM), circuit current(ICC,IVM), output on resistance(RONH,RONL), output current(IOUT).

In case of FULL STEP and slow decay mode,

Power consumption by VCC[W] = VCC[V]×ICC[A] ・・・・・・・①

Power consumption by VM W] = VM[V]×IVM[A] ・・・・・・・②

Power consumption by output DMOS [W] = $\underbrace{(RONH[\Omega]+RONL[\Omega])\times IOUT[A]^2\times 2[ch]\times on\_duty}_{\text{during output ON}}$

$+\underbrace{(2\times RONL[\Omega])\times IOUT[A]^2\times 2[ch]\times(1-on\_duty)}_{\text{during current decay mode}}$ ・・・・・・・③

RONH: output high side Pch DMOS on resistance, 2Ω(typ.):BD6775EFV, 0.7Ω(typ.):BD6384EFV
RONL: output low side Nch DMOS on resistance, 1Ω(typ.):BD6775EFV, 0.5Ω(typ.):BD6384EFV
on_duty: PWM on duty = Ton/(Ton+Toff)

Total power consumption W_total[W] = ①+②+③

Junction temperature Tj = Ta[℃]+θja[℃/W]×W_total [W]

θja[℃/W] depends on the condition of the board. See the power dissipation reduction curve (P12/16).
ROHM can measure θja[℃/W] in your application board. Please consult your ROHM representative.

Above calculation is in theory. When you excute themal design, please do not only the theoretical calculation but also sufficient thermal evaluation. Be sure to exeed Tjmax.=150°C under any circumstance by doing thermal design with a sufficient margin.

●Power dissipation reduction

Metal is embedded on the back of the HTSSOP-B24 (BD6775EFV) and HTSSOP-B40 (BD6384EFV). Therefore, heat dissipation from the through holes on the backside is possible. By providing a wide copper foil dissipation pattern on the back as well as the surface of the board, power dissipation can be increased. The metal on the back is shorted with the back of the IC chip and at ground potential. Do not short the backside with any part other than the GND. It is recommended to short the GND and the metal on the back with solder.

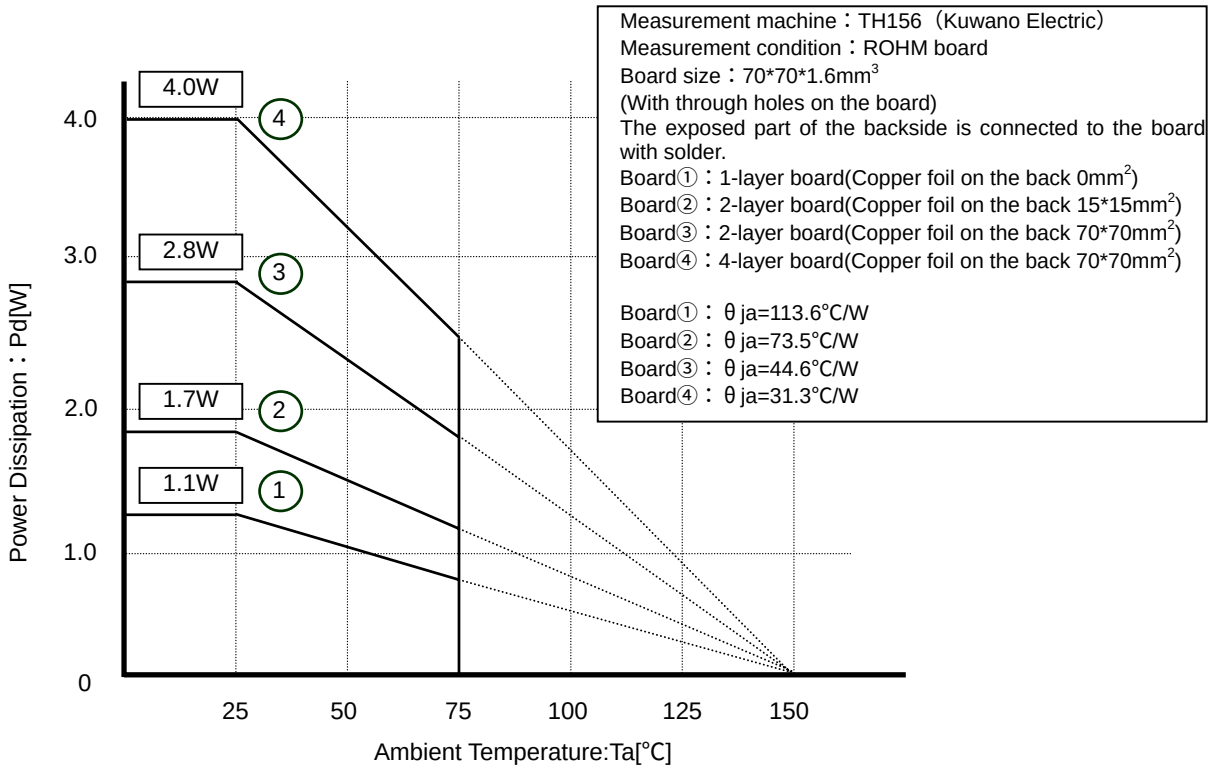


Fig.15 HTSSOP-B24(BD6775EFV) power dissipation reduction curve

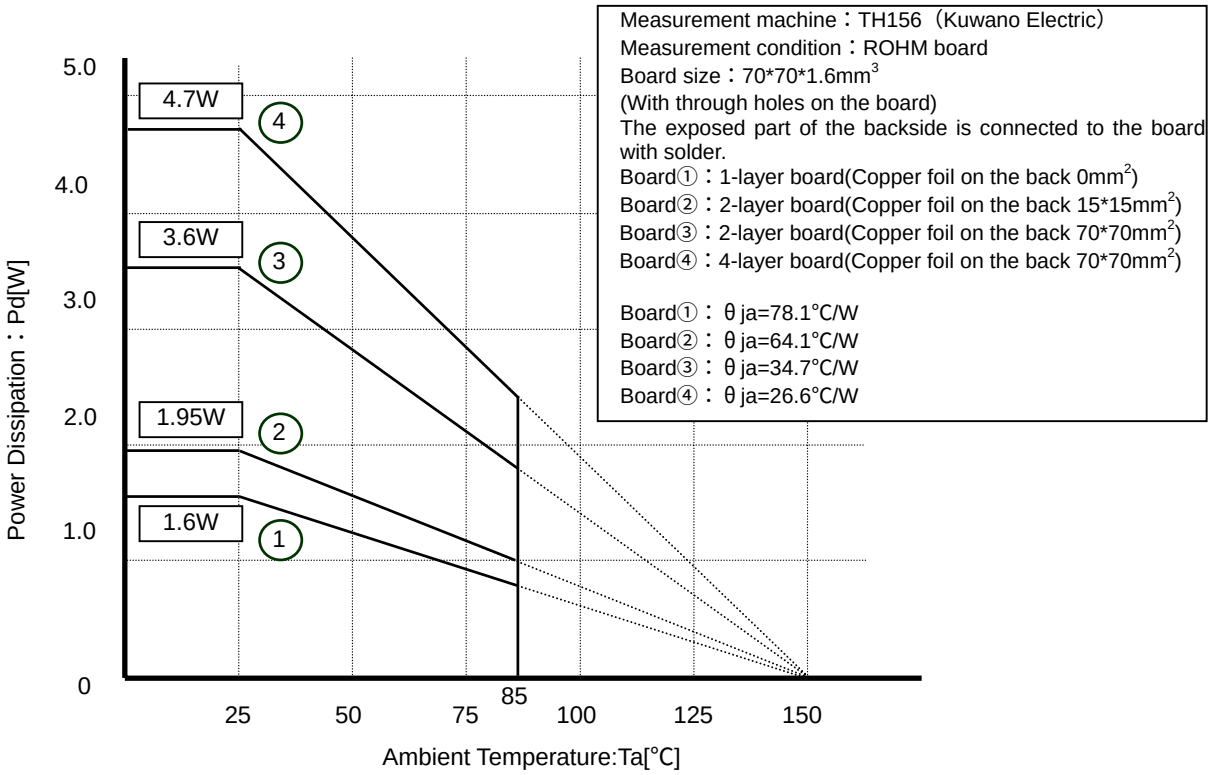


Fig.16 HTSSOP-B40(BD6384EFV) power dissipation reduction curve

●Evaluation board

Evaluation boards are available. Consult your ROHM representative.

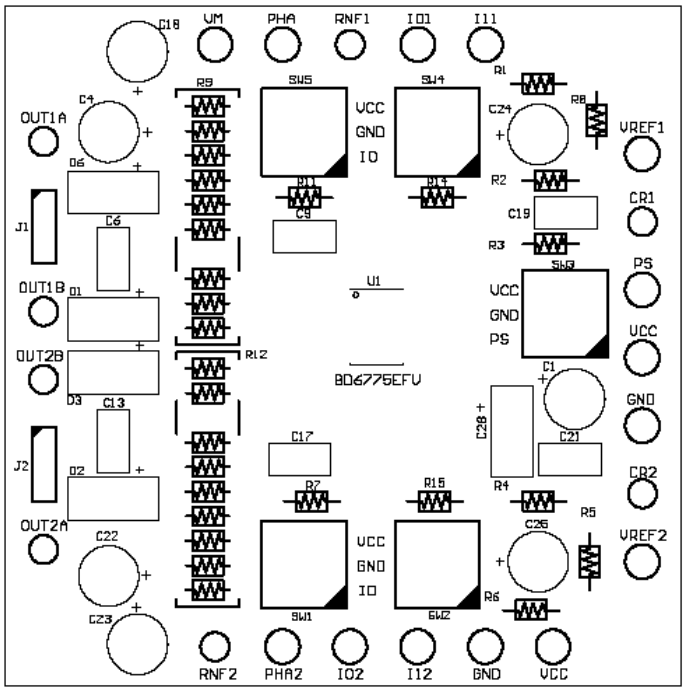


Fig.17 BD6775EFV　Evaluation board

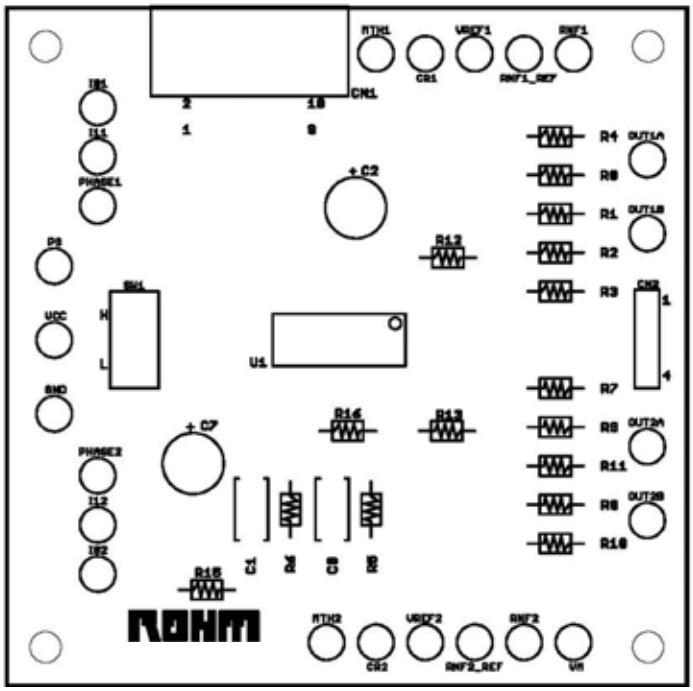


Fig.18 BD6384EFV　Evaluation board

●Operation Notes

1. Absolute maximum ratings

   An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2. Connecting the power supply connector backward

   Connecting the of power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

3. Power supply lines

   Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

4. GND voltage

   The potential of GND pin must be minimum potential in all operating conditions.

5. Thermal design

   Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

6. Inter-pin shorts and mounting errors

   Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

7. Operation in a strong electromagnetic field

   Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

8. ASO

   When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

9. Thermal shutdown circuit

   The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

TSD on temperature [°C] (Typ.)	Hysteresis temperature [°C] (Typ.)
175	25

10. Testing on application boards

    When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to, or removing it from a jig or fixture, during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting and storing the IC.

11. Regarding input pin of the IC

    This monolithic IC contains P^+ isolation and P substrate layers between adjacent elements to keep them isolated. P–N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

    When GND > Pin A and GND > Pin B, the P–N junction operates as a parasitic diode.

    When Pin B > GND > Pin A, the P–N junction operates as a parasitic transistor.

    Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

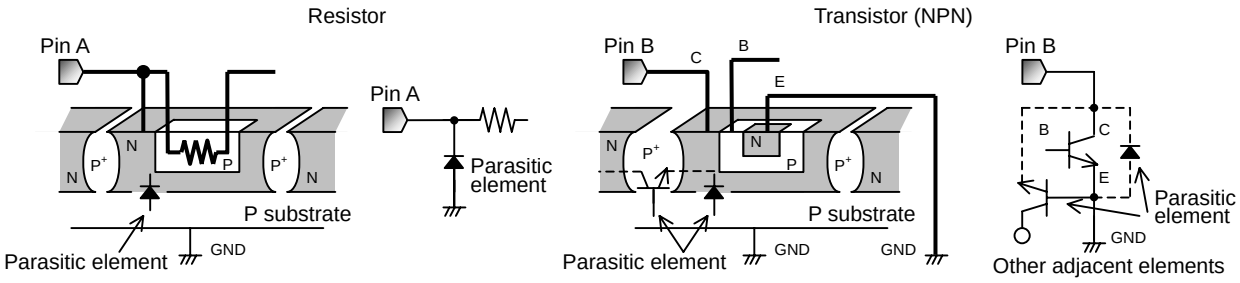


Fig.19 Example of IC structure

12. Ground Wiring Pattern

The power supply and ground lines must be as short and thick as possible to reduce line impedance. Fluctuating voltage on the power ground line may damage the device.

●Selecting a model name when ordering

B	D	6	7	7	5	E	F	V	–	E	2

ROHM model

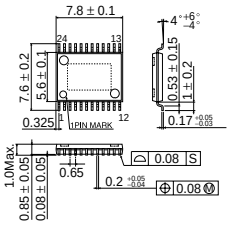
Part number

Package type
EFV=HTSSOP-B24(BD6775EFV)
EFV=HTSSOP-B40(BD6384EFV)

E2 = Reel-wound embossed taping

HTSSOP-B24

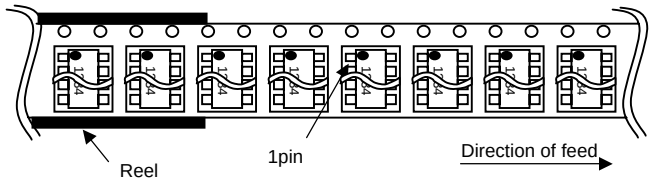
<Dimension>



(Unit:mm)

<Tape and Reel information>

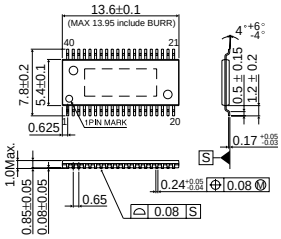
Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

HTSSOP-B40

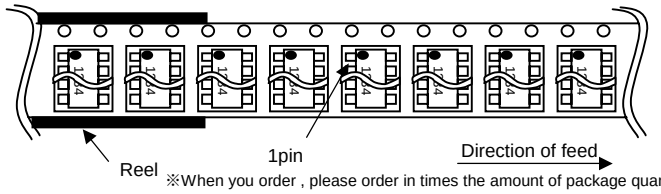
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



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Tianjin	TEL: +86-22-23029181	FAX: +86-22-23029183
Wuxi	TEL: +86-510-82702693	FAX: +86-510-82702992
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Xiamen	TEL: +86-592-239-8382	FAX: +86-592-239-8380
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Bangkok	TEL: +66-2-254-4890	FAX: +66-2-256-6334
Kuala Lumpur	TEL: +60-3-7958-8355	FAX: +60-3-7958-8377
Penang	TEL: +60-4-6585084	FAX: +60-4-6585167
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Stuttgart	TEL: +49-711-72723710	FAX: +49-711-72723720
France	TEL: +33-1-5697-3060	FAX: +33-1-5697-3080
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