Course code	Course Name	L-T-P -Credits	Year of Introduction
CS202	Computer Organization and Architecture	3-1-0-4	2016

Pre-requisite: CS203 Switching theory and logic design

Course Objectives

1. To impart an understanding of the internal organization and operations of a computer.
2. To introduce the concepts of processor logic design and control logic design.

Syllabus

Fundamental building blocks and functional units of a computer. Execution phases of an instruction. Arithmetic Algorithms. Design of the processing unit – how arithmetic and logic operations are performed. Design of the control unit – hardwired and microprogrammed control. I/O organisation – interrupts, DMA, different interface standards. Memory Subsystem – different types.

Expected outcome

Students will be able to:

1. identify the basic structure and functional units of a digital computer.
2. analyze the effect of addressing modes on the execution time of a program.
3. design processing unit using the concepts of ALU and control logic design.
4. identify the pros and cons of different types of control logic design in processors.
5. select appropriate interfacing standards for I/O devices.
6. identify the roles of various functional units of a computer in instruction execution.

Text Books:

1. Hamacher C., Z. Vranesic and S. Zaky, *Computer Organization* ,5/e, McGraw Hill, 2011.
2. Mano M. M., Digital Logic & Computer Design, 4/e, Pearson Education, 2013.

References:

1. Mano M. M., Digital Logic & Computer Design, 4/e, Pearson Education, 2013.
2. Patterson D.A. and J. L. Hennessey, Computer Organization and Design, 5/e, Morgan Kauffmann Publishers, 2013.
3. William Stallings, Computer Organization and Architecture: Designing for Performance, Pearson, 9/e, 2013.
4. Chaudhuri P., Computer Organization and Design, 2/e, Prentice Hall, 2008.
5. Rajaraman V. and T. Radhakrishnan, Computer Organization and Architecture, Prentice Hall, 2011.
6. Messmer H. P., The Indispensable PC Hardware Book, 4/e, Addison-Wesley, 2001

Course Plan

Module	Contents	Hours (51)	Sem.ExamMarks
I	**Basic Structure of computers**–functional units – basic operational concepts –bus structures – software. Memory locations and addresses – memory operations – instructions and instruction sequencing – addressing modes – ARM Example (programs not required). Basic I/O operations – stacks subroutine calls.	6	15%

II	**Basic processing unit** – fundamental concepts – instruction cycle - execution of a complete instruction –multiple- bus organization – sequencing of control signals. **Arithmetic algorithms: A**lgorithms for multiplication and division of binary and BCD numbers — array multiplier —Booth's multiplication algorithm — restoring and non-restoring division — algorithms for floating point, multiplication and division.	10	15%
FIRST INTERNAL EXAMINATION			
III	**I/O organization:** accessing of I/O devices – interrupts –direct memory access –buses –interface circuits –standard I/O interfaces (PCI, SCSI, USB)	8	15%
IV	**Memory system :** basic concepts –semiconductor RAMs –memory system considerations – semiconductor ROMs –flash memory –cache memory and mapping functions.	9	15%
SECOND INTERNAL EXAMINATION			
V	**Processor Logic Design:** Register transfer logic – inter register transfer – arithmetic, logic and shift micro operations –conditional control statements. **Processor organization:**–design of arithmetic unit, logic unit, arithmetic logic unit and shifter –status register –processor unit –design of accumulator.	9	20%
VI	**Control Logic Design:** Control organization – design of hardwired control –control of processor unit –PLA control. **Micro-programmed control:** Microinstructions –horizontal and vertical micro instructions – micro-program sequencer –micro programmed CPU organization.	9	20%
END SEMESTER EXAM			

Question Paper Pattern:

1. There will be *five* parts in the question paper – A, B, C, D, E
2. Part A
    a. Total marks : 12
    b. *Four* questions each having 3 marks, uniformly covering module I and II; All *four* questions have to be answered.
3. Part B
    a. Total marks : 18
    b. *Three* questions each having 9 marks, uniformly covering module I and II; T*wo* questions have to be answered. Each question can have a maximum of three subparts
4. Part C
    a. Total marks : 12
    b. *Four* questions each having 3 marks, uniformly covering module III and IV; All *four* questions have to be answered.
5. Part D
    a. Total marks : 18
    b. *Three* questions each having 9 marks, uniformly covering module III and IV; T*wo* questions have to be answered. Each question can have a maximum of three subparts
6. Part E
    a. Total Marks: 40
    b. *Six* questions each carrying 10 marks, uniformly covering modules V and VI; *four* questions have to be answered.
    c. A question can have a maximum of three sub-parts.
7. There should be at least 60% analytical/numerical/design questions..