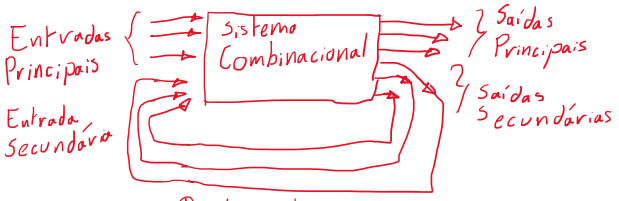
Sistemas Sequenciais

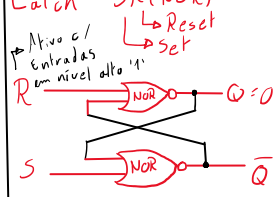


Latch SR (NOR)

Ativo c/ entradas em nível alto "1"

Reset

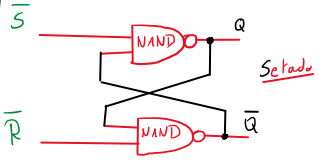
Set



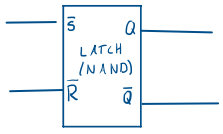
S	R	Q	$\bar{Q}$	
0	0	Q	$\bar{Q}$	Memória
0	1	0	1	Resetado
1	0	1	0	Setado
1	1	0	0	Proibido

Latch SR (NAND)

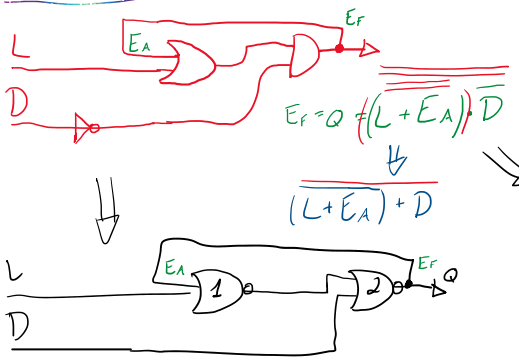
Sensível ao nível lógico baixo ('0')



$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$	
0	0	1	1	Proibido
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q	$\bar{Q}$	Memória



Ilustração

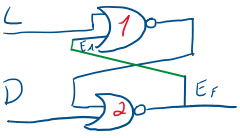


$E_F = Q = \overline{(L + E_A)} + \overline{D}$

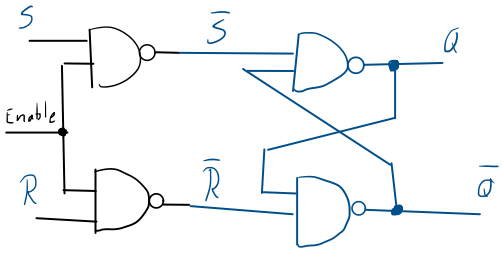
$\overline{(L + E_A)} + D$

Implementação usando NOR

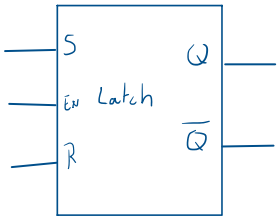
$\overline{A \cdot B} = \overline{A} + \overline{B}$



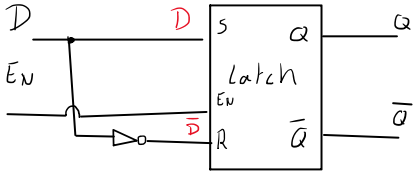
Latch SR Controlado

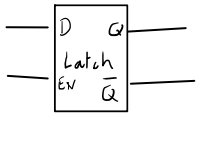


EN	S	R	Q	$\bar{Q}$	
0	X	X	Q	$\bar{Q}$	Memória
1	0	0	Q	$\bar{Q}$	Memória
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	1	1	Proibido



Latch Tipo D (Data)





EN	D	Q	$\bar{Q}$
0	x	Q	$\bar{Q}$
1	d	d	$\bar{d}$