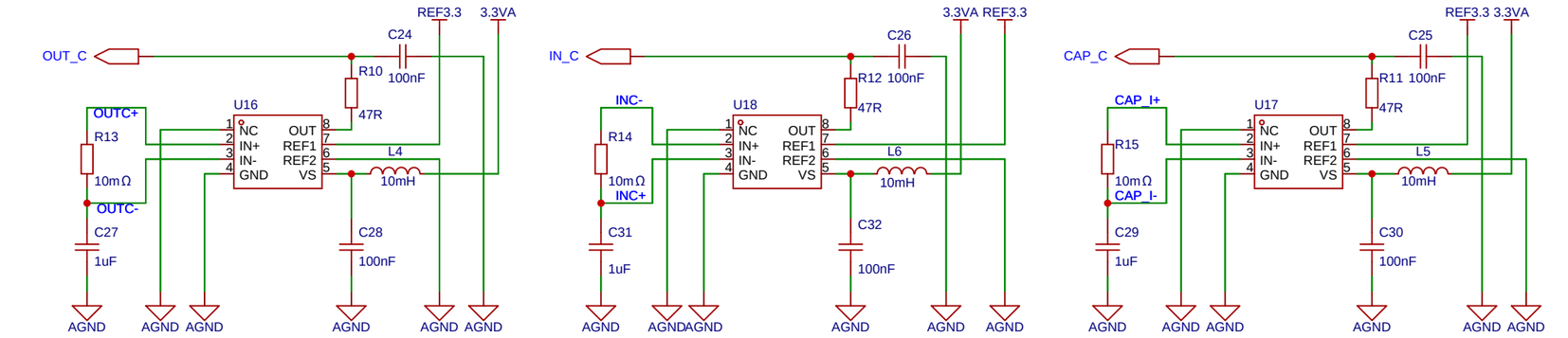
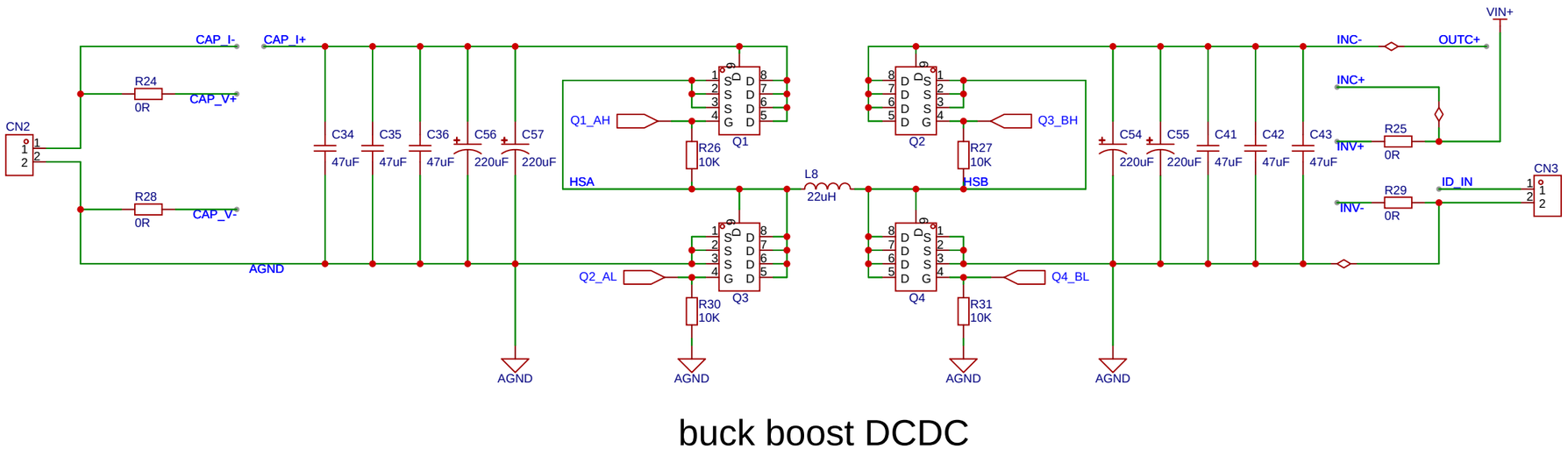
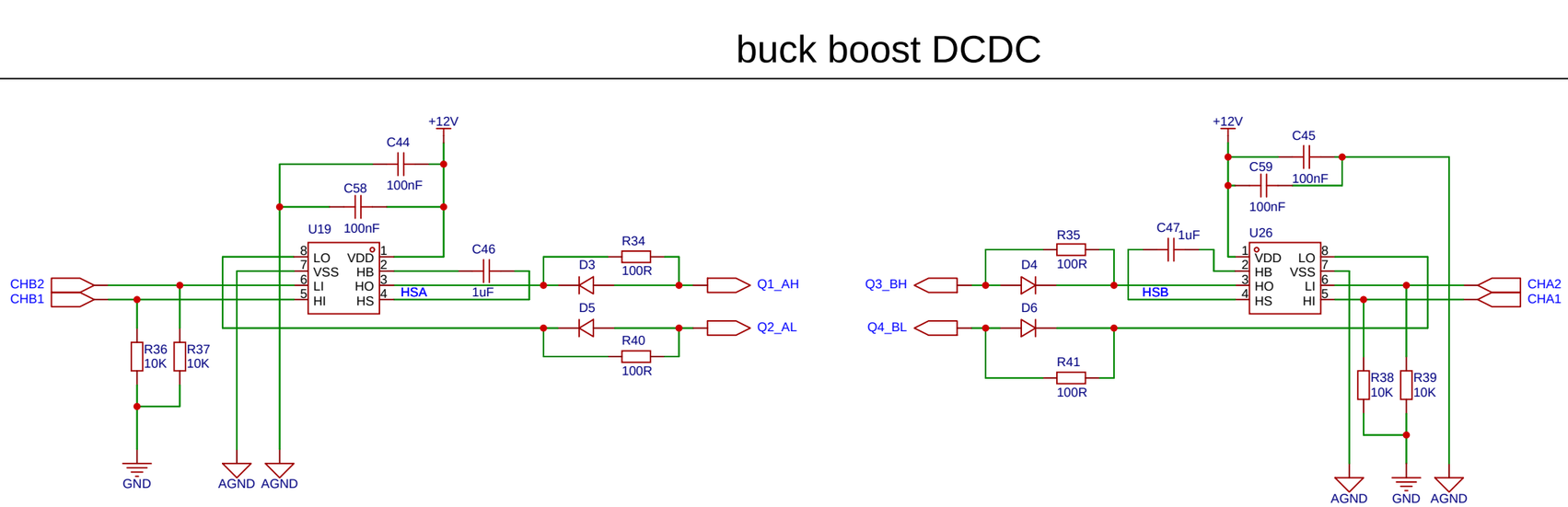


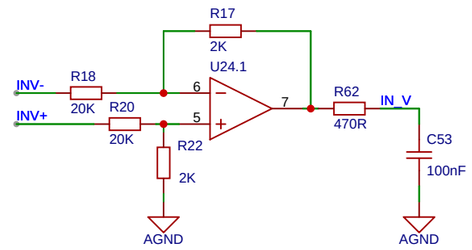
overload protection

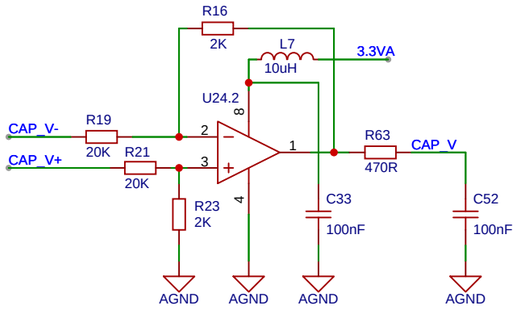


buck boost DCDC

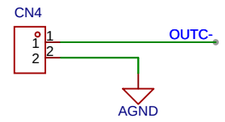


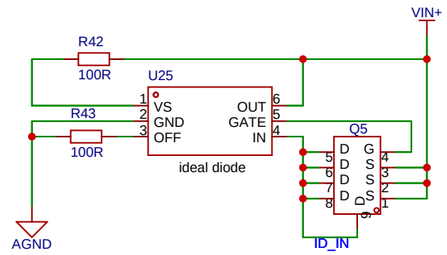
PWM booster





voltage and current sensing





unknown

Schematic	超级电容管理_3	Update Date	2024-03-24
		Create Date	2024-03-23
Page	主拓扑	Part Number	
Drawed		super_capacitor_control	
Reviewed			
		VER / SIZE / PAGE 3 OF 3	
嘉立创EDA		V1.0 / B	嘉立创EDA

必须注意避免将VDD迹线放置在LO、HS和HO信号附近
对LO和HO使用宽走线，紧密跟随相关的GND或HS走线。在可能的情况下，宽度为60至100密耳是可取的。