REVISION	PAGE	REVISION DESCRIPTION	APPROVAL	DATE
A1.0	---	Created	CEV	04/23/03
A1.1	7 8 8 10 11 11	Deleted "The host can still address Pages 1, 2, and 3, but the image..." from section 4.3 Added Note under table in section 4.5 Added "Approximate" to table in section 5.2 Deleted "using the current data write mode" from section 5.8 Added character kerning option to section 5.10 Deleted "If the monochrome mode is selected (G=0), the P1 and P0 bits..." from section 5.10	CEV	05/08/03
A1.2	4 4	V_{IH} Min. was 0, Typ. was -, Max. was 12 in section 3.6 V_{IL} Min. was -12, Typ. was -, Max. was 0 in section 3.6	CEV	05/13/03
A1.3	14	Added Command Execution Times in section 7.0	CEV	06/20/03
A2.0	8 All	“100% luminance” was “0% luminance” in section 5.1 Part Number was TGP1118BA1	CEV	07/14/03
A3.0	All	Part Number was TGP1118BA2	CEV	08/18/03
A4.0	4 5 All	R3 was JP1 in section 3.7 4.7 µF was 0.1 µF, 27 ms was 2 ms, and t_{WAIT} minimum was 41 ms in section 3.8 Part Number was TGP1118BA3	CEV	06/24/03

Futaba®

Futaba Corporation of America Schaumburg, IL

DRAWING TITLE:
PRODUCT SPECIFICATION

PART NUMBER:
TGP1118BA4

DESIGNED BY:	SYSTEMS ENGINEERING APPROVAL:	CUSTOMER NAME / PART NUMBER:	
Paul Lesiakowski	Charles Voegeli	STANDARD PRODUCT	
CHECKED BY:	QA APPROVAL:	FILE NAME:	
John Hohmeier	John Kowalewski	TGP1118BA4_REVA4.0_24JUN04.DOC	
CUSTOMER APPROVAL:	DIRECTOR OF ENGINEERING APPROVAL:	DATE PRINTED:	SHEET:
N/A	Gary Wires	06/24/04	1 OF 14

1.0 INTRODUCTION

This module consists of a Futaba 128 by 64 dot matrix graphic Vacuum Fluorescent Display (VFD), RS-232 serial interface, driver circuitry, DC to DC/AC converter, and a character generator. The module is capable of displaying 64 luminance levels and 4 grayscale levels.

2.0 APPLICABLE DOCUMENTS

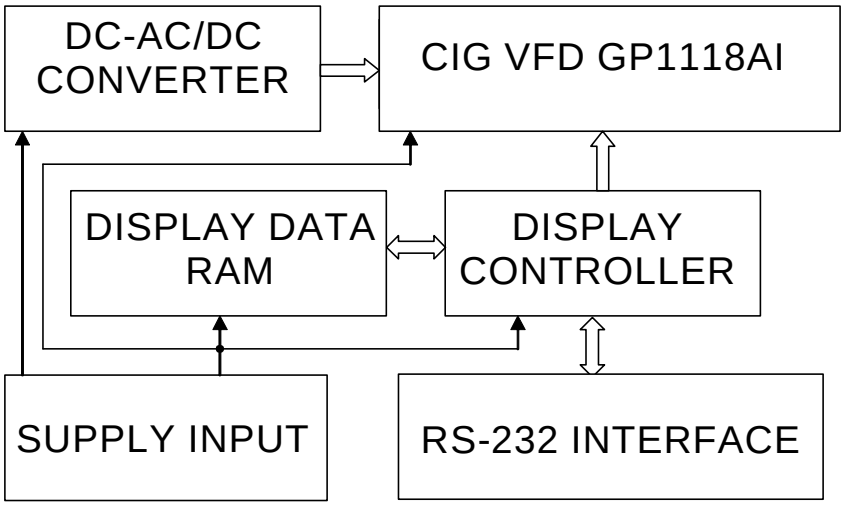
Futaba Vacuum Fluorescent Display Specification; GP1118AI

3.0 SPECIFICATIONS

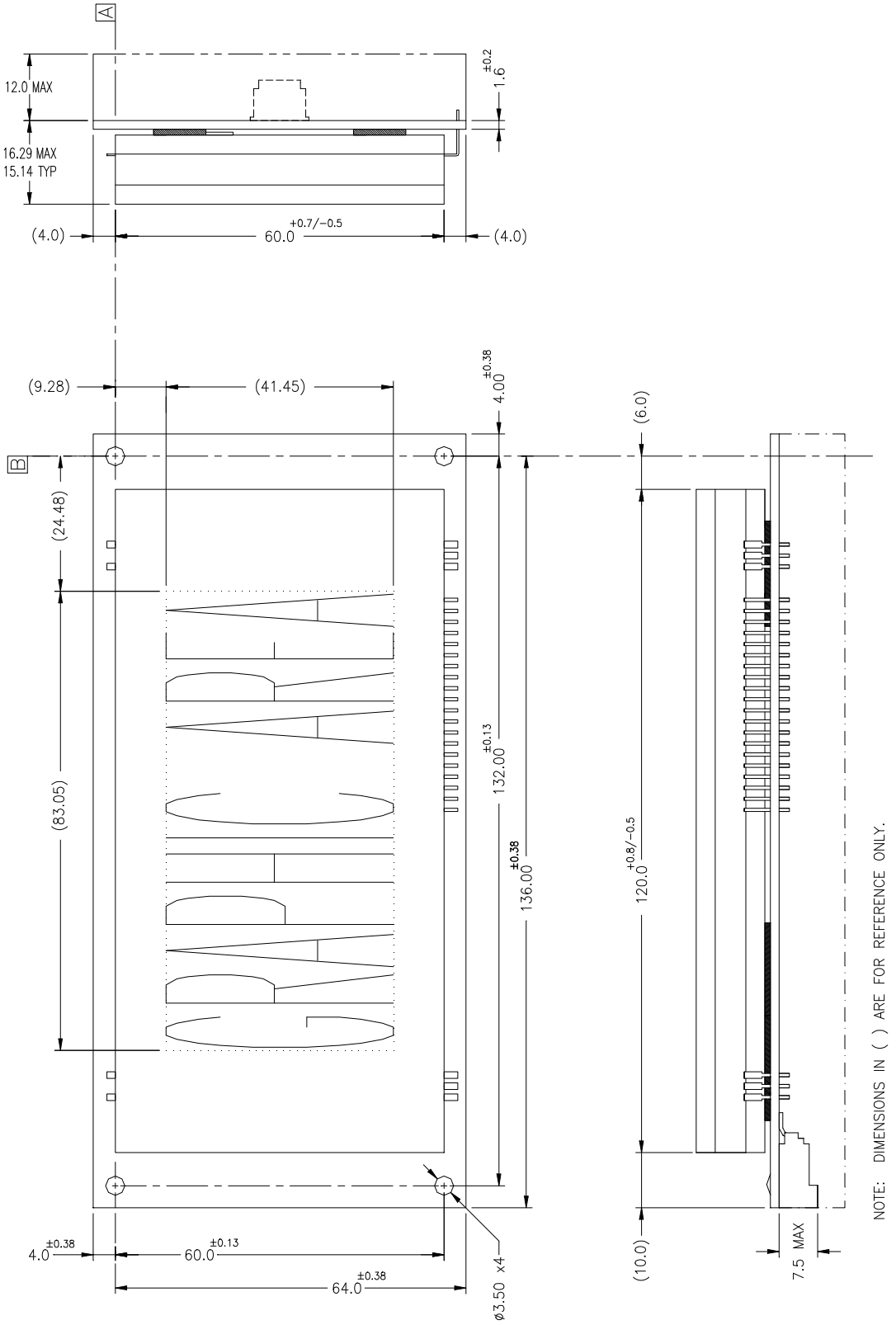
3.1 GENERAL SPECIFICATIONS

Item	Value	
Number of dots	128 x 64	
Dot height	0.5 mm	
Dot width	0.5 mm	
Dot pitch	0.65 mm	
Pattern width	83.05 mm	
Pattern height	41.45 mm	
Color of illumination	Green (x = 0.235, y = 0.405)	
Luminance	Minimum	Typical
	250 Cd/m^2, 73 fL	500 Cd/m^2, 146 fL

3.2 BLOCK DIAGRAM



3.3 MECHANICAL DRAWING



3.4 ENVIRONMENTAL SPECIFICATIONS

Item	Symbol	Min.	Max.	Unit
Operating temperature	T_{opr}	-40	+85	°C
Storage temperature	T_{stg}	-40	+85	°C
Relative storage humidity	H_{stg}	20	95	%
Vibration (see Note 1)	-	-	4	G
Shock (see Note 2)	-	-	40	G

Note 1: 10-55 Hz sine-wave, 1 minute/cycle, 2 hours/axis (x,y,z)
Note 2: Half sine-wave, 11 ms duration, 3 times each axis (x,y,z,-x,-y,-z)

3.5 ABSOLUTE MAXIMUM ELECTRICAL RATINGS

Item	Symbol	Min.	Max.	Unit
Display supply voltage	V_{VDD}	-0.3	12.6	V_{DC}
Logic supply voltage	V_{VCC}	-0.3	5.25	V_{DC}
RxD voltage	V_{RxD}	-25	25	V_{DC}

3.6 RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Min.	Typ.	Max.	Unit
Display supply voltage	V_{VDD}	11.4	12.0	12.6	V_{DC}
Display supply current	I_{VDD}	-	400	-	mA
Logic supply voltage	V_{VCC}	4.75	5.00	5.25	V_{DC}
Logic supply current	I_{VCC}	-	30	-	mA
High level RxD voltage	V_{IH}	3	12	-	V_{DC}
Low level RxD voltage	V_{IL}	-	-12	-3	V_{DC}

Note: A surge current of up to ten times the supply current can occur at power-up. However, the exact peak amplitude adn duration of the surge current is dependent on the characteristics of the host power supply.

3.7 SERIAL COMMUNICATION INTERFACE

The module receives commands and data from the host over an RS-232 single wire serial interface framed with one start bit, 8 data bits, and one stop bit. The baud rate is 115.2K or 9600 if R3 is placed on PCB.

3.8 RESET

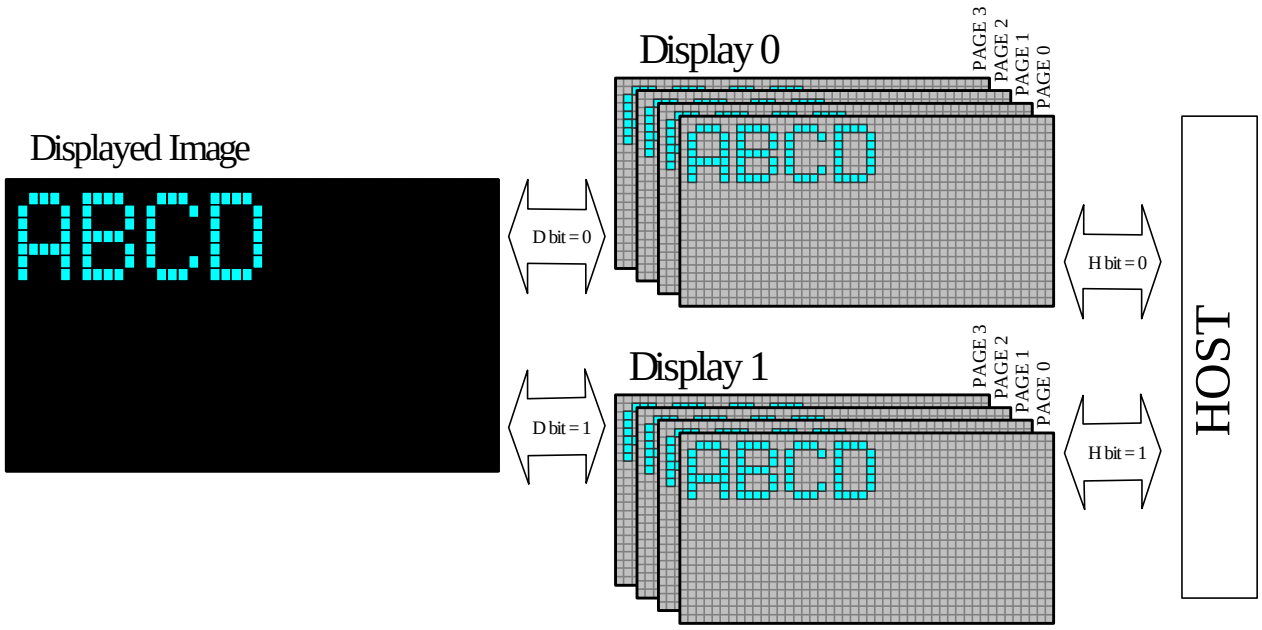
The module is reset at power-up by an R-C circuit. The host must wait for a period, t_{WAIT}, before sending data to the module.
t_{WAIT} is given by the equation; $t_{WAIT} = -(225\ k\Omega * 4.7\ \mu F) * \ln((0.2 * V_{CC} - 0.1) / V_{CC}) + 27\ ms$

Item	Symbol	Min.	Typ.	Max.	Unit
V_{CC} to RxD delay time	t_{WAIT}	1.82	-	-	s

4.0 DISPLAY ARCHITECTURE

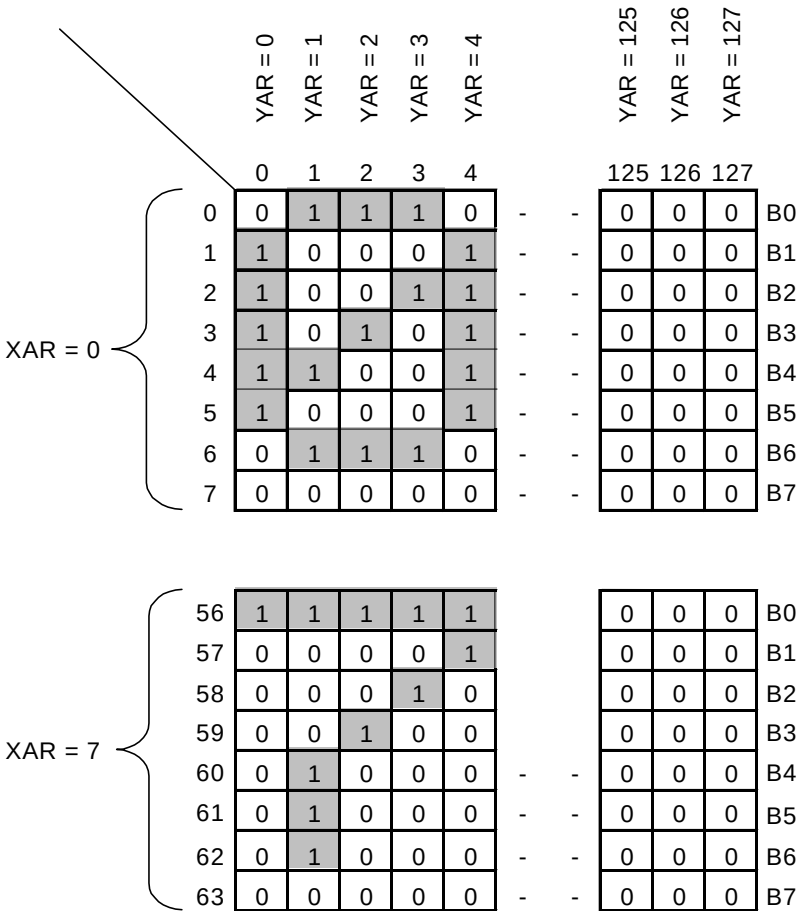
4.1 DISPLAY DATA RAM

The on-board Display Data Ram (DDRAM) stores the pixel information used for displaying images. DDRAM is divided into two equal sections, Display 0 and Display 1. The image in either section can be displayed and/or updated at any time using the D and H display control bits. Both DDRAM sections are further divided into 4 equal pages, Page 0 through Page 3. These pages are used to display 4-level grayscale images.



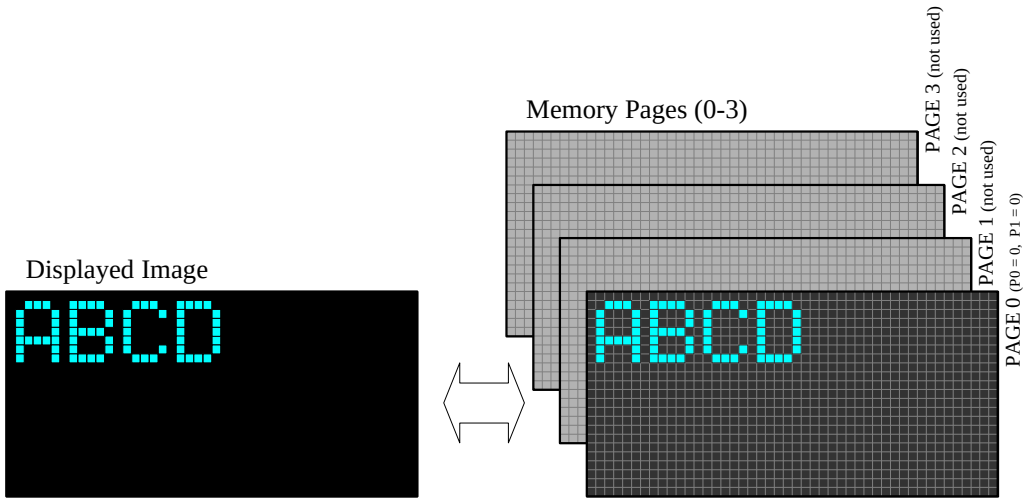
4.2 DISPLAY PAGE MAP

Image data for the 8192 pixels of each display page is stored as 1024 bytes which are addressed via the X Address Register (XAR) and the Y Address Register (YAR). The XAR corresponds to the display row, 8 pixels tall, and the YAR corresponds to the display column, 1 pixel wide, of a particular byte. The most (least) significant bit, B7 (B0), of each byte corresponds to the bottom (top) pixel of that address.



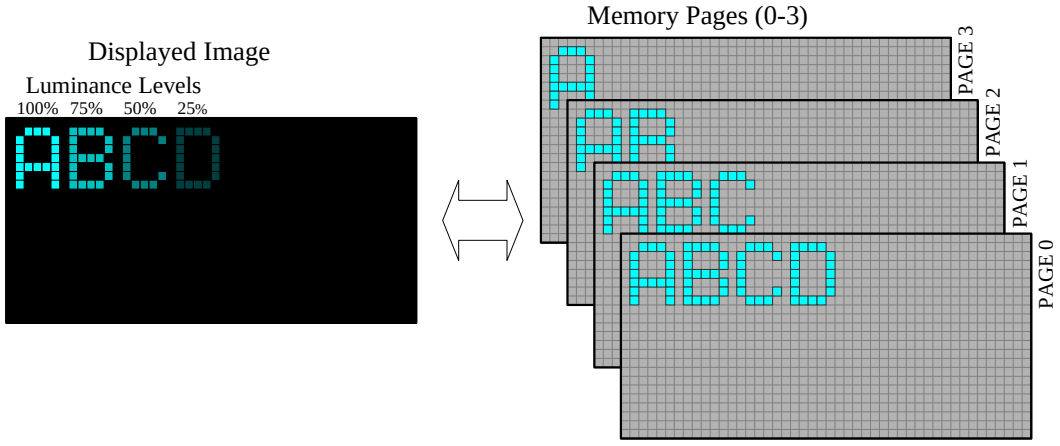
4.3 MONOCHROME DISPLAY MODE

In the monochrome display mode, image data is stored in DDRAM Page 0 only. Image data bits stored as logic 1's are illuminated and bits stored as logic 0's are dark. Overall luminance can be controlled to 64 levels.



4.4 GRAYSCALE DISPLAY MODE

In the grayscale display mode, image data is stored in DDRAM Pages 0, 1, 2, and 3. The display controller combines the data from all 4 pages to create a grayscale image. Image data bits add 25% relative luminance to the image for each page they are stored in as logic 1's. All of the 8192 pixels in an image can be configured for 0%, 25%, 50%, 75%, or 100% relative luminance independently. Overall luminance can also be simultaneously controlled to 64 levels.



4.5 DISPLAY CONTROL BITS

Display Control Bit		Description
H	0	DDRAM Display 0 selected for host communications (default)
	1	DDRAM Display 1 selected for host communications
D	0	DDRAM Display 0 image displayed (default)
	1	DDRAM Display 1 image displayed
P1,P0	0,0	DDRAM Page 0 selected for host communications (default)
	0,1	DDRAM Page 1 selected for host communications
	1,0	DDRAM Page 2 selected for host communications
	1,1	DDRAM Page 3 selected for host communications
G	0	Monochrome display mode selected (default)
	1	Grayscale display mode selected
I/D	0	XAR and YAR increment after a data write (default)
	1	XAR and YAR decrement after a data write

Note: P1 and P0 are automatically cleared if G is low.

5.0 COMMAND CODES (00H THROUGH 0FH)

5.1 RESET (00H)

This command resets the module to the following conditions:

- 100% luminance (0% at power-up reset)
- XAR and YAR set to 0
- Entire DDRAM cleared
- All display control bits set to 0
- Data write mode set to default mode (overwrite)
- Character size set to 5x7
- Character luminance set to 100%

5.2 SET LUMINANCE (01H, LUMINANCE)

This command sets the overall display luminance to 1 of 64 levels. Bits 5 through 0 of the LUMINANCE byte select the luminance level, bits 7 and 6 are ignored.

LUMINANCE byte	Approximate Display Luminance
00H	0%
01H	1.5%
- - -	- - -
3EH	98.5%
3FH	100%

5.3 SET Y ADDRESS REGISTER (02H, YAR)

This command sets the YAR. Bits 6 through 0 of the YAR byte are used, bit 7 is ignored.

5.4 SET X ADDRESS REGISTER (03H, XAR)

This command sets the XAR. Bits 2 through 0 of the XAR byte are used, bits 7 through 3 are ignored.

5.5 SET DISPLAY CONTROL BITS (04H, DCB)

This command sets the display control bits. Bits 5 through 0 of the DCB byte are used, bits 7 and 6 are ignored.

DCB byte							
B7	B6	B5	B4	B3	B2	B1	B0
x	x	I/D	G	P1	P0	D	H

5.6 WRITE DATA BYTE (05H, DATA)

This command writes the DATA byte, using the current data write mode, into the DDRAM location addressed by the XAR, the YAR, the P1 and P0 bits, and the H bit. This command also automatically increments (I/D=0) or decrements (I/D=1) the X and Y address registers. When the YAR overflows from 127 to 0, the XAR is also incremented, when the YAR underflows from 0 to 127, the XAR is also decremented.

5.7 WRITE DATA PAGE (06H, BYTE1, BYTE2,... BYTE1024)

This command writes BYTE1 through BYTE1024, using the current data write mode, into the DDRAM page addressed by the P1 and P0 bits, and the H bit. This command ignores the XAR, the YAR, and the I/D bit and stores BYTE1 at (XAR,YAR) location (0,0), BYTE2 at (0,1),... BYTE129 at (1,0),... and BYTE1024 at (7,127). This command also clears the XAR and the YAR.

5.8 WRITE DATA WITH SHIFT (07H, DIRECTION, ROW, BYTE1, BYTE2,... BYTE32)

This command shifts the image data, selected by the ROW byte and the data control bits, one column to the left or right depending on the DIRECTION byte and fills the empty column in DDRAM with new data. Data shifted off the end of each row is lost. Bit 0 of the DIRECTION byte selects the shift direction, 0=left, 1=right, bits 7 through *2 are ignored. Each bit of the ROW byte selects whether a given row is shifted or not, 1=row is shifted, 0=row not shifted. ROW byte bit 0 represents the top row (XAR=0), bit 1 the next row (XAR=1),... and bit 7 the bottom row (XAR=7). The data bytes, BYTE1, BYTE2,... BYTE32 fill the empty column from the top row to the bottom row skipping non-shifted rows, starting with Page 0 followed by Pages 1, 2, and 3 when in the grayscale mode. One data byte is required for each row shifted when in the monochrome mode (G=0), 4 are required for each row shifted when in the grayscale mode (G=1). The XAR, the YAR, and the display control bits are not affected by this command.

*TBD - If bit 1 of the DIRECTION byte is set, the module will use BYTE1 as the character code and BYTE2 as the character column number for the "new" data for filling the empty column in DDRAM.

5.9 DATA WRITE MODE (08H, MODE)

This command determines how incoming data and characters will be combined with existing data in DDRAM.

Description	MODE byte							
	B7	B6	B5	B4	B3	B2	B1	B0
DATA => DDRAM (default)	x	x	x	x	x	0	0	0
DATA AND DDRAM => DDRAM	x	x	x	x	x	0	0	1
DATA OR DDRAM => DDRAM	x	x	x	x	x	0	1	0
DATA XOR DDRAM => DDRAM	x	x	x	x	x	0	1	1
NOT DATA => DDRAM	x	x	x	x	x	1	0	0
DATA NAND DDRAM => DDRAM	x	x	x	x	x	1	0	1
DATA NOR DDRAM => DDRAM	x	x	x	x	x	1	1	0
DATA XNOR DDRAM => DDRAM	x	x	x	x	x	1	1	1

5.10 CHARACTER WRITE MODE (09H, MODE)

This command determines the size of incoming characters, which DDRAM page(s) they will be stored in, and enables/disables character kerning.

Description	MODE byte							
	B7	B6	B5	B4	B3	B2	B1	B0
5x7 character size (default)	x	x	x	x	-	-	-	0
10x14 character size	x	x	x	x	-	-	-	1
Character luminance 25%	x	x	x	x	-	0	0	-
Character luminance 50%	x	x	x	x	-	0	1	-
Character luminance 75%	x	x	x	x	-	1	0	-
Character luminance 100% (default)	x	x	x	x	-	1	1	-
Character kerning enabled (default)	x	x	x	x	0	-	-	-
Character kerning disabled (fixed width)	x	x	x	x	1	-	-	-

5.11 INVERT SCREEN (0AH)

This command logically inverts (0's become 1's, 1's become 0's) the contents of DDRAM selected by the H and G bits. In the monochrome mode (G=0) only Page 0 is affected. The XAR, the YAR, and the data control bits are not affected by this command.

5.12 RESERVED (0BH THROUGH 0FH)

These codes are reserved for future use and are currently ignored by the module.

6.0 CHARACTER CODES (10H THROUGH FFH)

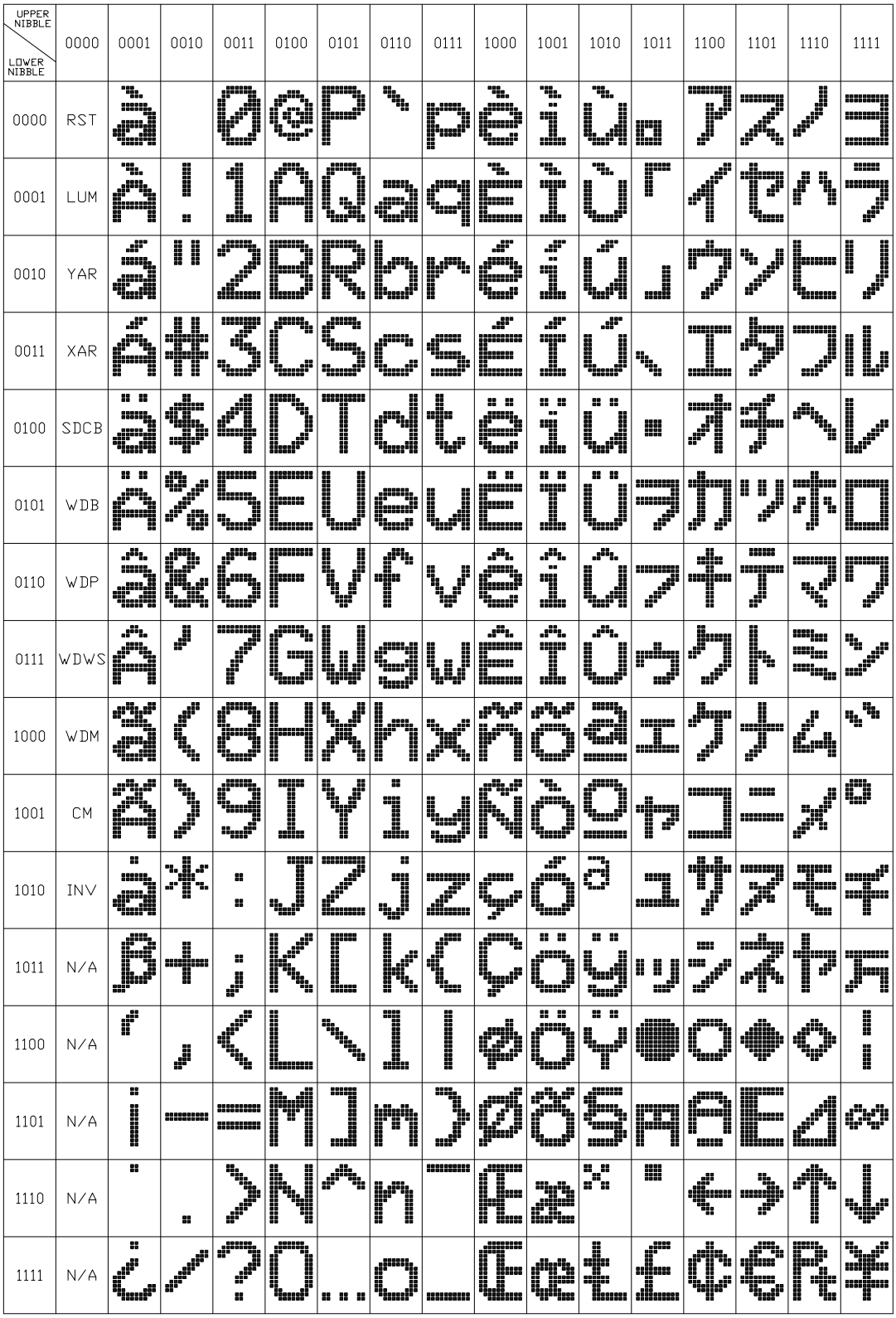
Data values received by the module that are within the range 10H through FFH, are character codes. The character selected from the character table by the character code is written, using the current character write and data write modes, into the DDRAM location addressed by the XAR, the YAR, the data control bits. The XAR and YAR point to the DDRAM location that the left hand side of a 5x7 (upper left hand side of a 10x14) character will be stored. This command adds 1 *blank column to 5x7 characters or 2 *blank columns to 10x14 characters, for character spacing. This command also automatically increments (I/D=0) or decrements (I/D=1) the X and Y address registers to point to the next character (some characters are wider than others, see font table for sizes). YAR overflows, 127 to 0, increment the XAR (by 2 for 10x14 characters) and YAR underflows, 0 to 127, decrement the XAR (by 2 for 10x14 characters). Characters are top-justified leaving the bottom pixel row (2 pixel rows for 10x14 characters) *blank.

*"blank" is dependent on the current data write mode.

6.1 5X7 CHARACTER TABLE

UPPER NIBBLE / LOWER NIBBLE	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	RST															
0001	LUM															
0010	YAR															
0011	XAR															
0100	SDCB															
0101	WDB															
0110	WDP															
0111	WDWS															
1000	WDM															
1001	CM															
1010	INV															
1011	N/A															
1100	N/A															
1101	N/A															
1110	N/A															
1111	N/A															

6.2 10X14 CHARACTER TABLE



7.0 COMMAND EXECUTION TIMES

Following table lists all available commands and their corresponding execution times. There are no delays required beteween command and parameter bytes in a multi-byte commands. All times shown below are measured from the receipt of the last byte (exept for the Write Data Page command)

Command	Code	Execution Time		Unit
		Monochroome	Grayscale	
Reset	00H	27		ms
Set Luminance	01H	N/A *see note 1		ms
Set Y Address Register	02H	N/A *see note 1		ms
Set X Address Register	03H	N/A *see note 1		ms
Set Display Control Bits	04H	N/A *see note 1		ms
Write Data Byte	05H	N/A *see note 1		ms
Write Data Page	06H	N/A *see note 1		ms
Write Data With Shift	07H	0.85/row	3.2/row	ms
Data Write Mode	08H	N/A *see note 1		ms
Character Write Mode	09H	N/A *see note 1		ms
Invert Screen	0AH	7	25	ms
Not used	0BH	N/A *see note 1		ms
Not used	0CH	N/A *see note 1		ms
Not used	0DH	N/A *see note 1		ms
Not used	0EH	N/A *see note 1		ms
Not used	0FH	N/A *see note 1		ms
5x7 Character Write	10H - FFH	0.35 *see note 2	0.8 *see note 2	ms
10x14 Character Write	10H - FFH	0.7 *see note 2	2.1	ms

Note 1: Execution times shorter than the time needed to transmit the next byte at 115.2K baud.
Note 2: N/A at 9600 baud

8.0 CONNECTOR INTERFACE

Connector type: Molex p/n 15-91-3044

Pin Number	Description
1	RxD
2	GND
3	V_{CC}
4	V_{DD}