

Pierre Ollivier

Paris, France | pollivie@student.42.fr | 07 85 61 33 47 | [linkedin.com/in/pollivie](https://www.linkedin.com/in/pollivie) | github.com/pierrelgol

Summary

Student at Ecole 42 Paris - RNCP 7.

Specialized in C/C++/Zig/AVR, ESP32, and Linux. Passionate about designing robust, real-time code in the defense sector.

Skills

Tools: C, C++, Zig, Bash, Rust, Python, Java, Git, Qt, SDL, SQL, PyTorch, NumPy

Platforms: Linux, Windows, AVR, ESP32, Raspberry Pi, RTOS (FreeRTOS, Zephyr), Docker

Languages: French (C2), English (C2), Spanish (B1), Russian (A1)

Experience

Embedded Software Engineer Apprentice, Thales – France

Sept 2025 – present

- Refactored legacy C++ codebase to pure C, removing Libcamera/OpenCV dependencies to enable seamless cross-compilation and reduce build time (6m → 20s).
- Shipped a custom stripped-down Linux kernel and drivers, slashing boot time (22s → 3s) and power consumption (450mA → 280mA).
- Architected a zero-copy V4L2/DMA pipeline with hand-written NEON intrinsics, achieving soft real-time performance with minimal memory footprint (200MB → 6MB).
- Engineered end-to-end MLOps pipeline for YOLO11: synthetic data generation, curriculum training, and TensorRT export for embedded inference.

Soldier, French Army - 13th DBLE – France

2017 – 2018

Projects

C11 Compiler in Zig

2025

- Developed a fully compliant C11 compiler from scratch in Zig.
- Robust enough to compile large-scale real-world projects like MySQL.

ZigCleaner (zc)

2025

- High-performance, multithreaded file system cleaner implemented in Zig.
- Capable of scanning 200,000+ directories in under 1 second using a custom work-stealing thread pool.
- Optimized for identifying and recursively removing large build artifacts to reclaim disk space.

Embedded Development on ATmega328p

2025

- Implemented low-level drivers for I2C, SPI, and UART protocols with direct register manipulation.
- Developed hardware interruption handlers and drivers for various sensors (temperature, display).

Multithreaded Netcode

2024

- Implemented cutting-edge Lock-Step simulation and Thread-per-game architecture in Zig.
- Designed a custom binary serialization format minimizing client latency (< 1 ms).
- Optimized memory footprint to under 512 Kb RAM.

Education

Ecole 42 Paris, in Low-level / Embedded / Kernel Specialization – Paris, France

2023 – 2025

UBS Vannes, in Bachelor in Applied Economics – Vannes, France

2020 – 2021