UNIVERSITY OF ESSEX

SWITCHED-RAIL POWER OPTIMISER

Final Report

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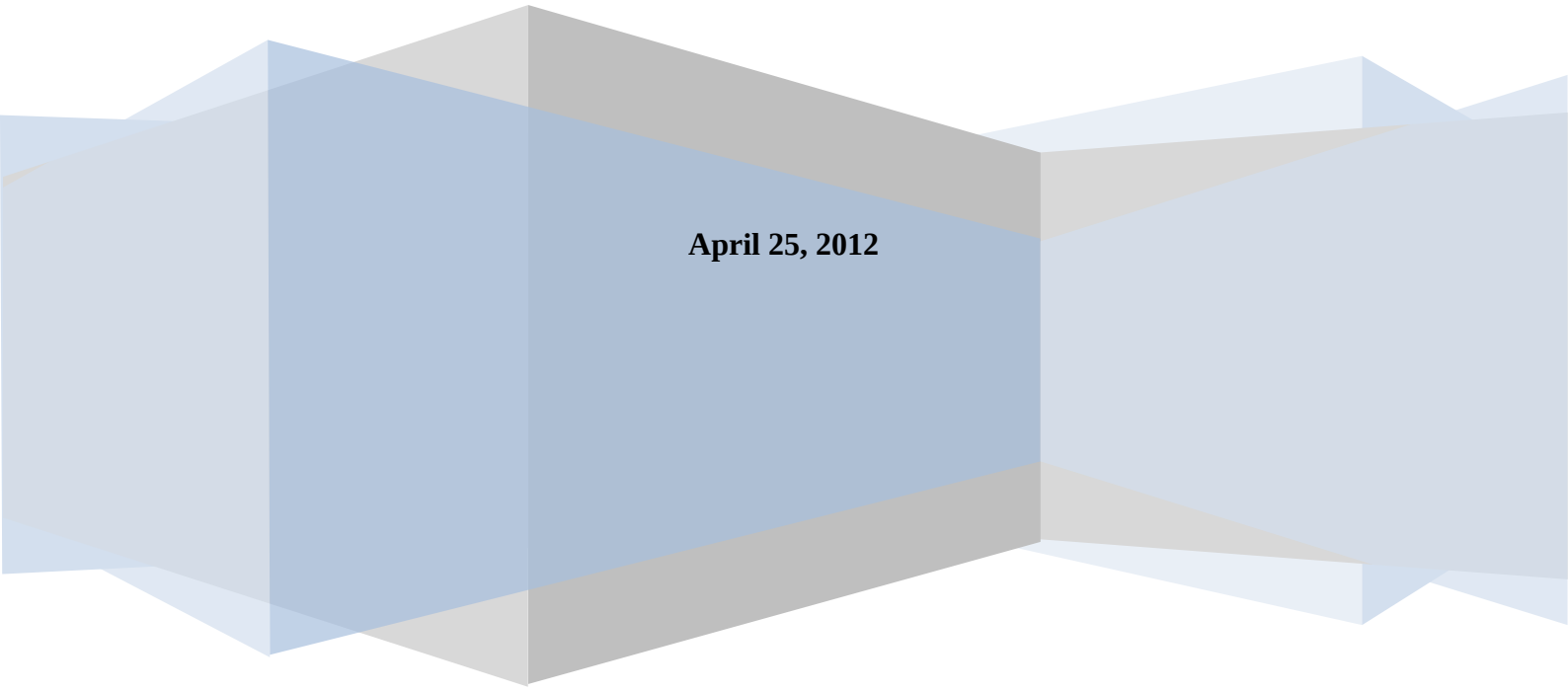

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Abstract

Switching techniques are widely used in electronic power control systems. They generally lead to significant reductions in power dissipation and improvement in the energy efficiency of the system. In recent years, power inverters using switching technique are becoming more popular for photovoltaic applications. Moreover, DC to AC multilevel inverters based on the Golomb ruler (unbalanced series sequence DC source) for photovoltaic applications are not exist.

This project shows a novel approach of a solar cell DC to AC (50 Hz) staircase inverter based on the third order Golomb ruler. This inverter is implemented with controllable opto-coupled MOSFET switches and a number of solar cells as a DC source. These cells are connected in an unbalanced series sequence to form a third order Golomb ruler. The embedded micro-controller controls the states of the MOSFET switches such that individual solar cell DC voltages selectively contribute to steps in the AC waveform output. Furthermore, this inverter is implemented without the use of inductors and capacitors. This report describes the full details of the design and implementation of the inverter before reaching the conclusion.

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List of Abbreviations:

PV	**P**hoto**v**oltaic
AC	**A**lternative **C**urrent
DC	**D**irect **C**urrent
MPPT	**M**aximum **P**ower **P**oint **T**racking
WTHD	Frequency **W**eighted **T**otal **H**armonic **D**istortion
EMI	**E**lectromagnetic **I**nterference
SMPS	**S**witch **M**ode **P**ower **S**upply
MPP	**M**aximum **P**ower **P**oint
FF	**F**ill **F**actor
SNR	**S**ignal to **N**oise **R**atio
MOSFET	**M**etal–**O**xide–**S**emiconductor **F**ield-**E**ffect **T**ransistor
PCB	**P**rinted **C**ircuit **B**oard
LED	**L**ight **E**mitting **D**iode
T	Absolute **T**emperature

Part I

Introduction and Background

1 Introduction

The use of solar photovoltaic power around the world is increasing rapidly. According to the GLOBAL STATUS REPORT 2011, PV supplied around 17 GW of worldwide generating capacity in 2010 [16]. The corresponding growth rate of solar power generation may increase as the price of oil is rising. Germany and Japan are the top leading markets in solar power generation and PV development applications [16]. High performance solar DC to AC inverters are one of the important components in solar power generation. The issue of power dissipation in solar inverters, due to capacitors, inductors and solar cell resistance for example, has been considered in recent years. One way that can reduce the power dissipation in the system and improve the conversion efficiency is using switching techniques.

This report sets out to show a novel approach of a DC to AC inverter with the use of Golomb ruler and solar cell. A Golomb ruler can be defined as a ruler that has unevenly spaced marks at integer locations such that the space between any two marks is unequal unlike normal ruler [5]. The inverter is implemented by using opto - coupled MOSFET switches, which are controlled by the embedded micro-controller, to converter the DC generated by the solar cells to 50 Hz stepping AC output fed to the load.

1.1 A Novel approach:

The Golomb solar DC to AC inverter is a new to photovoltaic based systems by offering the advantage of not only using switches, but also applying a third order Golomb ruler. This project shows the use of a third order Golomb ruler to define the sequence of the DC source.

1.2 Aim:

This project aims to implement a new DC to 50Hz AC staircase inverter with only 2% distortion for photovoltaic application using Golomb ruler and switching technique.

1.3 CAD Software Package and Software Compliers involved in this Project:

MultiSim 8, MATLAB (R2011b), **CIRCAD** *(OmniGlyph - V6)*, Online Mbed Microcontroller Complier

1.4 Report structure:

This report is structured as follows:

- The *First part* provides the overall introduction and background. It consists of three chapters: Chapter1 offers the introduction, Chapter 2 provides the existing commercial systems and selected IEEE papers and Chapter 3 contains the background information about multilevel inverters, SMPS inverters, Solar Cell and Golomb ruler.
- The *Second part* details the specification, design, implementation and results. It contains four chapters: Chapter 4 provides the specification, Chapter 5 offers the design, Chapter 6 describes the implementation procedures and Chapter 7 offers the overall results of the project
- The *Third part* shows the evaluation and conclusion. It contains two chapters: Chapter 8 offers the evaluation of the system; Chapter 9 provides the conclusions of the project including the project planning and lesson learnt.

2 Existing Systems and Selected IEEE Papers

(This chapter provides a number of commercial solar inverters and selected IEEE papers)

There is no question that carrying out a project requires knowledge and information from existed work. Although this project is a novel, there is an interesting related work that can be applied to it. The use of solar inverters is widely increased in the commercial world and in the research field. Two of many research papers are included in this chapter due to the important knowledge that helped in doing this project.

2.1 Commercial Inverters:

The use of solar inverters in particular grid tie inverters has become common nowadays for public and private sections. There are many companies manufacturing grid tie solar micro – inverters such as Enecsys in the UK, Direct grid and Enphase in the USA. PV grid tie inverters can be classified as centralized inverters, string inverters, multi string inverters and micro-inverters. Micro-inverters which use a single inverter per panel are the most commercial systems today. Some of the manufactured grid tie micro-inverters are able to perform the maximum power point tracking technique MPPT.

2.2 Selected IEEE Papers:

There is no doubt that the number of multilevel inverters with switching topology is increased due to the reliability, high efficiency and simplicity. Two IEEE papers are selected in particular as they provide very interesting knowledge could be applied to this project.

Fundamental of an Efficient and Reliable staircase Multilevel Inverter for Photovoltaic Application

(Esfandiari, Bin Mariun, Marhaban & Zakaria, 2009)

This paper illustrates an efficient and reliable DC to AC multilevel inverter based on two ladders of switches structure. This inverter has two advantages which are low on state power dissipation and reliability when the switches fail in an open circuit form by a good switching strategy choice. The paper shows a way of how to choose the duration time for each level to reach a high quality near sinusoidal waveform and holds other relevant work that is applied to this project.

WTHD-Optimal Staircase Modulation of Single-Phase Multilevel Inverters

(Diong & Corzine, 2005)

This paper introduced an interesting relevant work of achieving minimum frequency-weighted THD output voltage in multilevel inverters. This paper shows elimination in the 3th harmonic by using unequal DC voltage source. In other words, the amplitudes of the step level of the output are not equal. This paper shows that using unequal step level illuminates the distortion harmonic more than using equal step. This inverter was implemented using two series H-bridge inverter topology. The knowledge from the paper could be applied to any future work on this project.

3 Background Information

(This chapter offers background information about multilevel inverters, SMPS inverters, Solar cell and Golomb ruler)

3.1 Multilevel Inverters:

It is widely believed that multilevel inverters have the best efficiency due to low switching frequency, low output distortion and low EMI [10]. There are many types of multilevel inverters and only the main topologies are presented briefly in the following table.

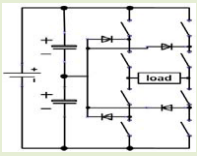
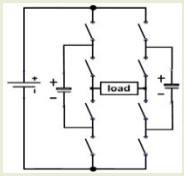
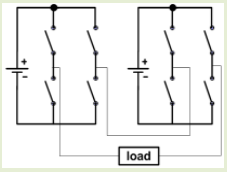
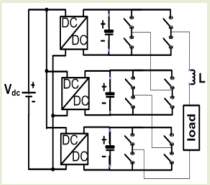
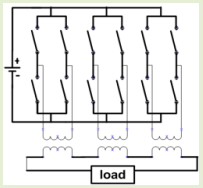
Diode Clamped	*Switched capacitor*	*Cascade H-bridge*		
		Transform less	**Bi-directional DC-DC**	**Multiple transformers**
				
- Single Source	- Single Source - Efficient	-Number of level =2S+1 (S: number of sources)	- Possible I/O Isolation - Single Source	- Single Source
- No I/O isolation	- No I/O isolation	- Multiple sources - No I/O isolation	High frequency	- Several low frequency transformers - I/O isolation

Table 1: Different design technique of multilevel inverters [content modified from 10 and figures taken from 10]

3.2 SMPS Inverters:

In general inverters can be identified by their output waveform such as modified sine wave inverters, multilevel inverters, pure sine wave inverters and square wave inverters. On other hand, some inverters can be specified by their circuit topology such as isolated SMPS inverters and non-isolated SMPS inverters. Reviewing the operations of the non- isolated converters such as Buck converter, Boost converter and Buck -Boost converter is more interesting than the isolated once. The reason of this is that the non- isolated design circuitry does not include transformer to isolate the input from the output. The three mentioned non-isolated converters are explained below.

3.2.1 Buck converter (step - down converter) [7]:

This is one of the forward modes DC -to- DC converters that have L-C filter circuit at the output, which is shown in Figure 1. The L-C filter generates a DC output voltage which is equal to the volt –time average of the AC input rectangular waveform of the LC filter. The output voltage is always less than the input voltage. The buck converter can be used for applications from few watts to several kilo watts output power.

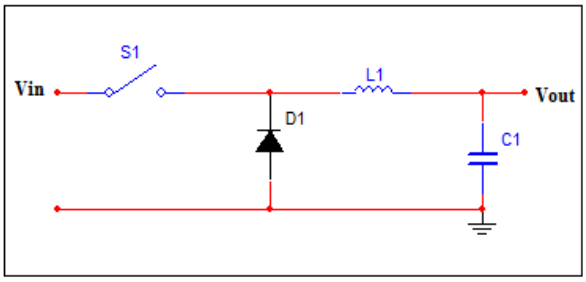


Figure 1: A single- switch buck inverter circuit

The operation of the above converter can be analysed into modes: continuous mode and discontinuous mode. In the continuous mode, the current through the inductor never drops to zero during the on and off periods, unlike discontinuous mode where the inductor current falls to zero at the end of the period. If the switch is closed, the diode is off (reverse biased). The inductor current forces the diode to become forward biased during the off state. The current and voltage waveforms of all D1, L1, S1, C1 and Vin for the continuous and discontinuous modes are included in the Appendix A with the steady state assumption.

3.2.2 Boost converter (step - up converter) [7]:

This is one of the flyback modes DC -to- DC converters that constructed from a diode and a capacitor circuit at the output, which is shown in Figure 2. The output voltage is always higher than the input voltage. The boost converter is used for applications from few watts to several kilowatts output power

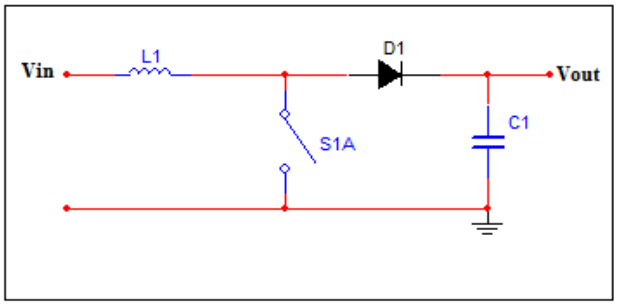


Figure 2: Single -switch boost converter

The operation of the above converter can also be analysed into modes: continuous mode and discontinuous mode. If the switch is closed, the diode is off (reverse biased). The inductor current forces the diode to become forward biased during the off state. The current and voltage waveforms of all D1, L1, S1, C1 and Vin for the continuous and discontinuous modes are included in the Appendix A with the steady state assumption.

3.2.3 Buck- boost converter [7]:

This is a DC -to- DC converter that produces an output with the reverse polarity of the input voltage. The output can be higher or lower than the input voltage.

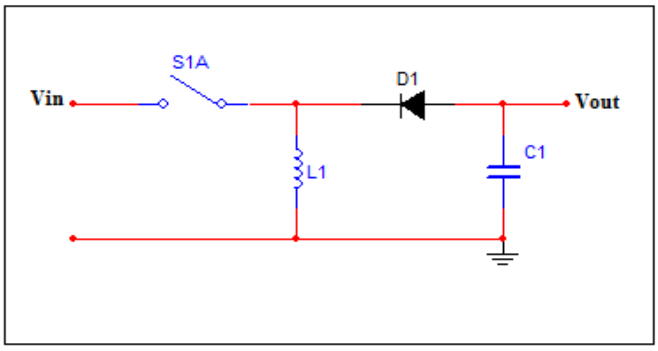


Figure 3: Single - switch buck -boost converter

Buck -boost converter with 4 switches and single inductor for DC to DC photovoltaic applications is exist with MPPT technique [9]. The overall performance of this existed system was good. However, the use of the capacitor and inductor in this converter makes the failure of the system is possible due to the high temperature, voltage stress and current stress.

3.3 Solar Cell:

3.3.1 Brief History of the Solar Cell:

The photovoltaic effect can be defined as a physical phenomenon which results from the conversion of the energy carried by optical electromagnetic radiation into electrical energy. The most common device that used in this conversion is solar cell. Solar cells are used as permanent energy sources in producing photovoltaic energy and they are now growing gradually on earth. In comparison with other sources, solar cells offer low cost and high power to weight ratio [1].

In 1839, Becquerel discovered the photovoltaic effect in electrochemical cells. He noticed that the action of light on an immersed of silver coated platinum electrode in electrolyte produced an electric current [2]. In fact, the first solid state photovoltaic devices were constructed forty years later. Adams and Day found in 1876 that the photocurrent can be produced in a sample of selenium when two heated platinum contacts contacted to it. The actions of photovoltaic and photoconductive of the selenium were different because of the fact that the current spontaneously produced by the action of light [2]. The early photovoltaic devices were fabricated by applying a junction between the metal and the semiconductor contact. In the 1950s, a good quality silicon wafer was introduced in the new solid state electronics. However, the first efficient silicon solar cell was developed by Chapin, Fuller and Pearson in 1954 [1]. The interest in photovoltaic expanded during the 1990s because of the need of the secure sources of electricity instead of fossil fuels [2]. The photovoltaic production expanded approximately by a rate of 15-25% per annum which led to cost reduction [2].

3.3.2 What is a solar cell? [2]

A solar cell can be defined as a two terminal device which conducts in the dark like a diode and produces photo- voltage in the light. In other words, when it is charged by the sun, it produces photo-voltage. It is fabricated as a thin slice of semiconductor material. Metal contacts are applied on the surface to produce electrical contact.

3.3.3 The Basic Structure of Solar Cell:

The basic structure of any solar cell consists of the following:

Contacts, Junction depth, Material and Doping (The basic structure figure is included in Appendix A)

3.3.4 Solar Cell Parameters:

- **Short Circuit Current and Open Circuit Voltage [1]:**

The greatest produced current by the cell is obtained under the short circuit conditions when the voltage is vanished V=0 and this current is called short circuit current I_{sc}. If the solar cell device is open circuit, it biases itself with a voltage that is called open circuit voltage V_{oc} which is equal to the greatest voltage value when the current is vanished as shown in the figure below.

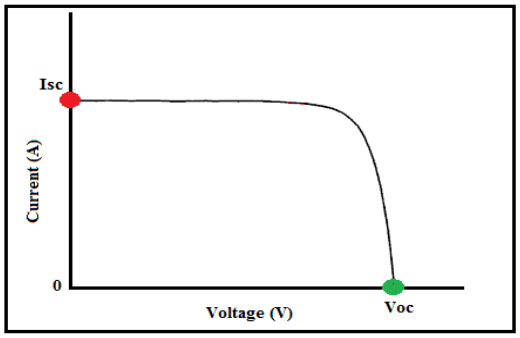


Figure 4: I-V characteristics curve of the solar cell

- **Maximum Power Point (MPP):**

It is a unique point on the I-V curve at which the cell operates with maximum efficiency and generates the maximum output power [4] as shown below.

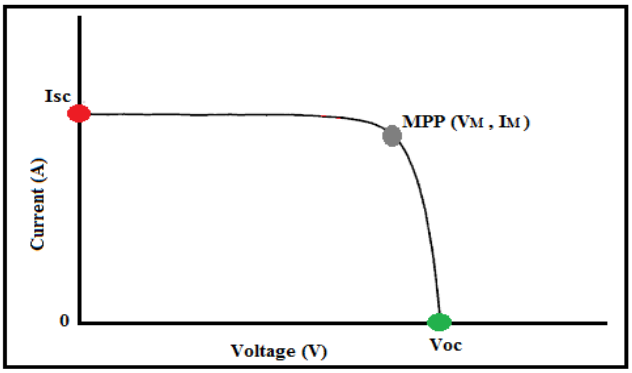


Figure 5: I-V curve for a solar cell with MPP

- **Fill Factor:**

It can be defined as the ratio of the maximum output power to the product of the open circuit voltage and short circuit current as given in the following equation [2].

$$FF = \frac{V_M I_M}{V_{OC} I_{SC}} \quad (1.1)$$

Where: $\mathbf{V_M}$: Voltage at MPP

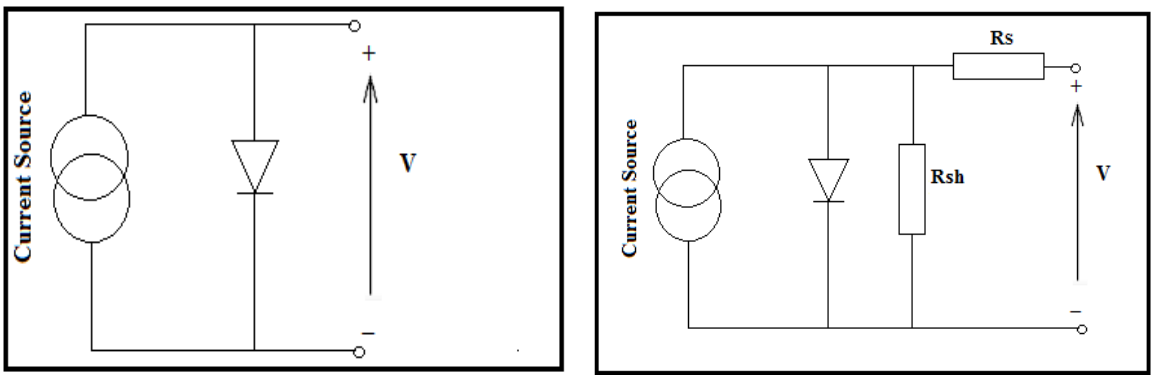
$\mathbf{I_M}$: Current at MPP

$\mathbf{V_{OC}}$: Open Circuit Voltage

$\mathbf{I_{SC}}$: Short Circuit Current

- **Series and Parallel Resistances:**

The ideal solar cell is equivalent to a current generator connected in parallel with a diode (non- linear resistive element) as shown in Figure 6 below. In fact, real solar cells are not perfect due to the appearance of the contact and the leakage current resistances which lead to power dissipation [2].



(a) (b)

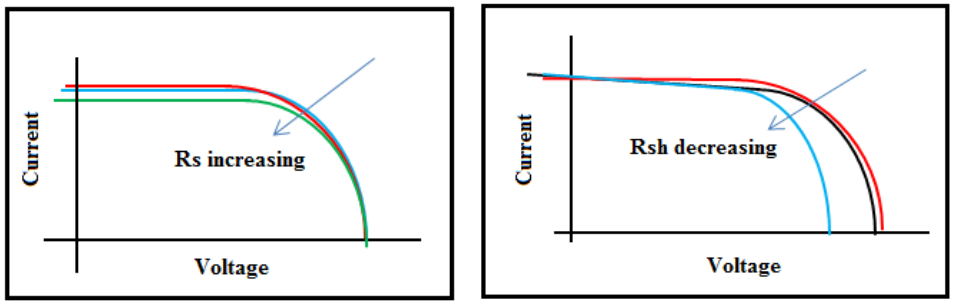
Figure 6: (a) Ideal solar cell equivalent circuit (b) Equivalent circuit of solar cell with resistances

The above figure shows the equivalent circuits of both cases ideal and non- ideal solar cell. The non- ideal case shows a series resistance which arises from the resistance of the cell material and the contact resistance whereas the shunt resistance arises from the leakage current through the cell [2].

Effects of the resistances [2]:

- Reducing Fill Factor
- Significant reduction in the short circuit current (I_{SC}) when R_s is high
- Significant reduction in the open circuit voltage (V_{OC}) when R_{sh} is low

The effect of the series resistance and the shunt resistance on the I-V curve is shown below:



(a) (b)

Figure 7: The effect of series and parallel resistances in the I-V characteristics

It can be absorbed from the figure above that the efficiency of the cell can be improved by reducing the series resistance and increasing the shunt resistance.

3.3.5 The Effect of Temperature on the Cell:

Temperature is one of the parameters that affect the behaviour of the device. For example, the photocurrent increases with temperature due to the greater number of the minority carrier and narrower band gap [1]. The open circuit voltage reduces more significant than the increase of photocurrent as shown in the following figure.

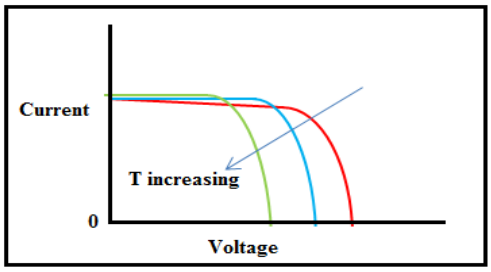


Figure 8: The effect of temperature on the IV characteristics

It can be concluded form the figure above that increasing temperature affects the open circuit voltage and FF more than the current.

3.3.6 The Effect of Illumination Intensity on the Cell [1]:

The solar cell operation is directly proportional to the light intensity. The effect of the light intensity on the current and voltage can be analysed as follows. If the photocurrent at a light level of unity is I_{L1}, the photocurrent at X light level is given by

$$I_L = X\ I_{L1} \qquad (1.2)$$

If the open circuit voltage at the unity light level is V_{oc1}, the voltage at X light intensity is given by:

$$V_{OC} = V_{OC1} + m\frac{kT}{q}lnX \quad (1.3)$$

Where: **m**: Ideality factor $1 \leq m \leq 2$ q: 1.6×10^{-19} Coulombs

k: Boltzmann's constant (1.381×10^{-23} J/K)

T: Absolute Temperature

The fill factor and the efficiency of the cell increase with the intensity of light level.

3.4 Golomb Ruler:

3.4.1 What is a Golomb ruler [5, 6]?

A Golomb ruler is a ruler that has unevenly spaced marks at integer locations. The distance between any two marks is different, unlike normal rulers where the distance between any two marks are equal. Golomb rulers have the ability to measure more distances than the number of marks on them. The required distance on Golomb ruler exists only in one place unlike common ruler where it can exist in different location. For example, if one mark is located at position 1 on Golomb ruler and the other at position 5 which forms a separated distance of 4 that should not appear between any other pair of marks.

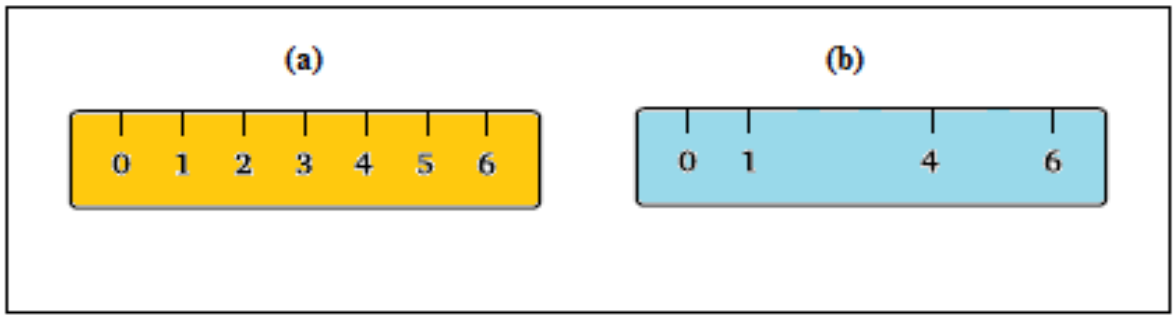


Figure 9: (a) Common ruler (b) Golomb ruler

The above figure illustrates an example of Golomb ruler and common ruler of length of six. Both rulers can measure distances from 1 to 6. Golomb ruler in the figure above can measure the distances [1, 2, 3, 4, 5, 6] and only two marks can be used to do the required measurement.

3.4.2 Perfect Golomb rulers [6]:

A perfect Golomb ruler has the ability to measure exactly $\frac{1}{2}m(m-1)$ distances with m marks. Figure 9 above illustrates an example of a perfect ruler with four marks. The following rulers are the only perfect rulers exist with their mirror images:

Original Ruler	Mirror Image	
(m=0) 0	0	
(m=2) 0 1	0 1	
(m=3) 0 1 3	0 2 3	(used in this project)
(m=4) 0 1 4 6	0 2 5 6	

3.4.3 Optimal Golomb ruler [6]:

It can be defined as the shortest possible length Golomb ruler with m marks beyond the highest order perfect ruler. For example, Golomb ruler with 5 marks of 0 1 4 9 11 can measure the following distances {1 2 3 4 5 7 8 9 10 11}. This ruler is called optimal ruler as distance 6 can not be measured as shown in the figure below.

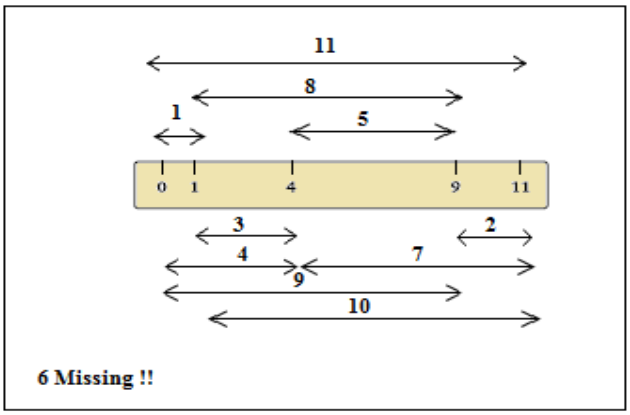


Figure 10: Optimum Golomb ruler

3.4.4 Uses of Golomb rulers [6]:

- Solving the interference between radio communication channels (illuminating third order interference)
- Ranging from coding theory to radio astronomy

Part II

Specification, Design, Implementation

And Results

4 Specification

(This chapter provides the project specification (product specification and component specification) in a standard format)

4.1 Product Specification:

Third order Golomb solar inverter is a product that converts the DC generated by three solar cells into a power that can drive a load resistance with only 2% distortion. Providing 8% less series solar cell resistance loss, low cost, low EMI and low switching frequency.

Technology:

- An embedded microcontroller is the core of this inverter to control the states of the switches
- No need for a cooling fan
- No need for capacitor and inductor

Features:

- Lightweight and Portable
- Low cost and simple design with 6 opto- coupled MOSFET switches
- Communication via USB cable
- Easy access to DC (solar cell) and AC terminals (Three terminals to the DC source and two for the AC output)
- Golomb inverter can be integrated

Performance:

- 8% less series solar cell resistance loss
- Low distortion (2%)
- 6 levels stepping AC waveform output
- Optimum load of 79Ω at MPP, best output performance in the range of 15kΩ - 1MΩ load resistance

Electrical Specification - Input		
Maximum short circuit current of three solar cell	69mA	(Maximum light level)
Maximum open circuit voltage of three solar cells	1.44V	(Maximum light level)
Voltage at MPP of one cell	0.33V	(Maximum light level)
Voltage at MPP of one two cells	0.711V	(Maximum light level)
Voltage at MPP of three cells	1.025V	(Maximum light level)

Electrical Specification - Output	
AC Frequency	50Hz
SNR	(17dB)
Output V_{pp}	3V
Output waveform	AC Stepping waveform
AC frequency range	49.8 -50Hz
Optimum load at MPP	79Ω (Distorted output waveform)
Load range for best stepping AC waveform	(15kΩ - 1MΩ)

Mechanical and Environmental Specification	
Temperature range	5-30°C
PCB size	L =13.2cm / W= 9.9cm
Cooling	Fan not required
Capacitor and inductor	Not required
Communication	USB cable

4.2 Component Specification:

(Regenerated from the Interim Report)

Golomb inverter is implemented by using the following specified components:

4.2.1 Solar Cell [11]: *(Three of these are required to form the DC source and satisfy the third order Golomb ruler)*

- Fully encapsulated solar cell modules mounted in a black polycarbonate cases
- Fitted with threaded stud terminals and a copper bus bar

Output voltage	0.45V
Output Current	100mA
Height	7.5mm
Width	26mm
Length	45mm
Module type	G100
Price	£1.18

This is the manufactured specification where the output voltage and current for are specified for A light intensity.

Figure 11: Solar cell [11]

4.2.2 MBED (ARM controller) [11]: *(One Mbed microcontroller is required to implement the system)*

This is the manufactured specification of the microcontroller.

Form-factor:

- 40-pin DIP package
- 0.1" pitch, 0.9" pin spacing
- 54mm x 26mm

Power:

- Powered by USB or 4.5v - 9.0v applied to VIN
- <200mA (100mA with Ethernet disabled)
- Real-time clock battery backup input VB
- 1.8v - 3.3v Keeps Real-time clock running
- Requires 27uA, can be supplied by a coin cell
- 3.3v regulated output on VOUT to power peripherals
- 5.0v from USB available on VU (only available when USB is connected!)
- Current limited to 500mA
- Digital IO pins are 3.3v, 40mA each, 400mA max total

Pin:

- Vin - External Power supply to the board
- 4.5v-9v, 100mA + external circuits powered through the Microcontroller
- Vb - Battery backup input for Real Time Clock
- 1.8v-3.3v, 30uA
- nR - Active-low reset pin with identical functionality to the reset button.
- Pull up resistor is on the board, so it can be driven with an open collector
- IF+/- - Reserved for Future use

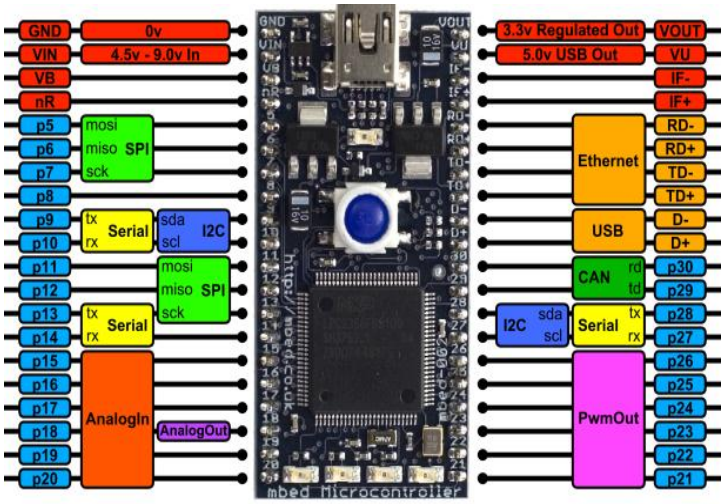


Figure 12: Mbed (ARM controller) [11]

This Mbed Microcontroller is based on a Cortex-M3 Core running at 96MHz, with 512KB FLASH, 64KB RAM and a load of interfaces including Ethernet, USB Device, CAN, SPI, I2C and other I/O package [11].

4.2.3 Opto- Coupled DC/AC MOSFET Switches [11]: *(Six of these are required to implement the system)*

This is the manufactured specification of the opto - coupled MOSFET switches.

Peak load voltage (AC/DC)	350V
Contact Form	1A SPNO
Number of terminal	4
Load current cont.	120mA
Manf. Part No.	G3VM-351A
ON++ Resistance Ω	Max. 50Ω, Typ.35Ω
LED trigger current	Max 3mA, Typ. 1mA
Turn on time	Max 1ms, Typ. 0.3ms
Turn off time	Max 1ms, Typ. 0.1ms

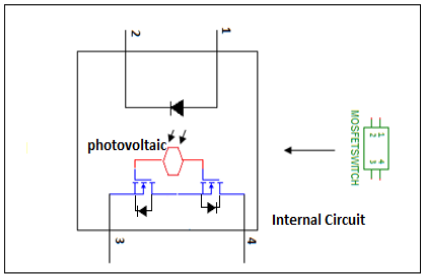


Figure 13: The internal circuit of Opto - coupled MOSFET [11]

The internal LED specification:

Reverse Voltage (max)	5V
Forward Voltage	Max 1.3V, Typ. 1.15V
Forward current (max)	50mA (HI-PERF 30mA)
Insulation resistance (min)	1000MΩ
Capacitance (Input to output)	0.8pF (typ.)
Off state leakage current (max)	1 μA
Operation temperature range	- 40°C to +85°C

5 Design

(This chapter offers the project design (Hardware and Software))

5.1 Design Description:

The aim of this project is to implement a new DC to AC (50Hz) multilevel inverter with 2% distortion for photovoltaic application using Golomb ruler and switching technique. One of the required procedures to satisfy the implementation of this product is the design which is a combination of *Hardware and Software*.

The basic structure of this inverter consists of two rails with six opto- coupled MOSFET switches in total which are controlled by the Mbed microcontroller in this project. Both rails employ equal number of controllable MOSFET switches connected to three identical solar cells (DC source) such that a third order Golomb ruler (perfect ruler)[1] is formed as shown in the basic structure below.

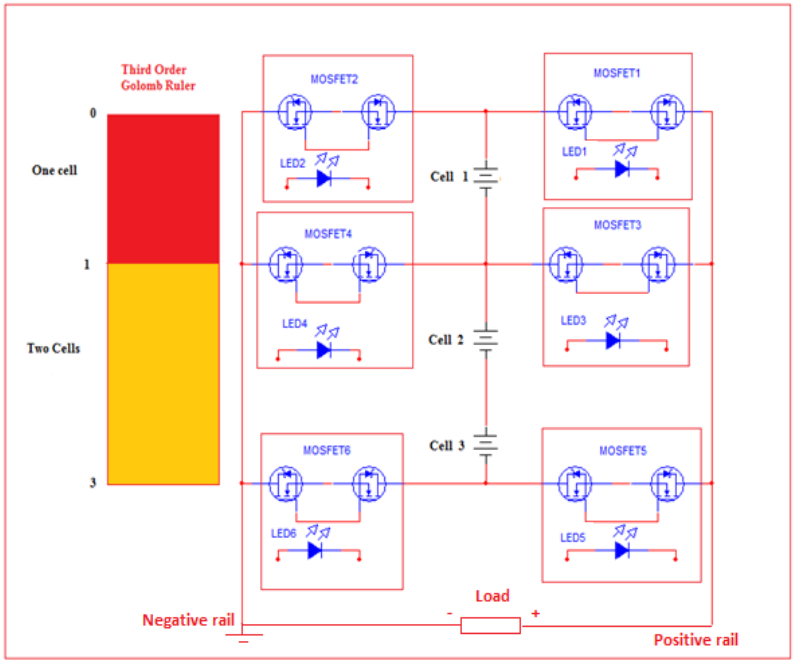


Figure 14: Basic structure of Golomb inverter of 6 levels

The figure above illustrates how Golomb ruler is applied to the structure of the inverter. The reason for using the Golomb ruler in this project is that the maximum number of different voltages is obtained for a given number of taps. This significantly reduces the number of MOSFETs required compared to a conventional equally-spaced ruler. The positive rail includes MOSFET1, MOSFET3 and MOSFET5 whereas the negative rail includes MOSFET2, MOSFET4 and MOSFET6.The different levels of DC voltages (V1 cell1, V2 cell2 and V3 cell3) are selected by controlling the switches in a specific way.

According to the structure of the 6 levels inverter in figure above, the switching states of the positive half cycle and negative half cycle are given in Table 2 and Table 3 respectively. (Note that the solar cells are identical (V1=V2=V3))

[1] The third order Golomb ruler can be defined as the non-trivial ruler with three marks and it is known as the third perfect Golomb ruler, more information is included in chapter 3, part 3.4.2

MOSFET1	MOSFET2	MOSFET3	MOSFET4	MOSFET5	MOSFET6	Output	Time duration
1	0	0	1	0	0	V1	T1
0	0	1	0	0	1	V2+V3	T2
1	0	0	0	0	1	V3+V1+V2	T3
1	0	0	0	0	1	V3+V1+V2	T3
0	0	1	0	0	1	V2+V3	T2
1	0	0	1	0	0	V1	T1

Table 2: Switching states for 6 levels Golomb inverter of the positive half cycle

MOSFET1	MOSFET2	MOSFET3	MOSFET4	MOSFET5	MOSFET6	Output	Time duration
0	1	1	0	0	0	-V1	T1
0	0	0	1	1	0	-V2-V3	T2
0	1	0	0	1	0	-V3-V1-V2	T3
0	1	0	0	1	0	-V3-V1-V2	T3
0	0	0	1	1	0	-V2-V3	T2
0	1	1	0	0	0	-V1	T1

Table 3: Switching states for 6 levels Golomb inverter of the negative half cycle

Table1 and Table2 above shows that at any instant only two switches are conducting and others are off. If MOSFET1 and MOSFET4 are switched on, the output voltage equals V1 while switching MOSFET2 and MOSFET3 on, the output equals to -V1.

To produce an efficient output near sinusoidal, T_n can be found by using the simple technique illustrated in figure 15 below.

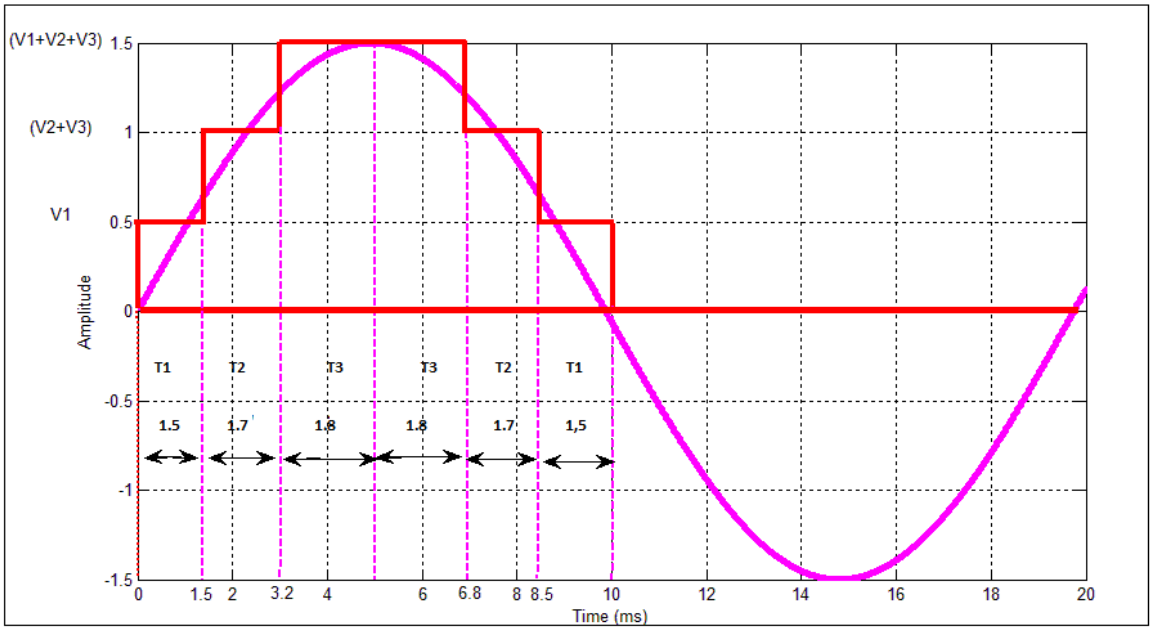


Figure 15: Time coordinates for the positive half cycle of the inverter (6 levels, 50Hz)

The time coordinates for the positive half cycle is chosen by drawing the step lines of the fixed amplitude on a pure 50 Hz sinusoidal output and then using line dropping to find the corresponding time values, T1,T2 and T3. The steps that contribute in the output waveform start with low time instant and increase gradually to approximate a sinusoidal output as clearly illustrated in the figure above (T1=1.5ms, T2=1.7ms and T3=1.8ms).The negative half cycle will follow the same roles. It is

true that the above figure shows the time instant for each level, in the implementation process is slightly tuned to produce a good quality stepping waveform with 6 levels.
The optimum load can be extracted from the MPP figure of the implemented system which is explained in details in chapter 6.

5.2 The simple software algorithm diagram:

The diagram below illustrates how the software algorithm is designed such that the required 50 Hz output waveform is generated.

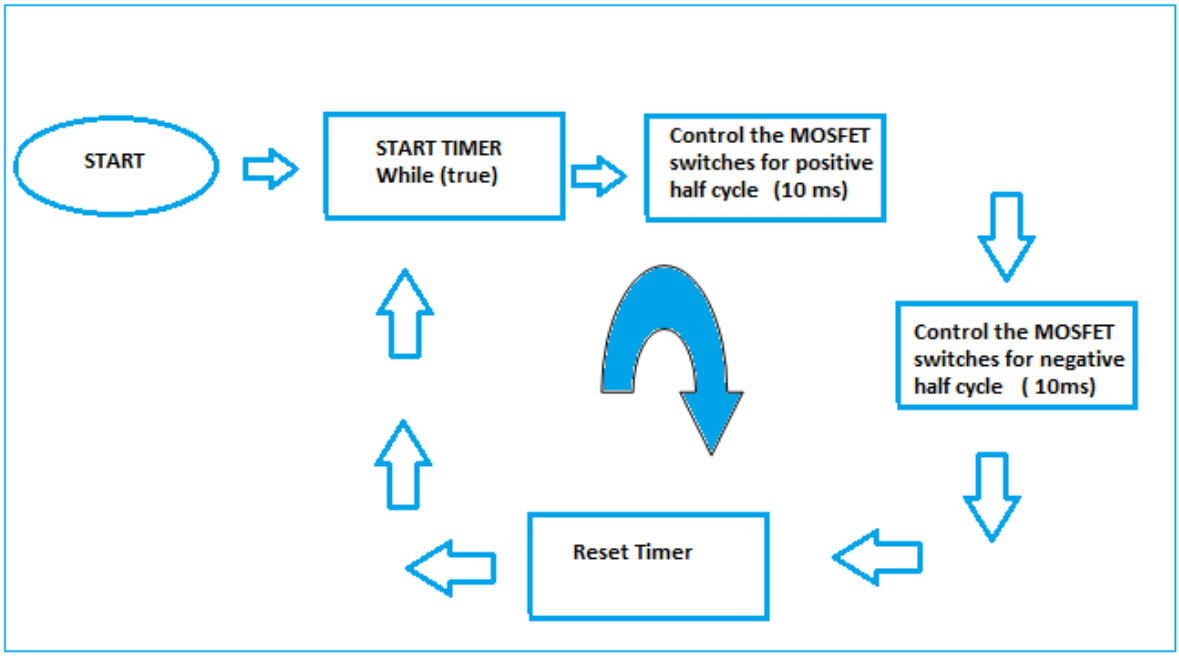


Figure 16: The simple software algorithm diagram

The Figure above clearly illustrates that the output waveform is generated in an infinite loop system. The program is designed such that only two MOSFET switches are conducting at any instant.

5.3 Low level project design:

This part illustrated the pin configuration of each component in low level format. It is shown in chapter 4 that the Mbed microcontroller consists of 40 pins whereas the opto- coupled MOSFET switches consist of 4 pins. The pins of the microcontroller are defined as **DigitalOut** pins to control the MOSFET switches.

- **Pin configuration:** *(Regenerated from the Interim Report)*

Mbed Pins	Connection
Pin15	Pin1 of MOSFET3
Pin16	Pin1 of MOSFET3
Pin17	Pin1 of MOSFET1
Pin18	Pin1 of MOSFET2
Pin19	Pin1 of MOSFET4
Pin20	Pin1 of MOSFET6
GND Pin1	Pin2 of MOSFET1, MOSFET2, MOSFET3, MOSFET4, MOSFET5, MOSFET6

Table 4: Pin configuration

The internal circuit of the MOSFET switches shows an LED which connected to Pin1 and Pin2 of the switch. The first pin of each switch is connected to the Mbed as specified in Table 4.

The second pin of each switch is connected to a limiting current resistance of 2 kΩ value to prevent the LED from burning up and then grounded in the Mbed side. Pin3 of MOSFET1, MOSFET3 and MOSFET5 are connected to the load impedance while Pin3 of MOSFET2, MOSFET4 and MOSFET6 are connected to the other side of the load. Pin4 of both MOSFET2 and MOSFET1 is connected to the positive side of the first cell while the negative side is connected to the second cell through the positive end and then to Pin4 of both MOSFET4 and MOSFET3. The negative side of the second cell is connected to the positive side of the third cell. The negative end of the third cell is connected to Pin4 of both MOSFET5 and MOSFET6. The complete MultiSim circuit design is illustrated below.

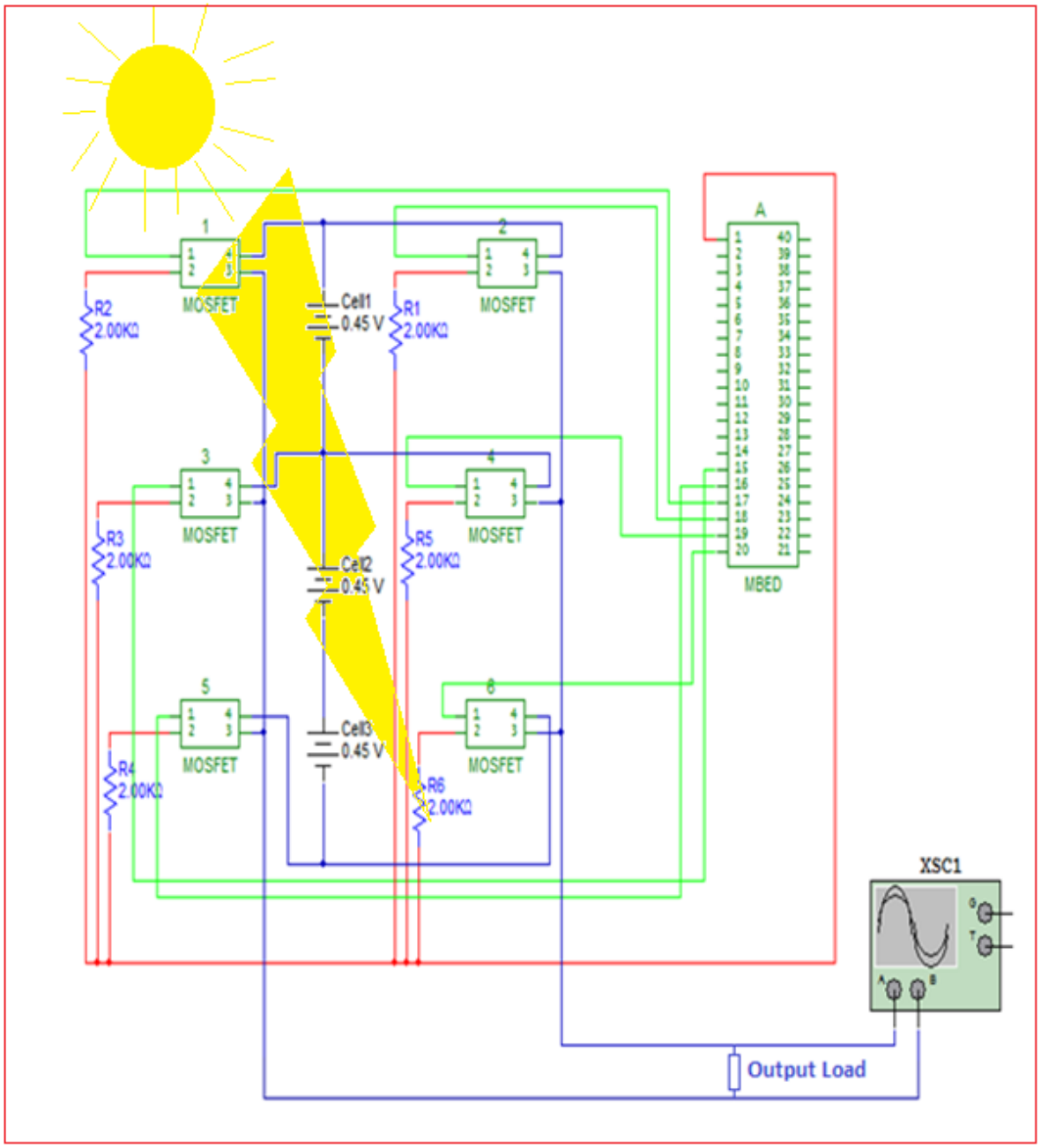


Figure 17: Project MultiSim Circuit Design

5.4 PCB design procedure:

PCB design is done in a single layer (Upper copper) board by using CIRCAD (**OmniGlyph - V6**) tool following the steps shown below:

a) **Open** CIRCAD tool and from the **File** menu select **New** to create a new file
b) **Save** as the created file when the dialog box appears and name the file and click **Confirm.**
c) Select **Build component** from **Block** menu to build the Mbed and the opto- coupled MOSFET switches as they are not exist in the component list of the package**.** In this process the user is asked to enter the PCB dimension of the new components, the number of Pins and save them as TH components.
d) **Place component (**one **Mbed**, six **MOSFET** switches and six **Resistances** of 1/2 Quarter size) from **Place menu.**
e) **Place** wires between the components as specified in the circuit design in Figure17 and ensure that they are not overlapping.
f) **Place** three Pads from **Place** menu (These Pads are connected to the solar cells)
g) Do **Connectivity** and **Netlist** checks for the circuit to ensure that the components are connected.
h) The PCB is sized to (13.2cm×9.9cm) to ensure enough space for the solar cells as shown in the figure below.
i) For fabrication Gerber file is exported

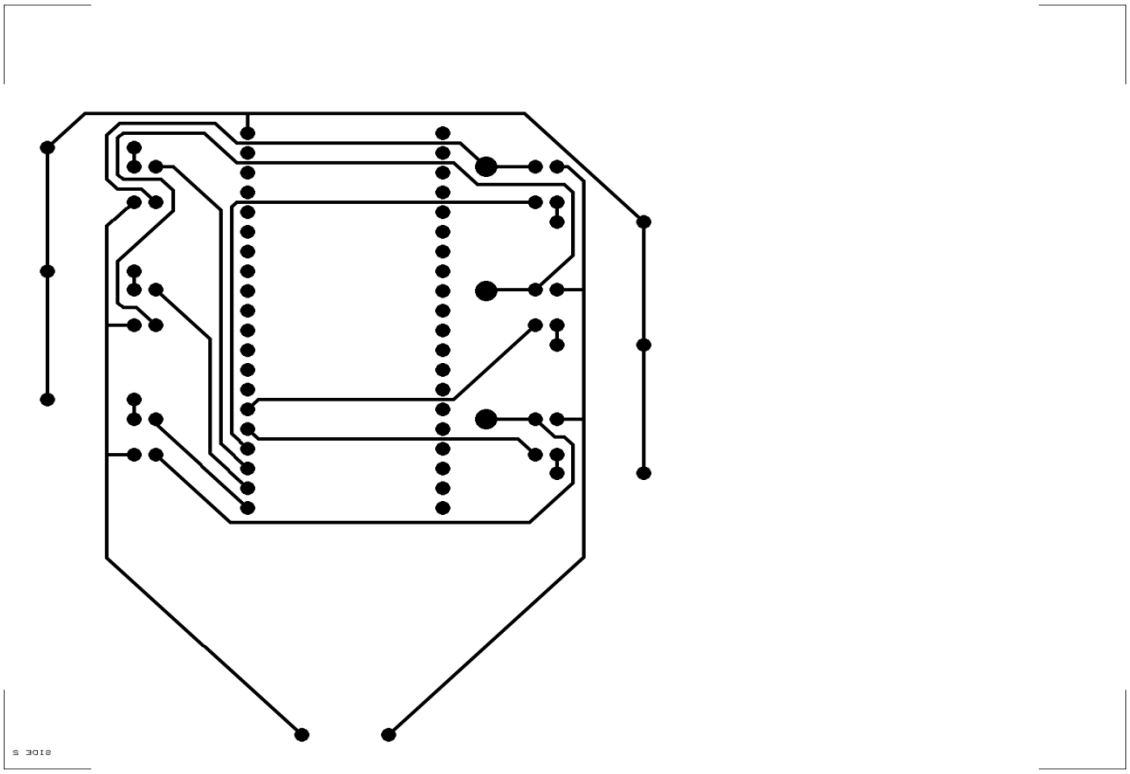


Figure 18: Project PCB Design

6 Implementation

(This chapter describes the project implementation procedures including all the required testing and problems faced)

This part of the report describes all the practical work including the required testing that carried out throughout the project period to meet the specification. The output characteristics of the solar cells such as open circuit voltage, short circuit current and maximum power point are analysed in the form of P-R and I-V curves. I-V and P-R test circuits (for one cell, two series and three series cells) and the corresponding results are explained in details in this chapter. The measurement of the short circuit current and open circuit voltage at different light intensity is included. Testing the operation of the opto- coupled MOSFET switches is also described in this section. The overall implementation of the inverter including all the problems is described in details in this part of the report.

6.1 How the solar cells used in this project work?

It is shown in chapter 5 that the inverter consists of three identical solar cells. These are expressed in this chapter in the form of I-V and P-R curves to investigate their characteristics. I-V and P-R curves for the individual cells are performed. I-V curves for two series cells and three series cells are also included. The behaviour of the solar cell at different light intensity is also performed (This particular test is done for only one cell).

6.1.1 Solar Cell Testing Procedures:

Equipment:

The equipment used in the different solar cell test circuits are stated below:

Power supply model GPS 3303, Ammeter: Model 8 MK III, solar Cells: 0.45V-100mA, Resistor box Briggs Tol. ±1% Max 99999, Voltammeter DM 441B Digital multimeter, Light sourced 1cm from the cells. (Light source is placed at 1cm from the cells)

Method[2]:

The short circuit Isc of a single cell, two series cells and three series cells is measured by using the simple test circuits shown in Figure (19.a), Figure (20.a), Figure (21.a) below when load impedance is 0. The I-V curves of a single solar cell, two series cells and three series solar cells are generated by varying the value of the variable resistor from 99999Ω to 1Ω (As it is available at the resistor box) and measuring the corresponding voltage as shown in Figure (19.b), Figure (20.b) and Figure (21.b) respectively. The corresponding current at different load resistance is calculated by using Kirchhoff law. The open circuit voltage is found when the current is 0 and the load resistance is large. The corresponding power **P** at different load resistance is calculated by $P = \frac{V^2}{R}$.

[2] In this testing procedure, all the measurements are taken under that same conditions of light level (light source is placed at 1cm from the cells) and environment.

- **Single Cell Test Circuits:**

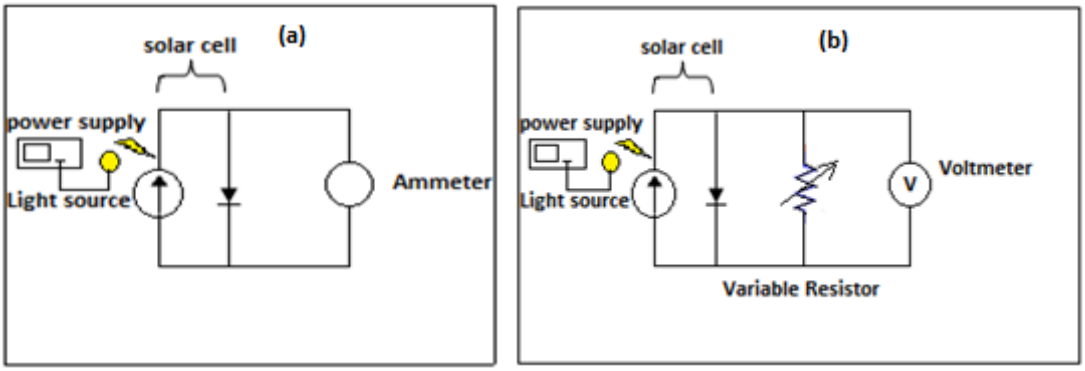


Figure 19: (a) Test circuit to measure Isc of a single solar cell, (b) Test circuit to measure the voltage at different load resistance [11]

- **Two Series Cells Test Circuits:**

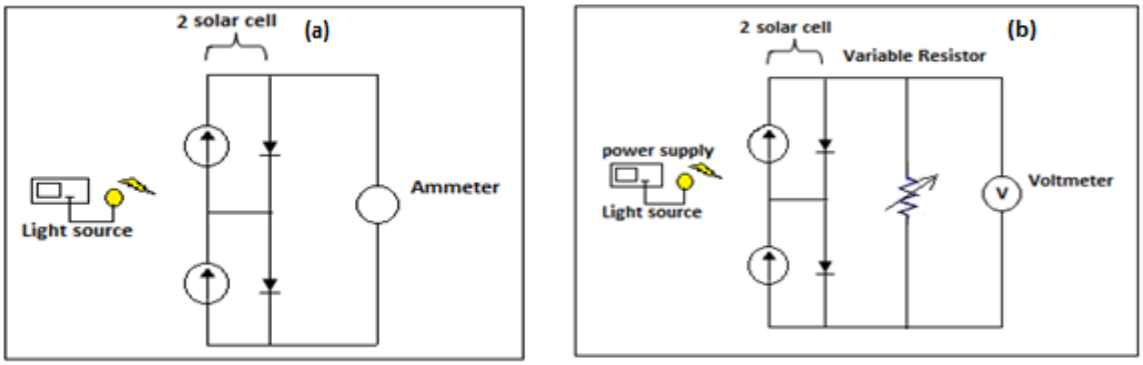


Figure 20: (a) Test circuit to measure Isc of Two series solar cells, (b) Test circuit to measure the voltage at different load resistance [11]

- **Three Series Cells test circuit:**

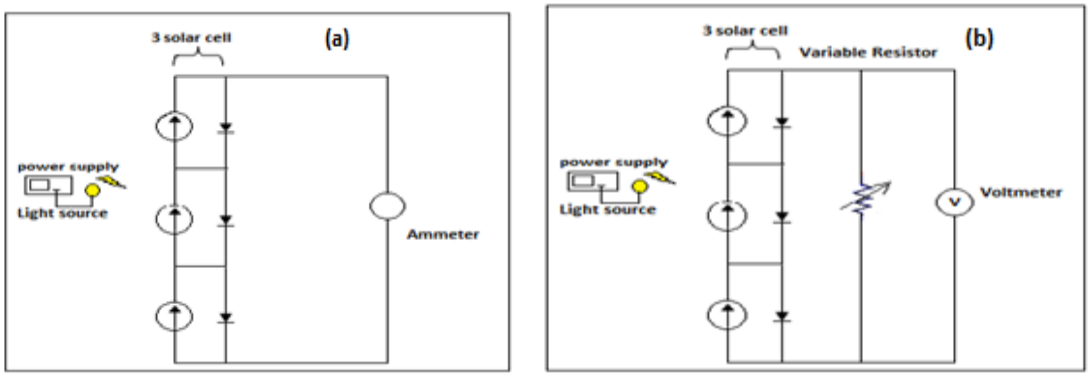


Figure 21: (a) Test circuit to measure Isc of Three series solar cells, (b) Test circuit to measure the voltage at different load resistance [11]

6.1.1.1 Output Characteristics of the Individual Solar Cell: *(Regenerated from the Interim Report)*

- **I-V and P-R Characteristics of Cell 1 :**

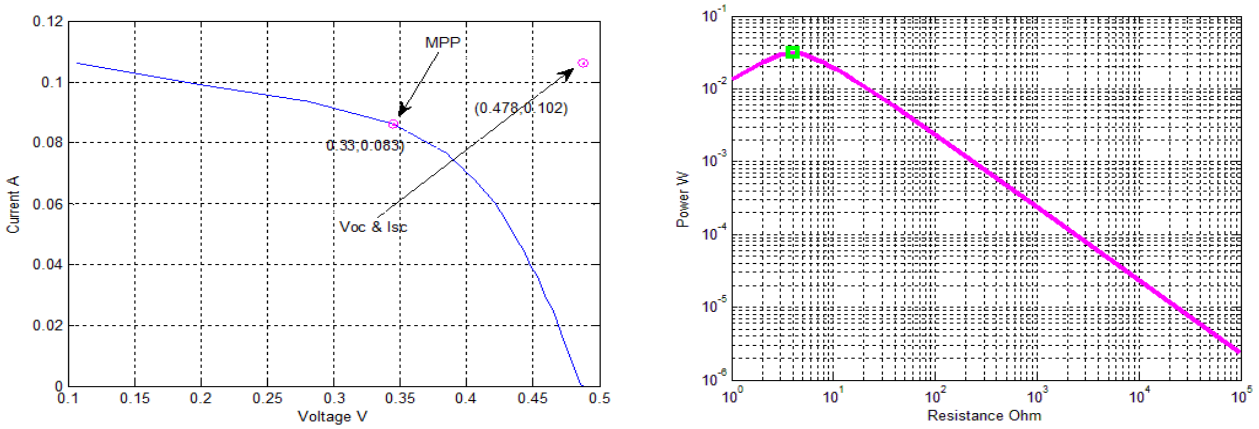


Figure 22: I-V and P-R curves of Cell1

The overall results of short circuit current I_{SC}, open circuit voltage V_{OC}, current at maximum power point I_{MPP}, voltage at maximum power point V_{MPP}, maximum power P_{max}, optimum resistance $R_{optimum}$ and fill factor FF of Cell 1 are illustrated in the table below:

I_{sc}	V_{oc}	V_{MPP}	I_{MPP}	P_{max}	$R_{optimum}$	FF
0.102A	0.478V	0.33V	0.083A	0.0239W	4Ω	0.55

Table 5: Cell 1 Results

- **I-V and P-R Characteristics of Cell 2 :**

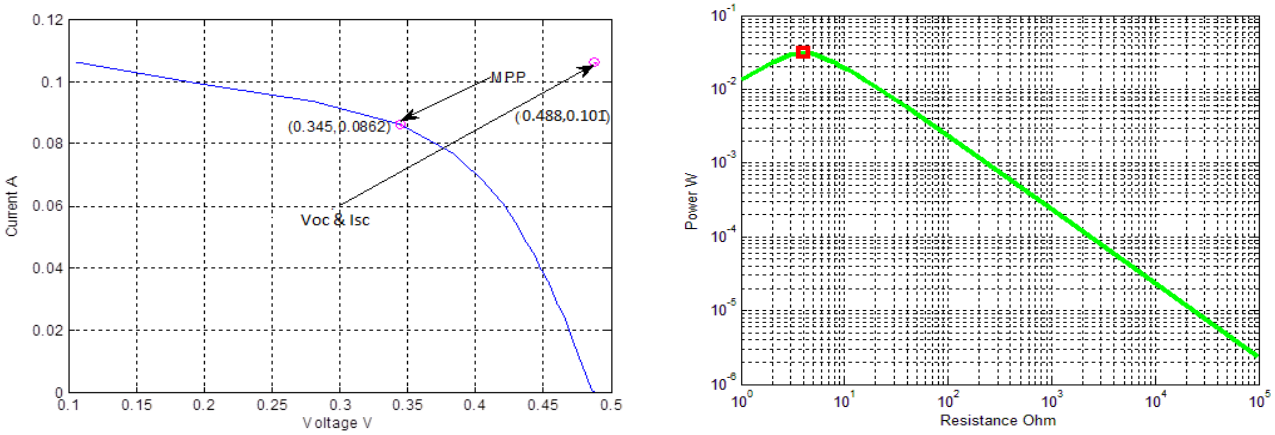


Figure 23: I-V and P-R curves of Cell 2

The overall results of short circuit current I_{SC}, open circuit voltage V_{OC}, current at maximum power point I_{MPP}, voltage at maximum power point V_{MPP}, maximum power P_{max}, optimum resistance $R_{optimum}$ and fill factor FF of Cell 2 are illustrated in the table below:

I_{sc}	V_{oc}	V_{MPP}	I_{MPP}	P_{max}	$R_{optimum}$	FF
0.101A	0.488V	0.345V	0.0862A	0.0297W	4Ω	0.6

Table 6: Cell 2 Results

- **I-V and P-R Characteristics of Cell 3 :**

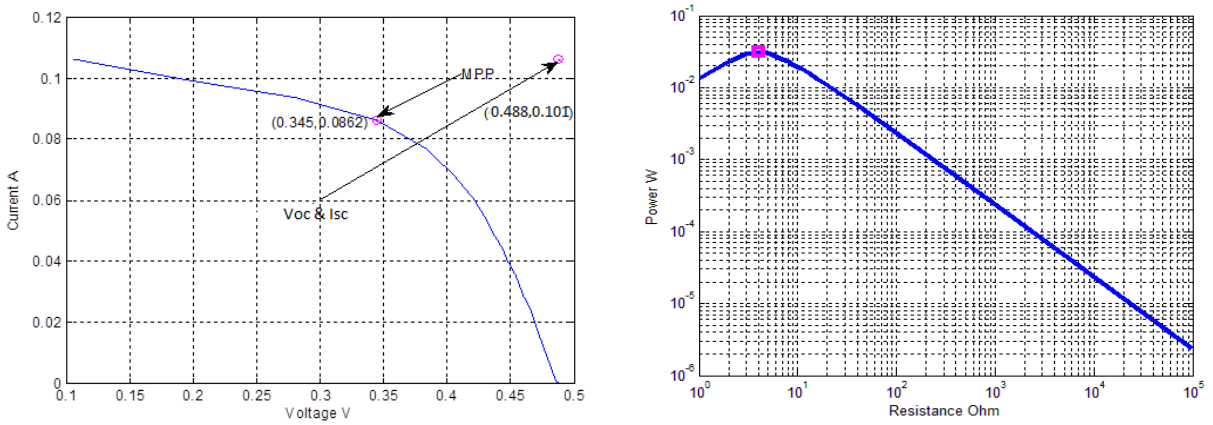


Figure 24: I-V and P-R curves of Cell 3

The overall results of short circuit current I_{SC}, open circuit voltage V_{OC}, current at maximum power point I_{MPP}, voltage at maximum power point V_{MPP}, maximum power P_{max}, optimum resistance $R_{optimum}$ and fill factor FF of Cell 3 are illustrated in the table below:

I_{sc}	V_{oc}	V_{MPP}	I_{MPP}	P_{max}	$R_{optimum}$	FF
0.101A	0.488V	0.345V	0.0862A	0.0297W	4Ω	0.6

Table 7: Cell 3 Results

6.1.1.2 Output Characteristics of Two Series Solar Cells: *(Regenerated from the Interim Report)*

- **I-V and P-R Characteristics of Cell 2 and Cell3 in series :**

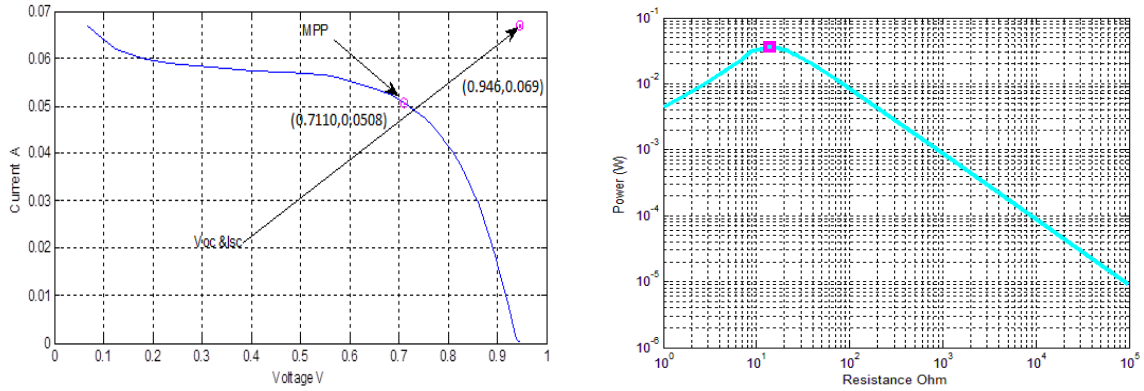


Figure 25: I-V and P-R curves of Cell 2 and Cell 3 in series

The overall results of short circuit current I_{SC}, open circuit voltage V_{OC}, current at maximum power point I_{MPP}, voltage at maximum power point V_{MPP}, maximum power P_{max}, optimum resistance $R_{optimum}$ and fill factor FF of Cell2 and Cell 3 in series are shown in the table below:

I_{sc}	V_{oc}	V_{MPP}	I_{MPP}	P_{max}	$R_{optimum}$	FF
0.069 A	0.946 V	0.7110 V	0.0508 A	0.036 W	14Ω	0.55

Table 8: Results of Cell 2 and Cell 3 in series

6.1.1.3 Output Characteristics of Three Series Solar Cells: *(Regenerated from Interim Report)*

- **I-V and P-R curves of Cell 1, Cell 2 and Cell 3 in series:**

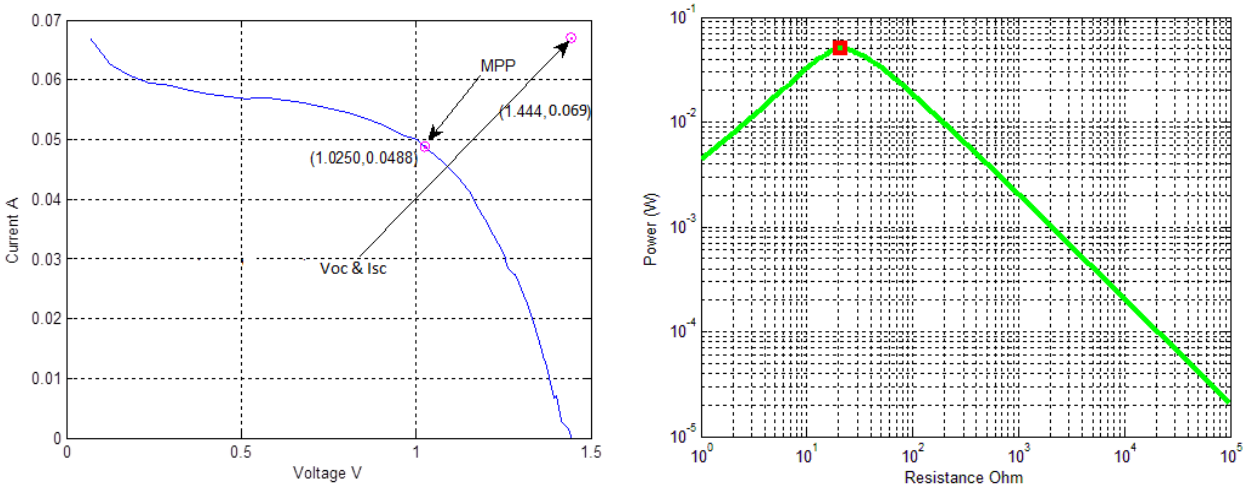


Figure 26: I-V and P-R curves of Cell 1, Cell 2 and Cell 3 in series

The overall results of short circuit current I_{SC}, open circuit voltage V_{OC}, current at maximum power point I_{MPP}, voltage at maximum power point V_{MPP}, maximum power P_{max}, optimum resistance $R_{optimum}$ and fill factor FF of Cell1, Cell2 and Cell3 in series are shown in the table below:

I_{sc}	V_{oc}	V_{MPP}	I_{MPP}	P_{Max}	$R_{optimum}$	FF
0.069 A	1.444 V	1.025 V	0.0488 A	0.05002 W	21Ω	0.5

Table 9: Results of Cell1, Cell2 and Cell3 in series

It can be concluded from the overall solar cells testing that the electrical parameters including open circuit voltage, short circuit current and optimum resistance of the individual cells are approximately equal. I-V and P-R curves for the individual cells are approximately identical. Although the measurements are taken under the same conditions of light level and environment, the short circuit current of the two cells in series is reduced and the optimum resistance is increased by a factor of three compared with individual resistance of each cell. The optimum resistance of Cell 2 and Cell 3 individually is 4 Ω, whereas 14Ω when they are in series. Besides that the optimum resistance of the three cells (Cell 1, Cell 2 and Cell 3) in series is approximately five times bigger than the individual optimum resistance. The question can be asked why the optimum resistance when the cells in series does not add up to their individual values. One reason could cause a reduction in the short circuit current and significant increasing in the optimum resistance is the partial shading effect which can be defined as half of cell area is shaded as shown in the figure 27 below. In real life situation, the shading effect occurs by weather parameters such as cloud.

Partial shading effect changes the electrical parameters of solar cells such as the short circuit current, the open circuit voltage and the optimum resistance [12]. Therefore, the reason of increasing the optimum resistance in the two cells and three cells in series illustrated earlier is that one or two cells are partially shaded. The parameters of the shaded cells are dominated in the results.

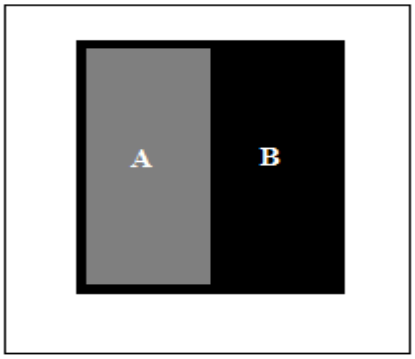


Figure 27: Model of partial shaded cell

It can be observed from the figure above that part B is completely shaded whereas part A is not shaded. To overcome the effect of this problem, a bypass diode is connect in parallel to each cell which can pass the current produced by the un shaded cell to avoid the high resistance and avoid damage the cell [12].

6.1.1.4 Performance of a Single Solar Cell at Different Light Intensity:

In real life situation the solar cells are affected by a number of different parameters such as rain, cloud and temperature. Changing light intensity (sun set and sun rise) is another parameter that affects the performance of the solar cell. This part shows how the behaviour of Cell1 changes under different light intensity. In this simple test, the open circuit voltage and short circuit current are measured under different light intensity by following the setup showed in the previous parts. The result of this simple test is shown in the table below. (Note that the light source is placed at 1cm form the cell)

V_{oc} (V)	I_{sc} (A)	Light level
0.489	0.1	**100%**
0.381	0.07	**70%**
0.271	0.05	**50%**
0.096	0.02	**20%**

Table 10: Cell 1 result under different light intensity

It can be concluded from the table above that short circuit current is directly proportional to the light intensity. The open circuit voltage decreases as the light intensity reduces. I-V and P-R curves of 50% light level of Cell 1 is produced and compared to 100% characteristics as shown below:

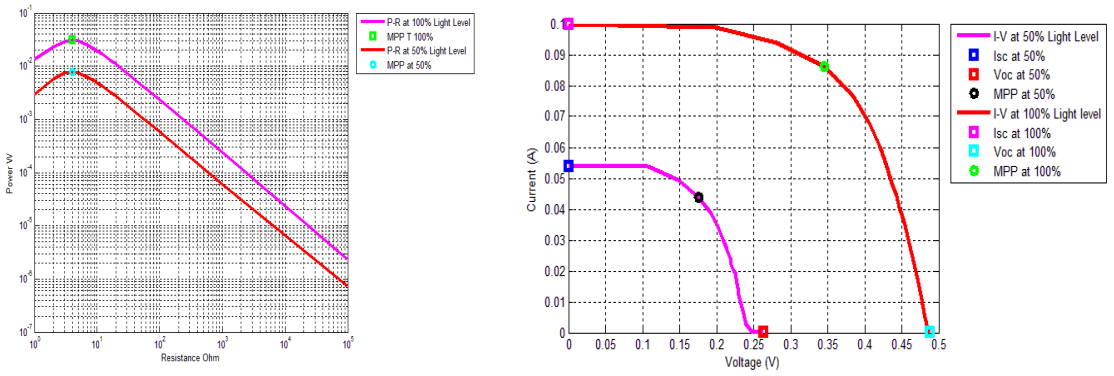


Figure 28: I-V and P-R of 100% and 50% light levels

It can be concluded from the figure above that at 50% light level the output power is reduced compared to the output power at 100% light level while the optimum resistance remains constant. The reason of this is that the open circuit voltage and short circuit current are approximately reducing by same factor. Therefore, the optimum resistance remains constant.

6.2 Testing the opto- coupled MOSFET Switches:

Few testing on the opto -coupled MOSFET switches is applied to investigate their behaviour. The first test is done to investigate the ON resistance of these devices to verify it with the manufactured value. In the specification section, it is stated that the ON resistance of these MOSFET is 35Ω. ON resistance test circuit is shown below:

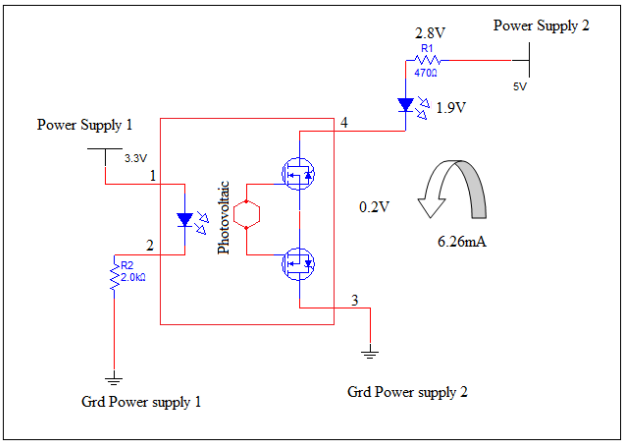


Figure 29: Opto - coupled ON resistance test circuit

The internal LED of the switch is turned on when the control signal 3.3V is applied. This light switches on the photovoltaic diode which in turn switches on the back to back MOSFET to switch the load (LED in this case). The current flows in the output circuit when the switch is on. Kirchhoff law and the obtained measurements are used to calculate the ON resistance. R_{ON} = 31Ω which closely agrees with the specified value (35 Ω).

The second testing is done to ensure that the switches are capable to switch a voltage source of 0.5V, 0.9V and 1.5V respectively. The output waveforms are measured across the load (1kΩ) as shown in the figure below.

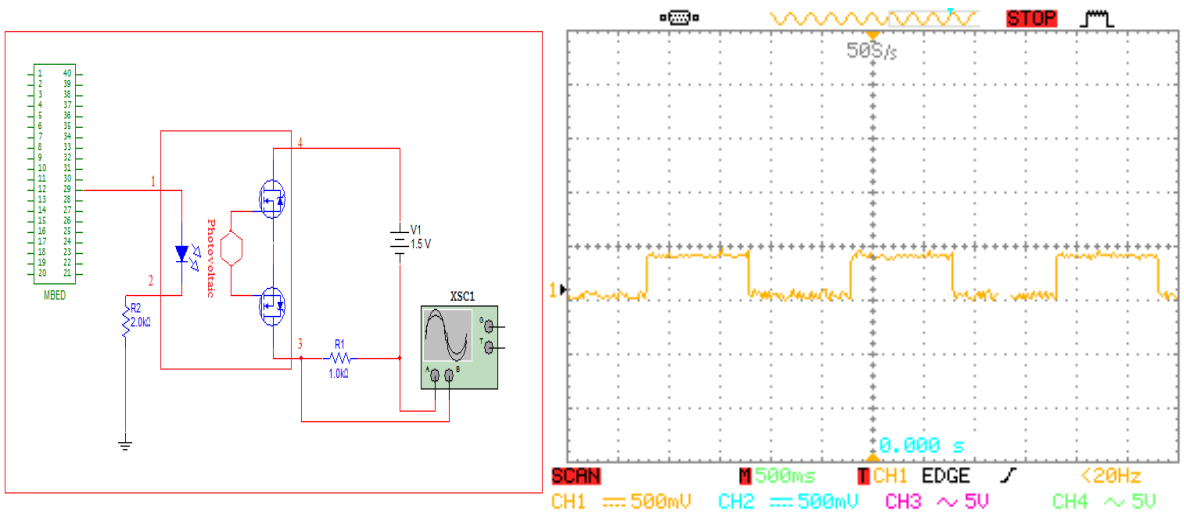


Figure 30: Test circuit and the output waveform when V=0.5V

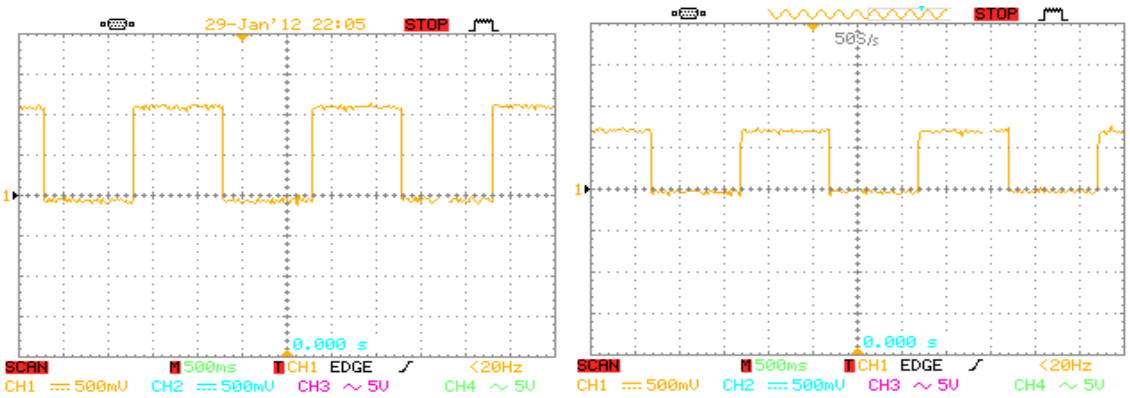


Figure 31: The output waveforms when V=1.5V and V=0.9V respectively

It can be concluded from this simple test that the MOSFET switches are capable to switch the required DC voltage levels that contribute in the desired AC output.

6.3 The overall Implementation and Problems:

This part of the report describes how the required product is produced as one complete system consists from several components. Not only it describes how the components fit together to produce the required system, but also shows some of the problems faced during the implementation procedure.

The required system is implemented on a breadboard as shown in Figure 51 in Appendix B to ensure that the system works as specified. P-R curve of the inverter is produced by varying load resistance from 1Ω to 99999Ω across the output terminals and measuring the corresponding voltage. This measurement is taken to find the optimum load (MPP load) of the system such that the delivered output power is maximised as shown in the figure below.

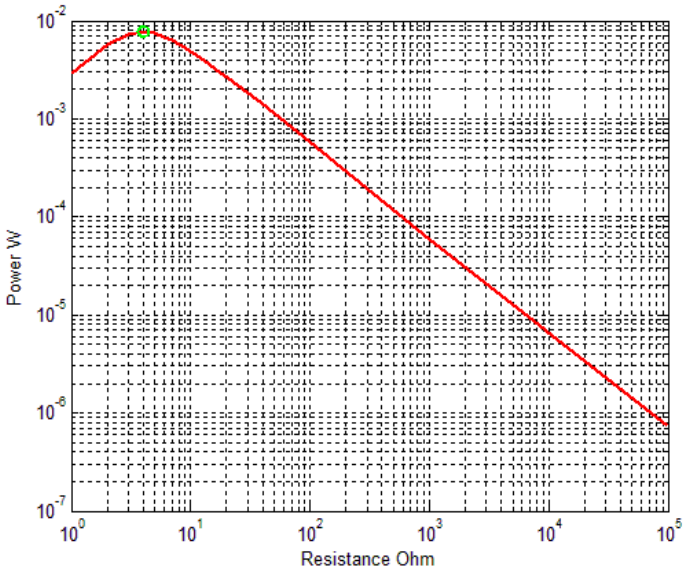


Figure 32: P-R curve of the implemented inverter

It can be deduced from the figure above that the optimum load resistance is 79Ω. The observed output waveform of the system at the optimum load is illustrated below.

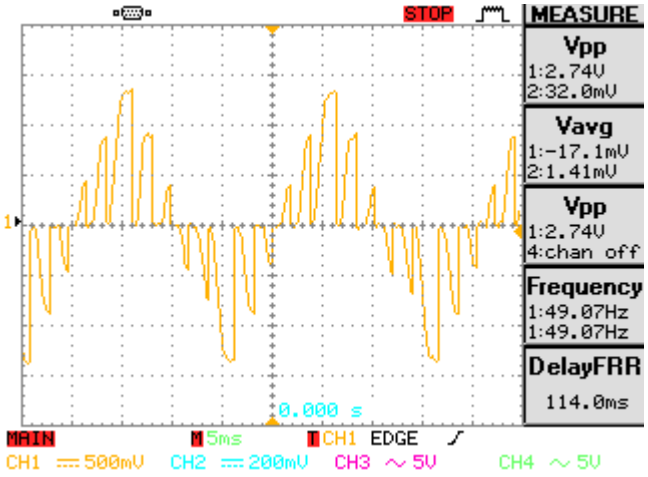


Figure 33: The output waveform at 79Ω load

The purpose of implementing this system is to produce a 50Hz stepping AC waveform, yet the figure above shows a distorted waveform. The required voltage levels which contribute in the AC waveform are clearly appeared in the above figure with small gaps between them. The small gaps can be treated by improving the switching time. The first three time steps in each half cycle of the above waveform have durations of T1=1.5ms, T2= 1.7ms and T3=1.8ms respectively. To eliminate the gaps between the steps and produce a stepping waveform, the time durations of the steps are increased such that the edges of the two consecutive steps intersect. However, the waveform becomes more distorted with increasing the time durations of the steps as shown in Figure 34 below.

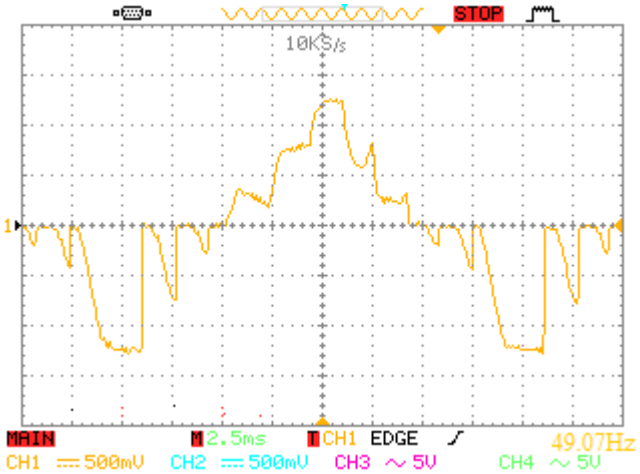


Figure 34: Increasing the time duration of the steps

At this particular point, the project is moved from implementation stage into a research stage to find out why the waveform distorted more when the time duration is increased. The first thought brought to my mind is to look back to the specification of the MOSFET switches as the only components could cause this problem. I found out that the ON resistance of these switches is very high 35Ω and the turn ON time is very slow 0.3ms. This indicates that the observed waveform measures the characteristics of the MOSFET switches instead of measuring the output waveform across the load. The reason of this is that the characteristics of the MOSFET switches are dominated. The behaviour of the power MOSFET switches is illustrated in the form of I-V characteristics curves as shown below.

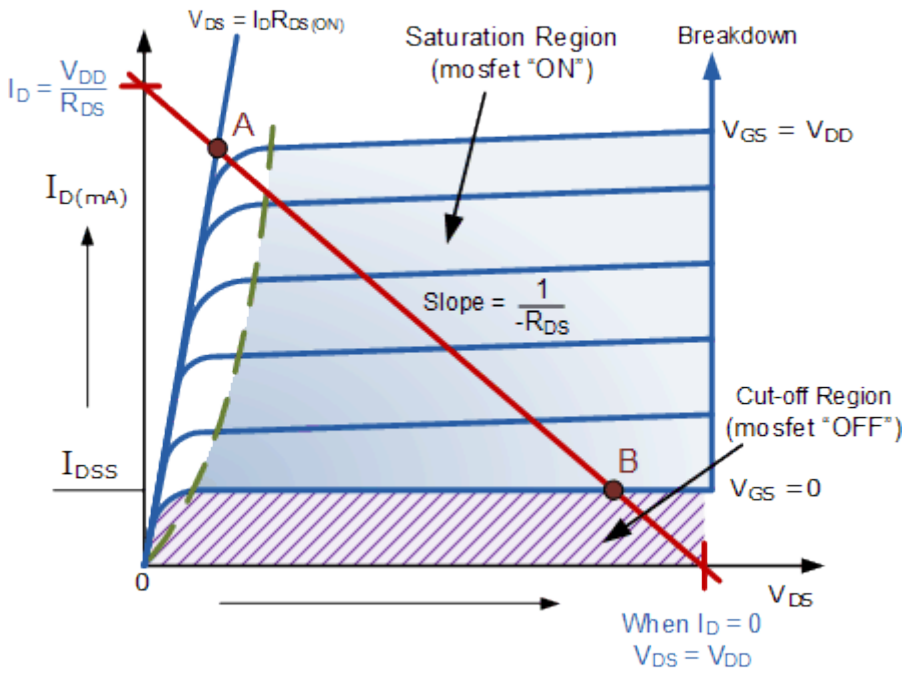


Figure 35: MOSFET I-V characteristics curves [13]

It is shown that the MOSFET is completely **OFF** (cut off region), if the control signal of the MOSFET is at the low state. This indicates that the input voltage of the gate is zero and the MOSFET conducts no current virtually and output voltage is equal to V_{DD} the supply voltage. However, the MOSFET is completely **ON** when the control signal is high and the input voltage to the gate is equal to the supply voltage. The drain current reaches to the maximum value due to a reduction in the channel resistance. This indicates that the MOSFET acts as a closed switch, but its **ON** resistance is not exactly zero due to the value of R_{SD} [13].

The problem with the MOSFET switches used in this implementation is that their ON resistance is very high and the optimum load at MPP is low. This causes a domination of the MOSFET characteristics at the output waveform. Furthermore, I-V characteristics of the MOSFET switches and I-V characteristics of the solar cells add up and form the distorted signal. To overcome this problem, large load resistance of 1MΩ value is connected to the inverter. This load resistance removes the effect of the MOSFET characteristics by a simple potential divider as shown in the figure below.

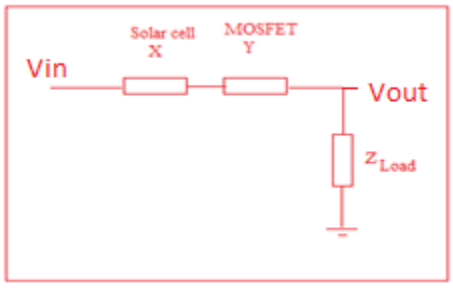


Figure 36: Potential divider circuit

The equation that can be derived from the potential divider circuit above is:

$$\text{Vout} = \text{Vin}\ \frac{Z_{load}\uparrow}{Z_{load}\uparrow+X+Y} \qquad (1.4)$$

Equation (1.4) shows that the effect of characteristics the MOSFET is removed by increasing the load resistance. Although at a maximum light level the output waveform of the inverter is not distorted with load resistance in the range (15kΩ -1MΩ), 1MΩ load shows the best AC stepping waveform with 6 different levels as shown in Figure 37 below.

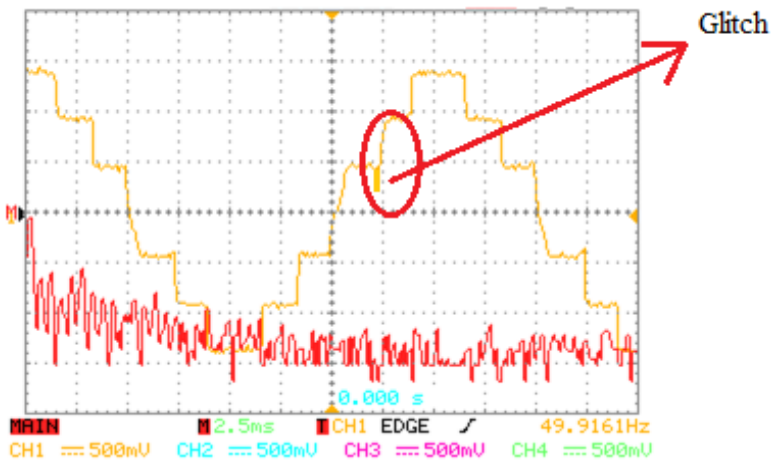


Figure 37: The output waveform of the inverter with 1MΩ load

The figure shows the AC waveform with 6 different levels with small glitch in the first step of the positive half cycle. This is solved by increasing the time coordinate of the edge where the glitch appears. The time coordinates of the steps are slightly overlapped to produce a good quality stepping AC waveform[3]. The overlapped or short circuit event is not problem in this project due to the fact that the solar cell is a current source.

- **Final Controlling signals of the switches:**
  These are the controlling signals of the six switches after tuning the time coordinates to eliminate the glitches in the waveform:

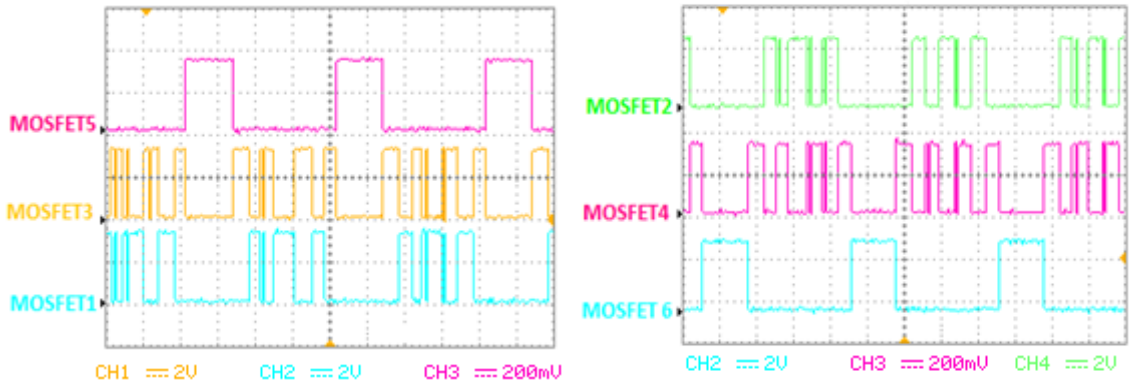
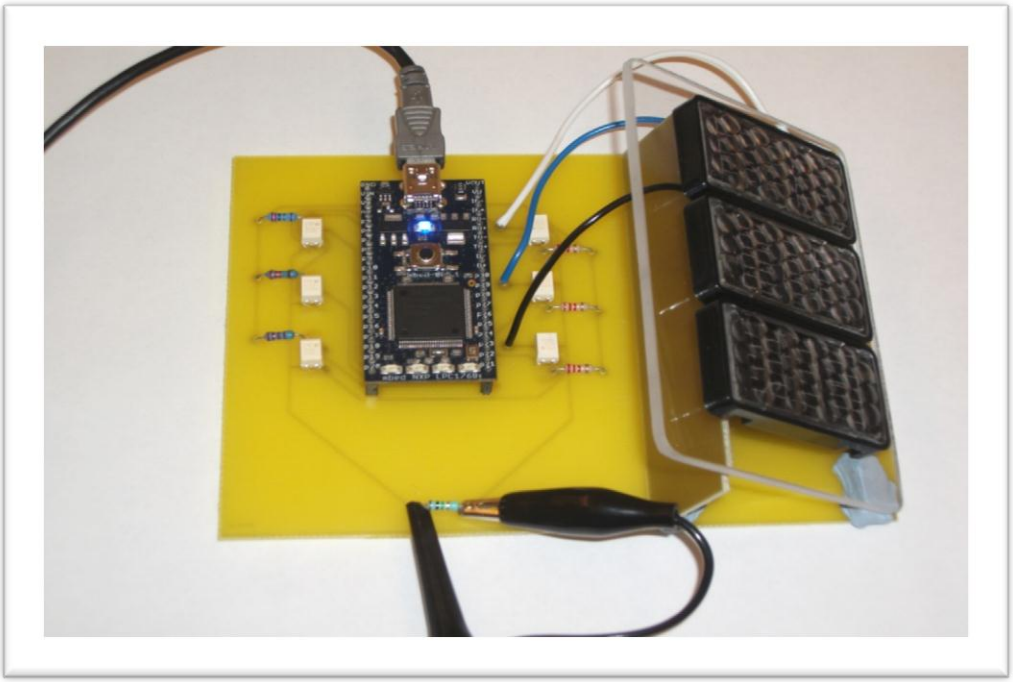


Figure 38: The controlling signals of the MOSFET switches [14]

(Note that the probes of **MOSFET1, MOSFET3, MOSFET6** and **MOSFET2** at 10)

[3] The final version of the software after tuning the time coordinates and fixing the glitches is included in **Appendix C**

- **PCB implementation:**
  After completing all the required testing and tuning the time coordinates, the implementation of the inverter is transferred to a PCB as below.



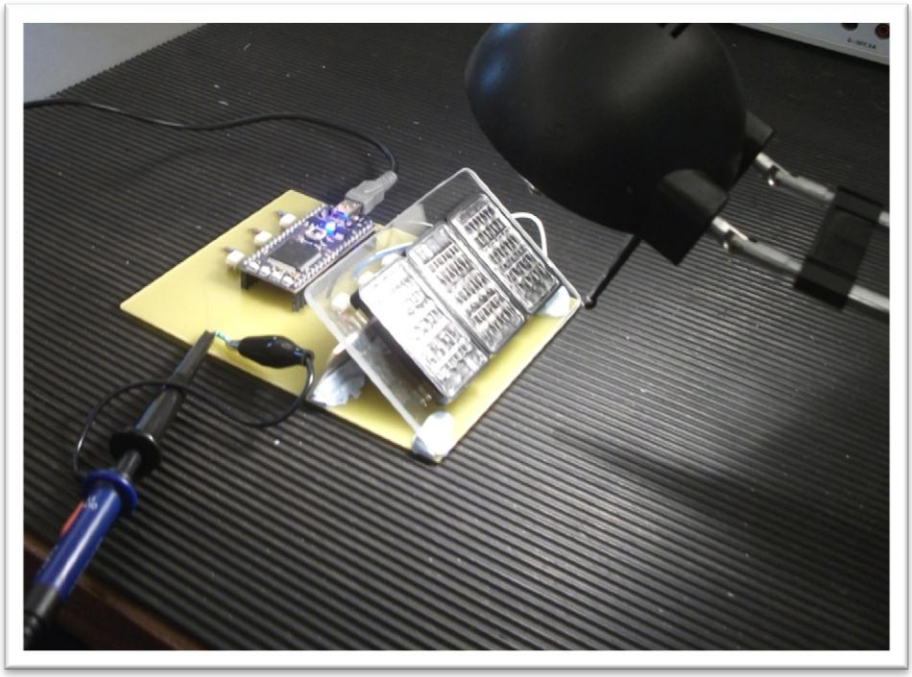


Figure 39: PCB implementation of the project

7 Results

(This chapter offers the overall practical and theoretical results of the project including the final testing and the Efficiency of the system)

7.1 The Overall Practical Result of the implemented system:

This part shows the result of the implemented Golomb inverter and how this meets the aim of the project. The generated waveform at maximum light level and its spectrum are captured via a Oscilloscope as shown in figure below.

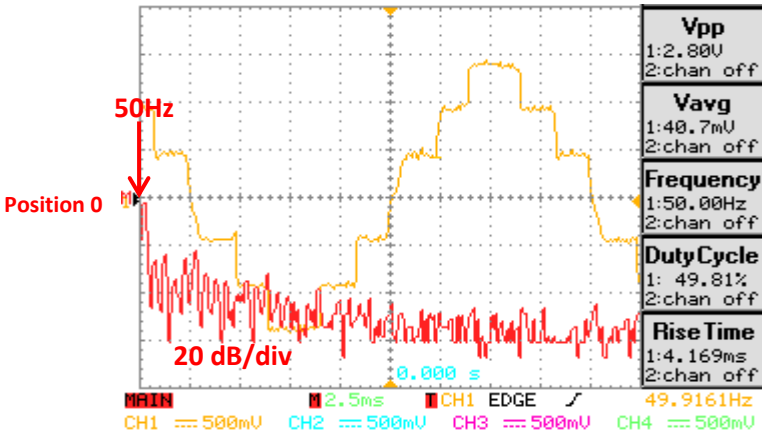


Figure 40: AC stepping waveform output and FFT spectrum of the implemented inverter

It can be deduced from the figure above that the signal produced by the inverter is a 50Hz stepping waveform with 6 different levels. The fundamental component (50Hz) is clearly marked on the spectrum. SNR of the generated signal is calculated by summing the power ratio of the significant harmonics (Noise) as shown below.

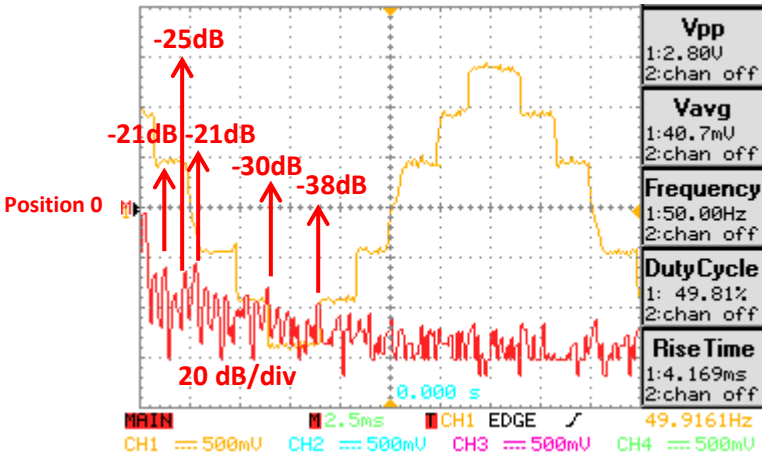


Figure 41: Significant harmonics in the FFT spectrum

The first five significant harmonics in the FFT result are included in calculating SNR[4]. The values in dBs are converted to power ratio by $dB = \frac{10logP}{1W}$, resulting in 0.00794 W, 0.00316W, 0.00794W, 0.001W and 0.000158W.

SNR= 16.9dB (2% distortion)

These results give strong grounds to conclude that the aim of the project is met.

[4] SNR is a way of measuring the level of the required signal to noise level. The total harmonics distortion of mains voltage is approximately in the range of 2.3% - 5.7% [17].

7.2 Efficiency in Golomb inverter structure compared with normal series DC source inverter:

Conversion efficiency of photovoltaic inverters is one of the important factors that considered in implementing power systems. In fact, all most all photovoltaic power systems suffer from power dissipation due to many factors such as switching losses and solar cell series resistance losses. The efficiency of Golomb inverter showed in this work compared with normal series DC source inverter is shown in this part of the report. In this project the solar cells are connected in an unbalanced sequence to satisfy the third order Golomb ruler. However, solar cells in normal inverter (H-bridge) are connected in normal series as below.

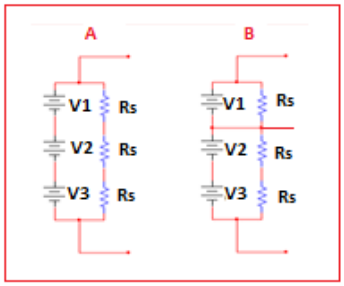
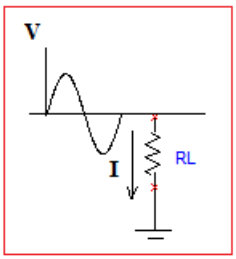


Figure 42: (A) Normal DC sequence (B) DC Golomb sequence

Figure above shows the difference between Golomb inverter and normal series inverter, the power dissipation in both cases are calculated as:

Power dissipation in Normal inverter:



Output current $I = \frac{V}{R_L}\sin(\omega t)$

$I^2 = \frac{V^2}{R_L^2}\sin^2(\omega t)$

$P_A = R_s \frac{V^2}{R_L^2}\sin^2(\omega t)$

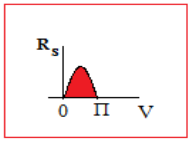
The average power dissipated due to normal DC source resistance: $P_{avg} = \frac{1}{\pi}\int_0^{\pi} P_A \, dt = \frac{1}{\pi}\int_0^{\pi} \sin(\omega t)^2 \, dt = \frac{\pi}{2\pi} = \frac{1}{2}$ =50%.

Power dissipation in Golomb inverter:

Output current $I = \frac{V}{R_L}\sin(\omega t)$

$I^2 = \frac{V^2}{R_L^2}\sin^2(\omega t)$

The power dissipated due to Golomb DC source resistance: $P_B = R_s \sin(\omega t) \frac{V^2}{R_L^2}\sin^2(\omega t)$, Rs varies with the voltage as:



Thus, the average power dissipated $P_{avg} = \frac{1}{\pi}\int_0^{\pi} P_B \, dt = \frac{1}{\pi}\int_0^{\pi} \sin^3(\omega t)\, dt = \frac{4}{3\pi} = 42\%$

Where: R_L: Load resistance

R_s: Solar series resistance

It can be concluded from the average power dissipated in both structures that Golomb provides 8% improvement. In other words, Golomb inverter offers 8% less series resistance loss than the normal structure. Furthermore, Golomb inverter has low switching losses because of low switching frequency. The switching losses are directly proportional to the switching frequency.

7.3 Theoretical Results: *(This part compares the practical results with theory)*

This part of the report verifies the practical results by theory. The measurement result of MPP of the I-V curves of the solar cells (single, two series and three series) is compared with theory. The practical result of SNR of the stepping AC waveform is also verified by theory.

7.3.1 Theoretical Solar Cell MPP:

This part shows how the I-V curve can be expressed in a mathematical form to verify the location of MPP. The expression of power can be derived as a function of voltage as:

$$P = \frac{VI_{sc}}{1+(\frac{V}{V_{OC}})^6} \qquad (1.5)$$

The power expression is extracted from low pass filter behaviour as both I-V solar curve and low pass filter curve are similar. It is possible to find the MPP voltage of the curve by finding the derivative of the above equation and set it to 0 as follows.

$$\frac{dP}{dt} = \frac{I_{sc}}{1+(\frac{V}{V_{OC}})^6} - \frac{6V^6 I_{sc}}{(1+\left(\frac{V}{V_{OC}}\right)^6)^2} = 0$$

$$\frac{I_{sc}}{1+(\frac{V}{V_{OC}})^6} = \frac{6V^6 I_{sc}}{(1+\left(\frac{V}{V_{OC}}\right)^6)^2}$$

$$\frac{1}{5} = (\frac{V}{V_{OC}})^6$$

$\left(\frac{V_{MPP}}{V_{OC}}\right) = 0.76$ This is the common ratio used in the MPPT technique [4].

$$(V_{MPP}) = 0.76\, V_{OC} \qquad (1.6)$$

The comparison between the obtained solar cell results in chapter 6 with this ratio is summarised in the following table:

Name	Practical V_{MPP} (V)	V_{OC} (V)	Theory $V_{MPP} = 0.76V_{OC}$	Error
Cell1	0.33	0.478	0.36	3%
Cell2	0.345	0.488	0.37	2.5%
Cell3	0.345	0.488	0.37	2.5%
Series Cell2 and Cell3	0.7110	0.946	0.7189	0.79%
Series Cell1,Cell2 and Cell3	1.025	1.444	1.097	7.2%

Table 11: Theory solar cell results

The maximum power point voltage obtained in the experiment closely agrees with the values obtained by equation (1.6).

7.3.2 Theoretical SNR:

The generated output waveform is a type of a staircase waveform. The different levels generated in the waveform can be known as a quantization steps. From the characteristics of the quantisation distortion as a function of signal level the signal to noise ratio SNR can be predicted [15]. For n-bit quantizer, the SNR can be calculated as:

$$SNR = (6.02n + 1.76)\ dB \qquad (1.7)$$

$$M = 2^n$$

Where: M: number of levels

n: number of bits

Applying this equation to the generated waveform of the inverter as: n=2.58bits, SNR_{Theory}= 17.29dB. The value of $SNR_{Practical}$ =16.9dB obtained in the practical closely agrees with the theoretical value. Note that SNR improves by 6.02dB per bit. This means if the number of levels is increased, the distortion is reduced.

Part III

Evaluations and Conclusions

8 Evaluations

(This chapter offers the possible improvements of the implemented system)

The implemented system has a wide range of improvements such that the best performance can be achieved. This chapter shows few of these possible improvements which discovered during the testing procedure.

I noticed during the testing time that the output waveform of the implemented system is changing significantly with light intensity. In fact, the output waveform starts with very weak signal at low light intensity and increasing gradually with more light level. Central tap Golomb inverter can improve the performance of the system when the light level is fluctuating. This structure can increase the number of levels with 6.02dB SNR improvement per bit. One basic structures of central tap Golomb inverter is illustrated below.

- **Sixth order central tap inverter is an improvement structure of the implemented third order Golomb inverter:**

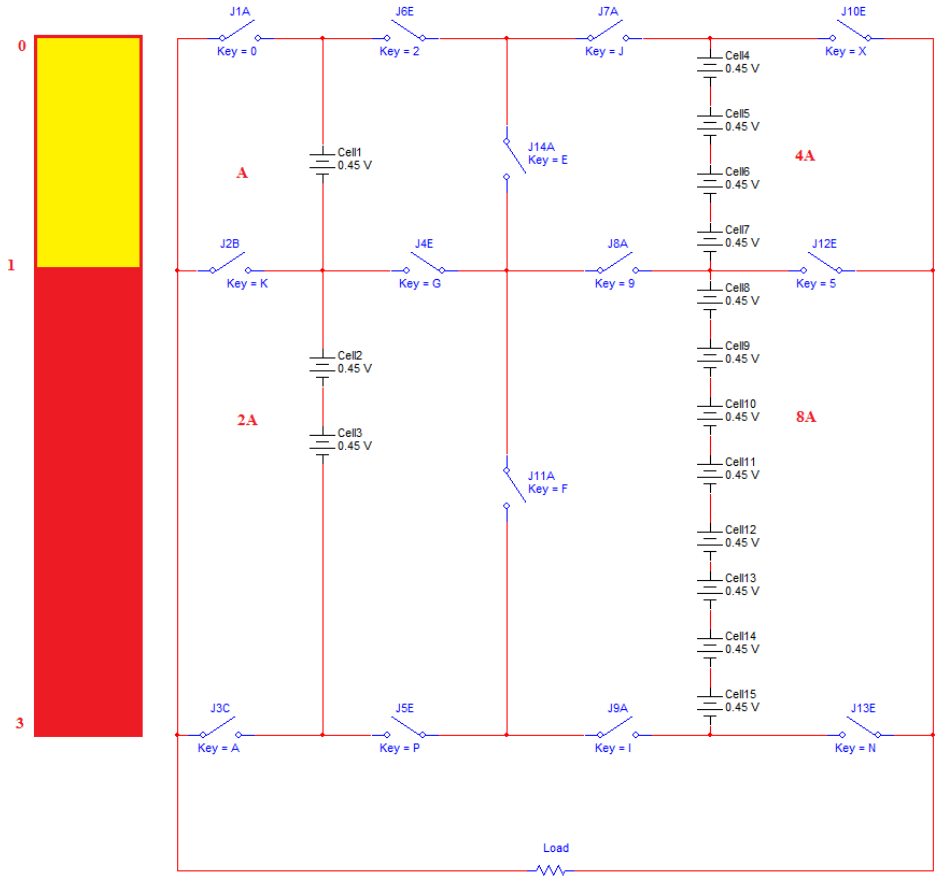


Figure 43: Central tap Golomb inverter

The structure above requires 15 solar cells with 0.45V each; the maximum output voltage that can be obtained from the structure is 6.75V whereas the implemented inverter can produce only 1.35V maximum. The above structure can produce 15 different levels compared with 6 levels from the implemented system. In full brightness, few levels are selected to perform the best waveform. However, in low light level which can occur in real life because of cloud or during the sun set time, more levels are selected to be involved in the output due to the reduction in the output voltage.

The above structure can produce all possible combinations from 1 to 15 without any missing compared to 6 marks optimum ruler. The sixth order optimum ruler (0 1 4 10 12 17) offers all combinations up to 17 with two missing values 14 and 15.

The idea of central tap Golomb inverter could be used in real life situation with cascading three 4^{th} order Golomb rulers to produce all different levels from 0 to 342 which indicate to 342V maximum of 1V step. However, the cost and the complexity are also increased.

Another feature can be applied to the implemented system beside the conversion is MPPT (Maximum power point tracking). This can be done by measuring the open circuit voltage across the solar cells when they are not used and set the operation voltage at 0.76Voc which is MPP. I believe I can add these features to my project if I have more time and budget.

9 Conclusions

(This chapter offers the overall conclusion including the project planning and lessons learnt)

9.1 Overall Conclusion:

From what has been discussed above, I can draw the conclusion that the product was a success as I met the goal of the project. Clearly, the results showed in chapter 7 give strong evidences that the aim of the project is met as specified. I am very pleased with what I have achieved in this project. The Golomb ruler ideas and the PCB implementation provided a success overall product. However, I was slightly disappointed with the behaviour of the system components, the solar cells and the switches in particular. I believe I could have implemented in an efficient way by using better components such as SANYO panels and power MOSFET with low ON resistance and fast turn on/off time. Further, the steps in the generated waveform did not have sharp edges. This may occur due to the capacitance in the wires of the oscilloscope or due to the MOSFET switches as they are very slow switches.

9.2 Project planning:

- **Method:**

This project was carried out using a sequential process as shown in figure below. The series can be defined as: specification, design, implementation, testing, maintenance and evaluation.

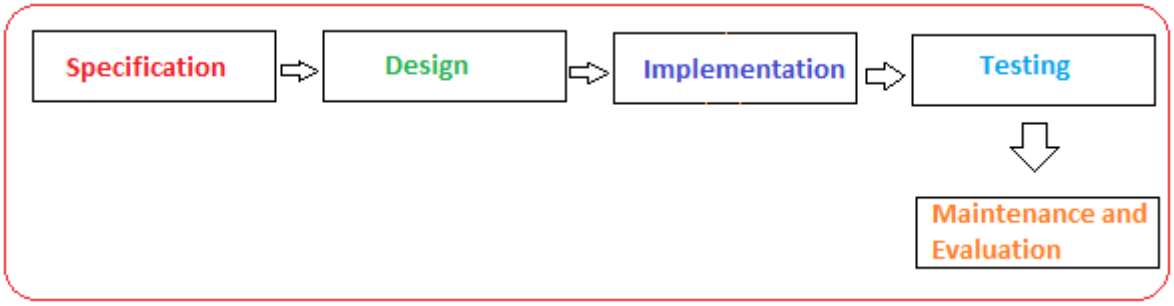


Figure 44: The project planning method

I had used this method in all projects I had done in this university. In my point of view, this method is the most suitable method in carrying out hardware projects.

The evaluation can be applied to the specification, design and implementation. This normally discovered during the testing and implementation procedures.

- **Time management:**

Despite the fact that the Gantt chart has been generated, this project is carried out by using my own time management style (Hours and Energy). I have planned all most all my project tasks on my log book (the same tasks set on the Gantt chart in **Appendix B**) by logging the estimation hours that can be spent in any particular task. I have decided the days such that the most important tasks accomplished on the day when I have the most energy and less important work done on the day of less energy. I assess myself on my logbook on each day and reflect on my results and achievements. However, this style may not be acceptable in work environment such as companies due to the personality issues and no solid deadlines. This may lead to significant delay in the work as there is no deadline set for the completion and the estimated hours may not be enough for the new tasks in particular such as hardware testing.

The number of hours logged in my logbook for each academic week is illustrated in the figure 45 below.

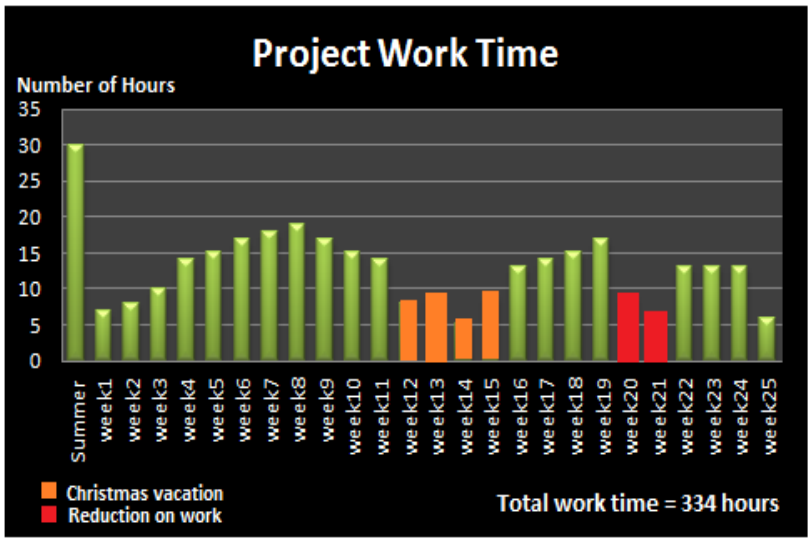


Figure 45: Project working hours

It can be concluded from the above figure that the maximum working hours spent in completing this project is approximately 334 hours. Approximately 30 hours spent in background reading during the summer time. The most reduction in the number of hours occurred during the academic weeks 20 and 21due to conflict with progress tests and course work deadlines. These caused slightly delay in the project work in particular designing the poster. Yet, I had few extra hours during the weekends to finish the delayed work.

I believe this time management style was very good in general. However, I wished if I could have followed the Gantt chart procedure as it is a professional way in working in companies.

9.3 Future plans:

I mentioned that the ideas of Golomb ruler in DC to AC inverters for photovoltaic application are completely new. I believe no one has used Golomb ruler in any type of conversions. This gives me the chance to publish my work. I am planning to write an IET paper to publish this novelty. I had already produced one, yet it needs more work in order to be accepted by the reviewers.

9.4 Lessons learn:

One of the important lessons I have learnt from this project is how to verify the practical results by applying the relevant theories which in general proof the experimental results with visual evidences. I have noticed from the investigation of the characteristics of the solar cells that it is not a good practice to change more than one parameter at the same time. This could lead to ambiguous results. I have also learnt how to manage my time to do my course work and project work.

Acknowledgements

First and foremost I give my sincerest gratitude to my supervisor, **Prof Stuart Walker**, who supported me with his knowledge and guidance throughout my project work.

I would also like to thank **Mr Anthony De Roy** for his help in ordering the project components and his support during my work in the laboratory. I also offer my thanks to **Mr Malcolm Lear** who fabricated my project PCB. My grateful thanks to the wonderful support I have received from My Husband and My Son.

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Selected IEEE papers:

- E. Esfandiari, M. Bin Mariun, M.H Marhaban & A. Zakaria, ''Fundamental of an Efficient and Reliable staircase Multilevel Inverter for Photovoltaic Application''*IEEE PES/IAS conference on Susrainable Alternative Energy*,2009,PP.1-8
- B. Diong, K. Corzine, ''WTHD-Optimal Staircase Modulation of Single-Phase Multilevel Inverters,'' *IEEE international conference on Electric Machines and Drives*, 2005, PP.1341-1344

Appendix A:

1. The Continuous and discontinuous modes waveforms for the buck converter

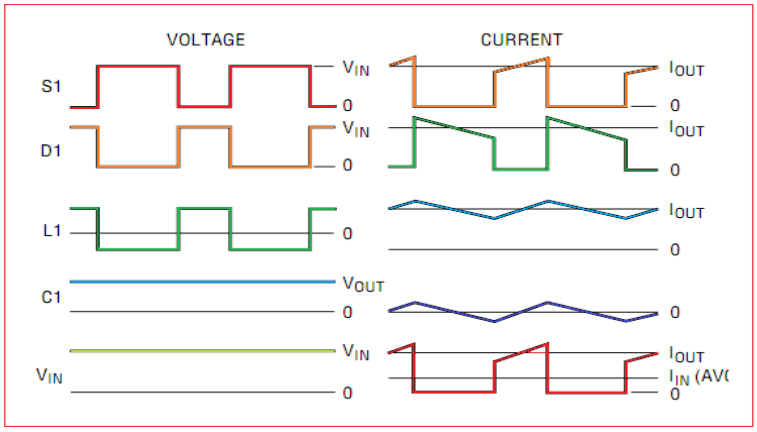

Figure 46: The continuous mode waveforms of the buck converter [modified from 8]

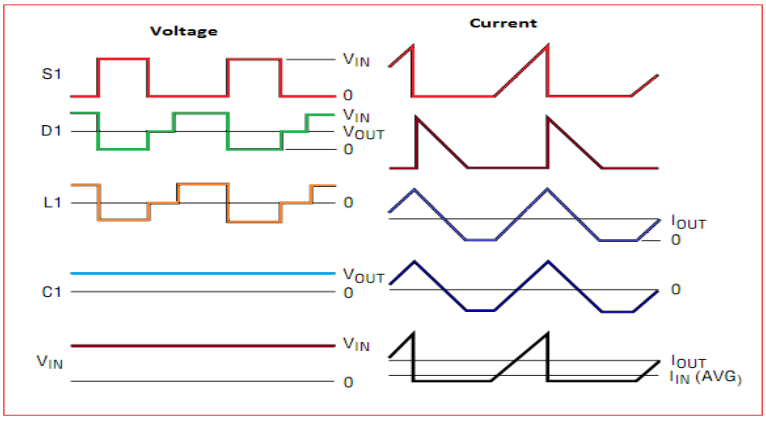

Figure 47: The discontinuous waveforms mode of the buck converter [modified from 8]

2. The Continuous and discontinuous modes waveforms for the boost converter:

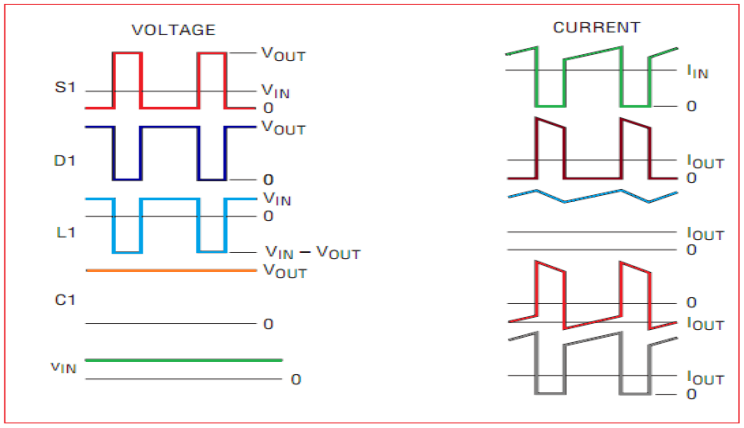

Figure 48: The continuous mode waveforms of the boost converter [modified from 8]

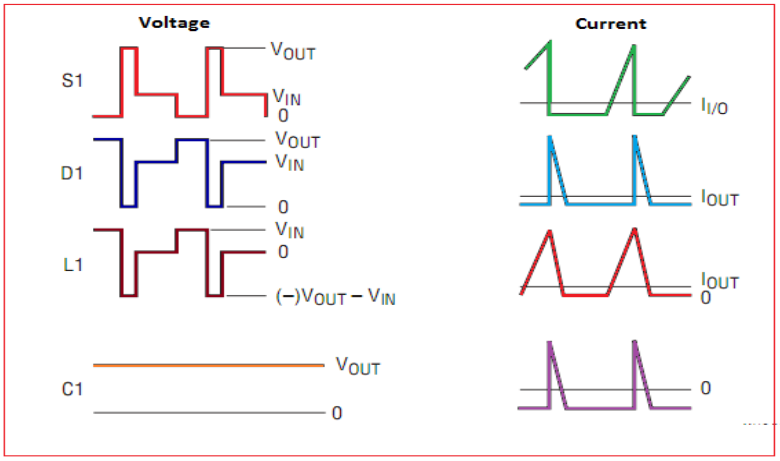

Figure 49: The discontinuous waveforms mode of the boost converter [modified from 8]

3. The basic structure of the solar cell:

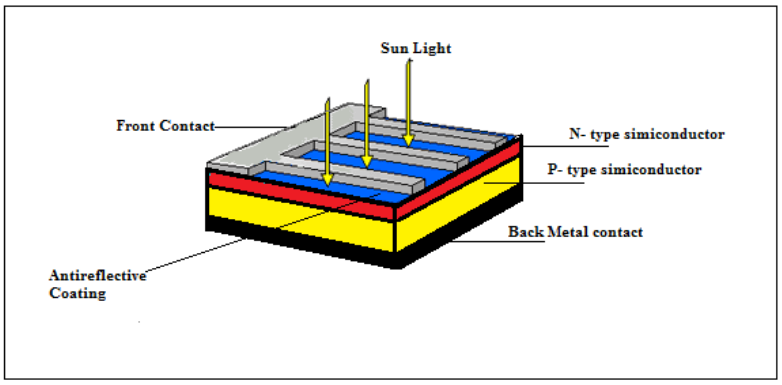

Figure 50: The basic structure of the solar cell

Appendix B:

- **Data results from testing the solar cells characteristics:**

1. Cell 1 Results at 100% light level

Current (A)	Voltage (V)	Resistance Ω	Power (W)
4.94005E-06	0.494	99999	2.44038E-06
0.000488488	0.488	999	0.000238382
0.004878788	0.483	99	0.002356455
0.012230769	0.477	39	0.005834077
0.016310345	0.473	29	0.007714793
0.024473684	0.465	19	0.011380263
0.0288125	0.461	16	0.013282563
0.035	0.455	13	0.015925
0.037666667	0.452	12	0.017025333
0.040727273	0.448	11	0.018245818
0.0444	0.444	10	0.0197136
0.048555556	0.437	9	0.021218778
0.05375	0.43	8	0.0231125
0.06	0.42	7	0.0252
0.0675	0.405	6	0.0273375
0.0762	0.381	5	0.0290322
0.08525	0.341	4	0.02907025
0.092666667	0.278	3	0.025761333
0.098	0.196	2	0.019208
0.100	0.100	1	0.011236

2. Cell 2 Results at 100%light level

Current (A)	Voltage (V)	Resistance (Ω)	Power (W)
4.87005E-06	0.487	99999	2.37171E-06
0.000486486	0.486	999	0.000236432
0.004868687	0.482	99	0.002346707
0.012179487	0.475	39	0.005785256
0.024421053	0.464	19	0.011331368
0.0286875	0.459	16	0.013167563
0.034846154	0.453	13	0.015785308
0.0375	0.45	12	0.016875
0.040545455	0.446	11	0.018083273
0.0442	0.442	10	0.0195364
0.048444444	0.436	9	0.021121778
0.053625	0.429	8	0.023005125
0.059857143	0.419	7	0.025080143
0.067666667	0.406	6	0.027472667
0.0772	0.386	5	0.0297992
0.088	0.352	4	0.030976
0.099	0.297	3	0.029403
0.1075	0.215	2	0.0231125
0.100	0.100	1	0.013456

3. Cell 3Results at 100% light level

Current (A)	Voltage (V)	Resistance Ω	Power (W)
4.88005E-06	0.488	99999	2.38146E-06
0.000486486	0.486	999	0.000236432
0.004868687	0.482	99	0.002346707
0.012205128	0.476	39	0.005809641
0.016275862	0.472	29	0.007682207
0.024473684	0.465	19	0.011380263
0.02875	0.46	16	0.013225
0.034923077	0.454	13	0.015855077
0.037583333	0.451	12	0.016950083
0.040636364	0.447	11	0.018164455
0.0443	0.443	10	0.0196249
0.048555556	0.437	9	0.021218778
0.05375	0.43	8	0.0231125
0.060142857	0.421	7	0.025320143
0.067666667	0.406	6	0.027472667
0.0768	0.384	5	0.0294912
0.08625	0.345	4	0.02975625
0.093666667	0.281	3	0.026320333
0.099	0.198	2	0.019602
0.100	0.100	1	0.011236

4. Cell 1 Results at 50%

Current (A)	Voltage (V)	Resistance (Ω)	Power (W)
2.71003E-06	0.271	99999	7.34417E-07
0.000243243	0.244	999	5.91081E-05
0.002434343	0.242	99	0.000586677
0.006089744	0.237	49	0.001146306
0.012210526	0.230	39	0.00135641
0.01434375	0.229	25	0.00209764
0.017423077	0.226	15	0.003405067
0.01875	0.226	13	0.00421875
0.020272727	0.223	11	0.004520818
0.0221	0.220	10	0.0048841
0.024222222	0.218	9	0.005280444
0.0268125	0.214	8	0.005751281
0.029928571	0.209	7	0.006270036
0.033833333	0.203	6	0.006868167
0.0386	0.193	5	0.0074498
0.044	0.176	4	0.007744
0.0495	0.148	3	0.00735075
0.05375	0.107	2	0.005778125
0.054	0.054	1	0.002916

5. Two series solar cells (2,3)at 100% light level

Current (A)	Voltage (V)	Resistance Ω	Power (W)
9.46009E-06	0.946	99999	8.94925E-06
0.000945619	0.939	993	0.000887937
0.009292929	0.92	99	0.008549495
0.013188406	0.91	69	0.012001449
0.018285714	0.896	49	0.016384
0.022641026	0.883	39	0.019992026
0.029689655	0.861	29	0.025562793
0.031592593	0.853	27	0.026948481
0.03372	0.843	25	0.02842596
0.034916667	0.838	24	0.029260167
0.037545455	0.826	22	0.031012545
0.038952381	0.818	21	0.031863048
0.04045	0.809	20	0.03272405
0.042	0.798	19	0.033516
0.043666667	0.786	18	0.034322
0.045411765	0.772	17	0.035057882
0.0471875	0.755	16	0.035626563
0.049	0.735	15	0.036015
0.050785714	0.711	14	0.036108643
0.052384615	0.681	13	0.035673923
0.053916667	0.647	12	0.034884083
0.055090909	0.606	11	0.033385091
0.0563	0.563	10	0.032
0.056777778	0.511	9	0.0315
0.057428571	0.402	7	0.023086286
0.057833333	0.347	6	0.020068167
0.0584	0.292	5	0.0170528
0.059	0.236	4	0.013924
0.06	0.18	3	0.0108
0.062	0.124	2	0.007688
0.067	0.067	1	0.004489

6. Three series solar cells (1,2,3)at 100 light level

Current (A)	Voltage (V)	Resistance Ω	Power (W)
1.44401E-05	1.444	99999	2.08516E-05
0.001438438	1.437	999	0.002067036
0.002839679	1.417	499	0.004023826
0.007035176	1.4	199	0.009849246
0.006679426	1.396	209	0.009324478
0.012587156	1.372	109	0.017269578
0.01362	1.362	100	0.01855044
0.015224719	1.355	89	0.020629494
0.019347826	1.335	69	0.025829348
0.022338983	1.318	59	0.02944278
0.023781818	1.308	55	0.031106618
0.02588	1.294	50	0.03348872
0.027319149	1.284	47	0.035077787
0.027652174	1.272	46	0.035173565
0.028659091	1.261	44	0.036139114
0.030536585	1.252	41	0.038231805
0.031175	1.247	40	0.038875225
0.031820513	1.241	39	0.039489256
0.0325	1.235	38	0.0401375
0.033216216	1.229	37	0.04082273
0.033944444	1.222	36	0.041480111
0.034742857	1.216	35	0.042247314
0.035529412	1.208	34	0.042919529
0.036363636	1.2	33	0.043636364
0.03721875	1.191	32	0.044327531
0.038129032	1.182	31	0.045068516
0.039066667	1.172	30	0.045786133
0.040137931	1.164	29	0.046720552
0.041142857	1.152	28	0.047396571
0.042185185	1.139	27	0.048048926
0.043230769	1.124	26	0.048591385
0.04432	1.108	25	0.04910656
0.045416667	1.09	24	0.049504167
0.046565217	1.071	23	0.049871348
0.047681818	1.049	22	0.050018227
0.048809524	1.025	21	0.050029762
0.04995	0.999	20	0.04990005
0.050736842	0.964	19	0.048910316
0.051722222	0.931	18	0.048153389
0.052647059	0.895	17	0.047119118
0.0534375	0.855	16	0.045689063
0.054266667	0.814	15	0.044173067
0.054928571	0.769	14	0.042240071
0.055538462	0.722	13	0.040098769
0.056083333	0.673	12	0.037744083
0.056545455	0.622	11	0.035171273
0.057	0.57	10	0.03249
0.056888889	0.512	9	0.029127111
0.05725	0.458	8	0.0262205
0.057714286	0.404	7	0.023316571
0.058333333	0.35	6	0.020416667
0.059	0.295	5	0.017405
0.0595	0.238	4	0.014161
0.060666667	0.182	3	0.011041333
0.0625	0.125	2	0.0078125
0.067	0.067	1	0.004489

- **Data results from testing the inverter:**

1. The measurement of the finding optimum Load resistance of the inverter

Current (A)	Voltage (Vpp) (V)	Resistance Ω	Power (W)
0.04	0.04	1	0.0016
0.013333333	0.04	3	0.0021333
0.02	0.08	4	0.0025
0.02	0.1	5	0.00392
0.02	0.14	7	0.0046286
0.0225	0.18	8	0.005
0.022222222	0.2	9	0.0053778
0.022	0.22	10	0.00576
0.02	0.24	12	0.0065333
0.02	0.28	14	0.0064286
0.02	0.3	15	0.0068267
0.02	0.32	16	0.007225
0.02	0.34	17	0.0076235
0.02	0.36	18	0.0080222
0.02	0.38	19	0.0084211
0.02	0.4	20	0.00968
0.018333333	0.44	24	0.0096
0.0192	0.48	25	0.01
0.019230769	0.5	26	0.0104
0.019259259	0.52	27	0.0108
0.01862069	0.54	29	0.0108138
0.018666667	0.56	30	0.012
0.018181818	0.6	33	0.0124121
0.017777778	0.64	36	0.0121
0.017837838	0.66	37	0.0132432
0.017948718	0.7	39	0.0132923
0.017560976	0.72	41	0.0133561
0.017209302	0.74	43	0.0134326
0.017272727	0.76	44	0.0138273
0.017333333	0.78	45	0.0142222
0.017021277	0.8	47	0.0143064

Current (A)	Voltage (Vpp) (V)	Resistance Ω	Power W
0.017083333	0.82	48	0.0147
0.017142857	0.84	49	0.015804082
0.016923077	0.88	52	0.015576923
0.015517241	0.9	58	0.015234483
0.015409836	0.94	61	0.015108197
0.015483871	0.96	62	0.015490323
0.015076923	0.98	65	0.015384615
0.014285714	1	70	0.017285714
0.013924051	1.1	79	0.018227848
0.013483146	1.2	89	0.01755618
0.012626263	1.25	99	0.017070707
0.010833333	1.3	120	0.016803333
0.010923077	1.42	130	0.017307692
0.009375	1.5	160	0.016
0.008421053	1.6	190	0.014503158
0.0083	1.66	200	0.01445
0.007391304	1.7	230	0.014086957
0.006206897	1.8	290	0.012844483
0.00603125	1.93	320	0.01225125
0.006	1.98	330	0.012121212
0.005128205	2	390	0.011307692
0.004285714	2.1	490	0.009172245
0.003539232	2.12	599	0.008080134
0.003147353	2.2	699	0.00730701
0.002828536	2.26	799	0.006853066
0.002602892	2.34	899	0.006300779
0.002382382	2.38	999	0.00567007
0.00119598	2.38	1990	0.003041005
0.001230615	2.46	1999	0.003126563
0.000833611	2.5	2999	0.002168223
0.000637659	2.55	3999	0.001716529
2.62003E-05	2.62	99999	6.86447E-05

- **Breadboard Implementation:**
  This is the first implementation stage of the inverter using the breadboard.

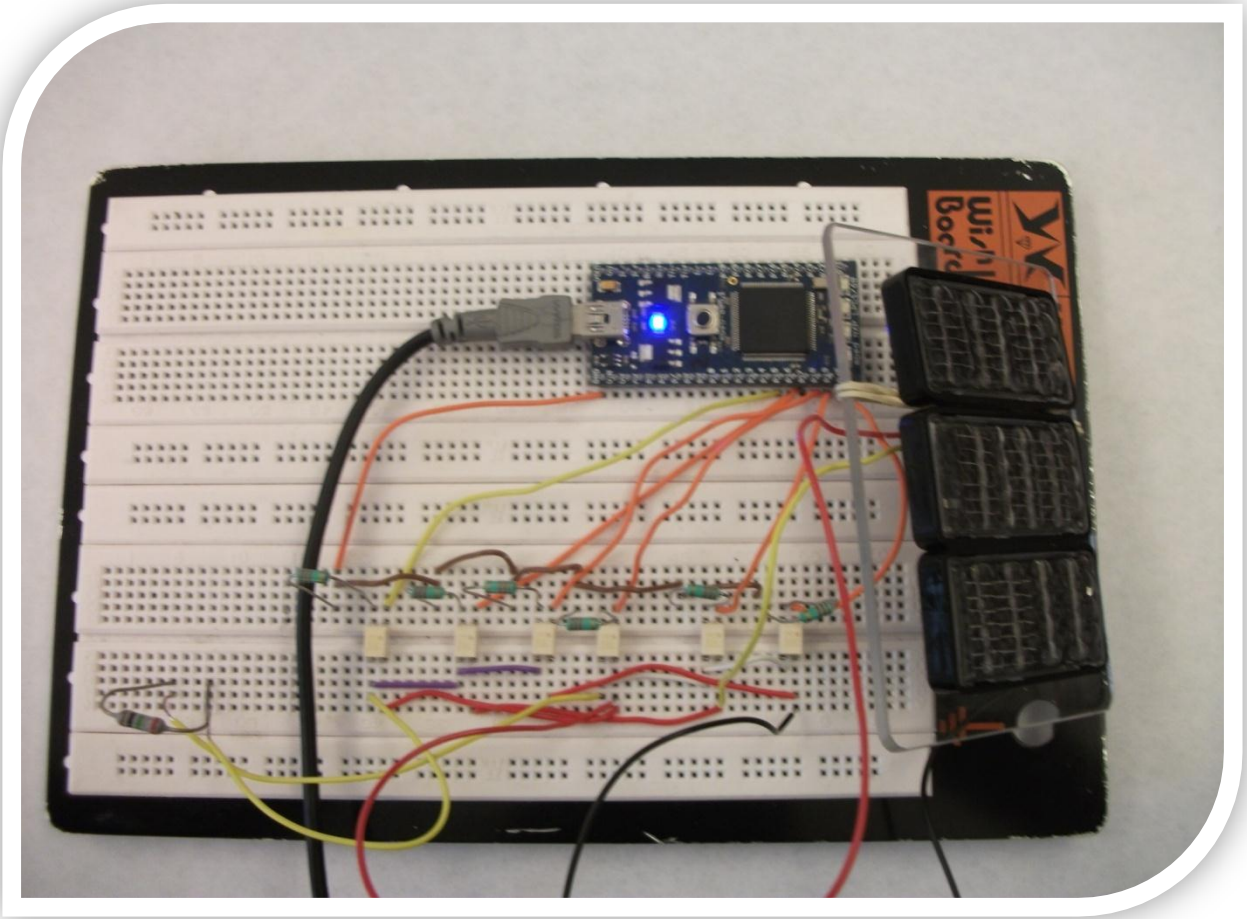

Figure 51: Initial implementation stage

Appendix C:

- **Software implementation:**

This is the final version of the software implementation of the inverter:

```
#include "mbed.h"
DigitalOut MOS1(p17);
DigitalOut MOS2(p18);
DigitalOut MOS3(p15);
DigitalOut MOS4(p19);
DigitalOut MOS5(p16);
DigitalOut MOS6(p20);
Timer t;
int main() {
    t.start();// This starts the timer
    while (1) {
        if (t.read()>=0.0 && t.read() <= 0.0016) {// First step in the
positive half cycle
            MOS1 = 1;
            MOS2 = 0;
            MOS3 = 0;
            MOS4 = 1;
            MOS5 = 0;
            MOS6 = 0;     }
        if (t.read()>0.0015 && t.read()<=0.0032) {
            MOS1= 0;
            MOS2= 0;
            MOS3= 1;
            MOS4= 0;
            MOS5= 0;
            MOS6= 1;       }
        if (t.read()>0.0032 && t.read()<=0.0068) {
            MOS1= 1;
            MOS2= 0;
            MOS3= 0;
            MOS4= 0;
            MOS5= 0;
            MOS6= 1;        }
        if (t.read()>0.0068 && t.read()<= 0.0085) {
            MOS1= 0;
            MOS2= 0;
            MOS3= 1;
            MOS4= 0;
            MOS5= 0;
            MOS6= 1;        }
         if (t.read ()>0.0085 && t.read ()<=0.01) {
            MOS1=1;
            MOS2=0;
            MOS3=0;
            MOS4=1;
            MOS5=0;
            MOS6=0;         }
        if (t.read ()>0.01 && t.read() <= 0.0116) { // This the first step
in the negative half cycle
            MOS1=0;
            MOS2=1;
            MOS3=1;
            MOS4=0;
            MOS5=0;
            MOS6=0;         }
        if (t.read ()>0.0115 && t.read ()<=0.0132) {
            MOS1=0;
```

```
    MOS2=0;
    MOS3=0;
    MOS4=1;
    MOS5=1;
    MOS6=0;          }
if ( t.read ()>0.0132 && t.read () <=0.0168) {
    MOS1=0;
    MOS2=1;
    MOS3=0;
    MOS4=0;
    MOS5=1;
    MOS6=0;          }
 if ( t.read() >0.0168 && t.read ()<=0.0185) {
    MOS1=0;
    MOS2=0;
    MOS5=1;
    MOS4=1;
    MOS3=0;
    MOS6=0;          }
if (t.read() >0.0185 && t.read ()<= 0.02) {
    MOS1=0;
    MOS2=1;
    MOS3=1;
    MOS4=0;
    MOS5=0;
    MOS6=0;          }
if (t.read() > 0.02) {
    t.reset();         }     }    } //This resets the timer
```

- **Gantt Chart:** *(Revised Gantt chart)*

	Task Name	Duration	Start	Finish
1	***SUMMER WORK***	**83 days?**	**Thu 16/06/11**	**Fri 07/10/11**
2	Initial Research	7 days?	Thu 16/06/11	Fri 24/06/11
3	Meeting Supervisor (Initinal)	1 day	Mon 27/06/11	Mon 27/06/11
4	Writing a Mini Proposal	4 days?	Tue 28/06/11	Fri 01/07/11
5	Studying Types of SMPS	6 days?	Mon 04/07/11	Mon 11/07/11
6	Simulating Basic SMPS Circuits	4 days?	Tue 12/07/11	Fri 15/07/11
7	Deciding Project Application	1 day?	Mon 18/07/11	Mon 18/07/11
8	The Possible Circuit to design the Projcet	8 days?	Tue 19/07/11	Thu 28/07/11
9	Reading about How to write a Good Specification	4 days?	Fri 29/07/11	Wed 03/08/11
10	Meeting supervisor (Summer Term)	4 days?	Tue 05/07/11	Thu 04/08/11
11	Deciding the Hardware Devices	1 day?	Thu 04/08/11	Thu 04/08/11
12	Summarising Background Sources and reading about Golomb ruler technique	23 days?	Fri 05/08/11	Mon 05/09/11
13	Having Rest for a Private Circumstances	12 days?	Tue 06/09/11	Wed 21/09/11
14	Writing up the Initial Report (first draft)	7 days?	Thu 22/09/11	Fri 30/09/11
15	Meeting Supervisor	2 days?	Mon 26/09/11	Mon 03/10/11
16	Ordering the Hardware Devices	1 day?	Tue 04/10/11	Tue 04/10/11
17	Resting before the New Term	3 days?	Wed 05/10/11	Fri 07/10/11
18	***AUTUMN TERM***	**51 days?**	**Mon 10/10/11**	**Fri 16/12/11**
19	Editing the Initial Report	5 days	Mon 10/10/11	Fri 14/10/11
20	Meeting Supervisor (Autumn Term)	10 days	Wed 12/10/11	Fri 09/12/11
21	***Submission the Initial Report***	***1 day?***	***Fri 21/10/11***	***Fri 21/10/11***
22	Testing the charcteristics of one solar cell	6 days?	Mon 17/10/11	Mon 24/10/11
23	plotting IV graph by Excel	4 days	Tue 25/10/11	Fri 28/10/11
24	Recording the Results of Power vrs Resistance	4 days	Tue 25/10/11	Fri 28/10/11
25	Amending the Design of the circuit by adding other cells in series	6 days	Mon 31/10/11	Mon 07/11/11
26	Testing the series circuit and plotting IV & PR	2 days	Tue 08/11/11	Wed 09/11/11
27	Plottting the IV and PR curves by MATLAB	4 days?	Thu 10/11/11	Tue 15/11/11
28	Design and simulate the circuit by MULTISIM when manual switches are added	1 day?	Wed 16/11/11	Wed 16/11/11
29	Switching the cells on and off by using manual switches on the breadbord	3 days?	Wed 16/11/11	Fri 18/11/11
30	Testing Circuit	2 days	Wed 16/11/11	Thu 17/11/11
31	Recording the Results	2 days	Fri 18/11/11	Mon 21/11/11
32	Replacing the manual switches with MOSFET switchses	3 days	Tue 22/11/11	Thu 24/11/11
33	Writing up the Interim Report	5 days	Fri 25/11/11	Wed 30/11/11
34	***Submission The Interim Report***	***1 day?***	***Fri 02/12/11***	***Fri 02/12/11***
35	Controlling the circuit by Mbed chip instead of manual switches	5 days	Mon 05/12/11	Fri 09/12/11
36	Testing the circuit and recording the result	3 days	Mon 12/12/11	Wed 14/12/11
37	Amending the code of the mbed controller and testing the circuit	2 days	Thu 15/12/11	Fri 16/12/11
38	**Christmas Holiday**	26 days?	Mon 19/12/11	Sun 22/01/12
39	***SPRING TERM***	**45 days**	**Mon 23/01/12**	**Fri 23/03/12**
40	Checking the Functionality of The Project and trying to make AC waveform	7 days	Mon 23/01/12	Tue 31/01/12
41	Final Testing to the Project circuit	5 days	Wed 01/02/12	Tue 07/02/12
42	Meeting Supervisor	8 days	Wed 25/01/12	Wed 14/03/12
43	Designing the Project Printed Circuit Board (PCB)	7 days	Wed 08/02/12	Thu 16/02/12
44	Transferring the Project to PCB and Testing it	5 days?	Fri 17/02/12	Thu 23/02/12
45	Designing the Project Poster	7 days?	Fri 24/02/12	Mon 05/03/12
46	Editing The design	1 day?	Tue 06/03/12	Tue 06/03/12
47	***Submission The Project Poster***	***1 day?***	***Wed 07/03/12***	***Wed 07/03/12***
48	***Submission The Abstract -open day***	***1 day?***	***Wed 07/03/12***	***Wed 07/03/12***
49	Practicing for the Open day	7 days?	Thu 08/03/12	Fri 16/03/12
50	Demonstrating the Project in the Open Day	1 day?	Mon 19/03/12	Mon 19/03/12
51	Editing The Logbook	4 days?	Tue 20/03/12	Fri 23/03/12
52	**Easter Holiday**	21 days?	Mon 26/03/12	Sun 22/04/12
53	***Summer Term***	***13 days?***	***Wed 25/04/12***	***Fri 11/05/12***
54	***Submission Logbook***	***1 day?***	***Wed 25/04/12***	***Wed 25/04/12***
55	***Submission the Final Report***	***1 day?***	***Wed 25/04/12***	***Wed 25/04/12***
56	***Final Oral demonstration***	***10 days?***	***Mon 30/94/12***	***Fri 11/05/12***