SPI Master Module Address Map

Registers in the SPI Master module

Module Instance	Base Address
spim0	0xFFF00000
spim1	0xFFF01000

SPI Master Module

Register	Offset	Width	Access	Reset Value	Description
ctrlr0	0x0	32	RW	0x7	Control Register 0
ctrlr1	0x4	32	RW	0x0	Control Register 1
spienr	0x8	32	RW	0x0	Enable Register
mwcr	0xC	32	RW	0x0	Microwire Control Register
ser	0x10	32	RW	0x0	Slave Enable Register
baudr	0x14	32	RW	0x0	Baud Rate Select Register
txftlr	0x18	32	RW	0x0	Transmit FIFO Threshold Level Register
rxftlr	0x1C	32	RW	0x0	Receive FIFO Threshold Level Register
txflr	0x20	32	RO	0x0	Transmit FIFO Level Register
rxflr	0x24	32	RO	0x0	Receive FIFO Level Register
sr	0x28	32	RO	0x6	Status Register
imr	0x2C	32	RW	0x3F	Interrupt Mask Register
isr	0x30	32	RO	0x0	Interrupt Status Register
risr	0x34	32	RO	0x0	Raw Interrupt Status Register
txoicr	0x38	32	RO	0x0	Transmit FIFO Overflow Interrupt Clear Register
rxoicr	0x3C	32	RO	0x0	Receive FIFO Overflow Interrupt Clear Register
rxuicr	0x40	32	RO	0x0	Receive FIFO Underflow Interrupt Clear Register
icr	0x48	32	RO	0x0	Interrupt Clear Register
dmacr	0x4C	32	RW	0x0	DMA Control Register
dmatdlr	0x50	32	RW	0x0	DMA Transmit Data Level Register
dmardlr	0x54	32	RW	0x0	DMA Receive Data Level Register
idr	0x58	32	RO	0x5510000	Identification Register
spi_version_id	0x5C	32	RW	0x3332302A	Component Version Register
dr	0x60	32	RW	0x0	Data Register
rx_sample_dly	0xF0	32	RW	0x0	RX Sample Delay Register

SPI Master Module Summary

Registers in the SPI Master module

ctrlr0

This register controls the serial data transfer. It is impossible to write to this register when the SPI Master is enabled. The SPI Master is enabled and disabled by writing to the SPIENR register.

ctrlr1

Control register 1 controls the end of serial transfers when in receive-only mode. It is impossible to write to this register when the SPI Master is enabled.The SPI Master is enabled and disabled by writing to the SPIENR register.

spienr

Enables and Disables all SPI operations.

mwcr

This register controls the direction of the data word for the half-duplex Microwire serial protocol. It is impossible to write to this register when the SPI Master is enabled. The SPI Master is enabled and disabled by writing to the SPIENR register.

ser

The register enables the individual slave select output lines from the SPI Master. Up to 4 slave-select output pins are available on the SPI Master. You cannot write to this register when SPI Master is busy and when SPI_EN = 1.

baudr

This register derives the frequency of the serial clock that regulates the data transfer. The 16-bit field in this register defines the spi_m_clk divider value. It is impossible to write to this register when the SPI Master is enabled. The SPI Master is enabled and disabled by writing to the SPIENR register.

txftlr

This register controls the threshold value for the transmit FIFO memory. It is impossible to write to this register when the SPI Master is enabled. The SPI Master is enabled and disabled by writing to the SPIENR register.

rxftlr

This register controls the threshold value for the receive FIFO memory. It is impossible to write to this register when the SPI Master is enabled. The SPI Master is enabled and disabled by writing to the SPIENR register.

txflr

This register contains the number of valid data entries in the transmit FIFO memory. Ranges from 0 to 256.

rxflr

This register contains the number of valid data entries in the receive FIFO memory. This register can be read at any time. Ranges from 0 to 256.

sr

This register is used to indicate the current transfer status, FIFO status, and any transmission/reception errors that may have occurred. The status register may be read at any time. None of the bits in this register request an interrupt.

imr

This register masks or enables all interrupts generated by the SPI Master.

isr

This register reports the status of the SPI Master interrupts after they have been masked.

risr

This register reports the status of the SPI Master interrupts prior to masking.

txoicr

Transmit FIFO Overflow Interrupt Clear Register

rxoicr
Receive FIFO Overflow Interrupt Clear Register

rxuicr
Receive FIFO Underflow Interrupt Clear Register

icr
Clear Interrupt

dmacr
This register is used to enable the DMA Controller interface operation.

dmatdlr
Controls the FIFO Level for a DMA transmit request

dmardlr
Controls the FIFO Level for a DMA receeive request

idr
This register contains the peripherals identification code, which is 0x05510000.

spi_version_id
Version ID Register value

dr
This register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SPI_EN = 1. FIFOs are reset when SPI_EN = 0. The data register occupies thirty-six 32-bit locations in the address map (0x60 to 0xec). These are all aliases for the same data register. This is done to support burst accesses. .

rx_sample_dly
This register controls the number of spi_m_clk cycles that are delayed (from the default sample time) before the actual sample of the rxd input occurs. It is impossible to write to this register when the SPI Master is enabled. The SPI Master is enabled and disabled by writing to the SPIENR register.