# Pietro Giuseppe Bressana

## Contact Information


| | |
|---|---|
| web | pietrobressana.github.io |
| email | pietro.bressana@usi.ch |
| Address | Faculty of Informatics, Università della Svizzera italiana (USI),<br>Via Giuseppe Buffi 13, 6904 Lugano, Switzerland. |


## Education

| | |
|---|---|
| 2016 - present | **PhD Candidate in Computer Science**<br>Università della Svizzera Italiana (USI), Switzerland.<br>*Advisors*: Prof. Robert Soulé & Dr. Noa Zilberman |
| 2015 | **Master's degree, Computer Engineering**<br>Politecnico di Milano, Italy. |
| 2013 | **Bachelor's degree, Electronic Engineering**<br>Politecnico di Milano, Italy. |

## Employment history

| | |
|---|---|
| 2018 | **Intern**<br>Western Digital, Milpitas, CA, USA.<br>Under the supervision of Dejan Vucinic. |
| 2016 - present | **Teaching Assistant**<br>Università della Svizzera Italiana (USI), Switzerland.<br>–› *Computer Architecture*, Prof. Marc Langheinrich (2017/18) |
| 2016 | **Research Assistant**<br>Università della Svizzera Italiana (USI), Switzerland. |

## Honors & Awards

| | |
|---|---|
| 2017 | **SNF Doc.Mobility Fellowship** (26,400 CHF)<br>6-months research period at the University of Cambridge, UK.<br>http://p3.snf.ch/project-178657 |

Updated on September 26, 2018

## Research interests

Programmable data planes, Network validation, FPGA-based hardware design.

## Research projects

| | |
|---|---|
| 2017 - present | **NetDebug** (USI & University of Cambridge)<br>A programmable framework for validating data planes. |
| 2017 | **Emu** (USI & University of Cambridge)<br>A framework for network functions on FPGAs. |
| 2016 | **NetPaxos** (USI)<br>Consensus as a network service. |
| 2015 | **exaFPGA** (Politecnico di Milano)<br>Hardware acceleration for the next generation of super-computing platforms. |

## Academic experience

| | |
|---|---|
| 2018 | **Visiting PhD Student**<br>The Computer Laboratory, University of Cambridge, UK.<br>*Supervisor*: Dr. Noa Zilberman.<br>Funded by SNF Doc.Mobility Fellowship. |
| 2017 | **Barefoot Academy \| BA 101**<br>Barefoot Networks, Santa Clara, CA, USA. |
| 2017 | **NetFPGA Developers Summit 2017**<br>The Computer Laboratory, University of Cambridge, UK. |
| 2016 | **Visiting PhD Student**<br>The Computer Laboratory, University of Cambridge, UK.<br>*Supervisor*: Dr. Noa Zilberman. |
| 2016 | **Sub-reviewer**<br>The International Conference on Reconfigurable Computing and FPGAs (ReConFig 2016).<br>*Reviewer*: Prof. Robert Soulé. |
| 2015 | **Visiting MSc Student**<br>Design Automation Conference 2015, San Francisco, CA, USA. |

## Publications

2017 **Emu: Rapid Prototyping of Networking Services.**
Nik Sultana, Salvator Galea, David Greaves, Marcin Wójcik, Jonny Shipton, Richard Clegg, Luo Mai, Pietro Bressana, Robert Soulé, Richard Mortier, Paolo Costa, Peter Pietzuch, Jon Crowcroft, Andrew W Moore, Noa Zilberman.
*The 2017 USENIX Annual Technical Conference (USENIX ATC '17)*.
https://atc17.usenix.hotcrp.com/paper/202?cap=0202a47MuHT4J7dc

2016 **A Polyhedral Model-based Framework for Dataflow Implementation on FPGA devices of Iterative Stencil Loops.**
Giuseppe Natale, Giulio Stramondo, Pietro Bressana, Riccardo Cattaneo, Donatella Sciuto, Marco D. Santambrogio.
*International Conference On Computer Aided Design (ICCAD) 2016*.
http://ieeexplore.ieee.org/document/7827654/
http://dl.acm.org/citation.cfm?id=2966995

2016 **Network Hardware-Accelerated Consensus.**
Huynh Tu Dang, Pietro Bressana, Han Wang, Ki Suh Lee, Hakim Weatherspoon, Marco Canini, Fernando Pedone, Robert Soulé.
*Arxiv*.
http://arxiv.org/abs/1605.05619
*USI Technical Report Series in Informatics*.
http://www.inf.usi.ch/faculty/soule/usi-tr-2016-03.pdf

2018 **Valutazione dell'emoglobina per lo screening dell'anemia preoperatoria ed alternative terapeutiche.**
Piazza M., Bressana M. F., Bressana M. M., Bressana P. G., Rosoaga Profiroiu R., Vitali F.
*Blood Transfusion Journal - Edizioni SIMTI*.

## Posters & Demos

2018 **A programmable framework for validating data planes** (Poster)
Xilinx Developer Forum (XDF).
San Jose, CA, USA.

2018 **Consensus for Non-Volatile Main Memory** (Demo)
Involved companies & institutions:
Western Digital, Barefoot Networks, Stordis, Delta,
USI, University of Cambridge, TU Darmstadt.
1st P4 European Workshop (P4EU).
University of Cambridge, United Kingdom.

2018 **A programmable framework for validating data planes** (Poster)
ACM Special Interest Group on Data Communication (SIGCOMM18).
Budapest, Hungary.

2017 **Emu: Rapid Prototyping of Networking Services** (Demo)
Design, Automation and Test in Europe (DATE17).
Lausanne, Switzerland.

## Talks

2018 **P4->NetFPGA**
Tutorial on Programming the Network Data Plane (P4).
ACM Special Interest Group on Data Communication (SIGCOMM18).
*Organizers*: Prof. Nate Foster, Prof. Robert Soulé & Dr. Noa Zilberman.

2018 **A programmable framework for validating data planes**
Multi-Service Networks workshop (MSN 2018).
The Cosener's House, Abingdon, UK.
http://coseners.net/coseners-2018/

2018 **A programmable framework for validating data planes**
Dagstuhl Seminar 18261.
Schloss Dagstuhl – Leibniz-Zentrum für Informatik, Germany.
https://www.dagstuhl.de/en/program/calendar/semhp/?semnr=18261/

2018 **A programmable framework for validating data planes**
Third Annual UK System Research Challenges Workshop.
Newcastle, United Kingdom.
http://sysws.org.uk/workshop/2018/

2018 **A programmable framework for validating data planes**
NetOS Group Talklets.
University of Cambridge, United Kingdom.
http://talks.cam.ac.uk/talk/index/102970

2018 **A programmable framework for validating data planes**
P4/SDN Workshop.
Politecnico di Milano, Italy.
http://www.inf.usi.ch/faculty/soule/chitchat.html

2017 **A programmable framework for validating data planes**
Western Digital.
Milpitas, CA, USA.

2016 **Consensus as a network service**
NetOS Group Talklets.
University of Cambridge, United Kingdom.
http://talks.cam.ac.uk/talk/index/69109

## Technical skills

### FPGAs

| | |
|---|---|
| Languages | Verilog, C, Bluespec BSV, VHDL, P4, PX. |
| Tools | Xilinx Vivado, VivadoHLS, SDK, Xilinx ISE, Xilinx SDNet, Xilinx P4SDNet, NetFPGA SUME framework (Cambridge University), Connectal framework (Cornell University), Bluespec, FLEXid license management. |
| Boards | NetFPGA SUME, VC707, VC709, ZC702, Avnet Spartan-6 LX9 MicroBoard. |
| Devices | Virtex7, Zynq, Spartan6, Opsero FPGADrive FMC NVMe, Cypress QDRII+ SRAM, Micron DDR3 SDRAM SODIMM, uSD card (SD-mode and SPI-mode). |
| IPs | PLDA QuickPCIe, Xilinx Aurora, Xilinx DCM and PLL, Xilinx MIG, Xilinx PCIe, Xilinx Microblaze, Xilinx Partial Reconfiguration, OpenCores SDSPI SD-card controller . |

### Programmable data planes

| | |
|---|---|
| Languages | P4. |
| Tools | Barefoot Capilano SDE. |
| Devices | Barefoot Tofino. |

### $\mu$Cs

| | |
|---|---|
| Languages | C |
| Tools | Arduino IDE, Fritzing. |
| Boards | Arduino UNO, Arduino pro mini. |
| Devices | ATmega328P, Wi-Fi (ESP8266), Bluetooth (BLE 4.0), GPS, GSM, Accelerometer, Magnetometer, Gyro. |

### Other Skills

| | |
|---|---|
| Languages | C, Java, Python, MATLAB, SQL, LaTeX, Bash Scripting, HTML, P4. |
| Tools | MATLAB, Eclipse, Eclipse JEE, MySQL, Python Kernprof, GitHub, Slurm, XCat, Pacemaker, Corosync, Ganglia, Paraview, Intel DPDK, Callgrind, Kcachegrind. |
| Operating systems | Linux (Ubuntu, CentOS), Microsoft Windows, Apple Mac OSX. |