Pietro Giuseppe Bressana

Contact Information

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Professional Profile

I have recently obtained a PhD in computer science from Università della Svizzera italiana (Lugano, Switzerland), under the supervision of Prof. Robert Soulé and Prof. Noa Zilberman. My research interests include programmable data planes, network debugging, network storage acceleration and FPGA-based hardware design.
Before starting my PhD degree, I worked as a research assistant for seven months at USI. I received my bachelor's degree in Electronic Engineering and my master's degree in Computer Engineering, both from Politecnico di Milano.

Education

2016 2020	**PhD Candidate in Computer Science** Università della Svizzera Italiana (USI), Switzerland
2015	**Master's degree, Computer Engineering** Politecnico di Milano, Italy
2013	**Bachelor's degree, Electronic Engineering** Politecnico di Milano, Italy

Professional Experience

2016 2020	**Teaching Assistant** Università della Svizzera Italiana (USI), Switzerland
2018	**Intern, Storage Architecture Research Group** Western Digital Research, Milpitas, CA, USA
2016	**Research Assistant, Distributed Systems Group** Università della Svizzera Italiana (USI), Switzerland

Languages

Italian	Native
English	Full Professional Proficiency
French	Basic

Research projects

2017 2020	**PTA** (USI & University of Cambridge) A Portable Test Architecture
2017	**Emu** (USI & University of Cambridge) A framework for network functions on FPGAs
2016	**NetPaxos** (USI) Consensus as a network service
2015	**exaFPGA** (Politecnico di Milano) Hardware acceleration for the next generation of super-computing platforms

Selected Publications

2020 | **Trading Latency for Compute in the Network**
Pietro Bressana, Noa Zilberman, Dejan Vucinic, Robert Soulé
Workshop on Network Application Integration/CoDesign, ACM SIGCOMM 2020 (NAI 2020)
Link to ACM Digital Library

2020 | **P4xos: Consensus as a Network Service**
Tu Dang, Pietro Bressana, Han Wang, Ki Suh Lee, Noa Zilberman, Hakim Weatherspoon, Marco Canini, Fernando Pedone, Robert Soulé
IEEE/ACM Transactions on Networking
Link to IEEE Xplore

2017 | **Emu: Rapid Prototyping of Networking Services**
Nik Sultana, Salvator Galea, David Greaves, Marcin Wójcik, Jonny Shipton, Richard Clegg, Luo Mai, Pietro Bressana, Robert Soulé, Richard Mortier, Paolo Costa, Peter Pietzuch, Jon Crowcroft, Andrew W Moore, Noa Zilberman
The 2017 USENIX Annual Technical Conference (USENIX ATC '17)
Link to usenix

2016 | **A Polyhedral Model-based Framework for Dataflow Implementation on FPGA devices of Iterative Stencil Loops**
Giuseppe Natale, Giulio Stramondo, Pietro Bressana, Riccardo Cattaneo, Donatella Sciuto, Marco D. Santambrogio
International Conference On Computer Aided Design (ICCAD) 2016
Link to IEEE Xplore

Technical skills

FPGAs	Xilinx 7 Series FPGAs Xilinx Vivado Xilinx SDNet Verilog language NetFPGA SUME framework P4 to FPGA design flow
μCs	STM Nucleo STM32Cube ARM Mbed ARM Mbed OS Arduino Ecosystem
In-Network Computing	Intel Barefoot Tofino $P4_{14}$ & $P4_{16}$ languages Intel Barefoot P4 Studio SDE
Other skills	Linux (Ubuntu, CentOS), Microsoft Windows, Apple Mac OSX C, Java, Python, LaTeX, Bash Scripting MATLAB, Eclipse, GitHub, Intel DPDK