Pietro Giuseppe Bressana

Personal Information

Date of Birth:	18 October 1989
Nationality:	Italian
Address:	Faculty of Informatics, Università della Svizzera italiana (USI), Via Giuseppe Buffi 13, 6904 Lugano, Switzerland.
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Research interests

Programmable data planes, Network debugging, FPGA-based hardware design.

Education

September 2016 - Present	**PhD Candidate in Computer Science** Università della Svizzera Italiana (USI), Via Giuseppe Buffi 13, 6904 Lugano, Switzerland. *Advisor*: Prof. Robert Soulé
February 2013 - December 2015	**Master's degree, Computer Engineering** Politecnico di Milano, Piazza Leonardo da Vinci, 32, 20133 Milano, Italy. Thesis date: 18 December 2015
October 2008 - February 2013	**Bachelor's degree, Electronic Engineering** Politecnico di Milano, Piazza Leonardo da Vinci, 32, 20133 Milano, Italy.
September 2003 - July 2008	**Diploma, Scientific High School** Liceo Scientifico Leonardo da Vinci, Via Stazione, 1, 26013 Crema, Italy.

Honors & Awards

November 2017	**SNF Doc.Mobility Fellowship** (26,400 CHF) 6-months research period at Cambridge University (UK).

Employment history

September 2016 - Present	**Teaching Assistant** Università della Svizzera Italiana (USI), Via Giuseppe Buffi 13, 6904 Lugano, Switzerland. –> *Computer Architecture*, Prof. Marc Langheinrich (2017/18)
August 2016 (one month)	**Research Assistant** Università della Svizzera Italiana (USI), Via Giuseppe Buffi 13, 6904 Lugano, Switzerland. *Main activity*: Leading the efforts to implement and evaluate consensus protocols in NetFPGA SUME boards and training a PhD student in programming NetFPGAs, within NetPaxos research project. *Advisors*: Prof. Robert Soulé and Prof. Rolf Krause
June 2016 - July 2016	**Research Assistant** Università della Svizzera Italiana (USI), Via Giuseppe Buffi 13, 6904 Lugano, Switzerland. *Main activity*: Installation, setup and configuration of the new cluster that will be used by the Institute of Computational Science (ICS). *Advisor*: Prof. Rolf Krause
February 2016 - May 2016	**Research Assistant** Università della Svizzera Italiana (USI), Via Giuseppe Buffi 13, 6904 Lugano, Switzerland. *Main activity*: Leading the efforts to implement and evaluate consensus protocols in NetFPGA SUME boards and training a PhD student in programming NetFPGAs, within NetPaxos research project. *Advisors*: Prof. Robert Soulé and Prof. Fernando Pedone

Academic experience

February 2018 - July 2018	**Visiting PhD Student** The Computer Laboratory. University of Cambridge, United Kingdom. *Advisor*: Dr. Noa Zilberman Funded by SNF Doc.Mobility Fellowship
December 2017	**Attending Barefoot Academy	BA 101** Barefoot Networks. Santa Clara, CA, United States.
April 2017	**Attending NetFPGA Developers Summit 2017** The Computer Laboratory. University of Cambridge, United Kingdom.
March 2017	**Leading a demo about Emu project at University Booth** *Emu: Rapid FPGA Prototyping of Network Services in C#*. Salvator Galea, Nik Sultana, Pietro Bressana, David Greaves, Robert Soulé, Andrew W. Moore, and Noa Zilberman. Design, Automation and Test in Europe (DATE17) Lausanne, Switzerland.
December 2016 (two weeks)	**Visiting PhD Student** The Computer Laboratory. University of Cambridge, United Kingdom. *Advisor*: Dr. Noa Zilberman
August 2016	**Sub-reviewer** The International Conference on Reconfigurable Computing and FPGAs (ReConFig 2016). Cancun, Mexico. *Reviewer*: Prof. Robert Soulé
June 2015	**Visitor** Design Automation Conference 2015. San Francisco, USA.

Research projects

P4Debug

September 2017 - Present

Despite the importance of computer networks and the abundance of network problems, engineers lack the tools and support necessary for debugging network hardware. This appears to be changing. A new breed of switches that can be programmed with high-level languages such as P4 match the speed of fixed function devices. This trend raises an important question: Can we leverage this new programmability for debugging network hardware? The goal of this project is to extend programmable network hardware with functionality to enable debugging. We propose a novel debugging framework, named P4Debug, that leverages recent advances in network programmability and hardware design, by providing unprecedented visibility into the internal state and operations of network devices. To evaluate P4Debug, we will develop a prototype that leverages several existing technologies, including the NetFPGA SUME framework and Xilinx SDNet P4-to-FPGA compiler.

Emu

January 2017 - September 2017

Emu is a framework for network functions on FPGAs, which builds upon Kiwi, a HLS compiler that allows computational scientists to program FPGAs with .NET code. The goal of Emu is to make it easy for software developers with no expertise in hardware languages to quickly develop, test, and deploy network applications on an FPGA. Moreover, using Emu, developers can run their network functions as normal processes, using virtual or real NICs, and using network simulators, simplifying debugging and testing. Indeed, the current implementation of Emu supports CPUs, simulation environments, and FPGAs. Further, Emu provides debugging and profiling tools that enable developers to inspect the behavior of the application at runtime.

NetPaxos

February 2016 - August 2016

The goal of this project is to develop a new set of optimized consensus protocols that leverage recent advances in network programmability and hardware design. These protocols will dramatically improve the performance of storage and replication systems that are the fundamental infrastructure for distributed and cloud computing services. My main task as a research assistant was to implement Paxos consensus protocol inside NetFPGA SUME boards using Connectal Framework (Cornell University), NetFPGA SUME Framework (Cambridge University) and Xilinx SDNet.
Project website: www.inf.usi.ch/faculty/soule/netpaxos.html

exaFPGA

October 2014 - December 2015

This project focuses on automatic hardware acceleration of C code with an explicit focus on power/performance metric, for the next generation of super-computing platforms, which is expected to deliver unprecedented performance for the benefit of all the scientific disciplines involving huge amount of computations. As a master's student, I was in charge to design and to build the multi-FPGA architecture of the system.
Project website: exafpga.necst.it

Publications

Conference publications

Title: **Emu: Rapid Prototyping of Networking Services.**
Authors: Nik Sultana, Salvator Galea, David Greaves, Marcin Wójcik, Jonny Shipton, Richard Clegg, Luo Mai, Pietro Bressana, Robert Soulé, Richard Mortier, Paolo Costa, Peter Pietzuch, Jon Crowcroft, Andrew W Moore, Noa Zilberman.
Submitted: The 2017 USENIX Annual Technical Conference (USENIX ATC '17).
Url: https://atc17.usenix.hotcrp.com/paper/202?cap=0202a47MuHT4J7dc

Title: **A Polyhedral Model-based Framework for Dataflow Implementation on FPGA devices of Iterative Stencil Loops.**
Authors: Giuseppe Natale, Giulio Stramondo, Pietro Bressana, Riccardo Cattaneo, Donatella Sciuto, Marco D. Santambrogio.
Submitted: International Conference On Computer Aided Design (ICCAD) 2016.
Url: http://ieeexplore.ieee.org/document/7827654/
Url: http://dl.acm.org/citation.cfm?id=2966995

Technical reports

Title: **Network Hardware-Accelerated Consensus.**
Authors: Huynh Tu Dang, Pietro Bressana, Han Wang, Ki Suh Lee, Hakim Weatherspoon, Marco Canini, Fernando Pedone, Robert Soulé.
Submitted: Arxiv - May 2016.
Url: http://arxiv.org/abs/1605.05619
Submitted: USI Technical Report Series in Informatics - March 2016.
Url: http://www.inf.usi.ch/faculty/soule/usi-tr-2016-03.pdf

Technical skills

FPGAs

Languages	Verilog, C, Bluespec BSV, VHDL, P4, PX.
Tools	Xilinx Vivado, VivadoHLS, SDK, Xilinx ISE, Xilinx SDNet, Xilinx P4SDNet, NetFPGA SUME framework (Cambridge University), Connectal framework (Cornell University), Bluespec, FLEXid license management.
Boards	NetFPGA SUME, VC707, VC709, ZC702, Avnet Spartan-6 LX9 MicroBoard.
Devices	Virtex7, Zynq, Spartan6, Opsero FPGADrive FMC NVMe, Cypress QDRII+ SRAM, Micron DDR3 SDRAM SODIMM, uSD card (SD-mode and SPI-mode).
IPs	PLDA QuickPCIe, Xilinx Aurora, Xilinx DCM and PLL, Xilinx MIG, Xilinx PCIe, Xilinx Microblaze, Xilinx Partial Reconfiguration, OpenCores SDSPI SD-card controller .

Data plane programming

Languages	P4.
Tools	Barefoot Capilano SDE.
Devices	Barefoot Tofino.

μCs

Languages	C
Tools	Arduino IDE, Fritzing.
Boards	Arduino UNO, Arduino pro mini.
Devices	ATmega328P, Wi-Fi (ESP8266), Bluetooth (BLE 4.0), GPS, GSM, Accelerometer, Magnetometer, Gyro.

Other Skills

Languages	C, Java, Python, MATLAB, SQL, LaTeX, Bash Scripting, HTML, P4.
Tools	MATLAB, Eclipse, Eclipse JEE, MySQL, Python Kernprof, GitHub, Slurm, XCat, Pacemaker, Corosync, Ganglia, Paraview, Intel DPDK, Callgrind, Kcachegrind.
Operating systems	Linux (Ubuntu, CentOS), Microsoft Windows, Apple Mac OSX.

Languages

Italian	Mother tongue.
English	Professional working proficiency.
French	Basic knowledge.

Courses

	First Certificate in English, Level B2.
	Autocad basic course.
	European computer driving licence (ECDL).
	Basic course on safety, Politecnico di Milano.
	Hazard analysis and critical control points (HACCP).

Driving license

Type	B (cars).

Volunteer work

2003 - 2017	Volunteer, Catholic Agency for International Aid and Development, Caritas Cremonese, Cremona (Italy).
2003 - 2017	Volunteer and Team leader, Food gathering management, Fondazione Banco Alimentare Onlus, Milano (Italy).
2005 - 2017	IT Responsible, Parrocchia San Vittore Martire, Agnadello (Italy).
2005 - 2017	Barista, Oratorio San Giovanni Bosco, Agnadello (Italy).