# Pietro Giuseppe Bressana

## Contact Information

| | |
|---|---|
| WEB | [pietrobressana.github.io](pietrobressana.github.io) |
| EMAIL | [pietro.bressana@usi.ch](pietro.bressana@usi.ch) |
| ADDRESS | Faculty of Informatics, Università della Svizzera italiana (USI), Via Giuseppe Buffi 13, 6904 Lugano, Switzerland. |

## Education

**2016 - PRESENT** — **PhD Candidate in Computer Science**
Università della Svizzera Italiana (USI), Switzerland.
*Advisors*: Prof. Robert Soulé & Dr. Noa Zilberman

**2015** — **Master's degree, Computer Engineering**
Politecnico di Milano, Italy.

**2013** — **Bachelor's degree, Electronic Engineering**
Politecnico di Milano, Italy.

## Employment history

**2016 - PRESENT** — **Teaching Assistant**
Università della Svizzera Italiana (USI), Switzerland.
–› *Computer Architecture*, Prof. Marc Langheinrich (2017/18)

**2016** — **Research Assistant**
Università della Svizzera Italiana (USI), Switzerland.

## Honors & Awards

**2017** — **SNF Doc.Mobility Fellowship** (26,400 CHF)
6-months research period at the University of Cambridge, UK.
[http://p3.snf.ch/project-178657](http://p3.snf.ch/project-178657)

## Research interests

Programmable data planes, Network validation, FPGA-based hardware design.

## Research projects

| | |
|---|---|
| 2017 - present | **NetDebug**<br>A programmable framework for validating data planes. |
| 2017 | **Emu**<br>A framework for network functions on FPGAs. |
| 2016 | **NetPaxos**<br>Consensus as a network service. |
| 2015 | **exaFPGA**<br>Hardware acceleration for the next generation<br>of super-computing platforms. |

## Academic experience

| | |
|---|---|
| 2018 | **Assistant**<br>Tutorial on Programming the Network Data Plane (P4).<br>ACM Special Interest Group on Data Communication (SIGCOMM18).<br>*Organizers*: Prof. Nate Foster & Prof. Robert Soulé. |
| 2018 | **Visiting PhD Student**<br>The Computer Laboratory, University of Cambridge, UK.<br>*Supervisor*: Dr. Noa Zilberman.<br>Funded by SNF Doc.Mobility Fellowship. |
| 2017 | **Barefoot Academy \| BA 101**<br>Barefoot Networks, Santa Clara, CA, USA. |
| 2017 | **NetFPGA Developers Summit 2017**<br>The Computer Laboratory, University of Cambridge, UK. |
| 2016 | **Visiting PhD Student**<br>The Computer Laboratory, University of Cambridge, UK.<br>*Supervisor*: Dr. Noa Zilberman. |
| 2016 | **Sub-reviewer**<br>The International Conference on Reconfigurable Computing<br>and FPGAs (ReConFig 2016).<br>*Reviewer*: Prof. Robert Soulé. |
| 2015 | **Visiting MSc Student**<br>Design Automation Conference 2015, San Francisco, CA, USA. |

# Publications

2017 — **Emu: Rapid Prototyping of Networking Services.**
Nik Sultana, Salvator Galea, David Greaves, Marcin Wójcik, Jonny Shipton, Richard Clegg, Luo Mai, <u>Pietro Bressana</u>, Robert Soulé, Richard Mortier, Paolo Costa, Peter Pietzuch, Jon Crowcroft, Andrew W Moore, Noa Zilberman.
*The 2017 USENIX Annual Technical Conference (USENIX ATC '17).*
https://atc17.usenix.hotcrp.com/paper/202?cap=0202a47MuHT4J7dc

2016 — **A Polyhedral Model-based Framework for Dataflow Implementation on FPGA devices of Iterative Stencil Loops.**
Giuseppe Natale, Giulio Stramondo, <u>Pietro Bressana</u>, Riccardo Cattaneo, Donatella Sciuto, Marco D. Santambrogio.
*International Conference On Computer Aided Design (ICCAD) 2016.*
http://ieeexplore.ieee.org/document/7827654/
http://dl.acm.org/citation.cfm?id=2966995

2016 — **Network Hardware-Accelerated Consensus.**
Huynh Tu Dang, <u>Pietro Bressana</u>, Han Wang, Ki Suh Lee, Hakim Weatherspoon, Marco Canini, Fernando Pedone, Robert Soulé.
*Arxiv.*
http://arxiv.org/abs/1605.05619
*USI Technical Report Series in Informatics.*
http://www.inf.usi.ch/faculty/soule/usi-tr-2016-03.pdf

2018 — **Valutazione dell'emoglobina per lo screening dell'anemia preoperatoria ed alternative terapeutiche.**
Piazza M., Bressana M. F., Bressana M. M., <u>Bressana P. G.</u>, Rosoaga Profiroiu R., Vitali F.
*Blood Transfusion Journal - Edizioni SIMTI.*

# Posters & Demos

2018 — **A programmable framework for validating data planes** (Poster)
ACM Special Interest Group on Data Communication (SIGCOMM18).
Budapest, Hungary.

2017 — **Emu: Rapid Prototyping of Networking Services** (Demo)
Design, Automation and Test in Europe (DATE17).
Lausanne, Switzerland.

# Talks

| | |
|---|---|
| 2018 | **A programmable framework for validating data planes**<br>Multi-Service Networks workshop (MSN 2018).<br>The Cosener's House, Abingdon, UK.<br>http://coseners.net/coseners-2018/ |
| 2018 | **A programmable framework for validating data planes**<br>Dagstuhl Seminar 18261.<br>Schloss Dagstuhl – Leibniz-Zentrum für Informatik, Germany.<br>https://www.dagstuhl.de/en/program/calendar/semhp/?semnr=18261/ |
| 2018 | **A programmable framework for validating data planes**<br>Third Annual UK System Research Challenges Workshop.<br>Newcastle, United Kingdom.<br>http://sysws.org.uk/workshop/2018/ |
| 2018 | **A programmable framework for validating data planes**<br>NetOS Group Talklets.<br>University of Cambridge, United Kingdom.<br>http://talks.cam.ac.uk/talk/index/102970 |
| 2018 | **A programmable framework for validating data planes**<br>P4/SDN Workshop.<br>Politecnico di Milano, Italy.<br>http://www.inf.usi.ch/faculty/soule/chitchat.html |
| 2017 | **A programmable framework for validating data planes**<br>Western Digital.<br>Milpitas, CA, USA. |
| 2016 | **Consensus as a network service**<br>NetOS Group Talklets.<br>University of Cambridge, United Kingdom.<br>http://talks.cam.ac.uk/talk/index/69109 |

## TECHNICAL SKILLS

**FPGAs**

| | |
|---|---|
| LANGUAGES | Verilog, C, Bluespec BSV, VHDL, P4, PX. |
| TOOLS | Xilinx Vivado, VivadoHLS, SDK, Xilinx ISE, Xilinx SDNet, Xilinx P4SDNet, NetFPGA SUME framework (Cambridge University), Connectal framework (Cornell University), Bluespec, FLEXid license management. |
| BOARDS | NetFPGA SUME, VC707, VC709, ZC702, Avnet Spartan-6 LX9 MicroBoard. |
| DEVICES | Virtex7, Zynq, Spartan6, Opsero FPGADrive FMC NVMe, Cypress QDRII+ SRAM, Micron DDR3 SDRAM SODIMM, uSD card (SD-mode and SPI-mode). |
| IPs | PLDA QuickPCIe, Xilinx Aurora, Xilinx DCM and PLL, Xilinx MIG, Xilinx PCIe, Xilinx Microblaze, Xilinx Partial Reconfiguration, OpenCores SDSPI SD-card controller . |

**Programmable data planes**

| | |
|---|---|
| LANGUAGES | P4. |
| TOOLS | Barefoot Capilano SDE. |
| DEVICES | Barefoot Tofino. |

**$\mu$Cs**

| | |
|---|---|
| LANGUAGES | C |
| TOOLS | Arduino IDE, Fritzing. |
| BOARDS | Arduino UNO, Arduino pro mini. |
| DEVICES | ATmega328P, Wi-Fi (ESP8266), Bluetooth (BLE 4.0), GPS, GSM, Accelerometer, Magnetometer, Gyro. |

**Other Skills**

| | |
|---|---|
| LANGUAGES | C, Java, Python, MATLAB, SQL, LaTeX, Bash Scripting, HTML, P4. |
| TOOLS | MATLAB, Eclipse, Eclipse JEE, MySQL, Python Kernprof, GitHub, Slurm, XCat, Pacemaker, Corosync, Ganglia, Paraview, Intel DPDK, Callgrind, Kcachegrind. |
| OPERATING SYSTEMS | Linux (Ubuntu, CentOS), Microsoft Windows, Apple Mac OSX. |