Pietro Giuseppe Bressana

Contact Information

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Education

2016 - present	**PhD Candidate in Computer Science** Università della Svizzera Italiana (USI), Switzerland. *Advisors*: Prof. Robert Soulé & Dr. Noa Zilberman (University of Cambridge, UK)
2015	**Master's degree, Computer Engineering** Politecnico di Milano, Italy.
2013	**Bachelor's degree, Electronic Engineering** Politecnico di Milano, Italy.

Employment history

2016 - present	**Teaching Assistant** Università della Svizzera Italiana (USI), Switzerland. –› *Computer Architecture*, Prof. Marc Langheinrich (2017/18) –› *Advanced Networking*, Prof. Robert Soulé (2018/19)
2018	**Intern** Western Digital Research, Milpitas, CA, USA. Under the supervision of Dejan Vucinic.
2016	**Research Assistant** Università della Svizzera Italiana (USI), Switzerland.

Honors & Awards

2019	**Google Inc.** Fellowship for attending BUCA 2019 summer school at The Castle of the Metamorphoses, Rocca Sinibalda, Italy.
2019	**Hasler Foundation** (48'636 CHF) 12-months research on Debugging Programmable Data Planes.
2017	**SNF Doc.Mobility Fellowship** (26'400 CHF) 6-months research period at the University of Cambridge, UK. http://p3.snf.ch/project-178657

Updated on May 22, 2019

Research interests

Programmable data planes, Network validation, Network storage acceleration, FPGA-based hardware design.

Research projects

2017 - present	**NetDebug** (USI & University of Cambridge) A programmable framework for validating data planes.
2017	**Emu** (USI & University of Cambridge) A framework for network functions on FPGAs.
2016	**NetPaxos** (USI) Consensus as a network service.
2015	**exaFPGA** (Politecnico di Milano) Hardware acceleration for the next generation of super-computing platforms.

Academic experience

2016 - present | **Contributing to the NetFPGA SUME Framework**
https://github.com/NetFPGA/NetFPGA-SUME-public/wiki

2019 | **Attending BUCA 2019 summer school**
The Castle of the Metamorphoses, Rocca Sinibalda, Italy.
https://sites.google.com/view/bici-buca-2019/home

2019 | **Attending NRP Research day 2019 - NFP 75 Big Data**
Fabrikhalle, Bern, Switzerland.
http://www.nfp75.ch/en/Events/Pages/190403-agenda-nfp75-research-day.aspx

2019 | **Organising P4 Hackathon at NSDI '19**
Boston, MA, USA.
https://p4.org/events/2019-03-01-nsdi/

2018 | **Teaching a full-day workshop on NetFPGA SUME & P4 Language**
School of Engineering, Santa Clara University, CA, USA.
Hosted by: Prof. Behnam Dezfouli & Prof. Shoba Krishnan

2018 | **Visiting PhD Student**
The Computer Laboratory, University of Cambridge, UK.
Supervisor: Dr. Noa Zilberman.
Funded by SNF Doc.Mobility Fellowship.

2017 | **Barefoot Academy | BA 101**
Barefoot Networks, Santa Clara, CA, USA.

2017 | **NetFPGA Developers Summit 2017**
The Computer Laboratory, University of Cambridge, UK.

2016 | **Visiting PhD Student**
The Computer Laboratory, University of Cambridge, UK.
Supervisor: Dr. Noa Zilberman.

2016 | **Sub-reviewer**
The International Conference on Reconfigurable Computing and FPGAs (ReConFig 2016).
Reviewer: Prof. Robert Soulé.

2015 | **Visiting MSc Student**
Design Automation Conference 2015, San Francisco, CA, USA.

Technical experience

2019 - present | Administering the cluster of the Distributed Systems Group (100 nodes).
Università della Svizzera Italiana (USI), Switzerland.

2019 | Designed a cluster for distributed system research, that provides 512 VMs, smart NICs and programmable switches.
Università della Svizzera Italiana (USI), Switzerland.

2016 | Contributed to build and to configure the new HPC cluster of the Institute of Computational Science (ICS).
Università della Svizzera Italiana (USI), Switzerland.

2016 | Built, configured and administered the first cluster in the university equipped with FPGAs, programmable switches and RDMA NICs.
Università della Svizzera Italiana (USI), Switzerland.

Publications

2019 **Partitioned Paxos via the Network Data Plane**
Huynh Tu Dang, Pietro Bressana, Han Wang, Ki Suh Lee, Noa Zilberman, Hakim Weatherspoon, Marco Canini, Fernando Pedone, Robert Soulé.
Arxiv.
https://arxiv.org/abs/1901.08806
USI Technical Report Series in Informatics.
https://search.usi.ch/en/publications/20177/partitioned-paxos-via-the-network-data-plane

2018 **Valutazione dell'emoglobina per lo screening dell'anemia preoperatoria ed alternative terapeutiche.**
Piazza M., Bressana M. F., Bressana M. M., Bressana P. G., Rosoaga Profiroiu R., Vitali F.
Blood Transfusion Journal - Edizioni SIMTI.

2017 **Emu: Rapid Prototyping of Networking Services.**
Nik Sultana, Salvator Galea, David Greaves, Marcin Wójcik, Jonny Shipton, Richard Clegg, Luo Mai, Pietro Bressana, Robert Soulé, Richard Mortier, Paolo Costa, Peter Pietzuch, Jon Crowcroft, Andrew W Moore, Noa Zilberman.
The 2017 USENIX Annual Technical Conference (USENIX ATC '17).
https://atc17.usenix.hotcrp.com/paper/202?cap=0202a47MuHT4J7dc

2016 **A Polyhedral Model-based Framework for Dataflow Implementation on FPGA devices of Iterative Stencil Loops.**
Giuseppe Natale, Giulio Stramondo, Pietro Bressana, Riccardo Cattaneo, Donatella Sciuto, Marco D. Santambrogio.
International Conference On Computer Aided Design (ICCAD) 2016.
http://ieeexplore.ieee.org/document/7827654/
http://dl.acm.org/citation.cfm?id=2966995

2016 **Network Hardware-Accelerated Consensus**
Huynh Tu Dang, Pietro Bressana, Han Wang, Ki Suh Lee, Hakim Weatherspoon, Marco Canini, Fernando Pedone, Robert Soulé.
Arxiv.
http://arxiv.org/abs/1605.05619
USI Technical Report Series in Informatics.
http://www.inf.usi.ch/faculty/soule/usi-tr-2016-03.pdf

Posters & Demos

2018 **A programmable framework for validating data planes** (Poster)
Xilinx Developer Forum (XDF).
San Jose, CA, USA.

2018 **Consensus for Non-Volatile Main Memory** (Demo)
Involved companies & institutions:
Western Digital Research, Barefoot Networks, Stordis, Delta,
USI, University of Cambridge, TU Darmstadt.
1st P4 European Workshop (P4EU).
University of Cambridge, United Kingdom.

2018 **A programmable framework for validating data planes** (Poster)
ACM Special Interest Group on Data Communication (SIGCOMM18).
Budapest, Hungary.

2017 **Emu: Rapid Prototyping of Networking Services** (Demo)
Design, Automation and Test in Europe (DATE17).
Lausanne, Switzerland.

Talks

2018 **A High-Performance Heterogeneous Network Computing Platform**
Barefoot Networks.
Santa Clara, CA, USA.

2018 **A High-Performance Heterogeneous Network Computing Platform**
Western Digital Research.
Milpitas, CA, USA.

2018 **P4–›NetFPGA**
Tutorial on Programming the Network Data Plane (P4).
ACM Special Interest Group on Data Communication (SIGCOMM18).
Organizers: Prof. Nate Foster, Prof. Robert Soulé & Dr. Noa Zilberman.

2018 **A programmable framework for validating data planes**
Multi-Service Networks workshop (MSN 2018).
The Cosener's House, Abingdon, UK.
http://coseners.net/coseners-2018/

2018 **A programmable framework for validating data planes**
Dagstuhl Seminar 18261.
Schloss Dagstuhl – Leibniz-Zentrum für Informatik, Germany.
https://www.dagstuhl.de/en/program/calendar/semhp/?semnr=18261/

2018 **A programmable framework for validating data planes**
Third Annual UK System Research Challenges Workshop.
Newcastle, United Kingdom.
http://sysws.org.uk/workshop/2018/

2018 **A programmable framework for validating data planes**
NetOS Group Talklets.
University of Cambridge, United Kingdom.
http://talks.cam.ac.uk/talk/index/102970

2018 **A programmable framework for validating data planes**
P4/SDN Workshop.
Politecnico di Milano, Italy.
http://www.inf.usi.ch/faculty/soule/chitchat.html

2017 **A programmable framework for validating data planes**
Western Digital Research.
Milpitas, CA, USA.

2016 **Consensus as a network service**
NetOS Group Talklets.
University of Cambridge, United Kingdom.
http://talks.cam.ac.uk/talk/index/69109

Technical skills

FPGAs

Languages	Verilog, C, Bluespec BSV, VHDL, P4, PX.
Tools	Xilinx Vivado, VivadoHLS, SDK, Xilinx ISE, Xilinx SDNet, Xilinx P4SDNet, NetFPGA SUME framework (Cambridge University), Connectal framework (Cornell University), Bluespec, FLEXid license management.
Boards	NetFPGA SUME, Xilinx VC707, Xilinx VC709, Xilinx ZC702, Avnet Spartan-6 LX9 MicroBoard, Avnet ZedBoard, Tul PYNQ-Z2.
Devices	Virtex7, Zynq, Spartan6, Opsero FPGADrive FMC NVMe, Cypress QDRII+ SRAM, Micron DDR3 SDRAM SODIMM, uSD card (SD-mode and SPI-mode).
IPs	PLDA QuickPCIe, Xilinx Aurora, Xilinx DCM and PLL, Xilinx MIG, Xilinx PCIe, Xilinx Microblaze, Xilinx Partial Reconfiguration, OpenCores SDSPI SD-card controller .

Programmable data planes

Languages	$P4_{14}$ & $P4_{16}$.
Tools	Barefoot P4 Studio SDE
Devices	Edge-core Wedge 100-BF.

μCs

Languages	C
Tools	STMicroelectronics STM32Cube, STMicroelectronics STM32CubeMX, Arduino IDE, Fritzing.
Boards	STMicroelectronics STM32VLDISCOVERY, Arduino UNO, Arduino pro mini.
Devices	STMicroelectronics STM32, ATmega328P, Wi-Fi (ESP8266), Bluetooth (BLE 4.0), GPS, GSM, Accelerometer, Magnetometer, Gyro.

Other Skills

Languages	C, Java, Python, MATLAB, SQL, LaTeX, Bash Scripting, HTML, P4.
Tools	MATLAB, Eclipse, Eclipse JEE, MySQL, Python Kernprof, GitHub, Slurm, XCat, Pacemaker, Corosync, Ganglia, Paraview, Intel DPDK, Callgrind, Kcachegrind.
Operating systems	Linux (Ubuntu, CentOS), Microsoft Windows, Apple Mac OSX.