Renhe Chen | Resume

393 Road Middle Huaxia – Shanghai, China
(+86) 173 1713 8562 • chenrh@shanghaitech.edu.cn
www.chenrenhe.com

Education

Master of Eng. candidate in Electrical Engineering
ShanghaiTech University *2021–2024 (Expected)*
Thesis supervisor: Dr. Xufeng Kou.
GPA:3.77/4.0
Major Courses: Analog IC II(A+), Nano Processing(A+), Physics of Semiconductor Devices(A+)

Bachelor of Eng. in Electrical Engineering
ShanghaiTech University *2017–2021*
GPA:3.71/4.0
Major Courses: Analog IC(A+), Digital IC(A+), Embedded Systems(A+), Electric Circuits(A)

Research Projects

High-performance analog-to-digital converter **in ShanghaiTech University**
Apr. 2022 – Present

- In charge of the entire IC tape-out process with circuit simulation, layout and measurement.
- Proposed a gain-boosting dynamic comparator featuring a modified pre-amplifier with 35% power reduction.
- Designed an asynchronous SAR logic enabling sufficient CDAC settling time and has low circuit complexity.
- Fabricated prototype in 28-nm CMOS, set up evaluation platform with dedicated PCB.
- Measured SNDR reached 60.9 dB at Nyquist and 63.8 dB at DC, FoM_W reached 12.7 fJ/conv-step.

Collaborator: Dr. Hao Xu from Fudan University, Shanghai, China.

Dynamic bias optimization circuit for MRAM **in ShanghaiTech University**
Jun. 2022 – Present

- Quantified the optimal read bias voltage of MRAM cell, in reference with measured results.
- Designed a dynamic bias optimization circuit (DBO) that can track the optimal read bias voltage in background, with respect to a wide range of process variation and thermal conditions.
- Simulated the proposed DBO with 1-Mb MRAM array, using 28-nm PDK and Verilog-A MRAM model.
- Simulated tracking accuracy over 90% and BER reduction over 2 orders of magnitude.

Collaborator: Dr. Albert Lee from Inston Technology, Jiangsu, China.

Cryogenic circuit design and evaluation **in ShanghaiTech University**
Jul. 2020 – 2021

- Simulated CMOS circuit operation down to 10K using cryogenic compact model.
- Implemented a 5-bit flash ADC using cryogenic modeled PDK.
- Cryogenic device measurement and circuit evaluation using liquid helium dewar and probe station.

Publications

Conference publications:

- **R.Chen**, A. Lee, Y. Hu, H. Xu, D. Wu, X. Kou." A 12-bit 75 MS/s Asynchronous SAR ADC with Gain-Boosting Dynamic Comparator" IEEE International Symposium on Circuits and Systems (ISCAS), 2024 (under review).

• Z. Wang, **R.Chen**, A. Lee, Y. Gu, D. Wu, X. Kou." A Lightweight Post-Processing Method for Voltage-Controlled MTJ based True Random Number Generator" IEEE International Symposium on Circuits and Systems (ISCAS), 2024 (under review).

• Y. Hu, Z. Wang, **R. Chen**, Z. Tang, A. Guo, C. Cao, W. Wu, S. Chen, Y. Zhao, L. Yu, G. Shang, H. Xu, S. Hu, X. Kou." Cryo-CMOS Model-Enabled 8-Bit Current Steering DAC Design for Quantum Computing" IEEE International Symposium on Circuits and Systems (ISCAS), 2022.

• Z. Wang, C. Cao, P. Yang, Y. Yuan, Z. Tang, **R. Chen**, W. Wu, X. Luo, A. Guo, L. Yu, G. Shang, Z. Zhang, S. Hu, X. Kou." Designing EDA-Compatible Cryogenic CMOS Platform for Quantum Computing Applications." IEEE Electron Devices Technology & Manufacturing Conference (EDTM), 2021.

Journal publications:

• **R.Chen**, A. Lee, Z. Wang, D. Wu, X. Kou. "A Read Margin Enhancement Circuit with Dynamic Bias Optimization for MRAM." IEEE Transactions on Circuits and Systems II - Express Briefs (under review, arxiv).

• P. Huang, Y. Gu, C. Fu, J. Lu, Y. Zhu, **R Chen**, Y. Hu, Y. Ding, H. Zhang, S. Lu, S. Peng, W. Zhao, X. Kou "SOT-MRAM-Enabled Probabilistic Binary Neural Networks for Noise-Tolerant and Fast Training" (under review, arxiv)

Skills

Software:
IC Design: Cadence Virtuoso, Synopsys Design Compiler, IC Compiler, Verdi, VCS, Formality
Embedded system: Altuim Designer, Xilinx Vivado, Keil uVision, NI Multisim
Other: Silvaco TCAD, Tanner L'edit, Adobe Photoshop, Illustrator

Programming: Matlab, C/C++, Python

Instrument: network analyzer, logic analyzer, signal source analyzer, cryogenic testing system, probe station

Language: Chinese (Native), English (Fluent, TOEFL iBT: 99), Japanese (Basic)

Work Experience

Jun. 2022 – Jan.2023: Internship as Analog IC Design Engineer, United Imaging, Shanghai

2021 Spring, 2021 Fall: Teaching Assistant of Digital Integrated Circuits I, ShanghaiTech University

Awards

2022,2023: Outstanding Student, ShanghaiTech University
2021: Outstanding Graduate, ShanghaiTech University
2019: Second Prize in Shanghai, National Undergraduate Electronics Design Contest
2019: First Prize in The North Region, RoboMaster Robotics Competition
2019: Third Prize National, RoboMaster Robotics Competition
2018,2020: Excellent Academic Scholarship of SIST, ShanghaiTech University

Activities

2018-2019: Vice President of the School's Volunteers' Association, ShanghaiTech University
2017-2021: Vice President of the School's Modelers' Club, ShanghaiTech University
Jul. 2019: Museum Docent in Shanghai Science and Technology Museum
Jun. 2018, Jun. 2021: Volunteer of the Open Day, ShanghaiTech University
Nov. 2022: Volunteer of the School's Music Festival