A 12-bit 75 MS/s Asynchronous SAR ADC with Gain-Boosting Dynamic Comparator

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***Abstract*—This paper proposes a successive-approximation-register (SAR) analog-to-digital converter (ADC) features a gain-boosting dynamic comparator design and a low-delay SAR logic. The proposed comparator incorporates a positive feedback in the pre-amplifier, which enables a high gain during the integration phase, thereby improving the energy efficiency. Meanwhile, to ensure a sufficient settling time for the internal capacitive digital-to-analog converter (CDAC), an asynchronous SAR logic with a low logic delay in the SAR logic loop is implemented. Accordingly, a prototype ADC is manufactured using the 28-nm CMOS technology, which achieves a power consumption of 860 μW at 75 MHz sampling frequency. Moreover, the measured signal-to-noise and distortion ratio (SNDR) of the prototype at Nyquist frequency is 60.9 dB, which translates to a Walden figure of merit (FoM_W) of 12.7 fJ/conversion-step.**

***Keywords*—Analog-to-digital converter, successive approximation register, asynchronous Logic, gain-boosting, dynamic comparator.**

I. Introduction

Successive-approximation-register (SAR) analog-to-digital converter (ADC) has emerged as an indispensable element for moderate-to-high resolution data conversion in a variety of applications, including biomedical sensors, wireless communication systems, and internet of things (IoT) [1]–[3]. A generic SAR ADC framework employs a feedback loop, which consists of a single comparator, a capacitive digital-to-analog converter (CDAC), and the SAR logic, as illustrated in Fig. 1. Compared to other types of ADCs, the SAR ADC benefits from its extensive use of digital components [4]. By leveraging switch capacitor circuits and incorporating only one dynamic comparator, the SAR ADC can be easily scaled down with the advancement of technology nodes, which in turn enables higher speed, lower power consumption, and a reduced layout area. Moreover, the SAR architecture also serves as a fundamental building block for various hybrid ADCs, such as SAR-assisted ADC, pipeline-SAR ADC, and noise-shaping ADC, thereby further expanding its operational capabilities [5]–[8].

Currently, a critical challenge of high-performance SAR ADCs lies in the energy efficiency of the comparator. In the case of medium resolution (10~12-bit) SAR-only ADCs, the comparator is the primary source of noise, thereby limiting the dynamic performance. In terms of high-speed designs, additional power consumption is often required to achieve the noise and speed benchmarks, which make the comparator one of the most power-intensive components in the entire ADC. While several comparator structures have been proposed, these approaches are primarily suitable for low-speed scenarios [9]–[11]. Therefore, a suitable dynamic comparator design that accommodates noise, speed, and power consumption metrics for a wider range of applications is of high demand.

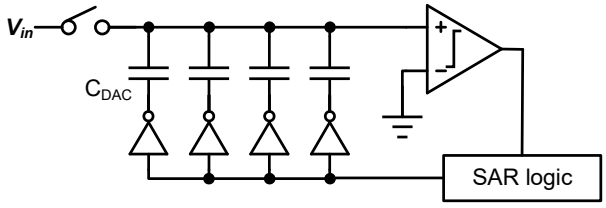

Fig. 1. The schematic of a typical SAR ADC, in single ended configuration.

Accordingly, in this paper, we present an asynchronous SAR ADC with a gain-boosting dynamic comparator to enhance its energy efficiency. The remainder of this paper is organized as follows: Section II introduces the operating principle of the proposed gain-boosting comparator. Section III elaborates on the circuit implementation for the SAR ADC. Section IV presents the measurement results of the manufactured ADC chip. Finally, Section V concludes this paper.

II. Gain Boosting Comparator

The conventional two-stage dynamic comparator comprises a pre-amplifier and a regenerative latch, as shown in Fig. 2(a) [12]. Generally, the operation process of such a comparator can be divided into the following phases. Initially, when CLK is low, both V_A and V_B are reset to V_{DD}, while the output signals stored in the latch are reset to 0. Subsequently, when a differential voltage $|v_{ip} - v_{in}|$ is applied and CLK=1, the input pair (M_1/M_2) in the pre-amplifier discharges V_A and V_B with different current amplitudes. This integration process amplifies the input differential voltage while reducing the common mode voltage of V_A and V_B. Finally, when the internal common mode voltage at the input of the regenerative latch surpasses the threshold level of the latch $V_{t,lat}$, the latch is triggered and generates the comparison result through a positive feedback.

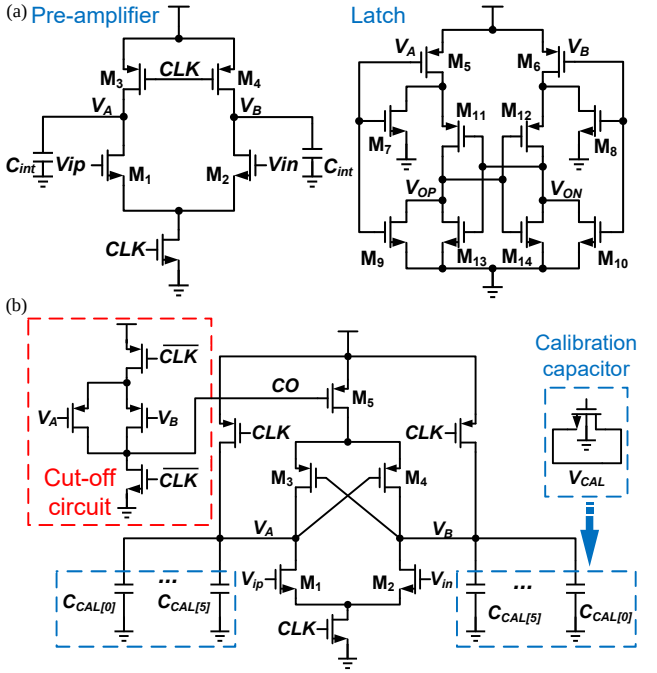

Fig. 2. (a) Conventional two-stage dynamic comparator, presented in [12]. (b) The proposed gain-boosting dynamic pre-amplifier.

Therefore, the differential voltage gain of the pre-amplifier during the amplification phase can be quantified as

$$A = T_{amp}\frac{i_d}{C_{int}v_{id}} = \frac{V_{t,lat}C_{int}}{G_mV_{OD}}\frac{g_mv_{id}}{C_{int}v_{id}} = \frac{g_mV_{t,lat}}{G_mV_{OD}} \quad (1)$$

where v_{id} is the input differential voltage, T_{amp} the amplification time, C_{int} the total internal capacitance at the output of the pre-amplifier, V_{OD} the overdrive voltage of the input pair, $V_{t,lat}$ the threshold level of the latch. g_m and G_m are the differential and common mode trans-conductance of M_1 and M_2, respectively.

Guided by (1), we can conclude that a low G_m will increase the integration time, while a high g_m will provide more differential current. In conventional designs, the values of g_m and G_m are the same as the transconductance of M_1/M_2. In contrast, our proposed gain-boosting dynamic comparator incorporates modifications to the first stage design to further enhance pre-amplifier gain, as depicted in Fig. 2(b). In particular, the redesigned pre-amplifier consists of an input pair (M_1/M_2), the gain-boosting PMOS ($M_3 - M_5$), the cut-off circuit, and the calibration capacitors. The threshold level of the latch is lowered by adjusting the relative aspect ratio of $M_5 - M_{10}$, which allows $M_3 - M_5$ to operate before the activation of the latch. In this context, when the CLK signal is triggered, the input pair M_1/M_2 initially operates in the same manner as the conventional design. Yet once the common-mode voltage of V_A and V_B reaches the threshold voltage of M_3/M_4, the cross coupled pair is activated. Under such circumstances, $M_1 - M_4$ function as a half latch, which provides a weak positive feedback, and leads to a slight reduction in the common-mode current (i.e., smaller G_m). Additionally, this positive feedback framework also increases g_m, hence realizing an enhanced differential current. In this regard, the proposed dynamic comparator increases pre-amplifier gain by increasing both integration time and current, as described in (1). On the other hand, the introduction of the cross-coupled pair would bring about static current in the steady state, which inevitably causes undesirable power overhead. To address this issue, a cut-off circuit is integrated to disable M_5 after the pre-amplifier has enabled the regenerative latch.

TABLE I: Simulated Performance of Comparators

	Conventional	Proposed (same power)	Proposed (same noise)
1σ Noise (μVrms)	210	170	210
Delay (ps)	199.4	193.9	199.1
Energy (fJ/conv)	180	183	117
Power@2GHz (μW)	360	366	234
Internal Cap. (fF)	41.8	57.9	11.8

Quantitatively, we compared the proposed gain-boosting dynamic comparator with the conventional two-stage counterpart in terms of power consumption and noise. Here, to ensure a fair comparison, the second stage circuits were kept identical in both designs. Accordingly, we evaluated the circuit performance in two aspects. As presented in Table I, when both circuits operate at the same speed with the same power, our gain-boosting comparator exhibits a 19% noise reduction compared to the conventional design. On the other hand, when configured with equivalent power and delay, our circuit achieves a 35% reduction in power consumption and consumes 75% less internal capacitance. Therefore, the above simulation results manifest the efficacy of the gain-boosting technique.

III. Circuit Implementation

A. 12-bit SAR ADC Architecture

The schematic of the 12-bit SAR ADC with gain-boosting dynamic comparator is shown in Fig. 3. In this architecture, the sampling switches are bootstrapped, which increase the linearity of the sampled signals. In view of the CDAC array, a 1-bit redundancy is introduced to mitigate the impact of incomplete settling. Meanwhile, the redundancy arrangement of the CDAC array described in [13] is also adopted to minimize the total sampling capacitance. Therefore, the weights of each bit, from the MSB to the LSB, are assigned as 1920, 1024, 512, 288, 160, 80, 48, 32, 16, 8, 4, 2, 1, respectively. Besides, except for the LSB capacitor, the CDAC array employs a split monotonic scheme to optimize the switching energy, and a low-delay asynchronous SAR logic is accompanied to minimize the logic delay while simplifying the circuit complexity.

B. Low Delay Asynchronous SAR Logic

In general, the cycle time of a 1-bit conversion operation in an asynchronous SAR ADC is determined by the sum of the comparator resolving time and the delay of the timing logic, which accounts for both the SAR logic delay and the CDAC settling time [14]. However, in the case of high-speed and high-resolution operations, the shortened SAR cycle time

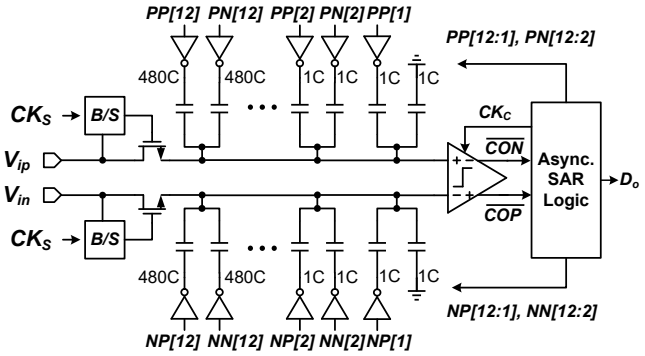

Fig. 3. The schematic of the proposed 12-bit asynchronous SAR ADC.

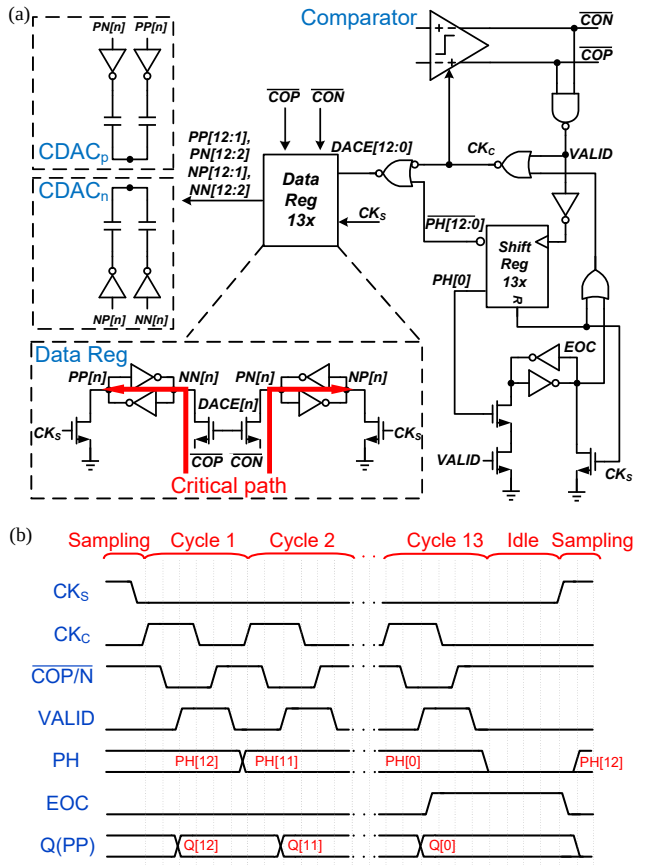

Fig. 4. (a) The detailed schematic of the proposed low delay asynchronous SAR logic, with the critical path highlighted in red. (b) The operating timing diagram of the SAR logic

imposes a tighter regulation on the CDAC settling time. Therefore, in order to meet the aforementioned time requirement while maximizing the CDAC settling time, we developed a low-delay SAR logic circuit topology that consists of the timing logic, the phase generation circuit, and the data registers, as illustrated in Fig. 4(a). Accordingly, the corresponding SAR loop time is given by $t_{CYCLE} = t_{COMP} + t_{RST} + 2t_{NOR} + 2t_{NAND}$, where t_{COMP} and t_{RST} represent the resolving time and the reset time of the dynamic comparator. As shown in Fig. 4(b), in each conversion cycle, a phase is selected by

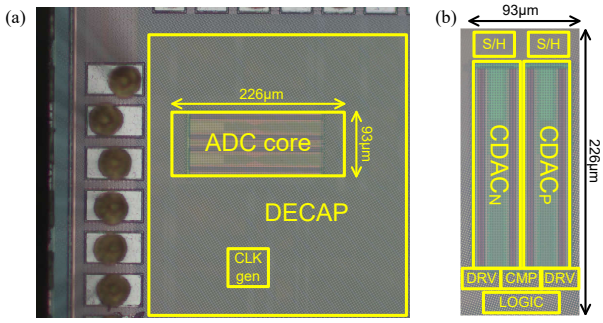

Fig. 5. The die micrograph of (a) the top view and (b) the core of the proposed ADC.

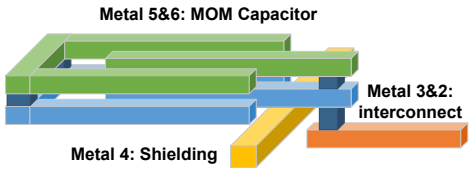

Fig. 6. The structure of a typical unit capacitor cell in the proposed ADC.

the PH signal through the shift register. Subsequently, the corresponding data register is enabled simultaneously with the comparator, which allows it to capture the comparison result as soon as the conversion is finished. As a result, this design ensures that the critical path delay from the comparator to the CDAC driver is only $t_{PT} + t_{INV}$, where t_{PT} is the delay of a single pass transistor and t_{INV} is the delay of an inverter. Furthermore, we need to point out that the proposed data register automatically generates the necessary signals for the split monotonic switching scheme, thereby reducing the circuit complexity.

C. Layout Implementation

Fig. 5 presents the overall layout of the SAR ADC core. To minimize the comparator loading and logic delay, the data registers were positioned adjacent to the dynamic comparator. In view of the CDAC array, a finger-like layout configuration, depicted in Fig. 6, was utilized to achieve both a low area occupation and a low capacitance mismatch. Finally, the placement strategy described in [15] was adopted, which groups the capacitors with the same weight to compromise parasitic capacitance and mismatch concerns. Additionally, a shield net was incorporated in the fourth metal layer to mitigate the weight imbalance resulting from parasitic capacitance between interconnections.

IV. Measurement Results

The 12-bit asynchronous SAR ADC was manufactured using the 28-nm CMOS process, and the area of the ADC core is 0.021 mm^2. During the electrical measurement, the digital components operated at a supply voltage of 1.0 V, whereas the analog section was set at 1.2 V.

The dynamic performance of the proposed ADC was firstly evaluated, and the relevant measured power versus frequency

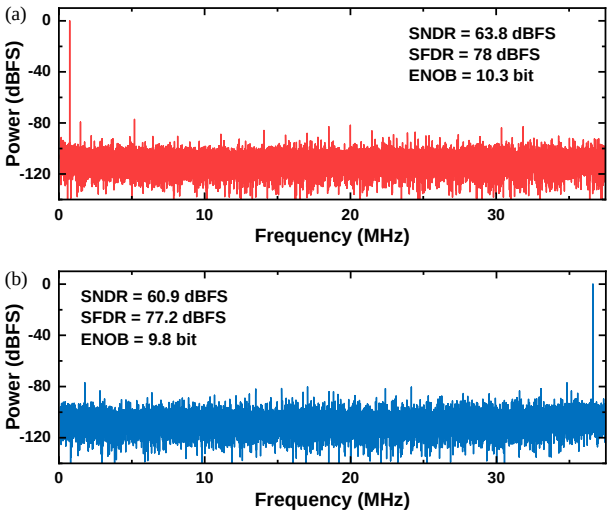

Fig. 7. Measured spectra at (a) low input frequency (b) Nyquist sampling of the proposed SAR ADC.

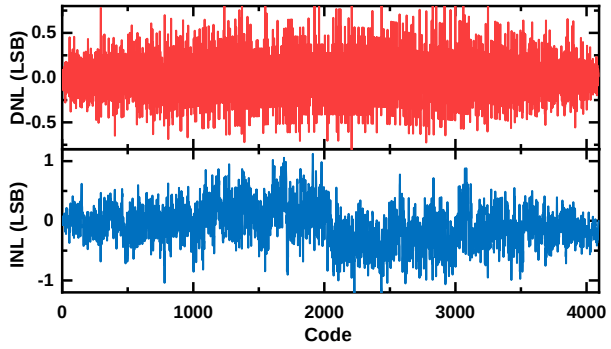

Fig. 8. Measured DNL and INL of the proposed SAR ADC with off-chip calibration.

spectra are summarized in Fig. 7 (i.e., the input common-mode voltage was biased at 0.6 V, and the amplitude of the input signal was 2.0 V_{PP}). It is seen that the SAR-ADC achieves a SNDR of 63.8 dB and an SFDR of 78 dB at low input frequency of f_{sig} = 500 KHz, indicating an ENOB of 10.3 bits. In the case of Nyquist sampling (i.e., $f_{sig} = 0.5f_S$), however, the SNDR drops to 60.9 dB (i.e., 9.8 bits of ENOB), such degradation may be mainly caused by the sampling aperture jitter. Besides, the static performance is assessed using the histogram method. As shown in Fig. 8, with off-chip calibration, the peak DNL is found to be +0.78/-0.80, and the INL level varies from +1.27 to -1.12.

Fig. 9 presents the total power consumption of the SAR ADC, along with a detailed breakdown of the power contribution from each component. The proposed design exhibits a total power consumption of 860 μW, with the SAR logic accounting for the largest portion of power consumption. Thanks to the gain-boosting technique, the dynamic comparator consumes 31% of the total power. Furthermore, benefiting from the low parasitic layout implementation and appropriate placement, the CDAC consumes 23% of the total power.

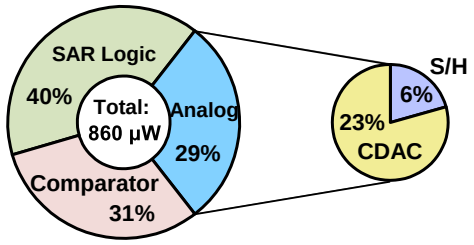

Fig. 9. Power breakdown of main components in the proposed SAR ADC.

Finally, Table II provides a comparison of the overall performance of our 12-bit asynchronous SAR ADC with other reported data. Despite employing a basic SAR architecture, the proposed design demonstrates comparable dynamic performance and power consumption.

V. Conclusion

In conclusion, we present an asynchronous SAR ADC that integrates a gain-boosting dynamic comparator and low-delay SAR logic. The modified pre-amplifier in the dynamic comparator allows for a higher gain compared to conventional designs, resulting in improved energy efficiency and noise performance. Additionally, the low-delay SAR logic ensures sufficient time for CDAC settling. The prototype of this design was fabricated using 28-nm CMOS technology and occupies an area of 0.021 mm^2. Under the Nyquist sampling condition, the ADC consumes 860 μW while achieving an SNDR of 60.9 dB and an SFDR of 77.2 dB. This performance corresponds to a Walden figure of merit (FoM_W) at 11.7 fJ/conversion-step. The gain-boosting comparator and low delay SAR logic can be utilized as a basic building block in other ADC architectures, replacing the traditional two-stage comparator and thereby enhancing their overall performance.

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TABLE II: Performance Comparison

	[5]	[6]	[7]	This work
Architecture	SubR.-SAR	Pipe.-SAR	Pipe.-SAR	SAR
Technology [nm]	65	65	65	28
Area [mm^2]	0.053	0.049	0.198	0.021
Supply voltage [V]	1.2	0.85	1.2	1.0/1.2[1]
Resolution [bit]	12	12	12	12
F_S [MS/s]	100	50	100	75
Power [μW]	1900	460	1900	860
SFDR [dB]	77	-	78.5	77.2
SNDR [dB]	60.7	65	65.7	60.9
ENOB [bit]	9.8	10.5	10.6	9.8
FoM_W [fJ/c-s][2]	21.3	6.3	12.1	12.7

[1] Digital/analog supply
[2] $FoM_W = P/(2^{ENOB} \times F_S)$

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