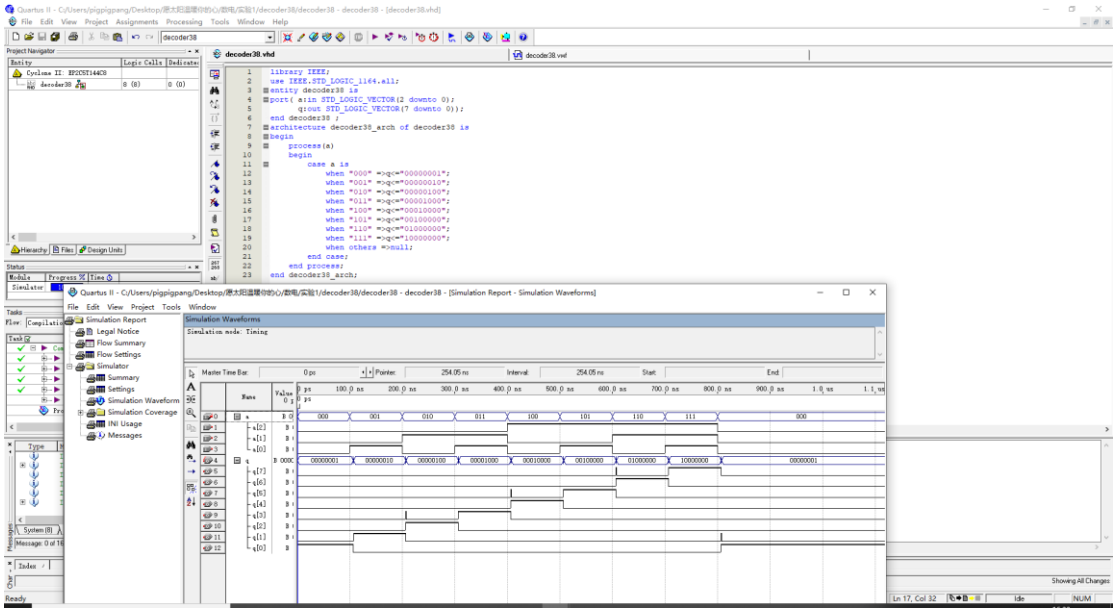
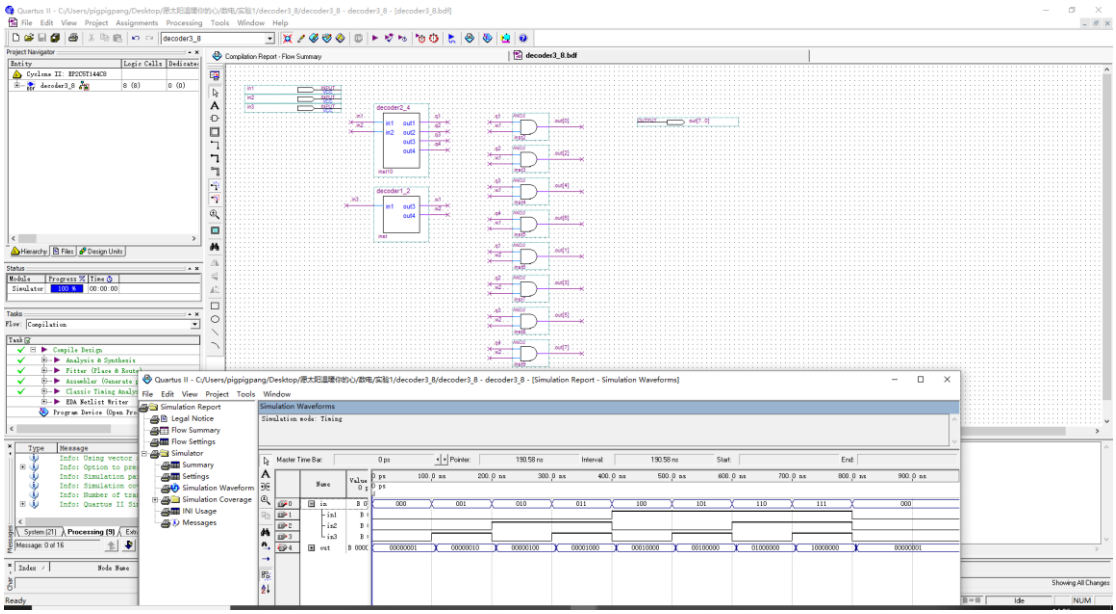
1.

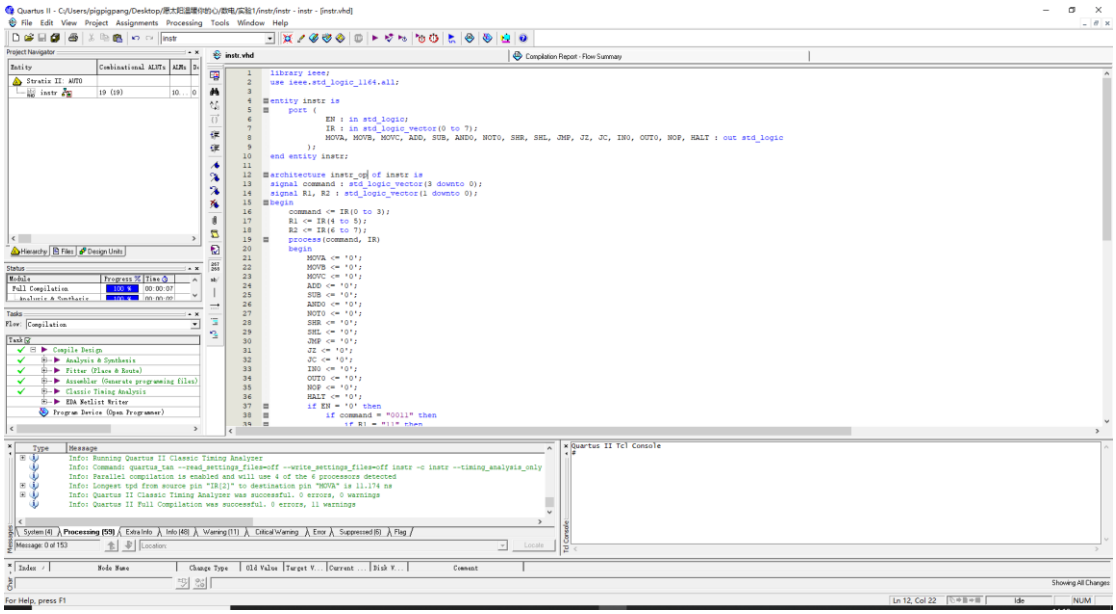
3-8 译码器的 VHDL 语言实现



3-8 译码器的原理图实现



2. 模型机指令译码器的 VHDL 程序


Quartus II - C:/Users/pigpigpang/Desktop/硬大粑是哪你的心/数电/实验1/instr/instr - instr - [instr.vhd]
File Edit View Project Assignments Processing Tools Window Help
instr.vhd
Compilation Report - Flow Summary
library ieee;
use ieee.std_logic_1164.all;
entity instr is
port (
EN : in std_logic;
IR : in std_logic_vector(0 to 7);
MOVA, MOVB, MOVC, ADD, SUB, ANDO, NOTO, SHR, SHL, JMP, JZ, JC, INO, OUTO, NOP, HALT : out std_logic
);
end entity instr;
architecture instr_op of instr is
signal command : std_logic_vector(3 downto 0);
signal R1, R2 : std_logic_vector(1 downto 0);
begin
command <= IR(0 to 3);
R1 <= IR(4 to 5);
R2 <= IR(6 to 7);
process(command, IR)
begin
MOVA <= '0';
MOVB <= '0';
MOVC <= '0';
ADD <= '0';
SUB <= '0';
ANDO <= '0';
NOTO <= '0';
SHR <= '0';
SHL <= '0';
JMP <= '0';
JZ <= '0';
JC <= '0';
INO <= '0';
OUTO <= '0';
NOP <= '0';
HALT <= '0';
if EN = '0' then
if command = "0011" then
Info: Running Quartus II Classic Timing Analyzer
Info: Command: quartus_tan --read_settings_files=off --write_settings_files=off instr -c instr --timing_analysis_only
Info: Parallel compilation is enabled and will use 4 of the 6 processors detected
Info: Longest tpd from source pin "IR[2]" to destination pin "MOVA" is 11.174 ns
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 0 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 11 warnings
Quartus II Tcl Console
For Help, press F1