CHAPTER 7

7-1.*

a) $A = 16, D = 8$ b) $A = 19, D = 32$ c) $A = 26, D = 64$ d) $A = 31, D = 1$

7-2.

a) $(835)_{10} = (11\ 0100\ 0011)_2$, $(15, 103)_{10} = (0011\ 1010\ 1111\ 1111)_2$

b) $(513)_{10} = (10\ 0000\ 0001)_2$, $(44{,}252)_{10} = (1010\ 1100\ 1101\ 1100)_2$

7-3.*

Number of bits in array = $= 2^{16} \times 2^4 = 2^{20} = 2^{10} * 2^{10}$

Row Decoder size = 2^{10}

a) Row Decoder = 10 to 1024, AND gates $= 2^{10} = 1024$ (assumes 1 level of gates with 10 inputs/gate)

Column Decoder = 6 to 64, AND gates = $2^6 = 64$ (assumes 1 level of gates with 6 inputs/gate)

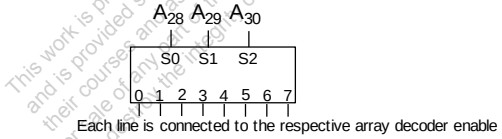
Total AND gates required = 1024 + 64 =1088

b) $(32000)_{10} = (0111110100\ 000000)_2$, $\text{Row} = 500$, $\text{Column} = 0$

7-4.

a) Number of RAM cell arrays $= 8$ $(2G = 2^{31}) / (2^{14} \times 2^{14} = 2^{28}) = (2^3 = 8)$

b)



7-5.

15 row pins + 14 column pins $= 2^{29} = 512$ M addresses

7-6.

With 4-bit data, the RAM cell array contains $2^{32}/2^2 = 2^{30}$ words.
The number of address pins is 30/2 = 15.

7-7.

Interval between refreshes = 64ms/8192 = 7.8125 μs

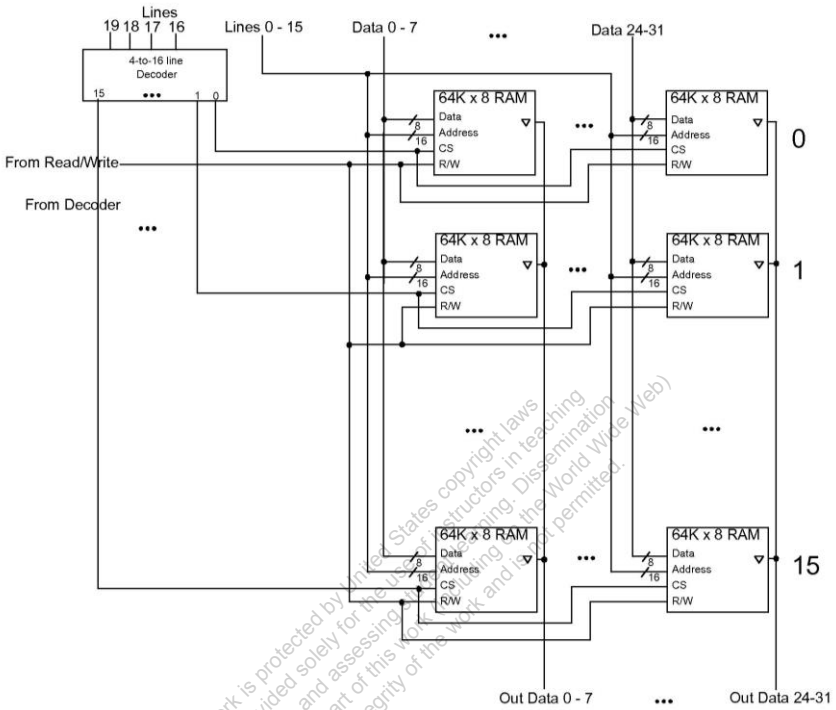
Using the 60 ns refresh time from the text example, total time for refresh = 8192 × 60 ns = 0.49 ms
Minimum number of pins = 13

7-8.*

a) 2 MB/128 K × 16 = 2MB/ 256 KB = 8 b) With 2 byte/word, $2MB/2\ B = 2^{20}$, Add Bits = 20

128K addresses per chip implies 17 address bits. c) 3 address lines to decoder, decoder is 3-to-8-line

7-9.



7-10.

An SDRAM simultaneously reads the desired row and stores all of the information in the I/O logic. Next the desired column is read from the I/O logic and the data appears on the output. During burst transfers, the subsequent data words are read from the I/O logic and placed on the output. This occurs for the predetermined number of words known as the burst length. For burst transfers, this is faster since the row has already been pre-read.

7-11.

A DDR SDRAM uses both the positive and negative edges of the clock to transfer data. This allows the DRAM to transfer twice as much data while keeping the same clock frequency.