CHAPTER 11

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11-1*

Heads × (cylinders/Head) × (sectors/cylinder) × (1 cylinder/track) × (bytes/sector)

a) 1 × 1023 × 63 × 512 = 32,224.5 Kbytes (K = 1024)
b) 4 × 8191 × 63 × 512 = 1,032,066 Kbytes
c) 16 × 16383 × 63 × 512 = 8,257,032 Kbytes

11-2.

8.5 msec + 4.17 msec + 0 msec + ((1 sec/(100 Mbytes)) × 1Mbytes)=22.67 ms

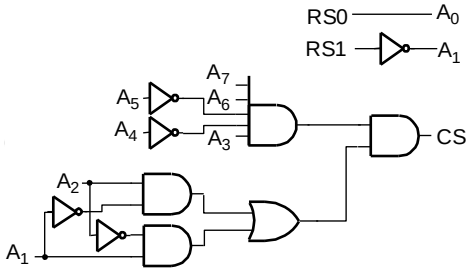
11-3.

	Pixels	Subpixels
a)	1,310,720	3,932,160
b)	1,920,000	5,770,000
c)	1,764,000	5,292,000
d)	2,304,000	6,912,000

11-4.

$(CA)_{16} = (1100\ 1010)_2$ RS1 = 1 RS0 = 0
$(CB)_{16} = (1100\ 1011)_2$ RS1 = 1 RS0 = 1
$(CC)_{16} = (1100\ 1100)_2$ RS1 = 0 RS0 = 0
$(CD)_{16} = (1100\ 1101)_2$ RS1 = 0 RS1 = 1

$RS0 = A_0,\ RS1 = \overline{A}_1,\quad CS = A_7A_6\overline{A}_5\overline{A}_4A_3(A_2\overline{A}_1 + \overline{A}_2A_1)$



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11-5.*

a) If each address line is used for a different CS input, there will be no way to address the four registers so 2 bits are needed to address the registers. Only 14 lines can be used for CS inputs permitting at most 14 I/O Interface Units to be supported.
b) Since two bits must be used to address the four registers, there are 14 bits remaining and 2^{14} or 16,384 distinct I/O Interface Units can be supported.

11-6.

#	Port A ADRS	Port B ADRS	Control ADRS	Status ADRS
1	0000 0001	0100 0001	1000 0001	1100 0001
2	0000 0010	0100 0010	1000 0010	1100 0010
3	0000 0100	0100 0100	1000 0100	1100 0100
4	0000 1000	0100 1000	1000 1000	1100 1000
5	0001 0000	0101 0000	1001 0000	1101 0000
6	0010 0000	0110 0000	1010 0000	1110 0000

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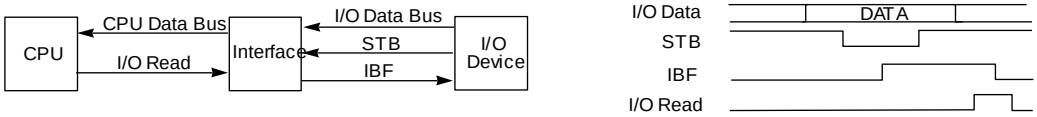
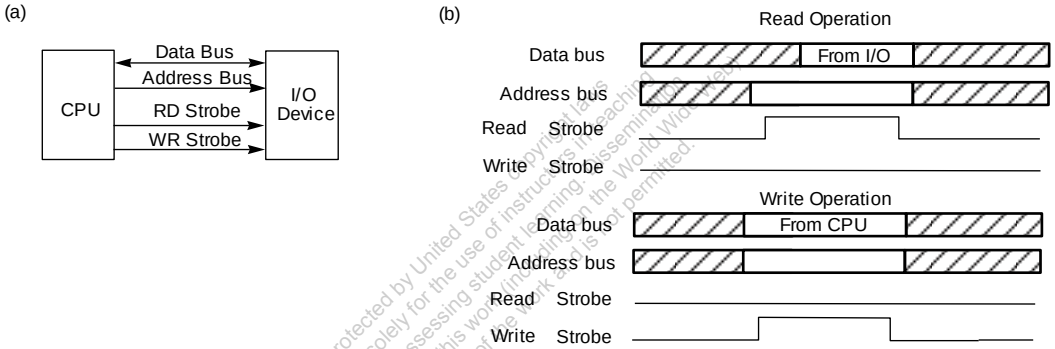
11-7.*

A given address can be shared by two registers if one is write only and one is read only. If a register is both written to and read from the bus, then it needs its own address. An 8-bit address provides 256 addresses. Suppose that the 50 % of registers requiring 1 address is X. Then the remaining 50 % of the registers, also X can share addresses requiring only 0.5 addresses. So 1.5 X = 256 and X = 170.67 registers for a total of 341.33 registers. To meet the original constraints exactly, the total number of registers must be divisible by 4, so 340 registers can be used, 170 of which are read/write, 85 of which are read only and 85 of which are write only. There is one more address available for either one read/write register or up to a pair with a read only register and a write only register.

11-8.



11-9.*



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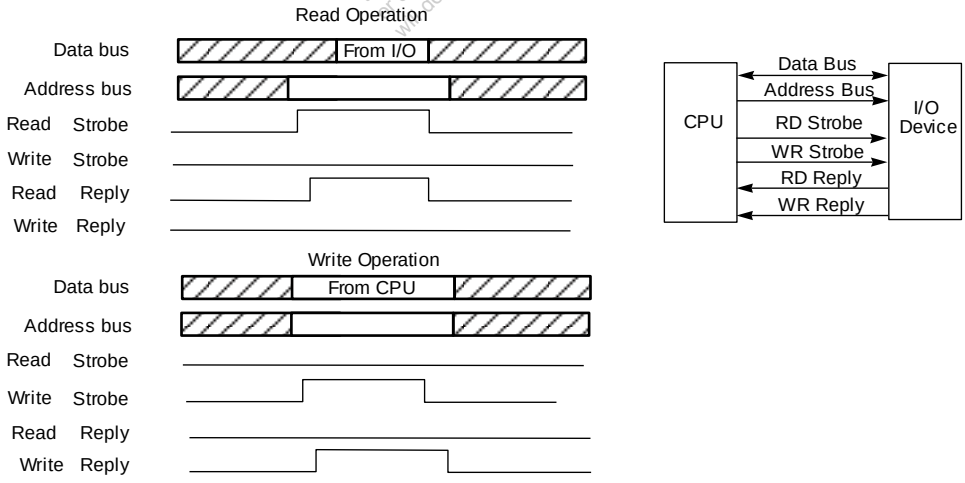
11-10.



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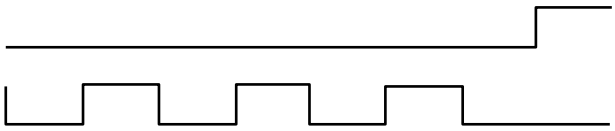
11-11.*



There are 7 edges in the NRZI waveform for the SYNC pattern that can be used for synchronization.

11-12.

(a) **0 1 1 1 1 1 1 1 0 0 1 0 0 0 0 0 0 0 0 1 1 0 1 1 1 0 0 0 0 0 1 1**

(b) **0 1 1 1 1 1 1 0 1 0 0 1 0 0 0 0 0 0 0 0 1 1 0 1 1 1 0 0 0 0 0 1 1**

(c)

11-13.*

SYNC 8 bits	Type 4 bits 1001	Check 4 bits 0110	Device Address 0100111	Endpoint Address 0010	CRC	EOP

(a) Output packet

SYNC 8 bits	Type 4 bits 1100	Check 4 bits 0011	Data 0100001010011101010011 0	CRC	EOP

(b) Data packet (Data0 type) (bits LSB first)

SYNC 8 bits	Type 4 bits 0111	Check 4 bits 1000	EOP

(c) Handshake packet (Stall type)

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11-14.

SYNC 8 bits	Type 4 bits 1001	Check 4 bits 0110	Device Address 0100111	Endpoint Address 0010	CRC	EOP

(a) Output packet

SYNC 8 bits	Type 4 bits 1100	Check 4 bits 0011	Data 1111011000110110000010010	CRC	EOP

(b) Data packet (Data0 type) (bits LSB first)

SYNC 8 bits	Type 4 bits 0101	Check 4 bits 1010	EOP

(c) Handshake packet (Stall type)

11-15.

Interrupt-initiated data transfer permits the action required by an interrupt to occur anywhere within the programs executing without specifically including code in those programs to sense the need for the action. This makes actions necessary in response to an interrupt invisible to the typical user program. In contrast, if the interrupt is not used, there would need to be code within unrelated programs that supports the same necessary actions.

11-16.*

Description	Device 0				Device 1				Device 2			
	PI	PO	RF	VAD	PI	PO	RF	VAD	PI	PO	RF	VAD
Initially	0	0	0	-	0	0	0	-	0	0	1	-
Before CPU acknowledges Device 2	0	0	1	-	0	0	0	-	0	0	1	-
After CPU sends acknowledge	1	0	1	0	0	0	0	-	0	0	1	-

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11-17.

The interrupt service routine polls the devices connected to the common interrupt line. The first device checked has the highest priority. The priority of the other devices corresponds to when they are checked.

11-18.*

Replace the six leading 0's with 000110.

11-19.

Fill in the VAD vector (top to bottom) as A_0, $\overline{A}_1$, $A\overline{1}$, 1, 1, 1, 1, 1, 0.

11-20.*

This is Figure 13-17 with the Interrupt and Mask Registers increased to 6 bits each, and the 4 × 2 Priority Encoder replaced by a 8 × 3 Priority Encoder. Additionally, VAD must accept a 3rd bit from the Priority Encoder.

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11-21.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A4	A3	A2	A1	V	1	0	W	X	Y	Z	0	1
1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1	1	1	1	1	0	1	1	1	1	0	1
0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1	1	0	1	1	0	1	1	1	0	0	1
0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1	0	1	1	1	0	1	1	0	1	0	1
0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	1	1	0	0	1	1	0	1	1	0	0	0	1
0	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	1	0	1	1	1	1	0	1	0	1	1	0	1
0	0	0	0	0	1	x	x	x	x	x	x	x	x	x	x	1	0	1	0	1	1	0	1	0	1	0	0	1
0	0	0	0	0	0	1	x	x	x	x	x	x	x	x	x	1	0	0	1	1	1	0	1	0	0	1	0	1
0	0	0	0	0	0	0	1	x	x	x	x	x	x	x	x	1	0	0	0	1	1	0	1	0	0	0	0	1
0	0	0	0	0	0	0	0	1	x	x	x	x	x	x	x	0	1	1	1	1	1	0	0	1	1	1	0	1
0	0	0	0	0	0	0	0	0	1	x	x	x	x	x	x	0	1	1	0	1	1	0	0	1	1	0	0	1
0	0	0	0	0	0	0	0	0	0	1	x	x	x	x	x	0	1	0	1	1	1	0	0	1	0	1	0	1
0	0	0	0	0	0	0	0	0	0	0	1	x	x	x	x	0	1	0	0	1	1	0	0	1	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	1	x	x	x	0	0	1	1	1	1	0	0	0	1	1	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	x	x	0	0	1	0	1	1	0	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	x	0	0	0	1	1	1	0	0	0	0	1	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x	0	-	-	-	-	-	-	-	-

11-22.*

When the CPU communicates with the DMA, the read and write lines are used as DMA inputs. When the DMA communicates with the Memory, these lines are used as outputs from the DMA.

11-23.

a) CPU initiates DMA by transferring the following:
   2048 to the word count register.
   4096 to the DMA address register.

b) 1) I/O Device sends the DMA controller a "DMA request."
   2) DMA sends BR (Bus Request) to CPU.
   3) CPU responds with BG (Bus Grant).
   4) Contents of DMA address register are placed on the address bus:
      DMA sends "DMA acknowledge" to I/O device.
      Address 4096 + (2048 – WCR) on address bus.
      DMA enables the Write control to Memory.
      Data word is placed on the data bus by I/O device.
      Decrement WCR.
   5) If DMA receives a "DMA request" from I/O device, it repeats Step 4, otherwise it disables the BR line to CPU.

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