## Sheet1

P1	P2	P3	P4
	HALT		
(PC)→アドレス・バン・PC++ ・データ・バス→IR		·BR+AR →DR1 set SZVC	
		·BR-AR →DR1 set SZVC	
		·BR&AR →DR1 set SZVC	
		·BR AR →DR1 set SZVC	
		·BR^AR →DR1 set SZVC	
		·set SZVC	
		·BR →DR1 set SZVC	
		·BR→DR1, AR→DR2	
	•r[Rd]→BR	·BR + I → DR1 set SZCV	
		·BR - I → DR1 set SZCV	
		$tate(BR, d) \rightarrow DR1$	
		$tate(BR, d) \rightarrow DR1$	
		·shift_right_lo gical(BR, d) → DR1	
		·shift_right_arithmetic(BR, d) $\rightarrow$ DR1	
			IN → M[
			AR → OUTPUT
		DD - 1 - 1/1 - DD1	DR1 → reg
	$r[Ra] \rightarrow AR, r[Rb] \rightarrow BR$	BR + sign_ext(d) → DR1	・DR1 → アドレスパス・AR -
		$sign_ext(d) \rightarrow DR1$	DR1 → reg
		$PC + sign_ext(d) \rightarrow DR1$	
	(PC)→アドレス・バ.	・r[Rd]→B, Rr[Rs] → AR  (PC)→アドレス・バラー・PC++ ・データ・バス→IR  ・r[Rd]→BR	HALT

## Sheet1

P5
DR1 → reg
DR1, DR2 → reg
DR1 → reg
DR → reg
_
→ データパス
DR1 → PC
$if(Z) \rightarrow DR1 \rightarrow PC$
$if(S^Z) \rightarrow DR1 \rightarrow PC$
$if(Z \parallel (S \land V)) \rightarrow DR1 \rightarrow PC$
$if(!Z) \rightarrow DR1 \rightarrow PC$