Unit 10

Analysis and design Common-Source amplifiers with simple current source loads

Analysis of CS gain stages:

Estimate Rout, Av, range of Vout for given circuit parameters

1. n-MOSFET CS gain stage

Impact of p-MOSFET current source gate length on voltage gain

2. p-MOSFET CS gain stage

Design of CS gain stages:

Estimate circuit parameters (Id, W, L, Vgs for both MOSFETs) for specified Rout, Av, Vout range

Summary of (most important) process and design parameters

Process parameters	Design parameters

Process parameters

1. Threshold voltages

$V_{tn} = 0.7$ V, $V_{tp} = -0.8$ V

2. Process transconductance parameters

$k_n' = 200$ uA/V^2 , $k_p' = 70$ uA/V^2

3. Early voltage parameters

$V_{An}' = 20$ V/um, $V_{Ap}' = 10$ V/um
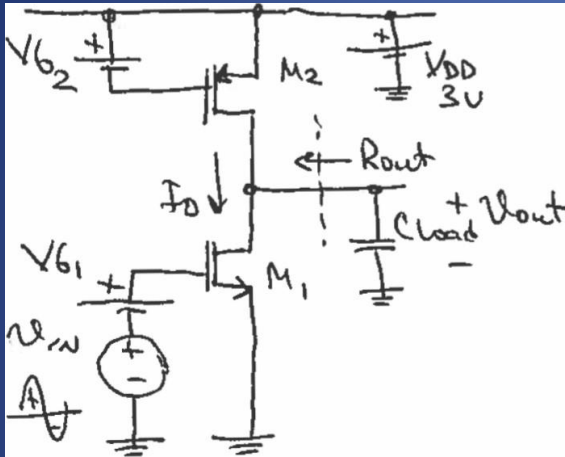
Design parameters

V_{GS_nmos}, V_{GS_pmos}

DC bias current: I_D

Gate lengths: L_n, L_p

Gate widths: W_n, W_p

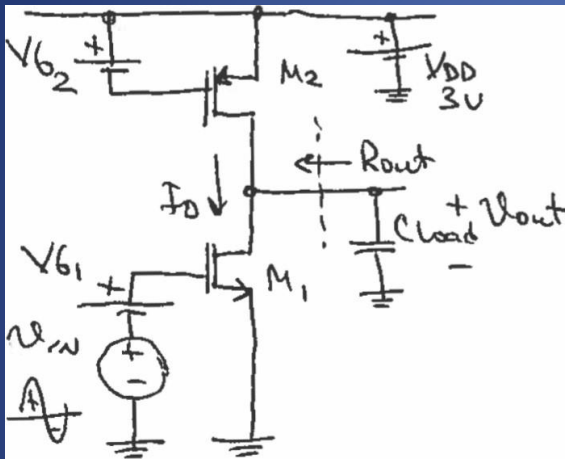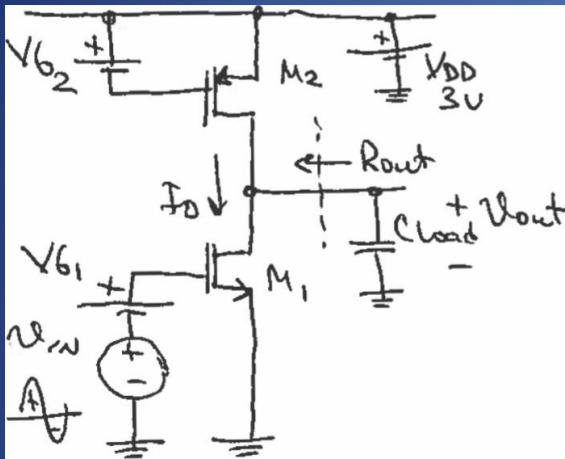# Analysis of n-MOS common-source stage ($r_o = r_{on}$) => ($L_p = 2L_n$)

nMOS common-source stage ($r_o = r_{on}$) => ($L_p = 2L_n$)
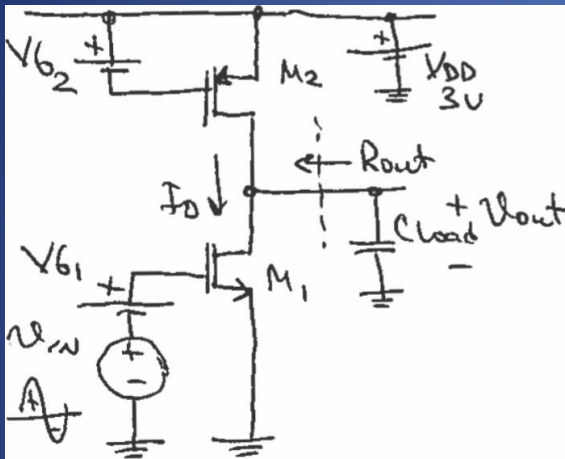
nMOS common-source stage
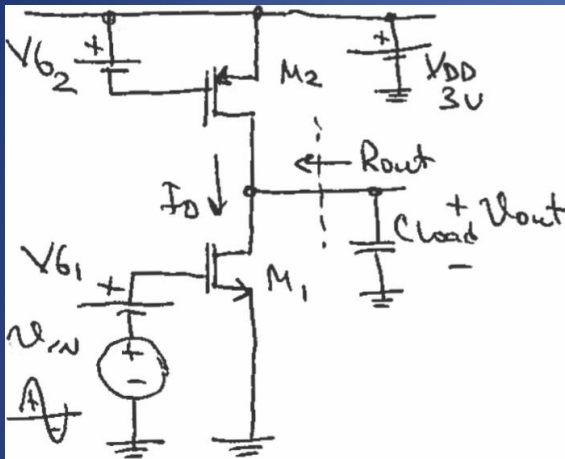## $r_{op} = r_{on}$

nMOS common-source stage
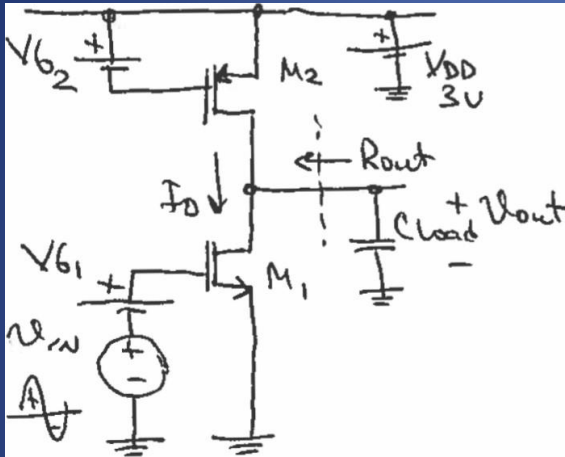## $L_p = 4L_n$

nMOS common-source stage
$L_p = L_n$

Analysis of p-MOS common-source stage

p-MOS common-source stage

Design of n-MOS common-source stage $(r_o = r_{on}) \Rightarrow (L_p = 2L_n)$

n-MOS common-source stage
$(r_o = r_{on}) => (L_p = 2L_n)$