

## EEO311 Simulation assignment 4

### Unity gain stable 2-stage Operational Amplifier

#### 1. Objectives

- Design of the 2-stage Op Amp with frequency compensation with required specification on slew rate, DC voltage gain and phase margin for operation as a buffer.
- Simulation of the transient response of the OpAmp in the buffer configuration, determination of the slew rate and overshoot.

#### 2. Description

The Opamp is intended for operation with negative feedback as the buffer (voltage gain with feedback  $A_f = 1$ ) driving a capacitive load. OpAmps of this kind find applications as a front-end buffer in IC operating with signals sources with high impedance, Analog to Digital Converters (ADC), switched capacitor filters, etc. The Opamp has to be stable with negative feedback. The unity gain configuration would be the most challenging from the point of view of stability (no oscillations seen at the output). The transient response to a step input voltage should be accurate with a small overshoot: operating as a buffer, the OpAmp output voltage has to follow the input signal with specified accuracy. A realistic transient response of the buffer would show the output waveform deviating from the input square-wave in two aspects:

- After an abrupt change of input voltage (step) the output would exhibit a linear rise with a finite slew rate ( $SR = dV_{out}/dt = I_{out}/C$ ) due to limited MOSFET bias currents charging capacitances
- After reaching the input voltage, the output voltage would continue to increase exhibiting an overshoot and decaying oscillations to a nominal voltage (ringing) due to a delayed response with large negative phase angle. Ringing occurs when phase shift at unity gain frequency in the feedback path approaches 180 deg, phase margin ( $PM = 180 - |\phi|$ ) approaches zero and the feedback becomes close to positive. A small overshoot without ringing is obtained with sufficiently high  $PM > 60$  deg. Here  $|\phi|$  is an absolute value of the phase difference between output and input sinusoidal voltages. Since an amplifier presents a low pass filter with negative phase angle, the phase margin can be found as  $PM = 180 + \phi$ .

The OpAmp circuit includes two stages with the schematic shown in Figure 1. The common-source (CS) PMOS differential stage loaded with NMOS current mirror for high gain with single-ended (SE) output  $V_{o1}$  is followed by the CS NMOS second stage with output  $V_{out}$  driving  $C_L = 5$  pF load.

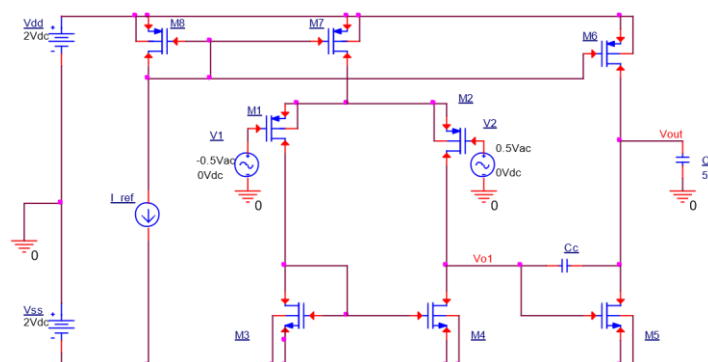


Figure 1. The OpAmp schematic with a 1 V AC differential input voltage source. The output voltage represents an open loop differential gain.

In the open loop configuration (no feedback) the OpAmp should meet the following specifications:

**1. Output voltage DC offset  $|V_{out}| < 0.5 \text{ V DC}$  with zero input voltages**

With differential inputs V1, V2 shorted to ground the output voltage ideally should be close to 0 V DC.

**2. Differential DC voltage gain  $> 70 \text{ dB}$**

**3. Slew rate in  $\text{V}/\mu\text{s} \geq (100 + \text{the last 2 non-zero digits of your ID number})/5$**

The SR would be in the range of 20 - 40  $\text{V}/\mu\text{s}$  depending on your ID digits.

**4. Phase margin  $> 60 \text{ deg}$  at unity gain frequency.**

This implies that the differential gain frequency response shows a single pole with a slope of -20 dB/dec all the way up to unity gain frequency and the second pole placed beyond the unity gain frequency. The later is realized with frequency response compensation.

Preferences should be given to sets of circuit parameters (bias currents, MOSFET dimensions, frequency response compensation capacitance and resistance) to provide the greatest gain-bandwidth product at the minimal DC current to meet the specs on the slew rate. The minimum gate length is 0.5  $\mu\text{m}$ . The OpAmp is powered from a bipolar voltage source with  $V_{DD}=+2 \text{ V}$ ,  $V_{SS}=-2 \text{ V}$ .

### 3. Design considerations

The specified PM of 60 degrees is obtained when the OpAmp transfer function for the differential gain (no feedback) is dominated by a single-pole response with the 1<sup>st</sup> pole frequency  $f_{p1} = \text{BW}$  in the frequency range beyond unity gain frequency  $f_t$  by at least an octave, the 2<sup>nd</sup> pole frequency  $f_{p2}$  is placed higher than  $f_t$  by a factor of  $> 2.2$  by frequency compensation. The compensation is obtained by loading the 1<sup>st</sup> stage with a large capacitance so that  $f_{p1}$  is formed by output resistance of the 1<sup>st</sup> stage ( $R_1$ ) and the large capacitance. The required large capacitance is realized with a reasonably small Miller capacitor  $C_c$  magnified by the voltage gain of the 2<sup>nd</sup> stage ( $g_{m5}R_{out}$ ). Here  $g_{m5}$  is the transconductance of NMOSFET in the 2<sup>nd</sup> stage. Connection of  $C_c$  between the gate and drain terminals of M5 in the 2<sup>nd</sup> stage results in pole splitting:  $f_{p1}$  is moved to a low enough frequency with a reasonably sized  $C_c$ ,  $f_{p2}$  is moved to high enough frequency. As a byproduct of using  $C_c$  there is undesirable decrease of zero frequency  $f_z$ . The transfer function of the 2-stage OpAmp in Figure 1 can be approximated with 2 negative poles on real axis on s-plane ( $s=-f_{p1}$ ,  $s=-f_{p2}$ ) and a positive zero on real axis ( $s=+f_z$ ) as shown below

$$A(s) = \frac{g_{m1} R_1 g_{m5} R_{out} \left(1 - \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \left(1 + \frac{s}{\omega_{p2}}\right)} \quad (1)$$

It is given as a function of complex variable  $s = \sigma + j\omega$ . On s-plane the negative and positive frequencies are located in the left half plane (LHP) and the right half plane (RHP), respectively. For sinwave signals  $s = j\omega$ . The frequency response of the differential gain is dominated by a single-pole behavior with the pole at  $f_{p1}$  and the slope of -20 dB/decade in a whole frequency range beyond unity gain frequency  $f_t$ . Thus, the later is the same as the GBW product. The positions of the 2<sup>nd</sup> pole  $f_{p2}$  and zero  $f_z$  are important because of the critical contribution to the phase angle at  $f_t$  and the phase margin PM, respectively. The frequencies of poles, zero and unity gain can be estimated from transconductances  $g_{m1}$  and  $g_{m5}$ , output resistances  $R_1$  and  $R_{out}$ , capacitances  $C_1$  and  $C_L$  at the outputs of the 1<sup>st</sup> and the 2<sup>nd</sup> stages, respectively and Miller capacitance  $C_c$  with the following expressions

$$f_{p1} = \frac{1}{2\pi R_1 (C_1 + C_c g_{m5} R_{out})}; \quad f_{p2} = \frac{g_{m5}}{2\pi (C_1 + C_L)}; \quad f_z = \frac{g_{m5}}{2\pi C_c}; \quad \text{GBW} = f_t = \frac{g_{m1}}{2\pi C_c} \quad (2)$$

Ignoring effects of zero  $f_z$ , a single-pole response with a PM  $\geq 60$  degrees implies that  $f_{p2} \geq 2.2 f_t$  and  $C_C \geq 0.22 C_L$  which requires  $g_{m5} \geq 2.2 g_{m1} C_L / C_C \approx 10 g_{m1}$ . The challenge to meet required PM with large  $C_C$  is due to reduction of  $f_z$  to a point when its contribution to the negative phase angle becomes essential. The latter makes it ineffective to increase the phase margin by  $C_C$  alone. A negative PM at  $f_t$  can be often seen which means the phase angle is  $> 180$  degrees at  $f_t$ . It would be absolutely unacceptable for OpAmp application as a buffer with the voltage gain of 1 as it would turn the feedback into positive resulting in circuit instability and oscillations of output voltage without presence of input signal. A small positive phase margin ( $|\phi| < 180$  deg) would be insufficient as well, it will result in a large overshoot (ringing) at the output in response to a square-wave input applied to the buffer. The simplest solution to obtain the required phase margin is to push  $f_z$  to higher frequencies by including resistor  $R_C$  in series with  $C_C$ . The frequency of zero  $f_z$  is moved to infinity with  $R_C = 1/g_{m5}$  as follows from the expression

$$\omega_z = \frac{1}{\left(\frac{1}{g_{m5}} - R_C\right)C_C}$$

$$R_C = \frac{1}{g_{m5}} \frac{C_L + C_C + C_1}{C_C}$$

Resistance  $R_C$  can be increased even further beyond  $1/g_{m5}$  which will make  $f_z$  very large and negative. Further increase of  $R_C$  will bring  $f_z$  down to  $f_{p2}$  which can result in the 2<sup>nd</sup> pole cancellation. This cancellation in theory can be realized if  $C_L$  is known. Also addition of  $R_C$  in series with  $C_C$  creates the 3<sup>rd</sup> pole  $f_{p3}$  at a very high frequency:  $f_{p3} = \frac{1}{2\pi C_1 R_C}$ . The phase angle contribution due to the 3<sup>rd</sup> pole should not create a problem meeting specs on phase margin.

The minimal required bias currents  $I_{bias} = I_7 = 2I_1$  and  $I_5$  for the 1<sup>st</sup> and the 2<sup>nd</sup> stages, respectively, are estimated from the specification on slew rate which can be limited by either the 1<sup>st</sup> or the 2<sup>nd</sup> stage. Often bias currents  $I_{bias} = I_7$  and  $I_5$  are selected from the requirements on slew rate SR

$$SR = \frac{dV_{out}}{dt} = \frac{I_{bias}}{C_C} = \frac{I_5}{C_L + C_C} \quad (3)$$

The transition frequency of NMOS devices M3, M4 should be at least an order of magnitude greater than  $f_t$  to neglect the effects of the pole and zero of the current mirror load on the PM. It is easier to obtain the response with a small phase angle with high enough overdrive voltages of NMOS and PMOS devices. These can be selected to be 0.2 V and 0.3 V, for NMOS and PMOS devices, respectively. One can see from the schematic that  $V_{gs6} = V_{gs7} = V_{gs8}$ , and therefore,  $V_{ov6} = V_{ov7} = V_{ov8}$ . However, it is possible that  $V_{gs5} = V_{ds4} \neq V_{gs3}$  and with incorrectly selected W scaling and large  $V_{ov4}$  one can realize M4 operating in the triode mode with  $V_{ds4} < V_{ov4}$ . In order to avoid the triode region and to have  $V_{gs5} = V_{ds4} = V_{gs3}$ , and  $V_{ov5} = V_{ov4} = V_{ov3}$ , respectively, the balance conditions have to be satisfied with the correct aspect ratio scaling:  $(W_5 L_4 / W_4 L_5) = 2(W_6 L_7 / W_7 L_6)$  because M7 is referenced to  $I_{bias} = I_7$  and  $I_4 = \frac{1}{2} I_{bias}$ . The resistance of PMOS M6 current source load can match that of NMOS M5 by doubling the gate length of M6 compared to M5. In order to obtain moderate widths of M6 and M5 one can select the minimal gate length for M7 since the common-mode gain was not specified. In estimations of output resistances assume Early voltage parameters of 20 V/ $\mu\text{m}$  and 10 V/ $\mu\text{m}$  for NMOS and PMOS devices, respectively.

#### 4. Assignment

1. Obtain the set of the circuit parameters to satisfy the specifications on the DC gain and the SR listed above. One can assume  $C_c = 1.1$  pF. Estimate  $W$  and  $L$  for each MOSFET for the DC gain of the 1<sup>st</sup> and the 2<sup>nd</sup> stages  $A_1$  and  $A_2$  to be in the range from 50 to 100 (+34 to 40 dB). Select the initial aspect ratios for the MOSFET in the 2<sup>nd</sup> stage to meet the balance condition. Adjust the width of NMOS or PMOS devices in the 2<sup>nd</sup> stage for the systematic DC offset at the output  $V_{out}$  to be smaller than  $\pm 0.5$  V DC. The DC gain  $A_D = A_1 A_2$  should be greater than 70 dB. Record MOSFET parameters, bias currents of the 1<sup>st</sup> and the 2<sup>nd</sup> stages, differential gain, bandwidth at -3 dB point, the output voltage DC offset. Make a table and keep the records of the above parameters for your design iterations for the report.
2. Simulate the frequency response of the open-loop differential gain without  $C_c$ : obtain the Bode plot, determine the PM at the unity gain frequency. Save the Bode plot for the initial design without frequency compensation for the final report.
3. Compensate the frequency response with minimal value  $C_c$  which results in required PM > 60 deg. If necessary, include resistor  $R_c$  in series with  $C_c$ . Simulate Bode plot with a gradual increase of  $C_c$ , determine unity gain frequency  $f_t$  and phase margin PM for each iteration. Vary  $R_c$  in a range: the suggested values of  $R_c$  are 1, 2, 4, 8 kOhm.

In the process of optimization of the frequency compensation, record the parameters in a table including PM,  $f_t = \text{GBW}$ , bandwidth at -3 dB frequency. For the final circuit save the Bode plot for the open loop differential gain to include into the report.

4. Obtain the transient response of the OpAmp with the best GBW product and compensated response for the PM > 60 deg in the buffer configuration with a square-wave input voltage with the amplitude of 0.5V. For the transient response analysis delete input AC sources  $V_1$ ,  $V_2$  in Figure 1, connect VPULSE to the noninverting input, connect the inverting input to  $V_{out}$  (or assign the same net alias to both of them), place voltage probe to  $V_{out}$ , select the transient analysis in the simulation profile.
5. Determine the slew rates and overshoot in % for rising and trailing edges of  $V_{out}$  from the transient response.

#### 5. Report.

The report should include

1. 2 copies of the schematic in the open loop configuration. One copy should show MOSFET dimensions with no bias currents and DC voltages, another copy should show DC operating points which can obscure MOSFET dimensions.
2. Calculations of bias currents, selected  $L$  and calculated  $W$  for each MOSFET, simulated Bode plots for the open loop differential gain with and without compensation, bandwidth ( $f_{p1}$ ), GBW product, phase margin at unity gain frequency, tables showing simulated parameters in design iterations.
3. The schematic for simulation of the transient response (the buffer), estimates of the slew rate and overshoot made from the simulated transient response.
4. A brief summary of the OpAmp parameters.