EEO352 Lab 4
Digital Gates

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October 15, 2023

Copy of Original Assignment

EEO 352 Fall 2023 - Assignment 4 – Digital Gates

Please document each step with snapshots of the built circuit, plots, pictures and your observations. Please include this page.

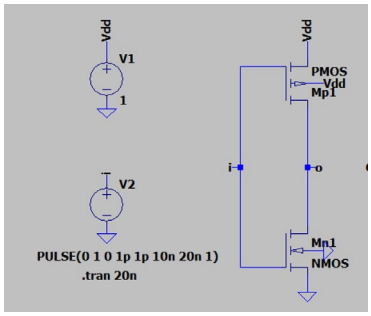

Fig.1a

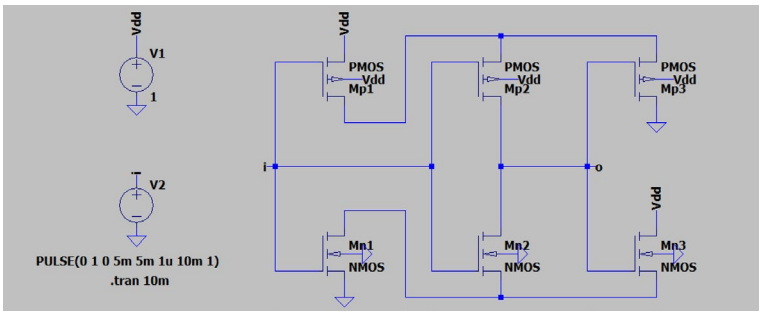

Fig.1b

1) Design and simulate as follows (**50pts**):

a) CMOS inverter, as shown in Fig.1a using the nmos4 and pmos4 ideal parts:
- using a pulse waveform simulate and plot the input and output
- using a 100Hz triangular waveform plot the input and output and extrapolate and report the threshold voltages at 50% of the output swing
- replace the ideal MOSFETs (right-click on the parts) with the Si7540DP-P/N, increase the voltages to 5V, plot the input and output, extrapolate the delays (1ns input edges) and extrapolate the thresholds (10Hz triangular waveform)

b) CMOS Schmitt trigger, as shown in Fig.1b using the nmos4 and pmos4 ideal parts:
- using a pulse waveform simulate and plot the input and output
- using a 100Hz triangular waveform plot the input and output and extrapolate and report the threshold voltages at 50% of the output swing

c) NAND and NOR gates using the nmos4 and pmos4 ideal parts:
- simulate and plot (use three plot panes) the inputs and output

d) XOR gate using four ideal NAND parts (inverted output of the AND part) in the Digital library:
- simulate and plot (use three plot panes) the inputs and output

e) XOR gate using four ideal NOR parts (inverted output of the OR part) and one inverter:
- simulate and plot (use three plot panes) the inputs and output

Note1: when using the Si7540DP please replace the nmos4 and pmos4 with nmos and pmos first; note that the bulk gets internally connected with the source.
Note2: the ideal parts in the Digital library nominally operate between 0V and 1V, the Si7510DP operate between 0V and 5V

2) Using the CD4007 CMOS array, build and measure (**115 pts**):

a) The circuit at (1a), measuring the delays and the threshold voltages and plotting the corresponding inputs and outputs

b) The circuit at (1b), measuring the delays and the threshold voltages and plotting the corresponding inputs and outputs

c) The two circuits at (1c), using one 1kHz 5V square wave and one 500Hz square wave, plotting the 500Hz input and the output

Note1: CD4007 requires supply and signal voltages as per datasheet, 5V recommended.

3) Using the 74LS00 NAND array, build and measure (**35 pts**):

a) The circuit at (1d), using one 2kHz 5V square wave and one 1kHz square wave, plotting the input and the output

1 Summary

In this lab we designed and tested several types of logic gates. In several cases we also modeled the behavior. Where we modeled the propagarion delay, we used fast rising signals. When modeling input voltages at the 50% point of the output voltage, we used sawtooth input signals.

To measure the input/output delay in Digilent Waveforms, I applied the needed input signals. Then, I used the built in "Midpoint" measurement on the output channel. I used this value to set a trigger on the rising, then falling output channel signal. This allowed me to to directly measure the delay by using the cursor time delta feature.

To measure the input voltage at the 50% point of the output signal, I used the same Midpoint value trigger method described above. Then, zooming in on the signal I was able to use the built in "Average" measure on the input channel to determine the voltage.

With respect to the circuits designed, we were not able to see the similarities or differences in the model behavior vs real-world measurements since none of models designed were based on the actual IC's used in the experiment. However, we were able to see real-world IC's do have propagation times that far exceed the idealized models behavior.Also, the Schmitt trigger produced signifigant asymmetry with respect to input voltage showing this type of circuit could be useful for cleaning up slow moving signals.

2 Design and Simulate

a)

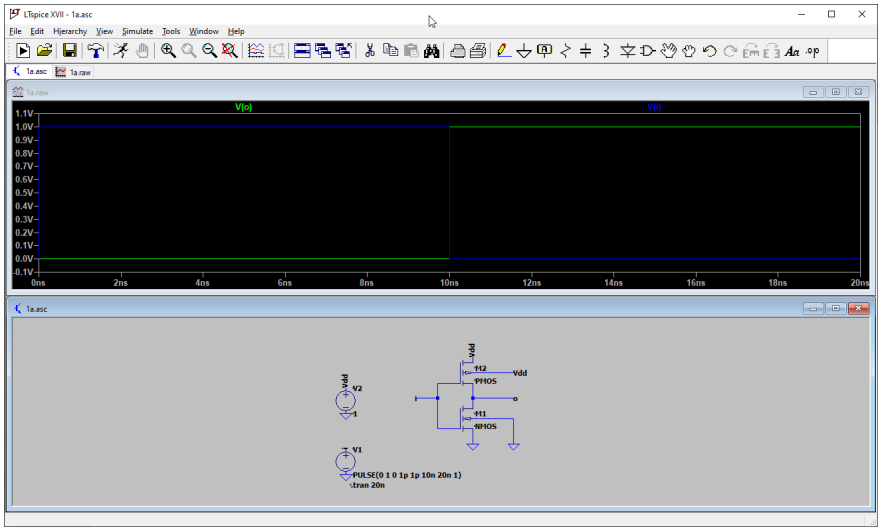

Figure 1: CMOS inverter model using idealized parts

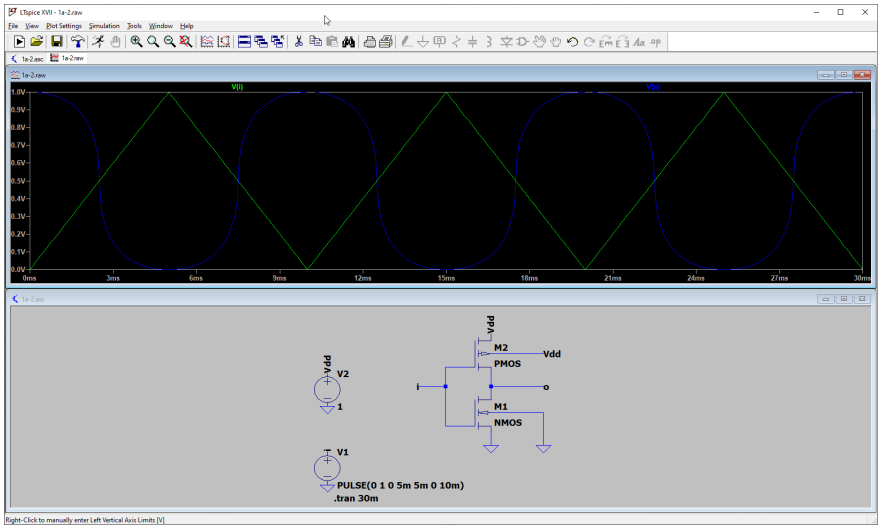

Figure 2: Overview of triangular input signal

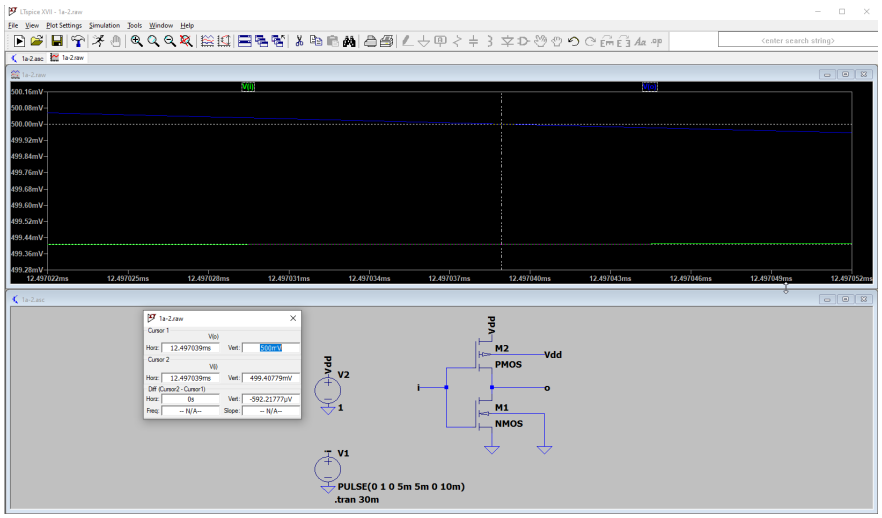

Figure 3: Measuring the rising input signal at 50% of the output swing with a 100 Hz triangular waveform input, the input voltage is 499.408 mV.

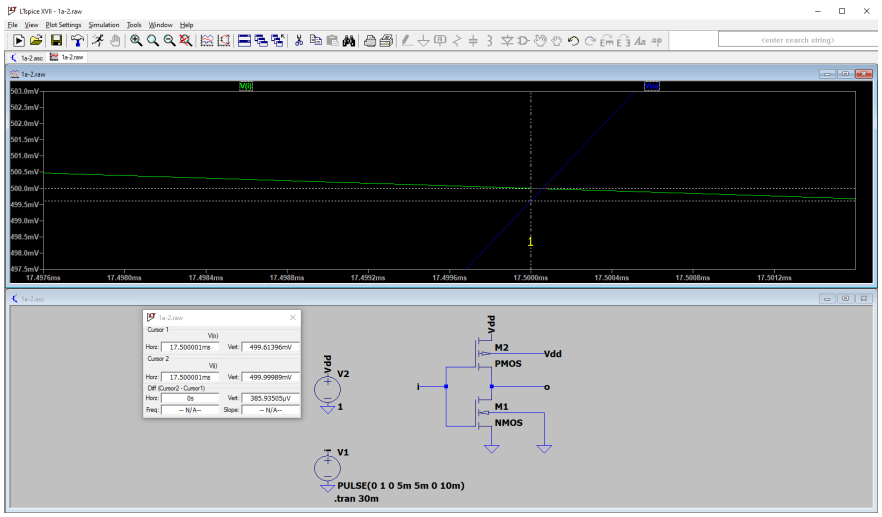

Figure 4: Measuring the falling input signal at 50% of the output swing with a 100 Hz triangular waveform input, the input voltage is 499.614 mV

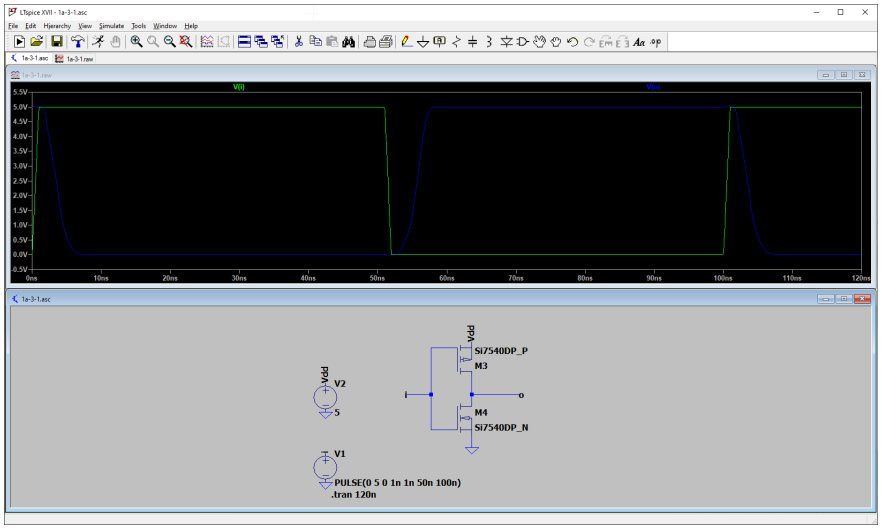

Figure 5: CMOS inverter model using Si7540DP parts

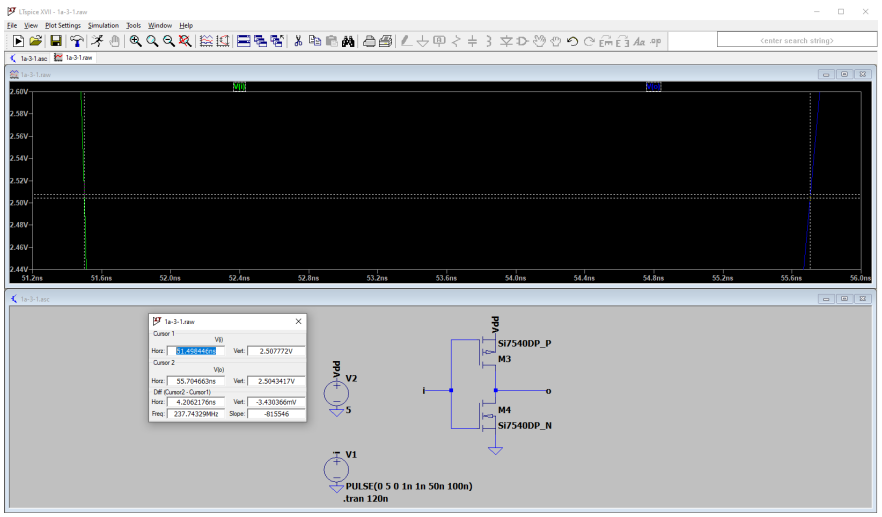

Figure 6: Measuring the time delay between the input signal and the output signal at 50% point, the rising output lags the falling input by 4.206 nS.

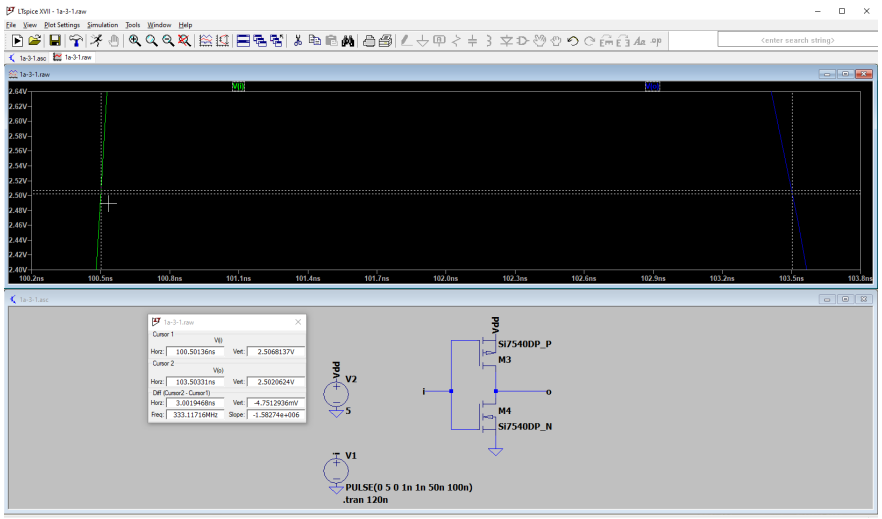

Figure 7: Measuring the time delay between the input signal and the output signal at 50% point, the falling output lags the rising input by 3.002 nS.

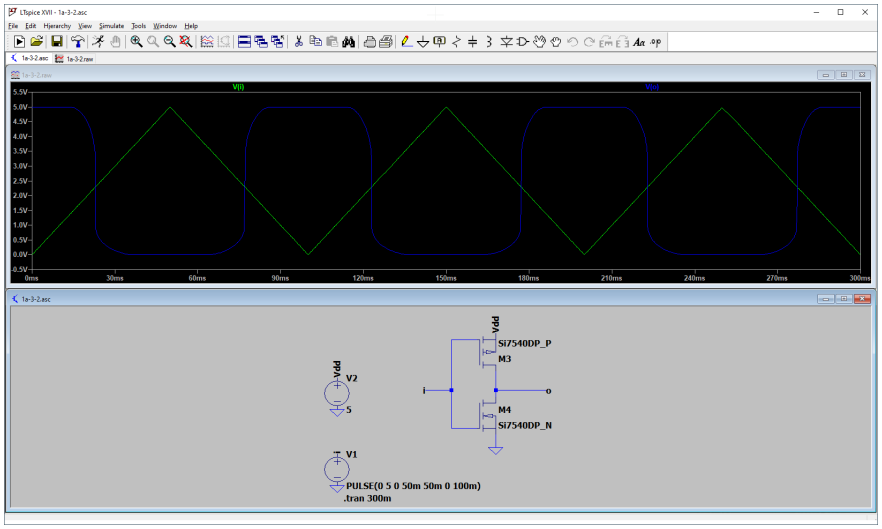

Figure 8: Overview of triangular input signal

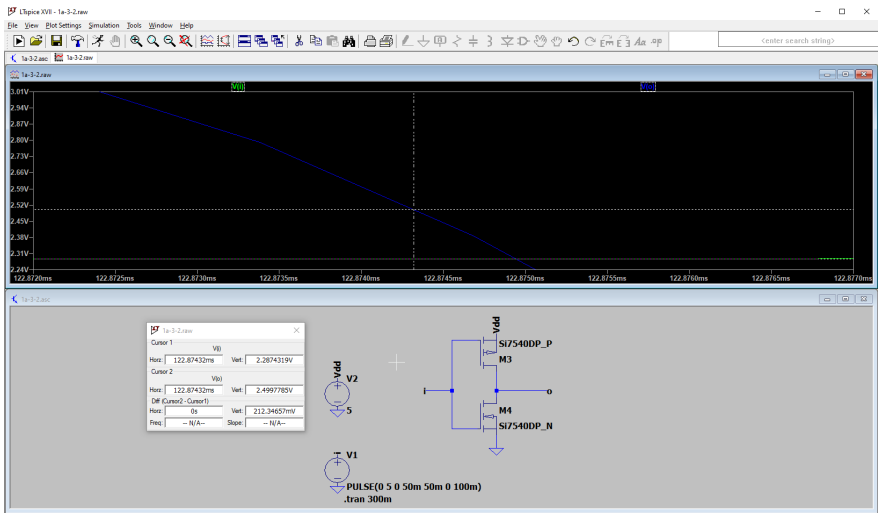

Figure 9: Measuring the rising input signal at 50% of the output swing with a 100 Hz triangular waveform input, the input voltage is 2.287 432 V.

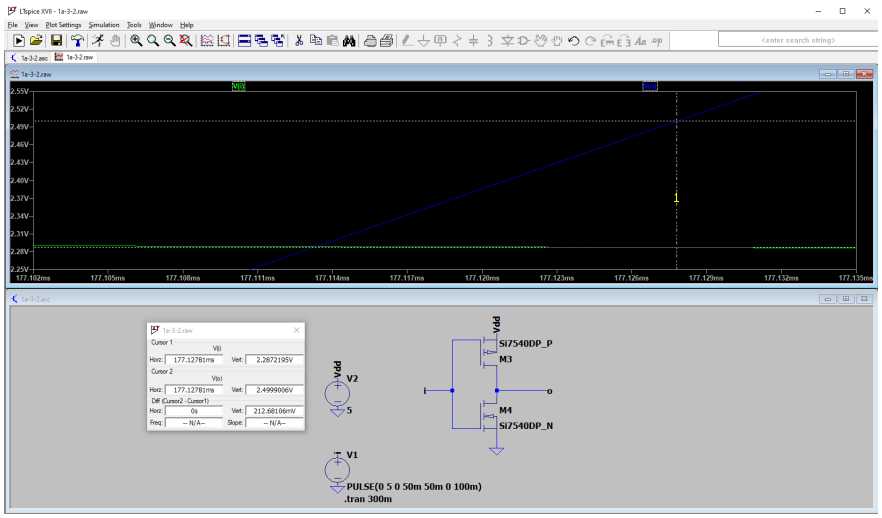

Figure 10: Measuring the falling input signal at 50% of the output swing with a 100 Hz triangular waveform input, the input voltage is 2.287 220 V.

b)

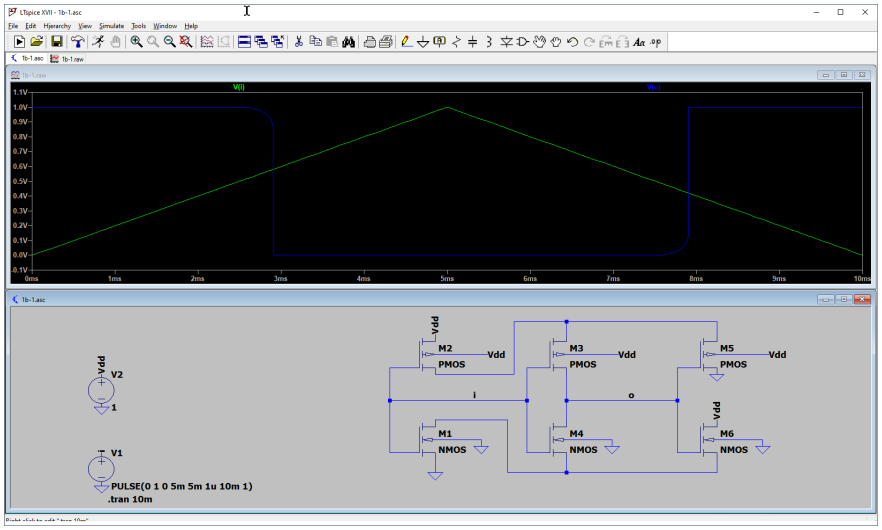

Figure 11: Pulse input

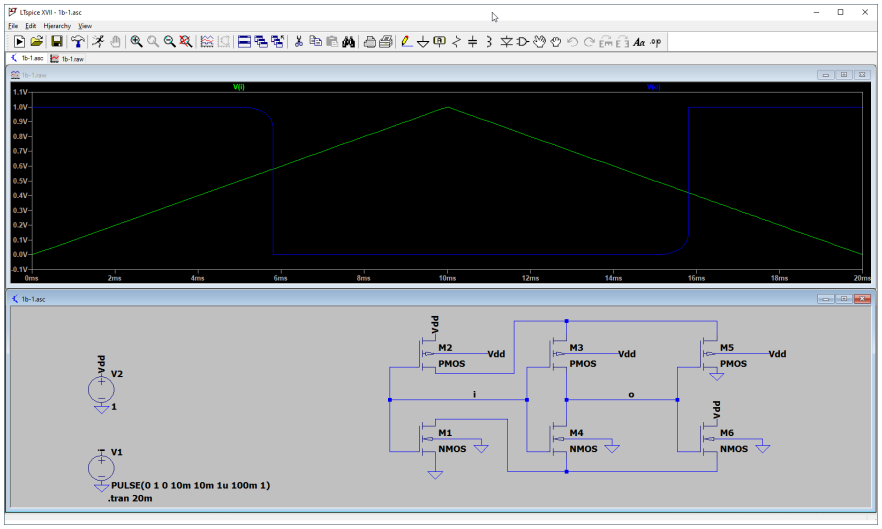

Figure 12: Overview of triangular input signal

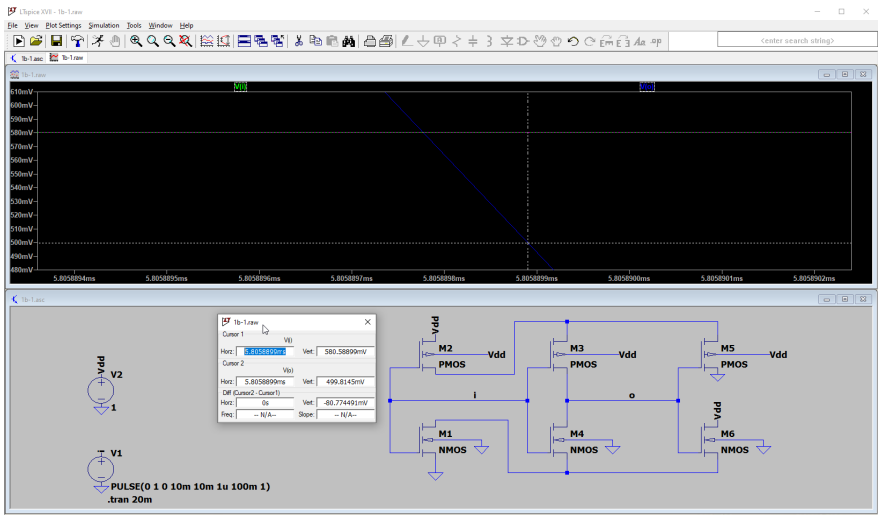

Figure 13: Measuring the rising input signal at 50% of the output swing with a 100 Hz triangular waveform input, the input voltage is 580.588 99 mV.

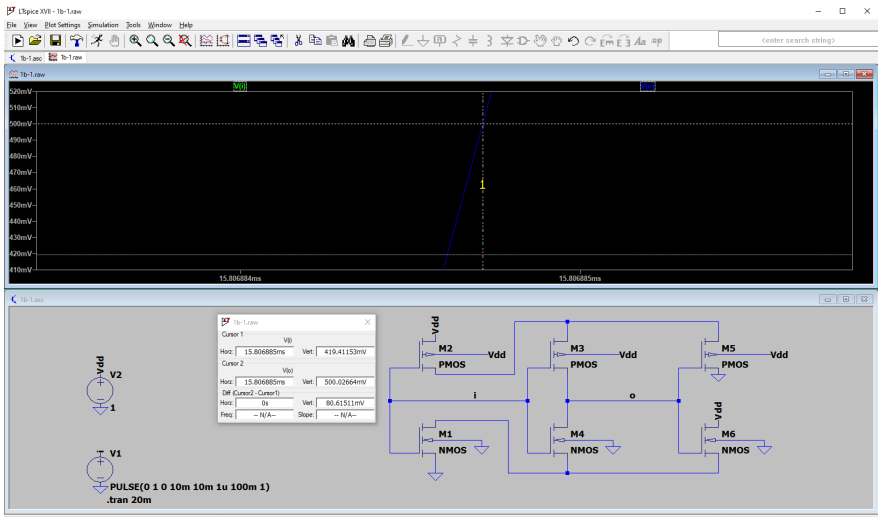

Figure 14: Measuring the falling input signal at 50% of the output swing with a 100 Hz triangular waveform input, the input voltage is 419.411 53 mV.

c)

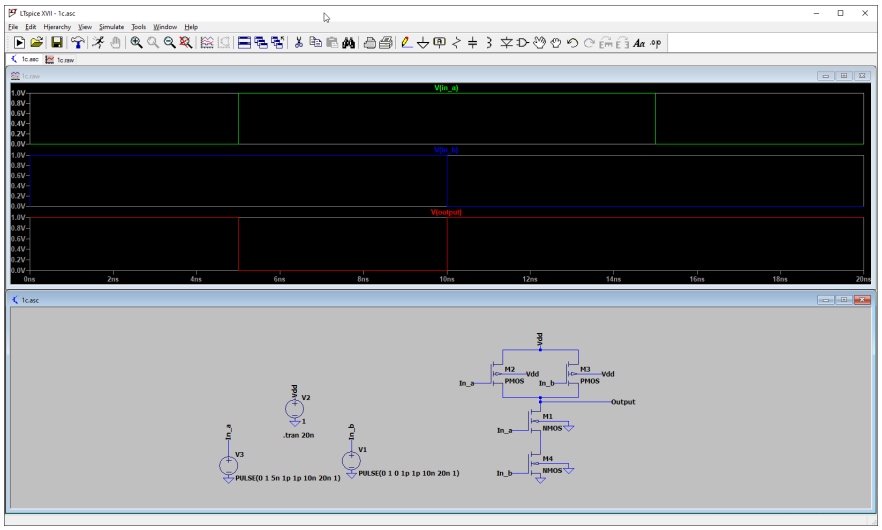

Figure 15: NAND gate using discrete MOS models

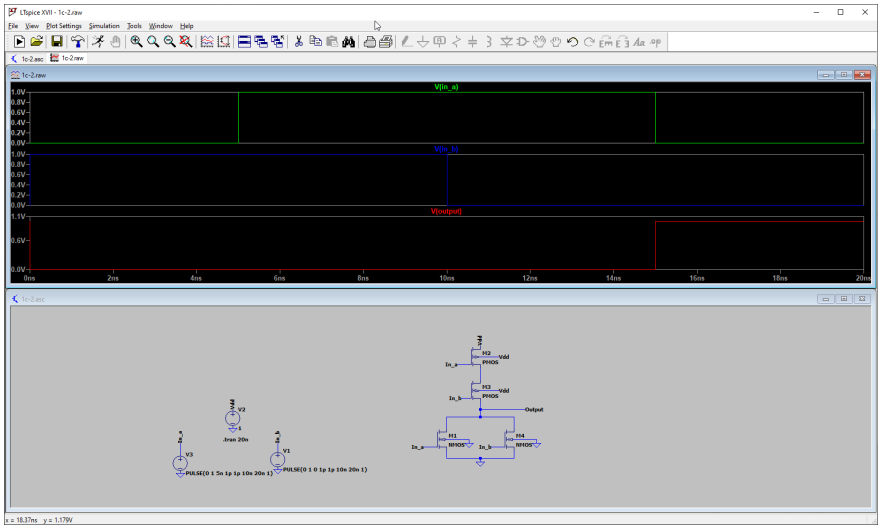

Figure 16: NOR gate using discrete MOS models

d)

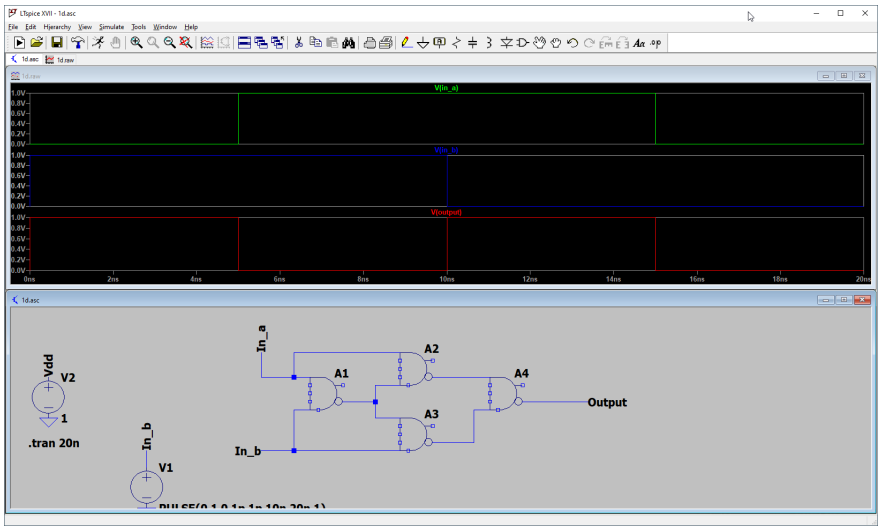

Figure 17: XOR gate using discrete NAND models

e)

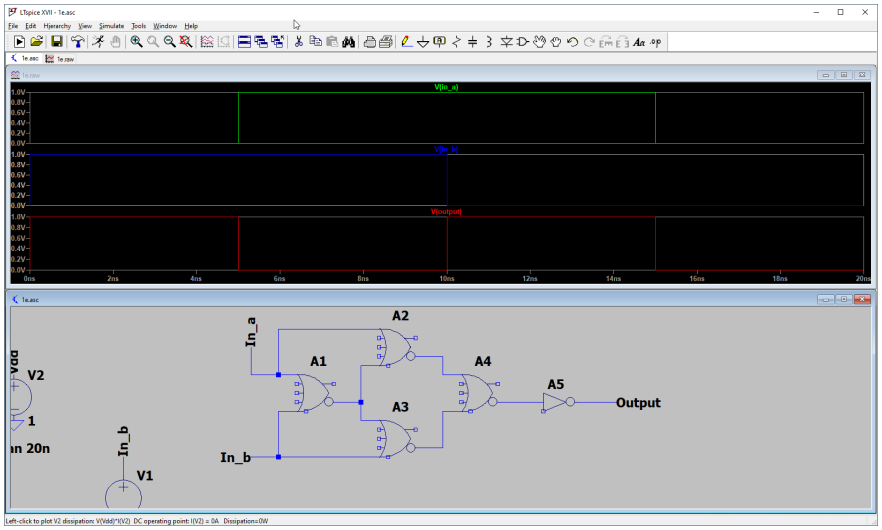

Figure 18: XOR gate using discrete NOR and inverter models

3 Using the CD4007 CMOS array, build and measure

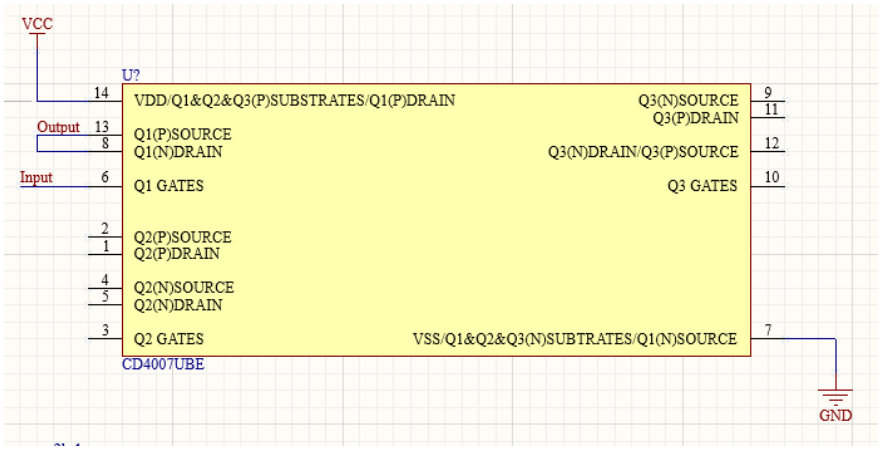

Figure 19: Schematic of inverter circuit 1a

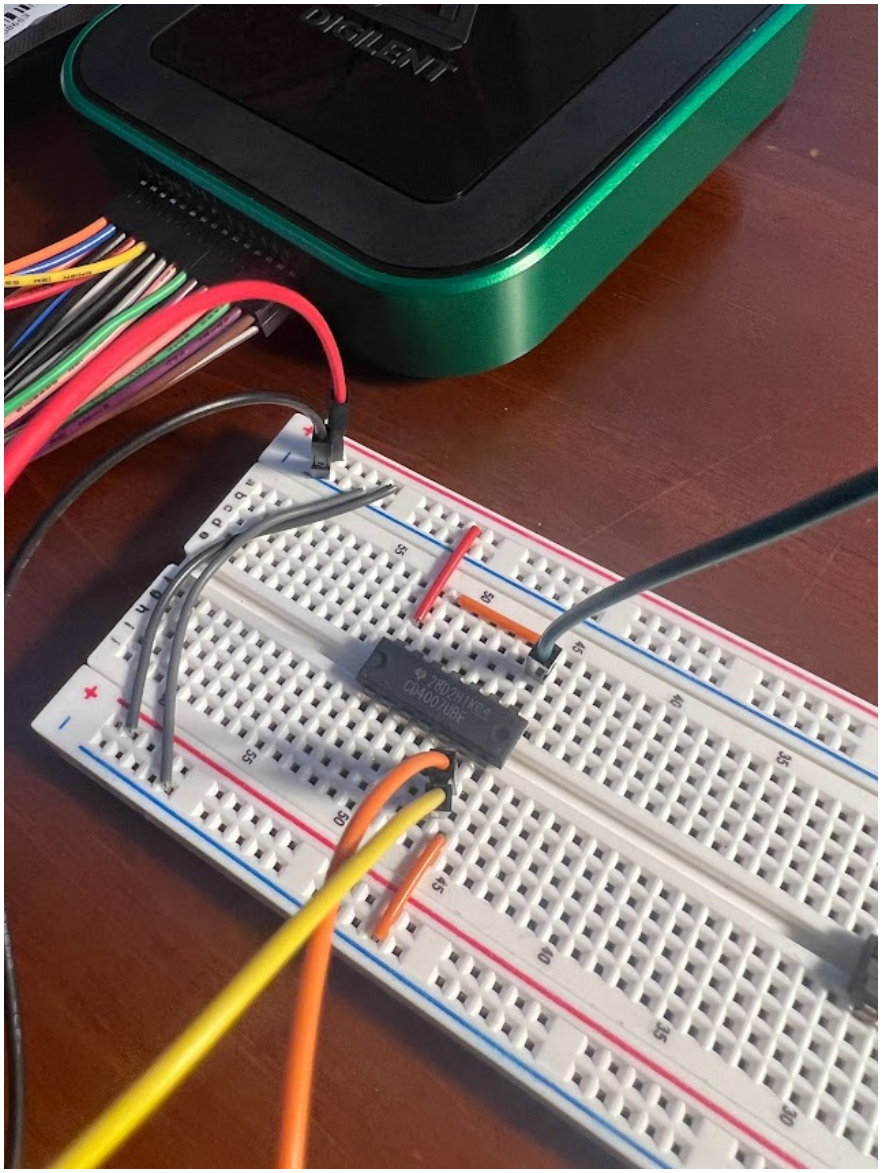

Figure 20: Photo of test setup

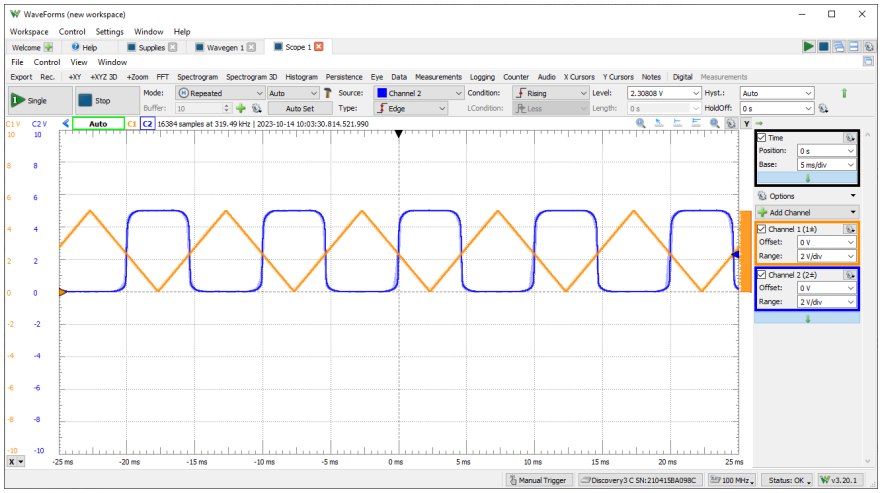

Figure 21: Overview of test signals for threshold measurement

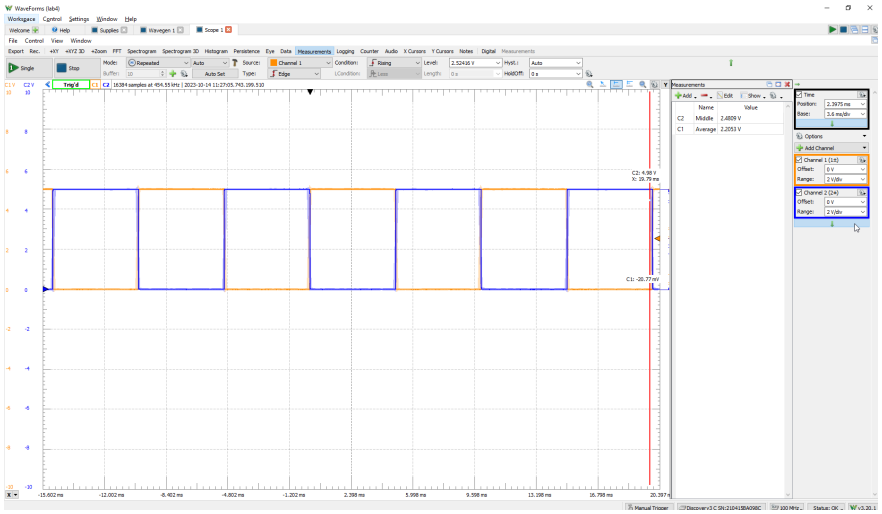

Figure 22: Overview of test signals for delay measurement

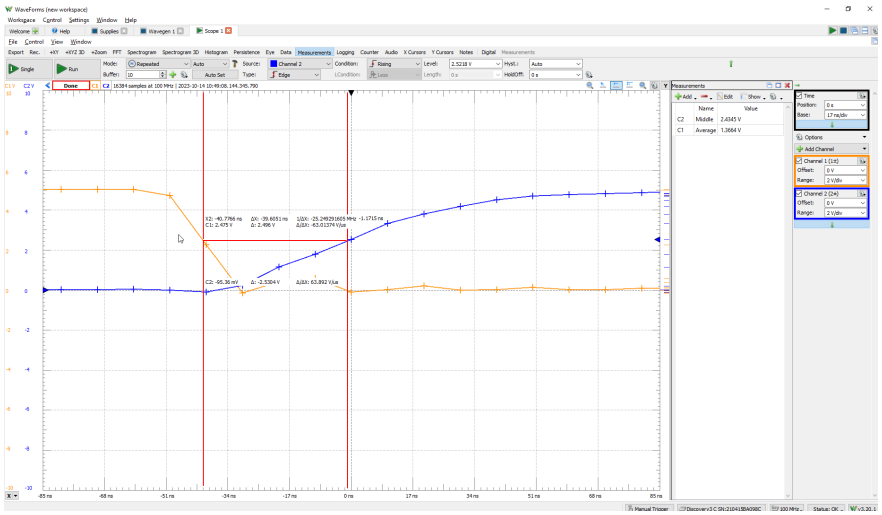

Figure 23: Measuring the time delay between the input signal and the output signal at 50% point, the rising output lags the falling input by 39.605 nS.

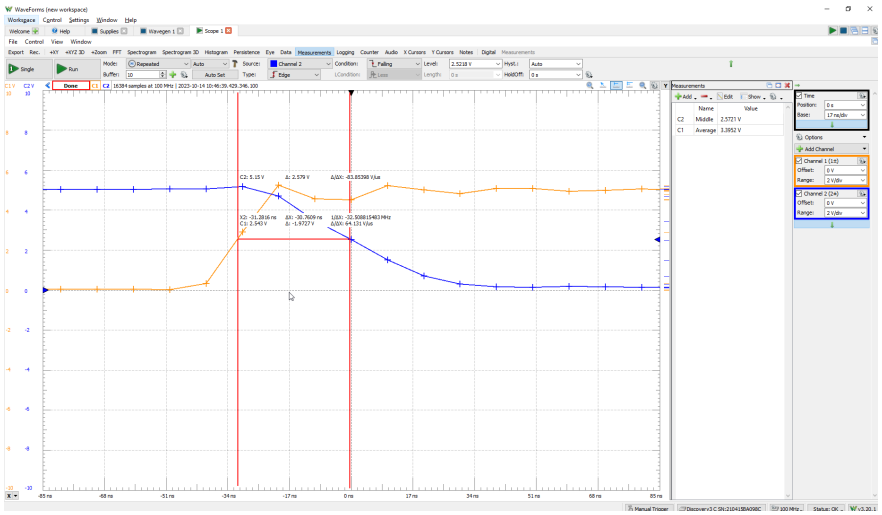

Figure 24: Measuring the time delay between the input signal and the output signal at 50% point, the falling output lags the rising input by 30.761 nS.

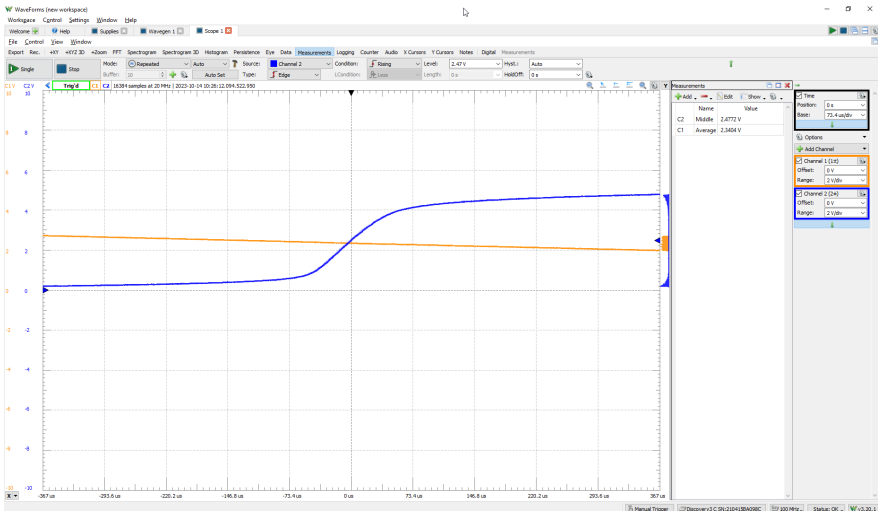

Figure 25: Measuring the falling input signal at 50% of the output swing with a 100 Hz triangular waveform input, the input voltage is 2.3404 V.

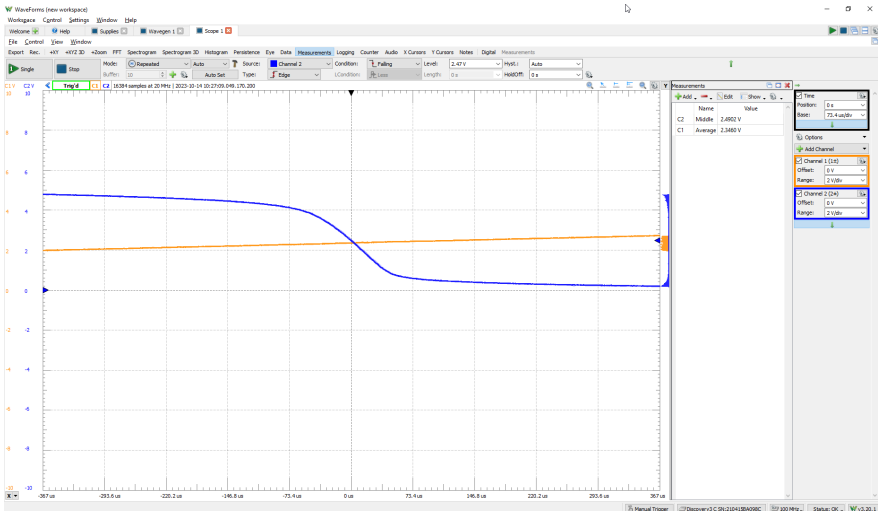

Figure 26: Measuring the rising input signal at 50% of the output swing with a 100 Hz triangular waveform input, the input voltage is 2.3460 V.

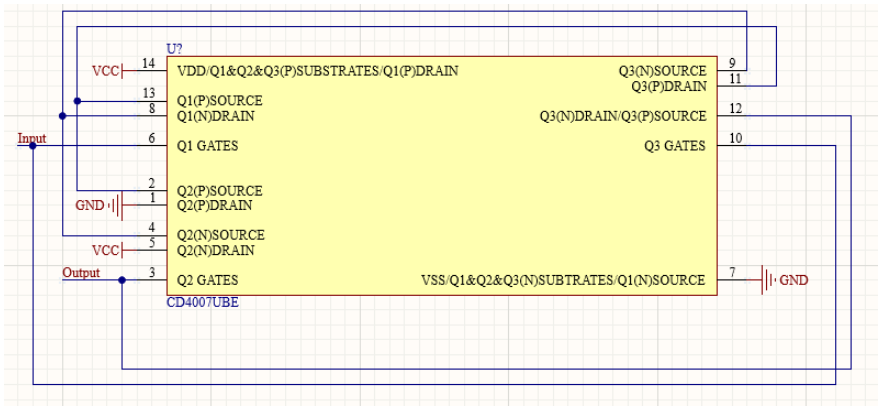

Figure 27: Schematic of Schmitt trigger circuit 1b

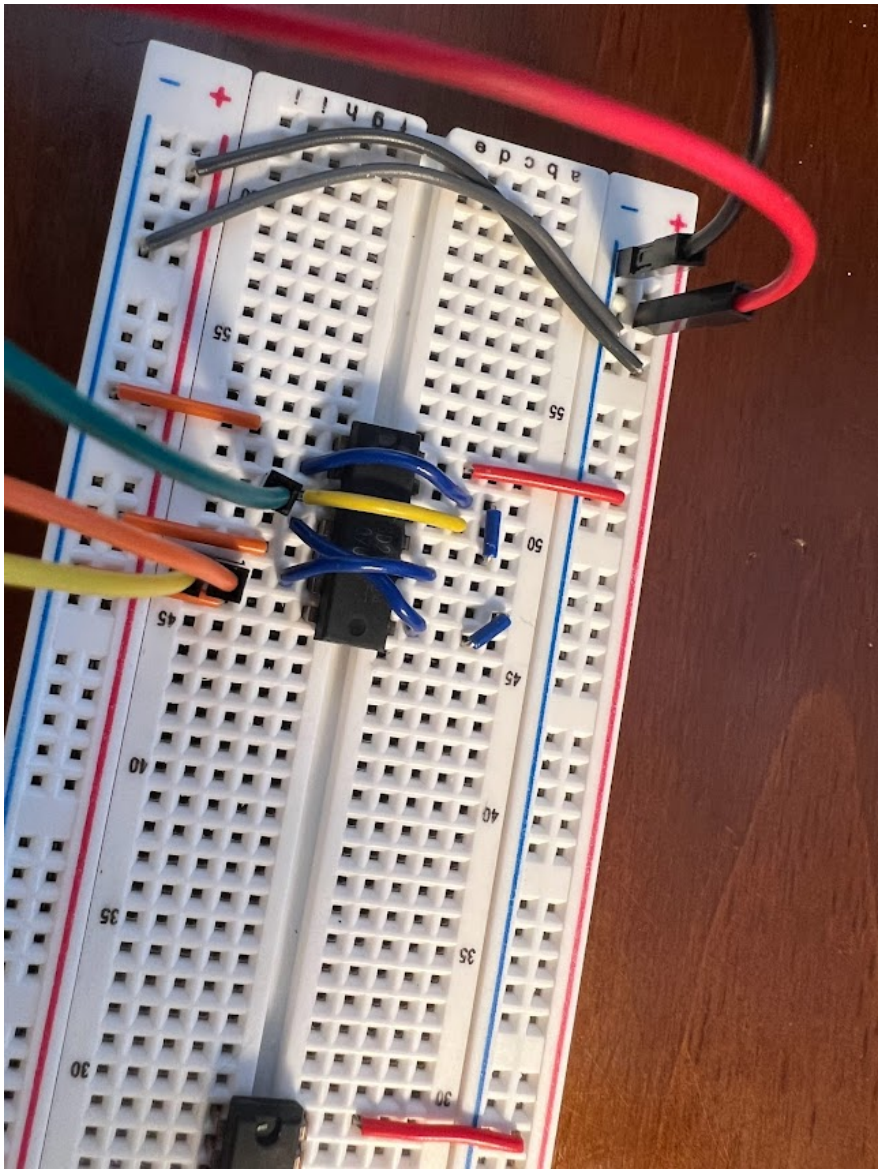

Figure 28: Photo of test setup

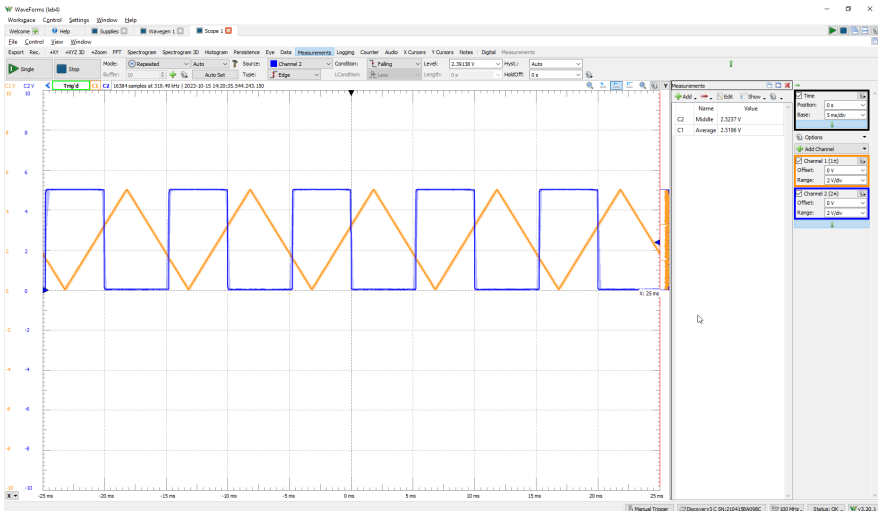

Figure 29: Overview of test signals for threshold measurement

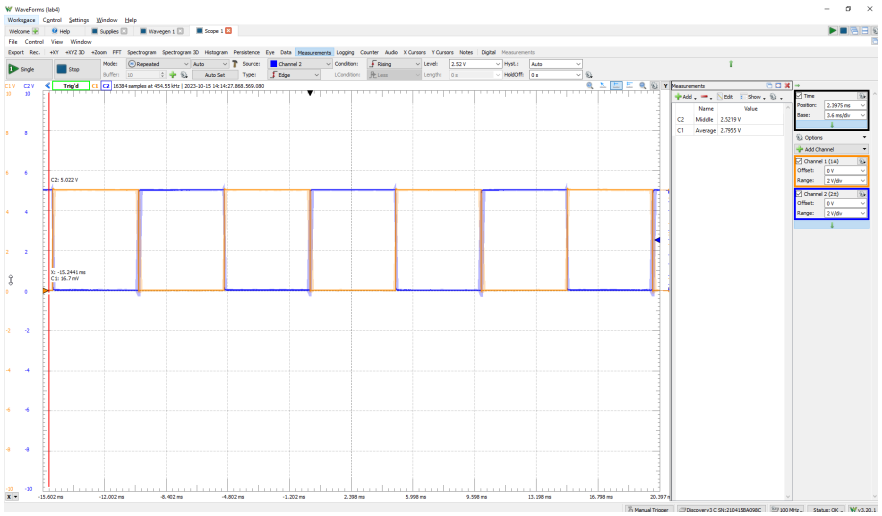

Figure 30: Overview of test signals for delay measurement

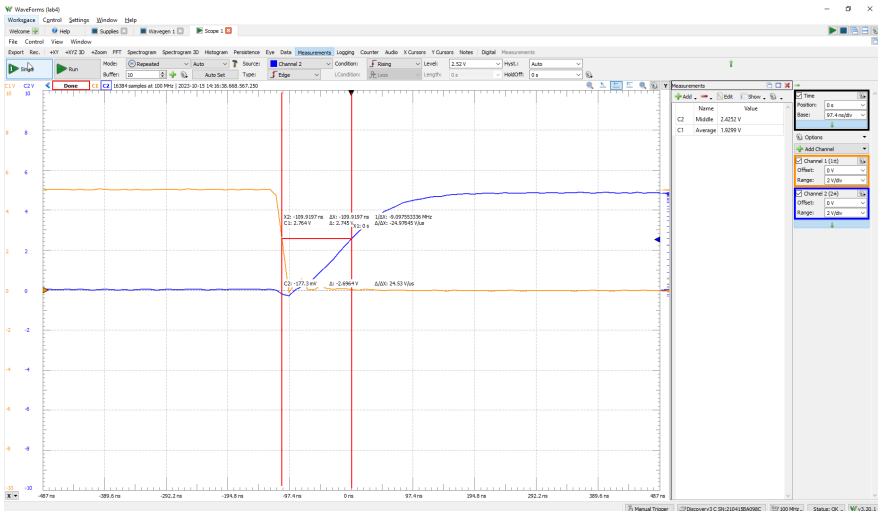

Figure 31: Measuring the time delay between the input signal and the output signal at 50% point, the rising output lags the falling input by 109.920 nS.

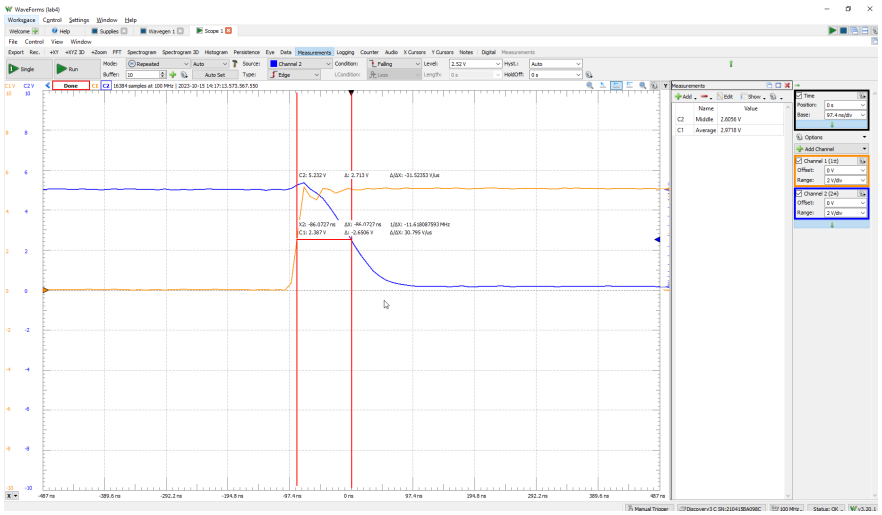

Figure 32: Measuring the time delay between the input signal and the output signal at 50% point, the falling output lags the rising input by 86.073 nS.

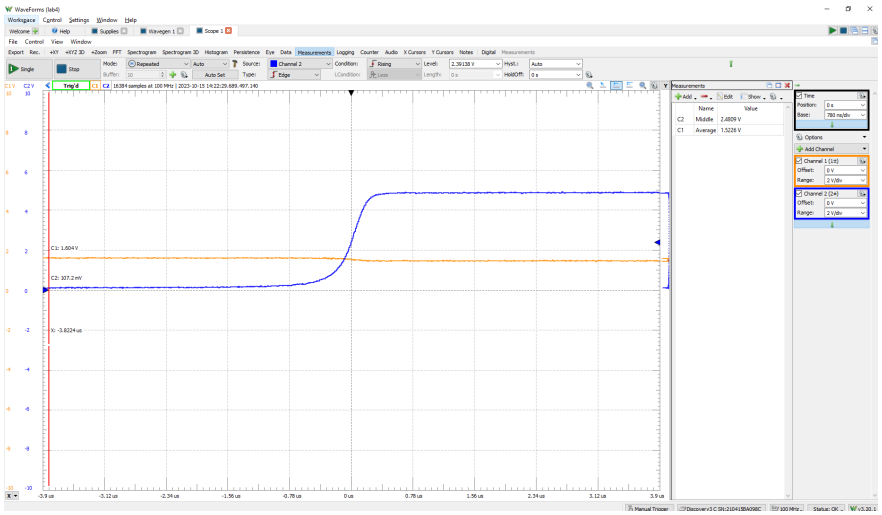

Figure 33: Measuring the falling input signal at 50% of the output swing with a 100 Hz triangular waveform input, the input voltage is 1.5226 V.

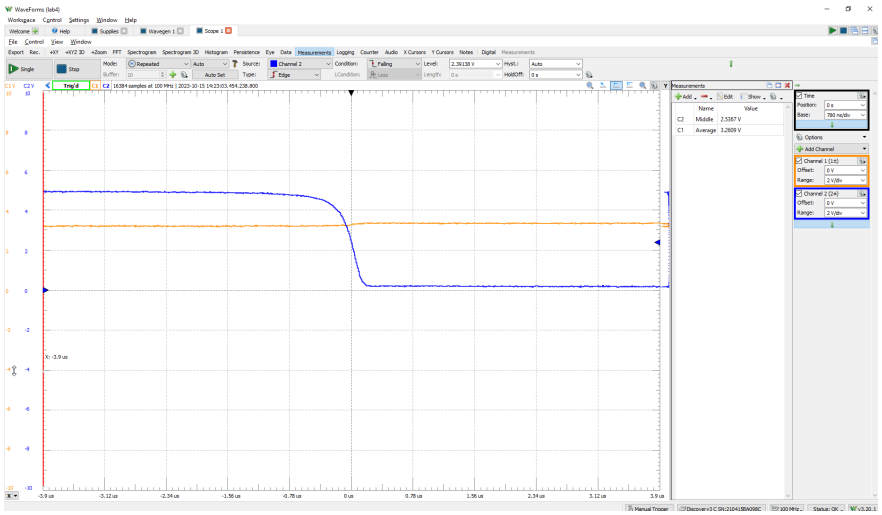

Figure 34: Measuring the rising input signal at 50% of the output swing with a 100 Hz triangular waveform input, the input voltage is 3.2609 V.

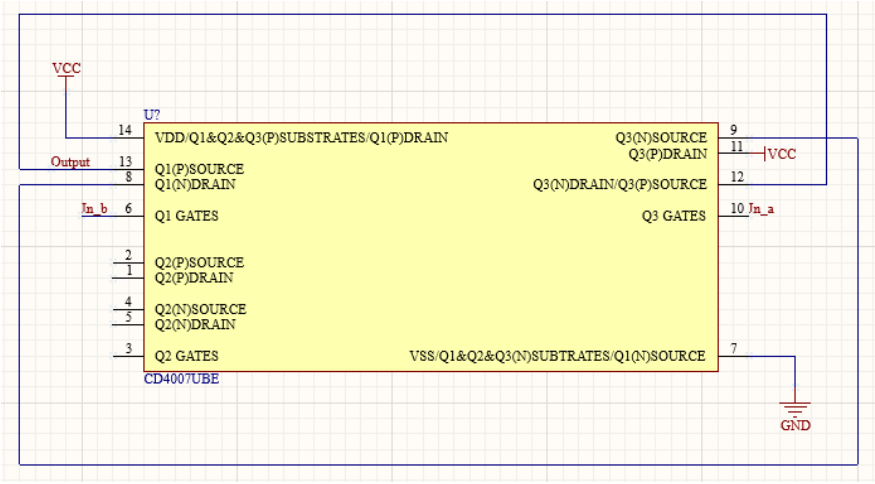

Figure 35: Schematic of NAND gate circuit 1c

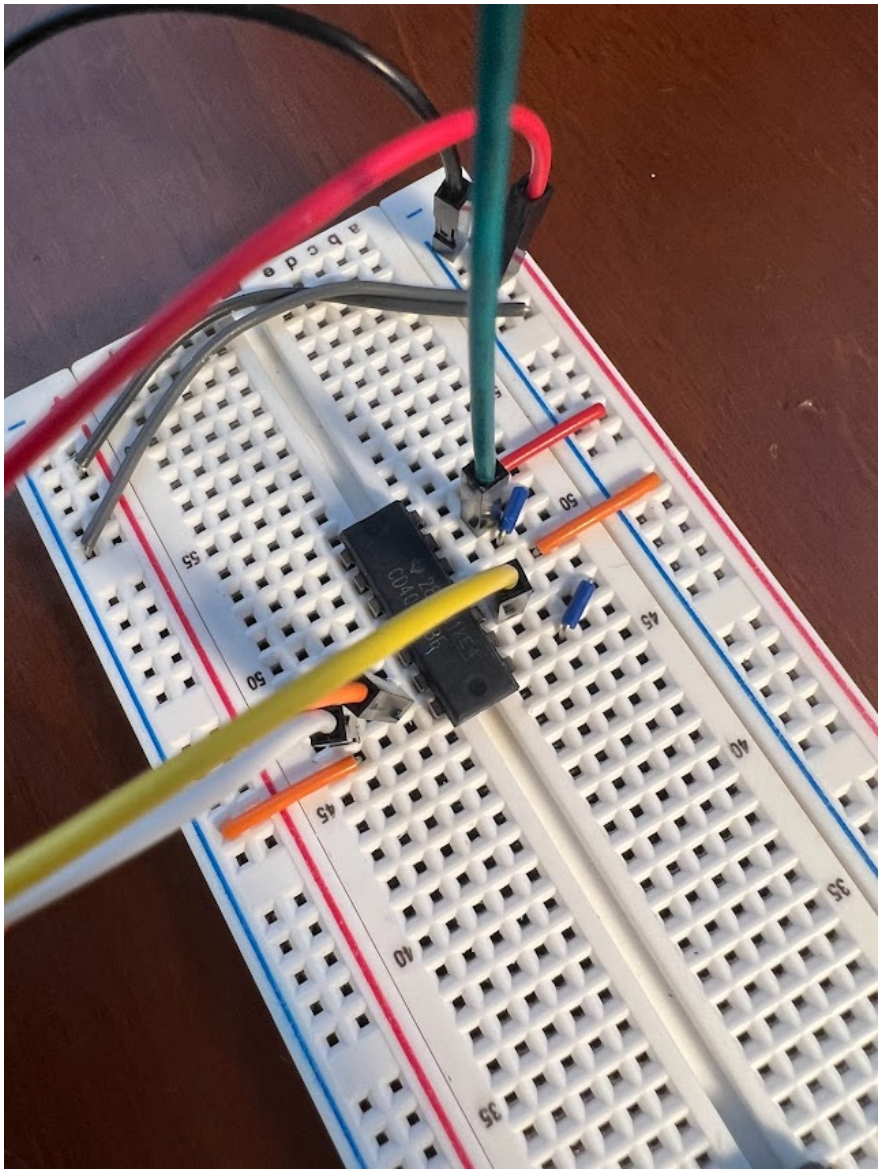

Figure 36: Photo of test setup

Figure 37: Overview of input A and input B waveforms

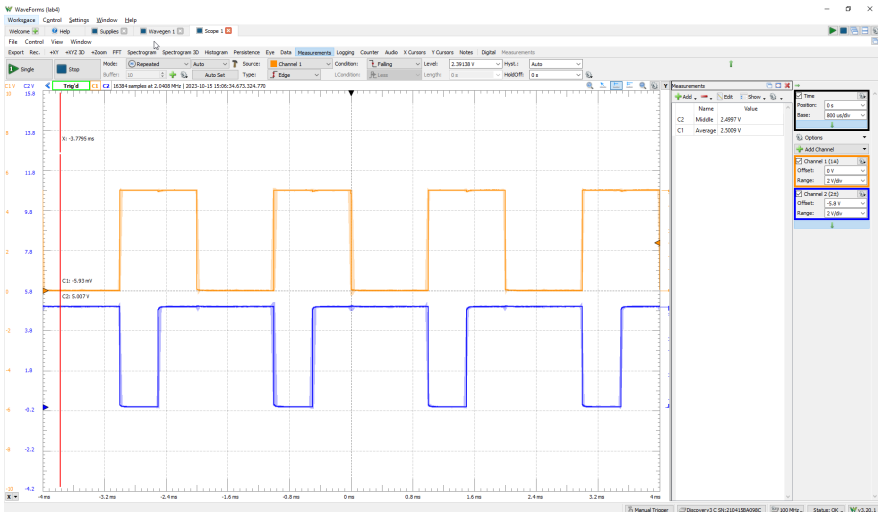

Figure 38: Input B and output showing correct NAND logic

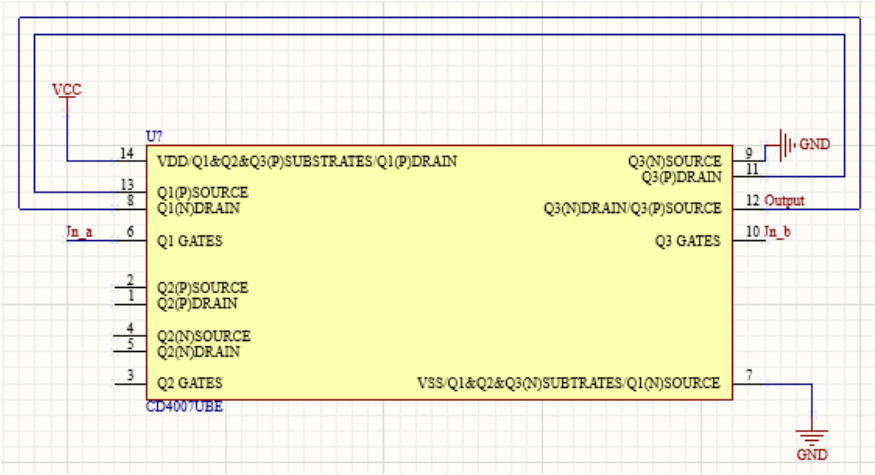

Figure 39: Schematic of NOR gate circuit 1c

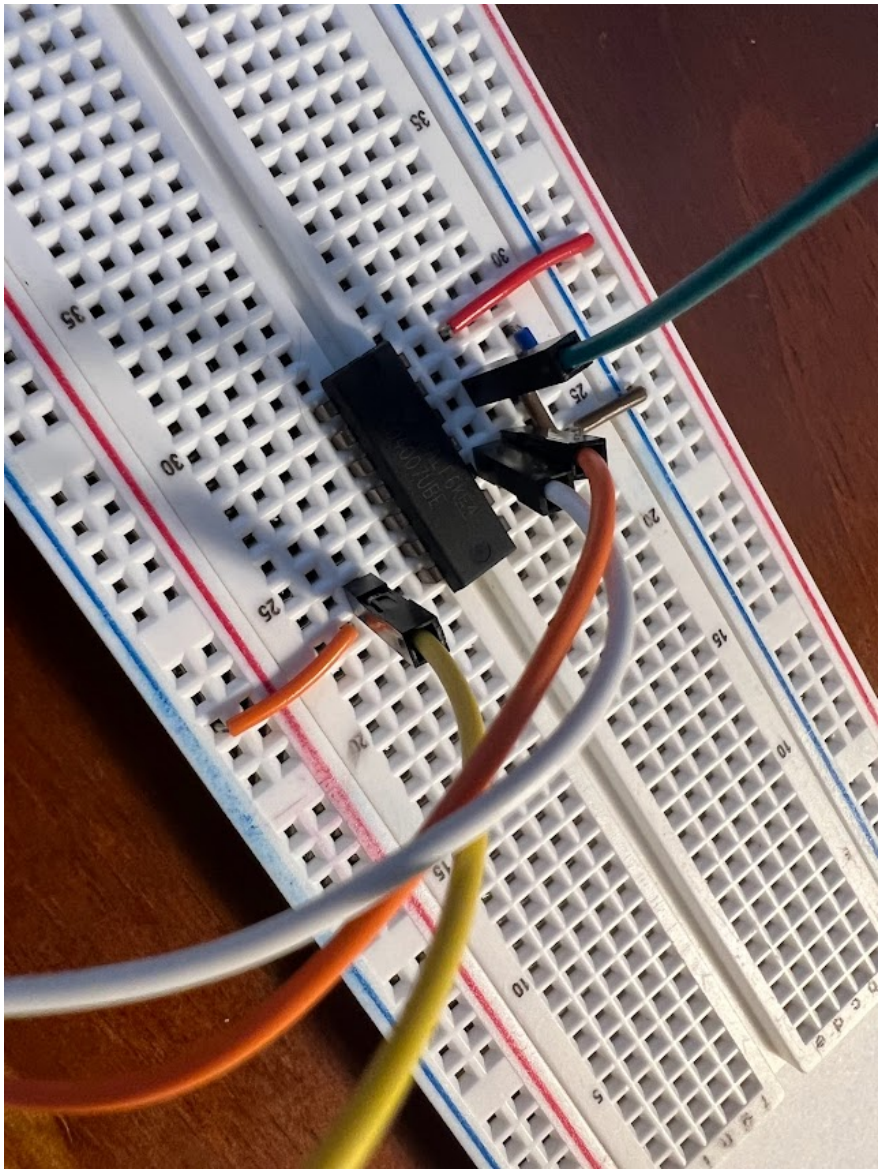

Figure 40: Photo of test setup

Figure 41: Overview of input A and input B waveforms

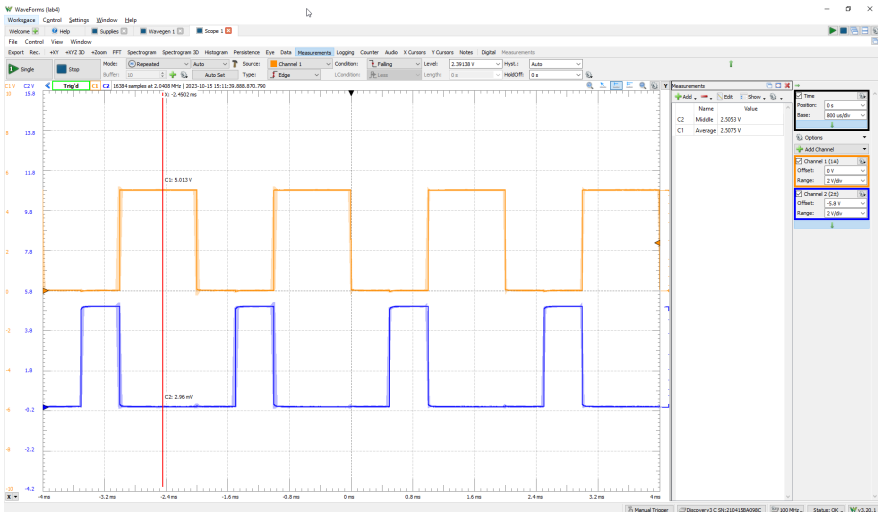

Figure 42: Input B and output showing correct NOR logic

4 Using the 74LS00 NAND array, build and measure

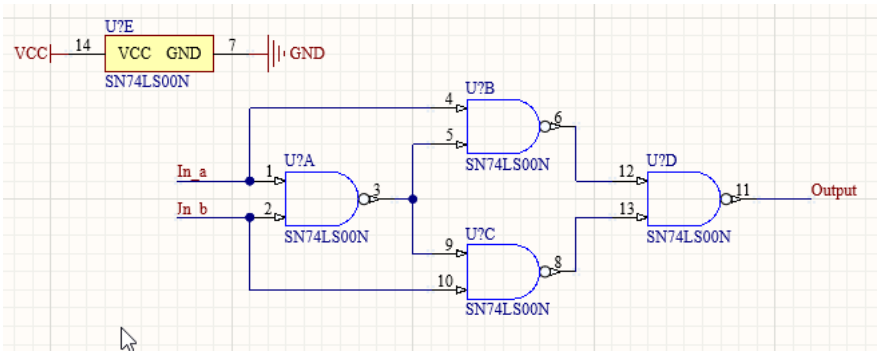

Figure 43: Schematic of XOR gate 1d

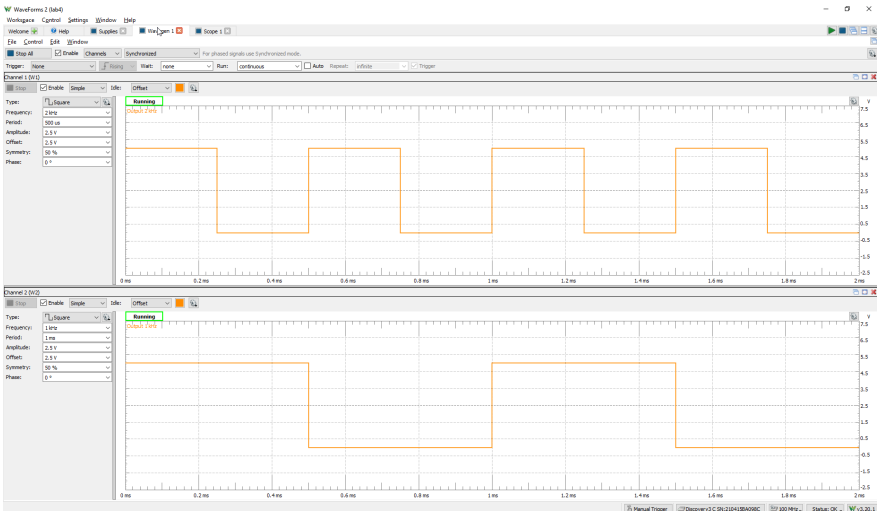

Figure 44: Overview of input A and input B waveforms

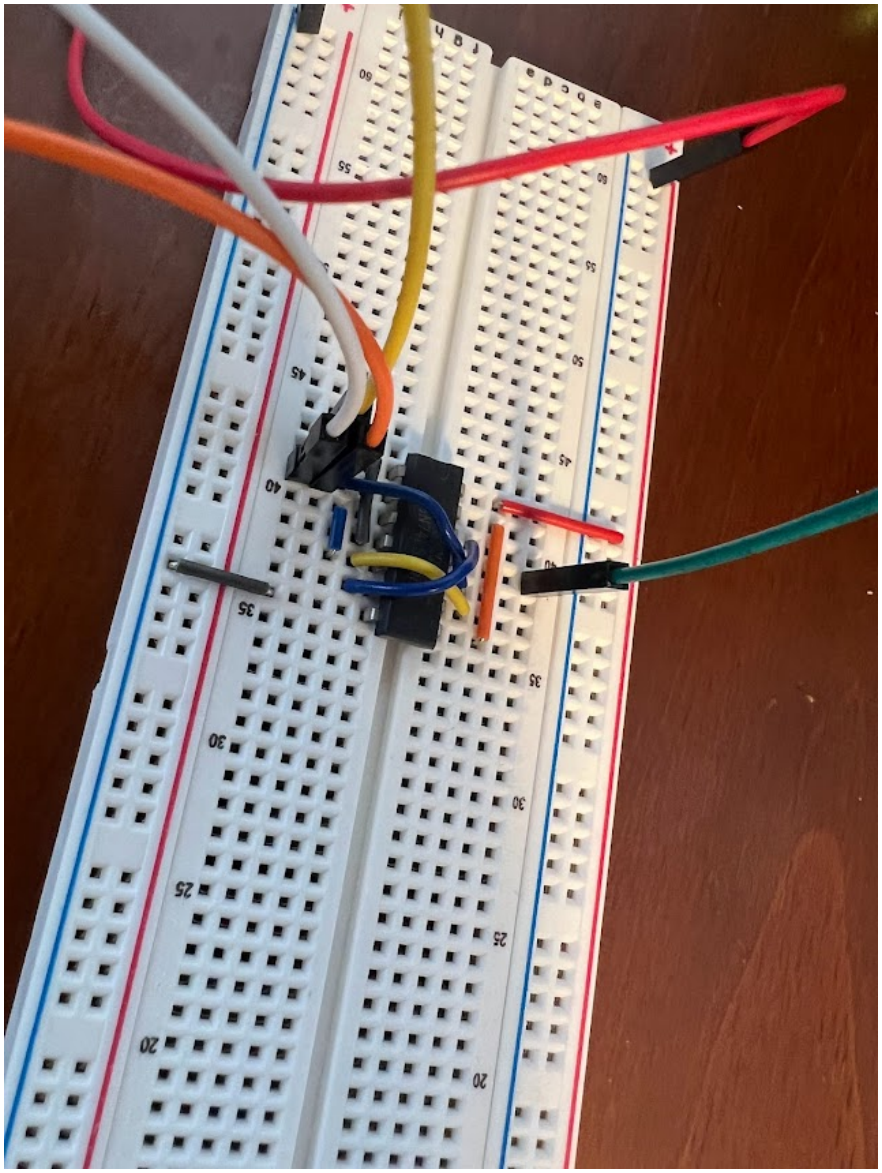

Figure 45: Photo of test setup

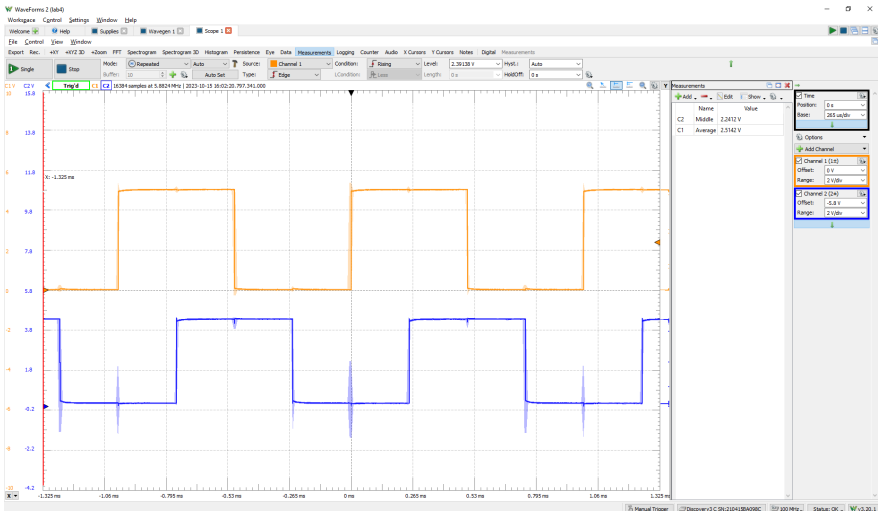

Figure 46: Input B and output showing correct XOR logic