

ESE411 Simulation assignment 3

Design of Common-Source Gain Stage Loaded with Current Mirror

1. Objectives

Application of gm/I_d methodology to design and analysis of MOSFET gain stages.

Simulation of the differential and common-mode gain frequency responses and estimates of the pole and zero frequencies.

2 . The amplifier schematic

The amplifier stage with PMOSFETs M1, M2 in common-source configuration has differential inputs V1, V2 and single ended output Vout. The single-ended output is obtained with NMOS current mirror load M3, M4. The stage is powered from a bipolar voltage source $V_{dd} = +2V$, $V_{ss} = -2V$ DC and loaded with capacitance $C_L = 100$ fF. The gain stage is biased with current mirror M5, M6.

In the differential mode as shown in Figure 1: $V_1 = -V_2 = 0.5$ V AC, 0 V DC.

In the common mode: $V_1 = V_2 = 1$ V AC, 0 V DC.

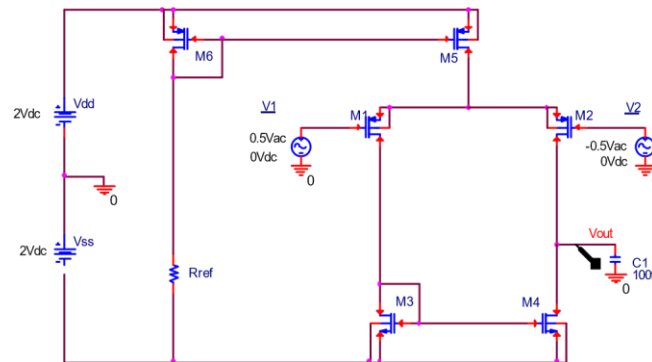


Figure 1. Schematic of the PMOS gain stage with NMOS current mirror load

3. Assignment:

1. For the amplifier in Figure 1 set the bias current as follows: assign Rref the value in kOhm equal to 100 + last two non-zero digits of your ID number to have it in the range $100\text{ k} < R_{ref} < 200\text{ k}$. Select the ratio of MOSFET widths in the current mirror M5, M6 to be $W_5/W_6 = 5$. Keep gate lengths equal: $L_5 = L_6$. Select MOSFET dimensions W, L for M1, M2, M3, M4, M5, M6 to meet the following specifications:

Low frequency differential-mode gain: $A_d > 40$ dB

Low frequency common-mode gain: $A_{cm} < -40$ dB

Preference should be given to a set of parameters (W, L) resulting in greater bandwidth of the differential gain with external capacitive load of 100 fF. Do not exceed recommended $gm/I_d = 20$.

2. Obtain Bode plots for A_d and A_{cm} in the frequency range from 10 kHz to 10 GHz. Estimate the 1st pole frequency in the response of A_d and the 1st zero frequency in the response of A_{cm} .

4. Report

The report should include objectives, target specs, estimates of initial parameters W, L obtained with gm/I_d and I_d/W charts, the schematic with final W, L, DC voltages and currents shown, Bode plots for A_d and A_{cm} , frequencies of the requested pole and zero and a summary with achieved specs.