Simulation 3

Suggested approaches

Given: the schematic with a 100 fF capacitive load, the bias current (set by Rref and the PMOS widths ratio of 5 in the current mirror), design specs with DC gain values of Ad > 40 dB, Acm > -40 dB.

Goals: learn use of gm/Id (VGS) and Id/W (VGS) charts for achieving the design objectives in a short period of time (with the smallest number of PSPICE iterations).

Objectives: obtain the set of L and W to meet the specs on DC gain values with greater BW for the given DC bias current.

The specs can be meet in broad ranges of MOSFET dimensions. Preferences should be given to the smallest MOSFET dimensions.

Suggested approach:

1. Select the minimal L = 0.5 um for the lowest MOSFET capacitances and the smallest dimensions. Estimate VGS and W for all MOSFETs with gm/id and id/W charts.
2. Enter the schematic into PSPICE with selected L and W values, verify the DC currents, VGS and VDS values, correct W for desired VDS.
3. Obtain Bode plots for Ad and Acm, compare the DC gain values for Ad and Acm with the specs. For improved Ad select greater L for the PMOS devices in the differential pair. For lower Acm select greater L for the PMOS devices in the current source (the mirror) biasing the stage.

Examples:

1. Rref was requested to be 150 k. Estimate the bias current:

In order to get low Acm the PMOS of the current source should operate in the saturation region with a small Vov. Let VGS for the PMOS in the current mirror to be 1V (the absolute value).
The voltage drop across Rref would be VDD –VSS – VGS = 3V. The reference current would be 3/0.15M = 20 uA.
Neglect the dependence of the drain current on VDS of the PMOS in the current source (early effect).
With that and PMOS width ratio of 5 the bias current of the stage would be 5x20=100 uA.

2. The PMOSFETS in the differential pair would operate at Id= 50 uA. Select gm/Id= 20.
With L=0.5 um it would result in VGS = 0.87V and 0.2 mA per micron of the width. Thus, W= Id/0.2= 250 um.
Do not be discouraged if estimates result in W values of hundreds of um. Wide MOSFETs are obtained by parallel connection of devices with smaller W.

3. The NMOSFETs in the current mirror load would operate at the same Id = 50 uA (52 um with the optional correction).
VGS =VDS due to the diode connection and symmetry: both NMOS devices have the same W, L and the currents for the pair. Selection of W for the meeting the gin specs is not so critical. Primarily, it would affect the DC output voltage. Let us select VGS =0.8 V, it would be Vout = VSS+VDS= -1.2V DC.
For L= 0.5 um and VGS =0.8 V the Id/W would be 10 uA/um which results in W = 5 um. Do not select W < 2.5 um. It would be too small for fabrication with a 0.5 um gate length technology.

4. For the PMOS in the current source (mirror) one can start with L= 0.5 um to see where we are with Acm.
One would anticipate smaller Vov (select VGS closer to the absolute value of Vtp) however it would result in wider PMOS.
Initially for the reference source (the diode) we started with VDS =VGS =1V. With that it would be 1.5 uA/W and W= 100 uA/1.5 = 67 um.

The PMOS threshold for this model is about -0.9V (see sim 1). Therefore, the absolute value of Vov would be 0.1 V. In the PMOS differential pair the absolute value of VGS =0.87V. Thus, the PMOS of the current source would operate with VDS = VDD –VGS in the diff. pair = 2-0.87= 1.13V. It is much greater than 0.1 V so one can expect the operation of the PMOS current source in the saturation mode with high differential output resistance ro =Rss required for low Acm.

For VGS = 1.1V it would result in 3 uA/W and W= 100 uA/2= 33 um. It would be ni proble with Acm as well.

For the given bias current one can obtain greater differential voltage gain with increase of the Early voltage by increasing L in the PMOS differential pair. Say, let L=1 um: VGS would be 0.98V, Id/W would be 90 nA/um, and W= 50/0.09= 550 um.

Vout AC would be equal to Ad with Vid =1 V. For that input voltages would be selected to be 0.5 V and -0.5 V AC.
Vout AC would be equal to Acm with Vicm = 1 V. For that the both input voltages would be selected to be 1 V AC.

4. Trading gain for bandwidth.
In Sim 3 the bias current was set initially for simplicity. With the maximum recommended gm/Id =20 it would result in moderate MOSFET widths and high gm for greater GBW product.

The GBW is defined by gm and CL, one would estimate it as
50 uAx 20 1/V/6.28/ 0.1 pF =1e-3/0.628e-12 = 1.6 GHz.

With the differential gain of 40 dB (x100) one would expect the -3 dB level BW of 16 MHz.

Selecting greater L would result in greater Ad at the cost of higher output resistance.
the bandwidth would be reduced.
In addition, greater W would result in additional load capacitance.

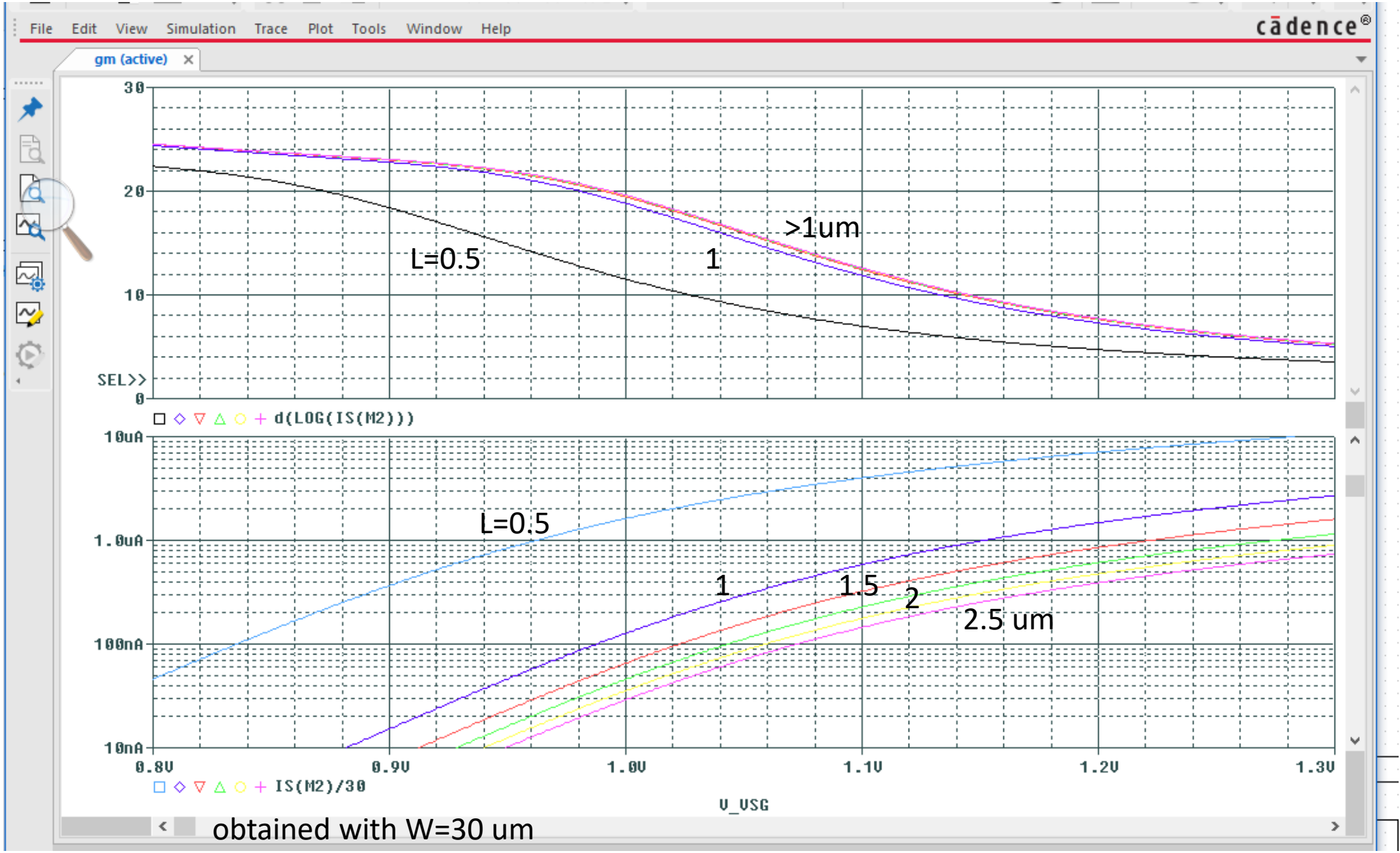
With L = 0.5 um Cgd of PMOS = Cov x W = 0.4 fF/um x 250 um = 100 fF I addition to CL =100 fF.
The impact of Cgd of NMOS can be neglected. The total capacitive load would double.
One expect a half of GBW product and the BW, respectively.
With L=1 um the BW would be even lower due to greater Cgd and the capacitive load, respectively.

One can increase L of NMOS to 1 um for a minor increase of the DC voltage gain.
The output resistance of the MOSFTETs and the stage, respectively would be hard to estimate numerically (as seen in Sim1). Basically , one has to watch VDS for the devices and make sure it is high enough compared to Vov.
An accurate value of the differential gain would be obtained with PSPICE simulation.

PMOSFET

gm/Id (1/V)

Id/W (A/um)

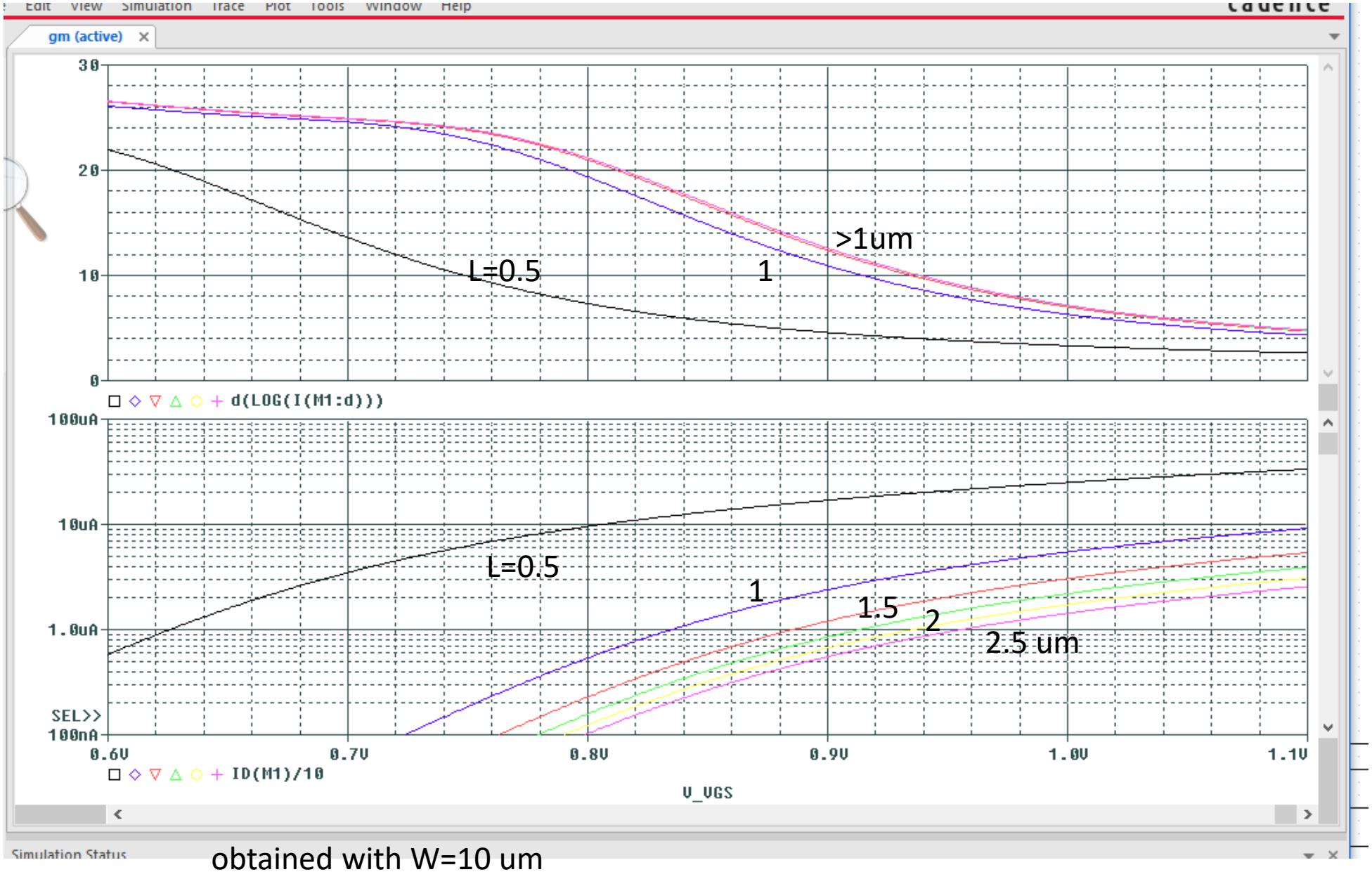


obtained with W=30 um

NMOSFET

gm/Id (1/V)

Id/W (A/um)



obtained with W=10 um