Stony Brook University

EEO311

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Design of Common-Source Gain Stage Loaded with Current Mirror

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Copy of Original Assignment

ESE411 Simulation assignment 3

Design of Common-Source Gain Stage Loaded with Current Mirror

1. Objectives

Application of gm/Id methodology to design and analysis of MOSFET gain stages.
Simulation of the differential and common-mode gain frequency responses and estimates of the pole and zero frequencies.

2 . The amplifier schematic

The amplifier stage with PMOSFETs M1, M2 in common-source configuration has differential inputs V1, V2 and single ended output Vout. The single-ended output is obtained with NMOS current mirror load M3, M4. The stage is powered from a bipolar voltage source Vdd = +2V, Vss = - 2V DC and loaded with capacitance CL=100 fF. The gain stage is biased with current mirror M5, M6.

In the differential mode as shown in Figure 1: V1 = - V2 = 0.5 V AC, 0 V DC.
In the common mode: V1 = V2 = 1 V AC, 0 V DC.

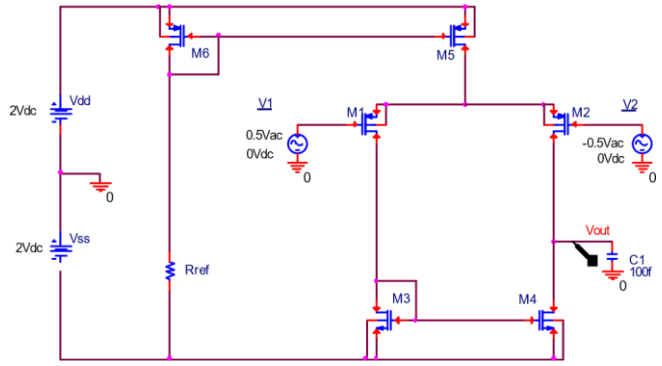

Figure 1. Schematic of the PMOS gain stage with NMOS current mirror load

3. Assignment:

1. For the amplifier in Figure 1 set the bias current as follows: assign Rref the value in kOhm equal to 100 + last two non-zero digits of your ID number to have it in the range 100 k < Rref < 200 k. Select the ratio of MOSFET widths in the current mirror M5, M6 to be W5/W6=5. Keep gate lengths equal: L5=L6. Select MOSFET dimensions W, L for M1, M2, M3, M4, M5, M6 to meet the following specifications:
Low frequency differential-mode gain: Ad > 40 dB
Low frequency common-mode gain: Acm < - 40 dB
Preference should be given to a set of parameters (W, L) resulting in greater bandwidth of the differential gain with external capacitive load of 100 fF. Do not exceed recommended gm/Id = 20.
2. Obtain Bode plots for Ad and Acm in the frequency range from 10 kHz to 10 GHz. Estimate the 1st pole frequency in the response of Ad and the 1st zero frequency in the response of Acm.

4. Report

The report should include objectives, target specs, estimates of initial parameters W, L obtained with gm/Id and Id/W charts, the schematic with final W, L, DC voltages and currents shown, Bode plots for Ad and Acm, frequencies of the requested pole and zero and a summary with achieved specs.

Overview

In simulation 3 we design a differential amplifier. We are actually designing the L/W of each mosfet at makes up the amplifier, initially starting with gm/Id and Id/W charts to get approximate values. From there, the parameters are tuned based on the performance objectives of the amplifier. This is analogous to how an IC designer would design an amplifier directly on silicon. This is actually very exciting.

1 Assignment

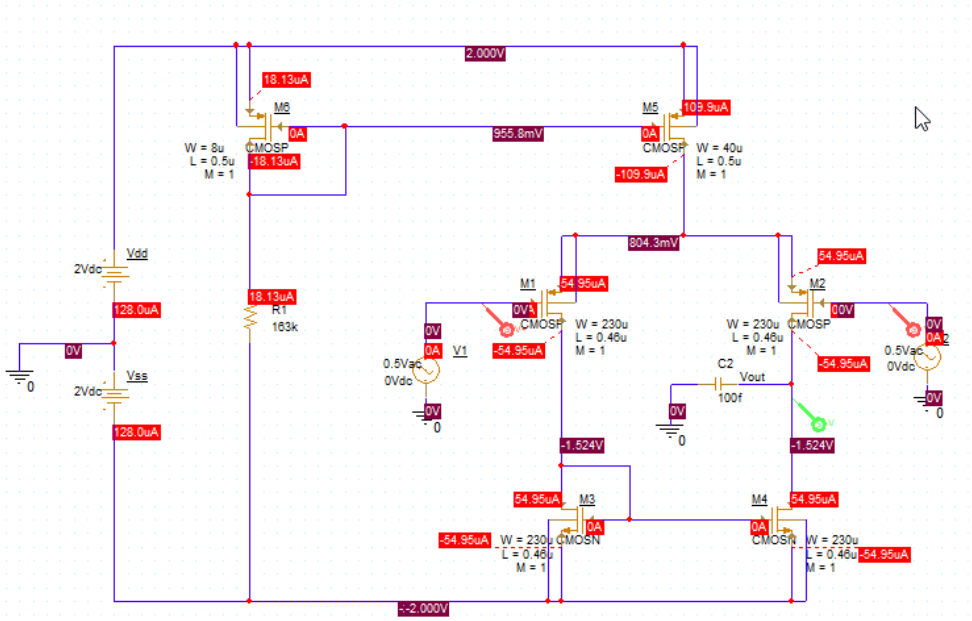

Figure 1: Bias point simulation with reference current resistor value set to 163 kΩ.

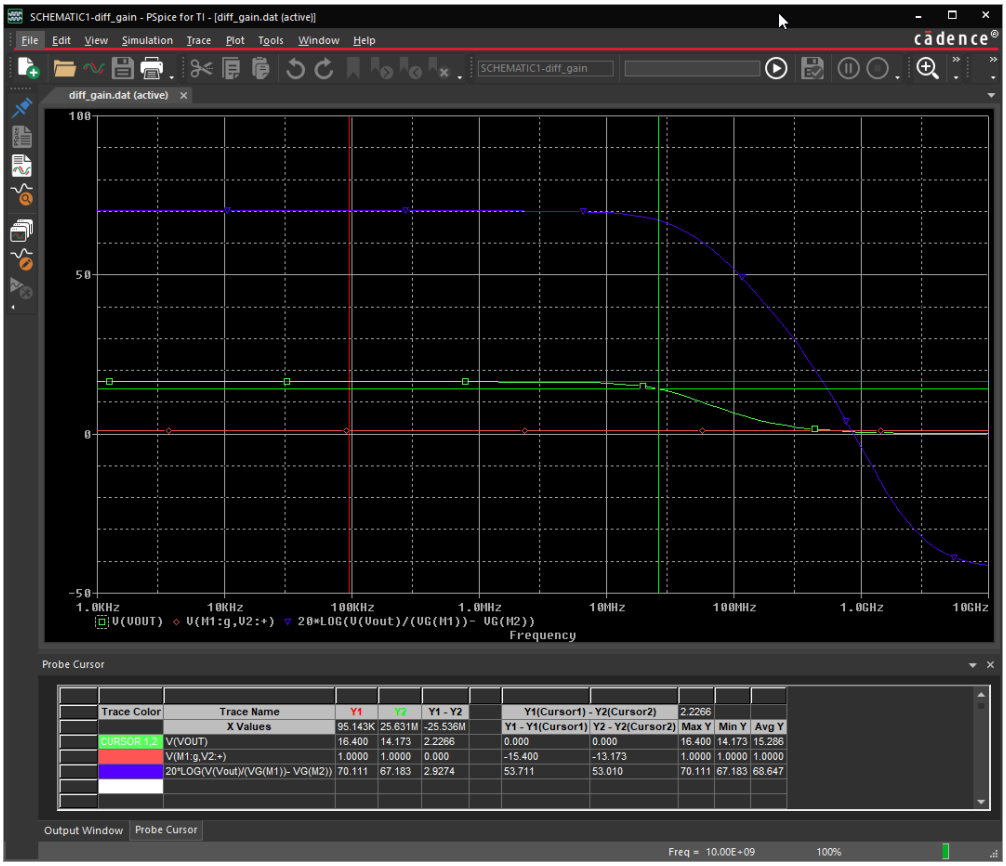

Figure 2: Simulation Showing Ad gain of about 70 and bandwidth of 25.6 MHz.

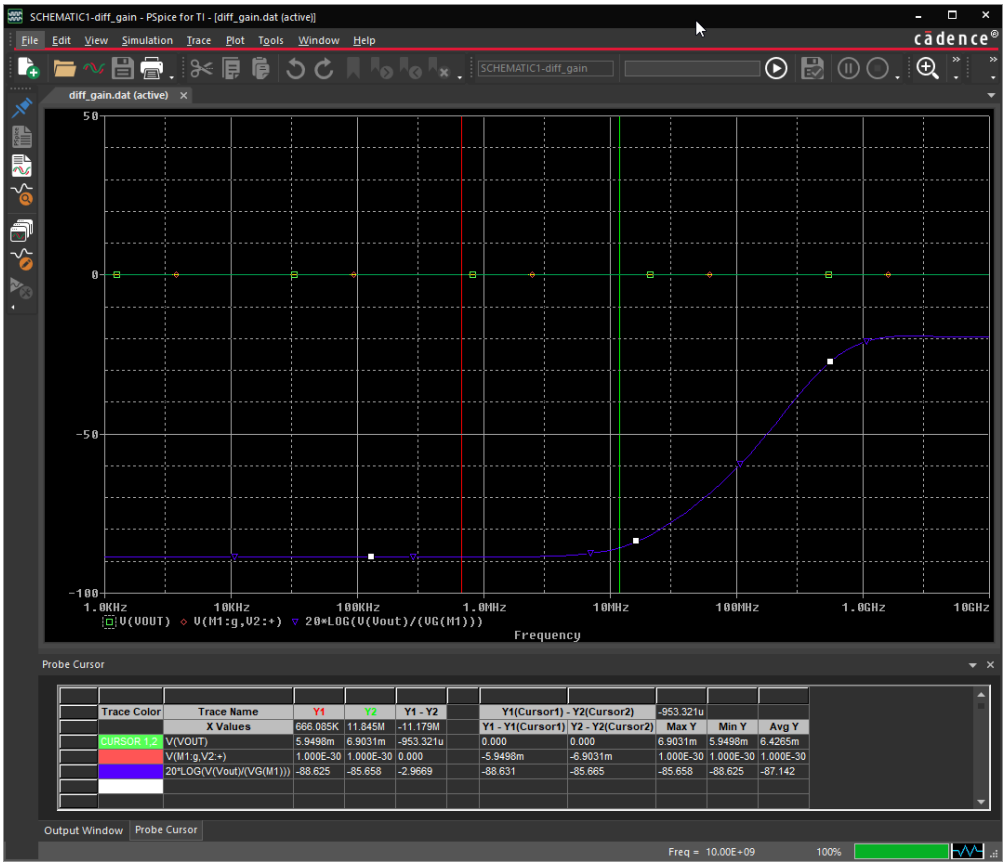

Figure 3: Simulation Showing Acm gain of about -88 and bandwidth of 11.8 MHz.