Unit 7

MOSFET output resistance

Early voltage

Early voltage parameter

Load line (review)

MOSFET output resistance

Measurement of the MOSFET output resistance

MOSFET design parameter: Early voltage

Dependence on gate length L

Process parameter:

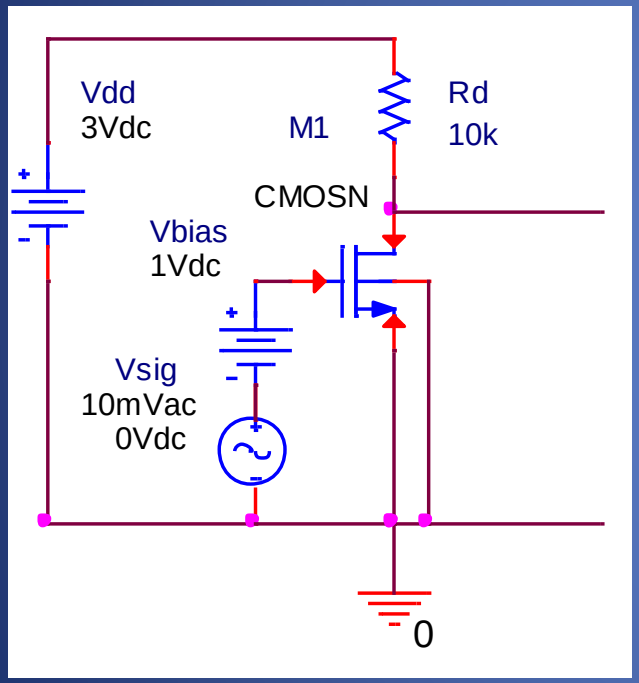
Early voltage PARAMETER

Typical values of Early voltage parameters for L= 0.5 um node

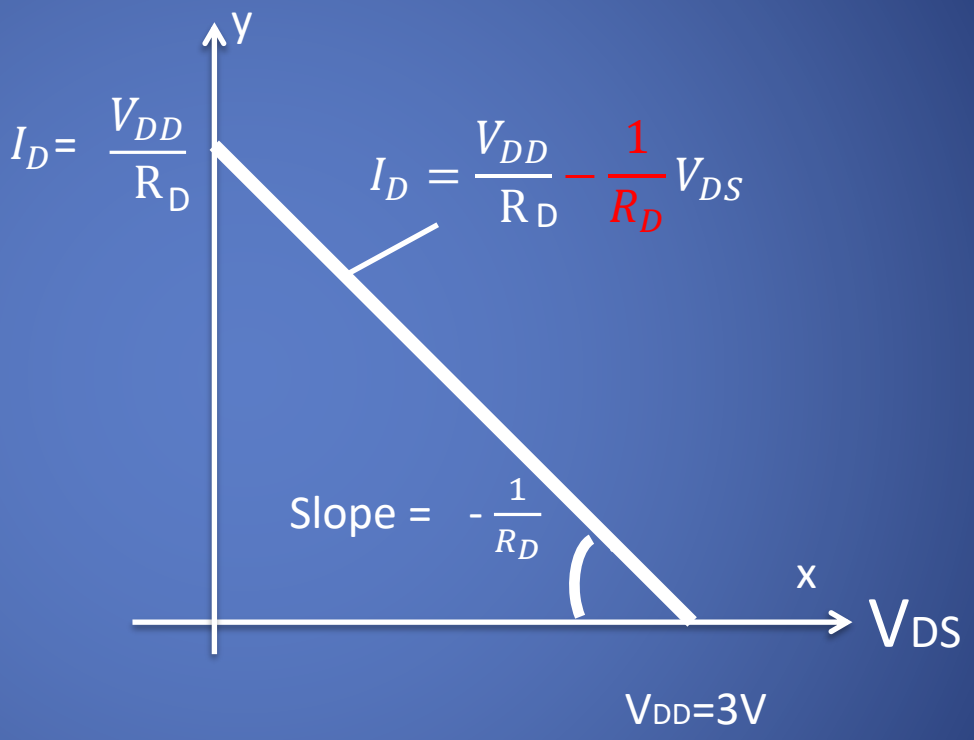
Load Line equation: $V_{DD} = V_{DS} + I_D R_D$

x y plot y(x)

Load resistor converts change of the drain current into change of the output voltage



Output voltage change

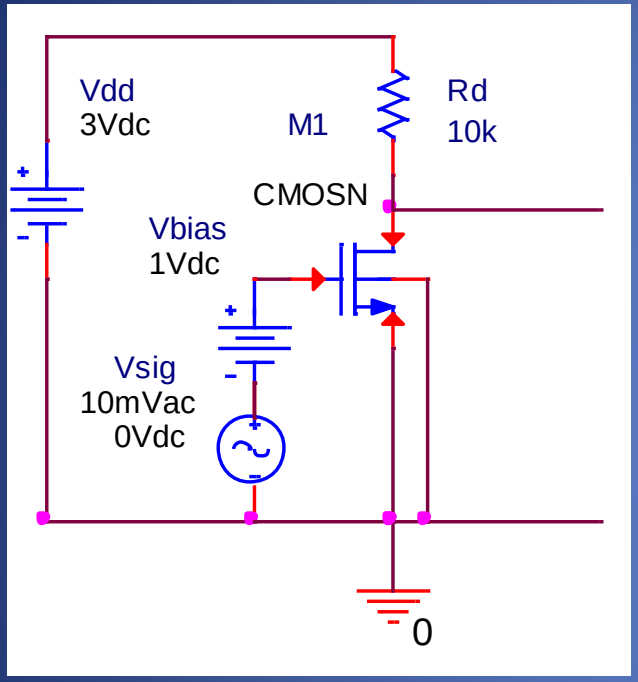


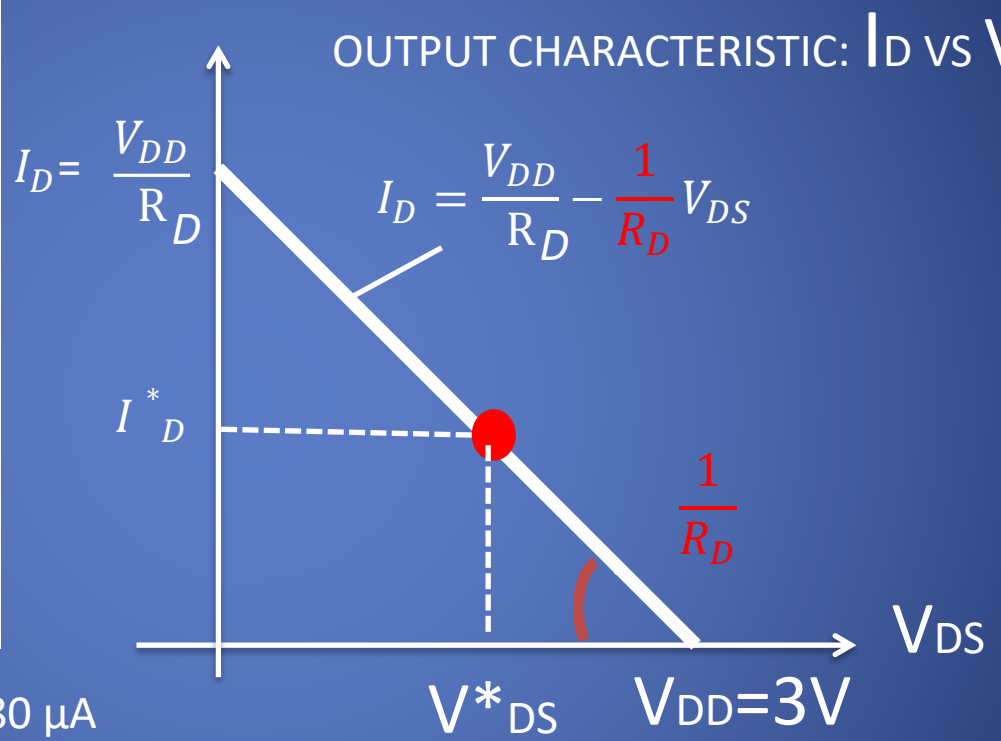
Load Line is the I-V characteristic of the resistive load presented as I_D vs V_{DS}

Let us estimate the MOSFET operating point: V^*_{DS} and I_D

For the drain current we assume that the square law is valid

(the MOSFET operates in the saturation mode)



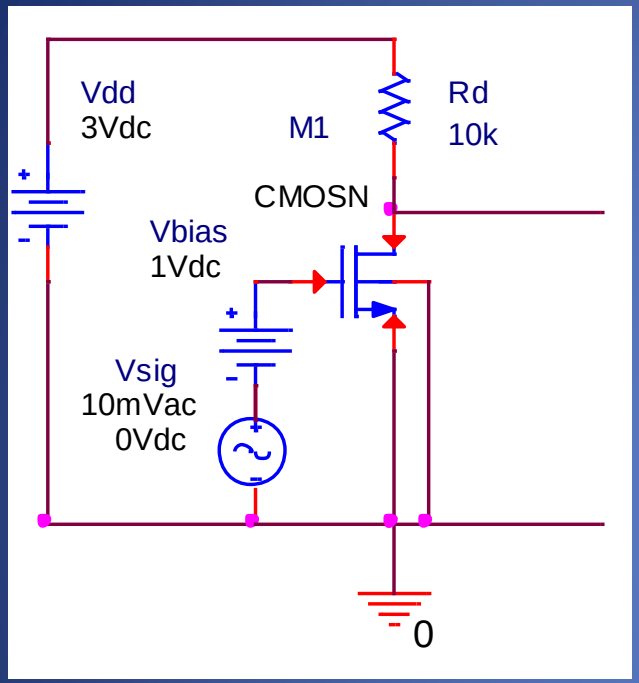


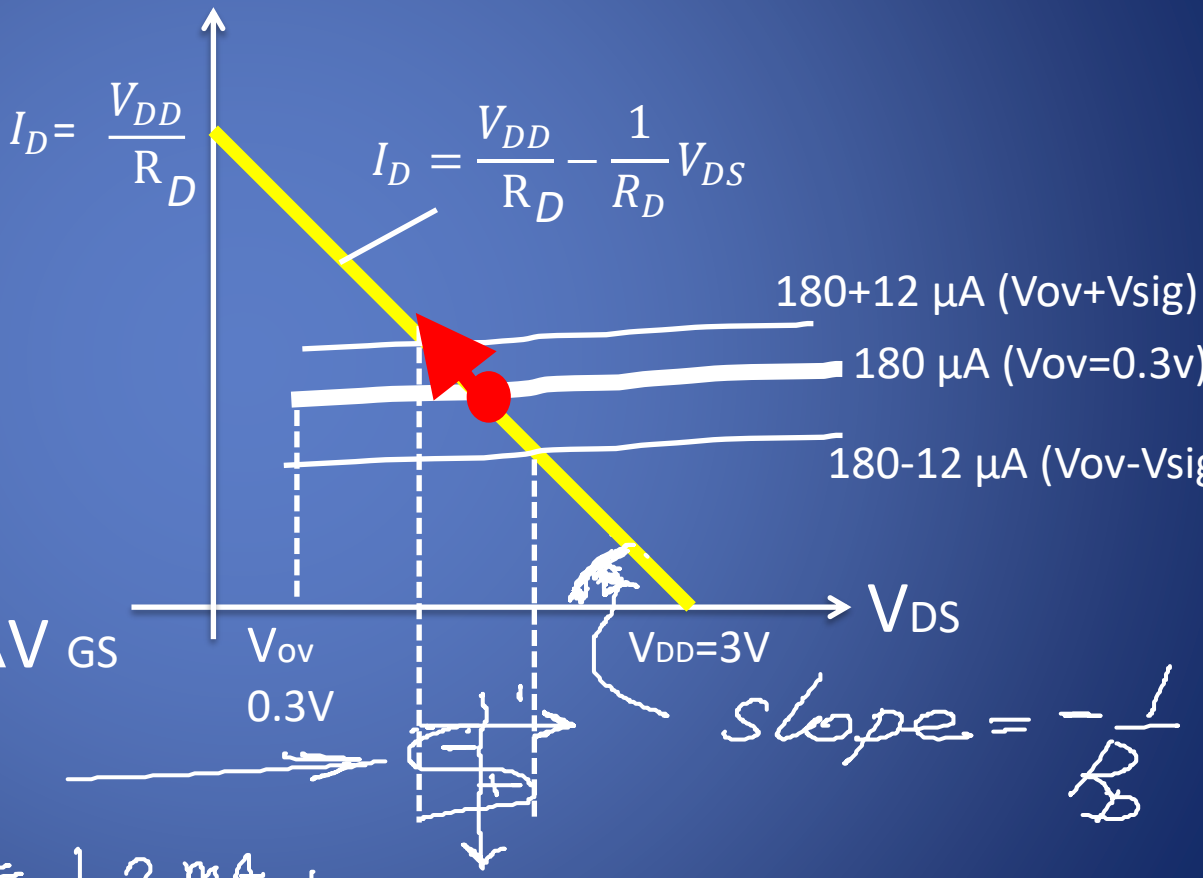
$I^*_D = ½ k_n' (W/L) V_{ov}^2 = 180\ \mu A$

$V^*_{DS} = V_{DD} - I_D R_D = 3 - 0.18\ mA * 10k = 1.2\ V > Vov = 0.3\ V$

Indeed, MOSFET operates in the saturation mode and use of the square low for estimation of the drain current was adequate

With change of I_D the intersection point of the MOSFET output characteristic and the load line moves along the load line, the change of drain current converts to change of V_{DS}:





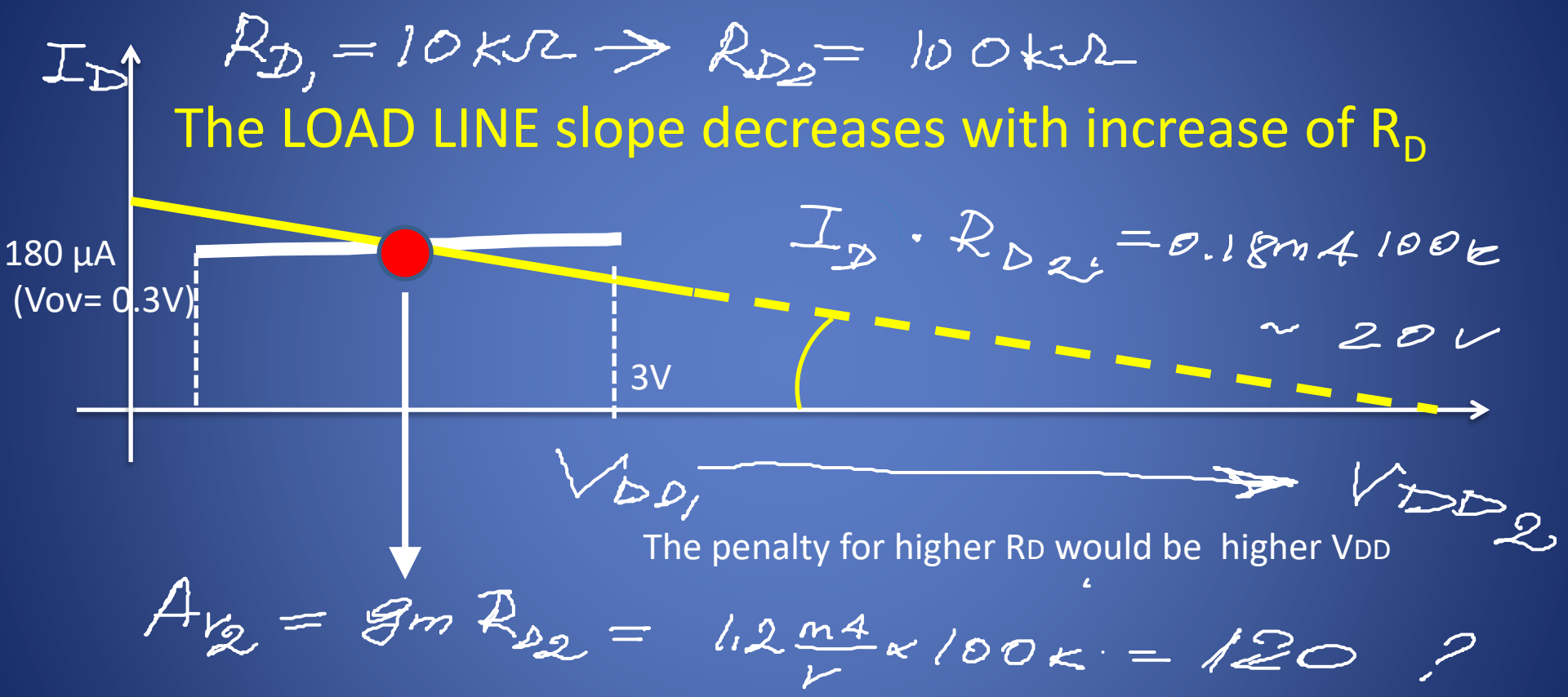
$\Delta V_{DS} = -\Delta I_D R_D = -g_m R_D \Delta V_{GS}$

$|A_v| = g_m R_D = 1.2 \frac{mA}{V} \cdot 10 k\Omega = 12$ times only

slope $= -\frac{1}{R_D}$

One can obtain much greater voltage gain from a single MOSFET stage with use of a current source load constructed with a complementary MOSFET.

Load line for the current source with large resistance RD



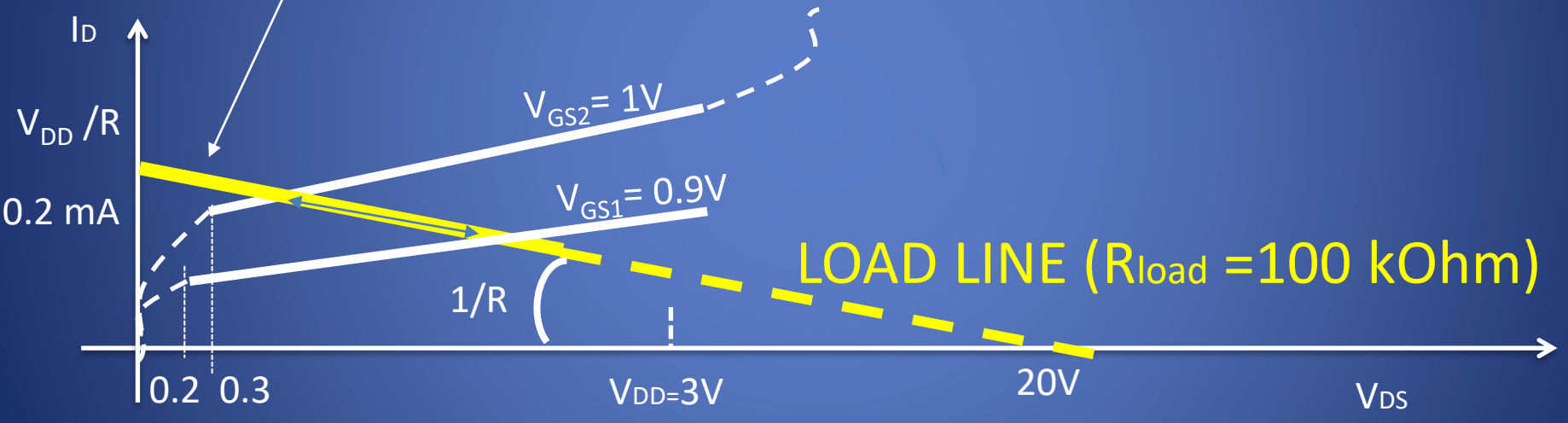
The price for that would be the need in a very high DC voltage source: V_{DD2}
The power would be dissipated inefficiently due to a large voltage drop across R_D.

MOSFETs with a submicron gate length can operate at V_{DD} limited to few volts.

LOAD LINE (in context of a MOSFET gain stage) is the current-voltage characteristic of the MOSFET load which shows the dependence of drain current versus voltage between drain and source terminals : $I_D = f(V_{DS})$

$$V_R = I_D * R = V_{DD} - V_{DS}$$

$$I_D = V_{DD}/R - (1/R) * V_{DS}$$

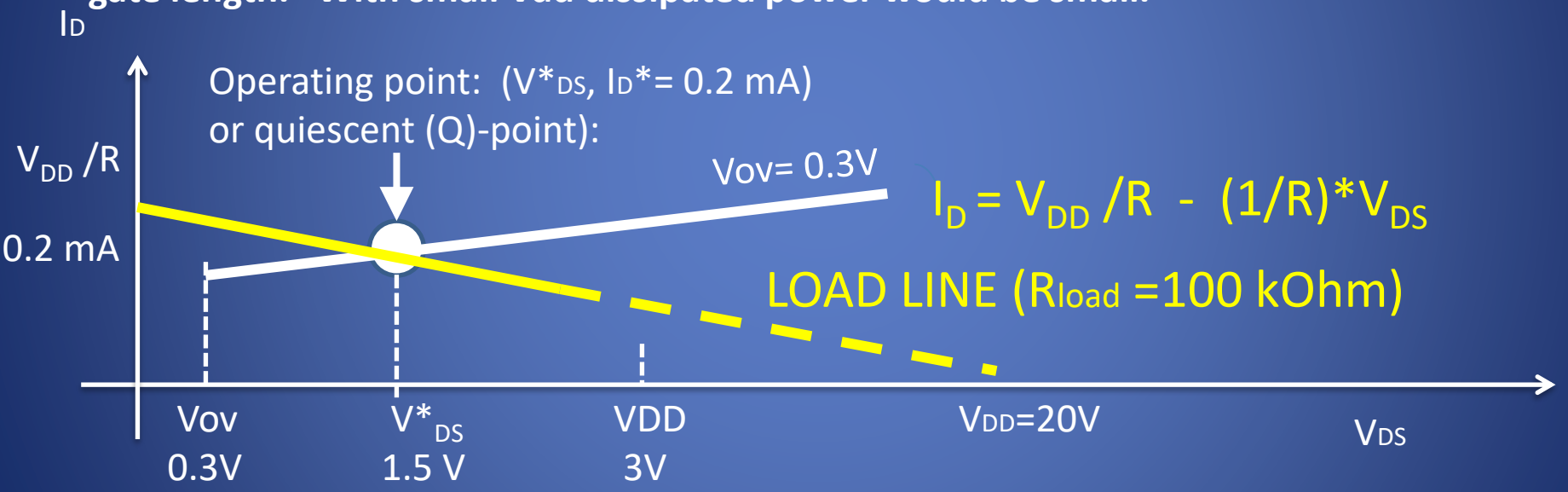


In the following viewgraphs a p-MOSFET will be used as a high resistance load which converts a small AC current to a large AC voltage with a small DC voltage drop across the p-MOSFET load

With a smaller slope of the load line the given change of drain current would result in greater change of the output voltage, and greater voltage gain, respectively.

A small slope could be obtained with a high value of resistive load.
It would result in a large DC voltage drop across it, a large Vdd would be required and large DC power would be dissipated.

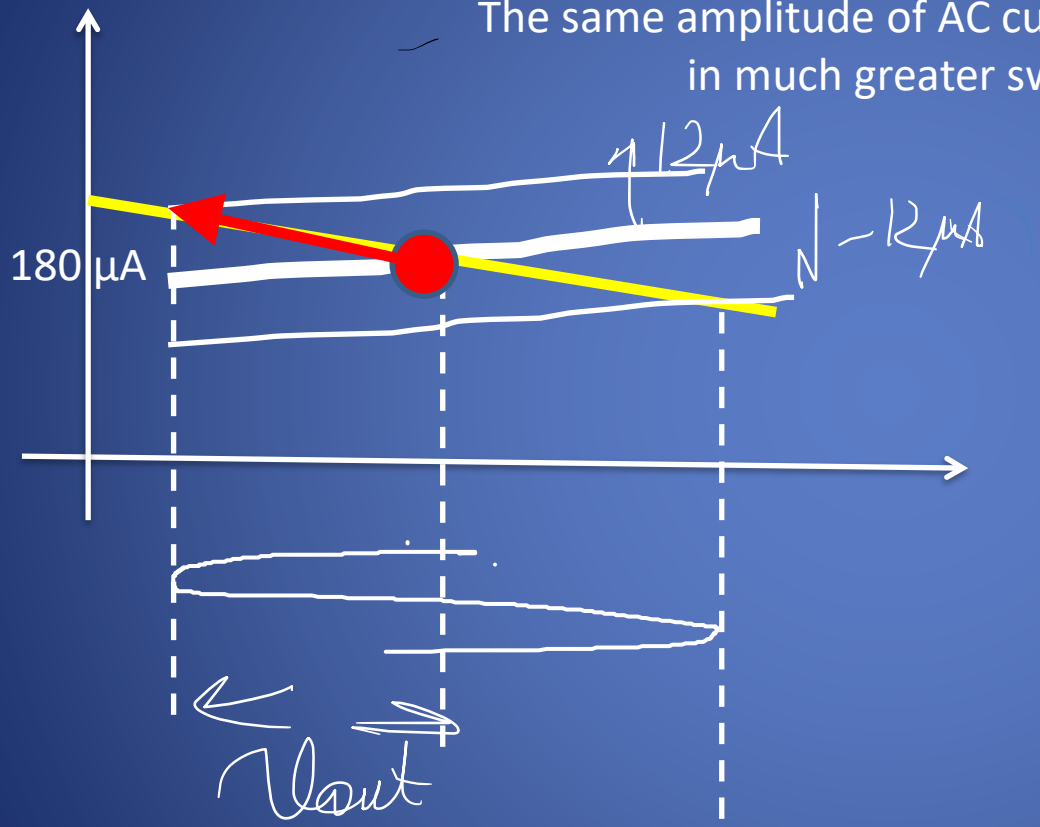
Large V_{DD} is not an option for integrated circuits (IC) because MOSFETs in IC can withstand a relatively small V_{DD}: typically +3 V for the MOSFET technology with a 0.5 um gate length. With small Vdd dissipated power would be small.



In the following viewgraphs a p-MOSFET will be used as a high resistance load which converts a small AC current to a large AC voltage with a small DC voltage drop across the p-MOSFET load

Increase of load resistance increases voltage gain

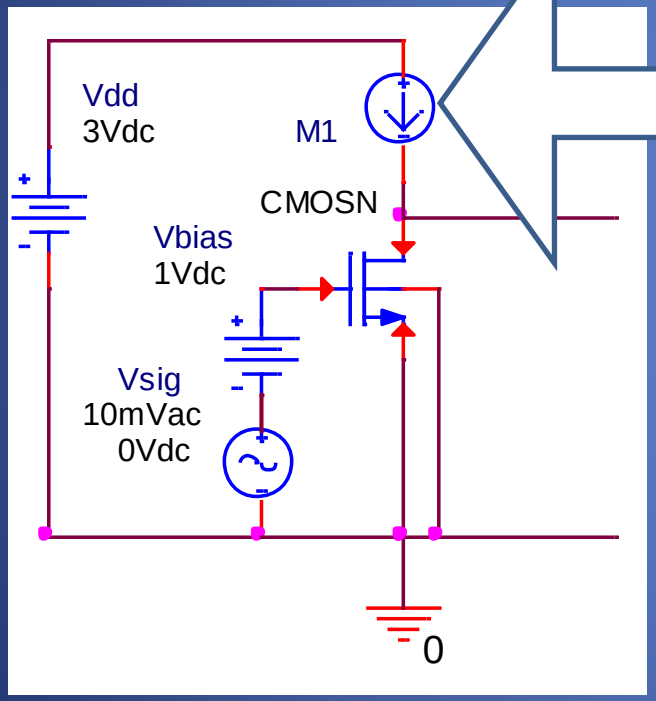
The same amplitude of AC current of 12 µA will results in much greater swing of output voltage



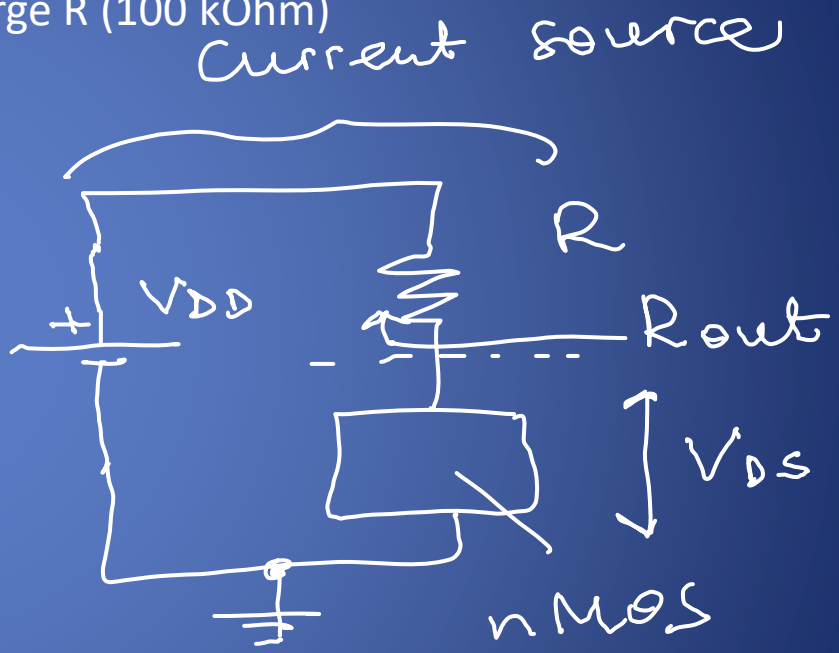
Suppose load resistance R_D was made very large – infinity.
Would the stage show an INFINITE voltage gain?
THE ANSWER IS NO – the stage will achieve a finite gain value – INTRINSIC GAIN Ao

An ideal current source has no current change with change of output voltage.
A good current source can be constructed with large DC voltage source V_{DD} and large resistor R in series.

Target: generation of a 200 uA DC (ideally independent from output voltage)



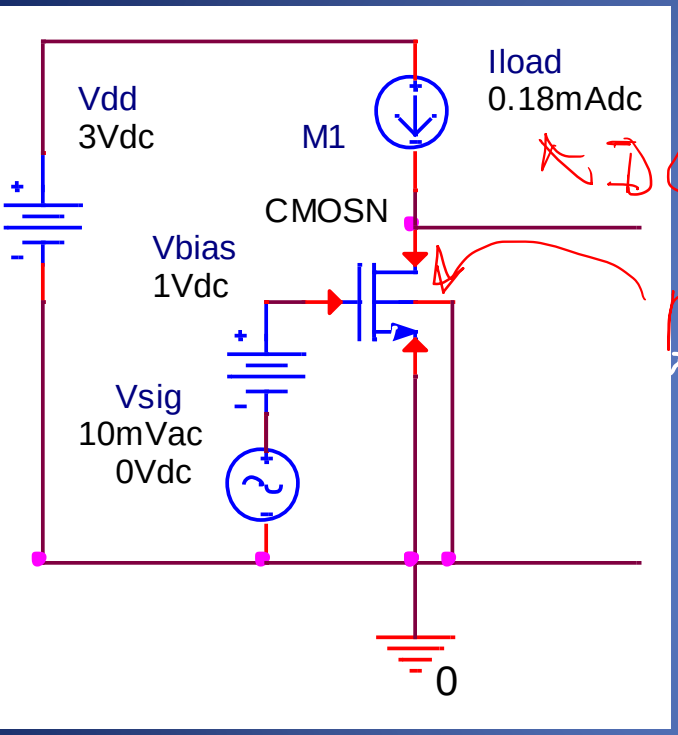
Possible solution: large V_{DD} (20V DC) in series with large R (100 kOhm)



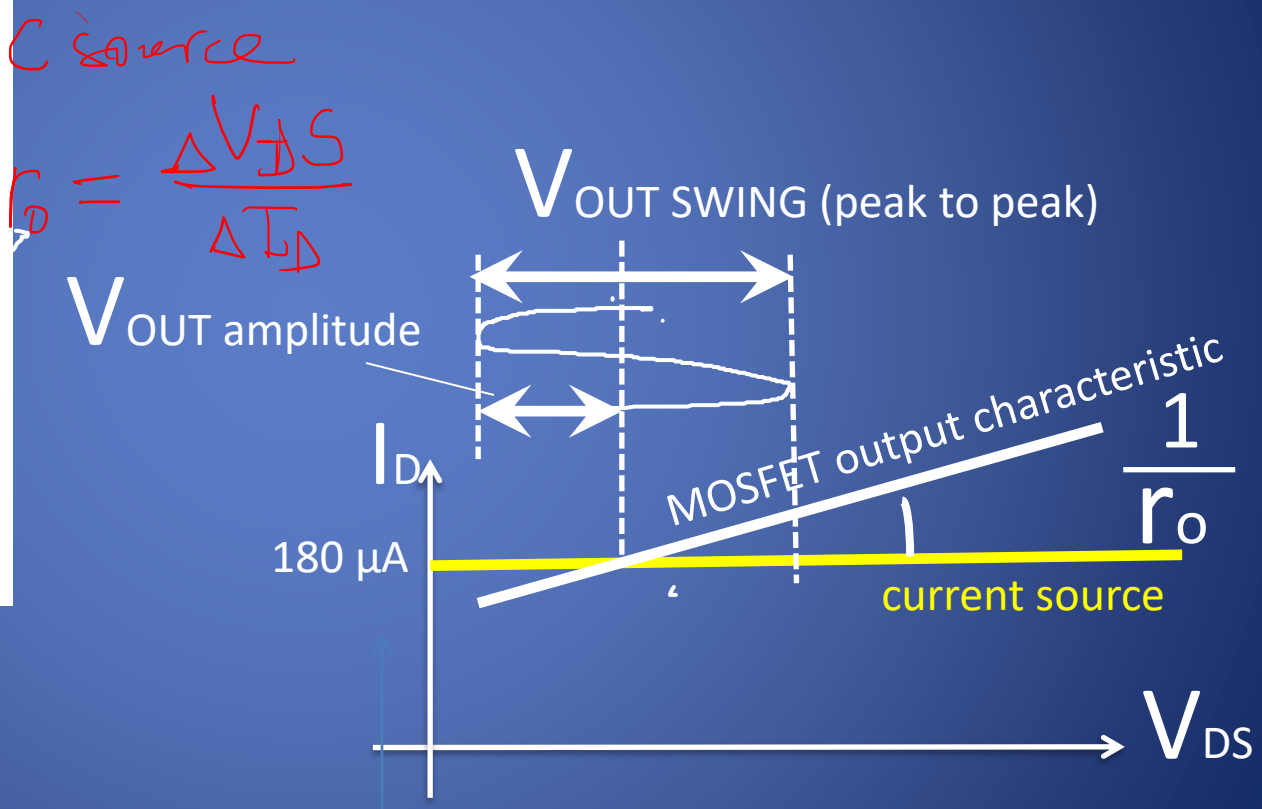
Result: n-MOSFET is loaded with a large R
The gain stage would have large AC voltage gain:
$A_v = g_m R$ = 1.2 mA/V x 100 kOhm = 120

(+) Large voltage gain for AC signal
(-) n-MOSFET with L= 0.5 um can withstand the max V_{DD} = 3 DC

MOSFET output impedance ro

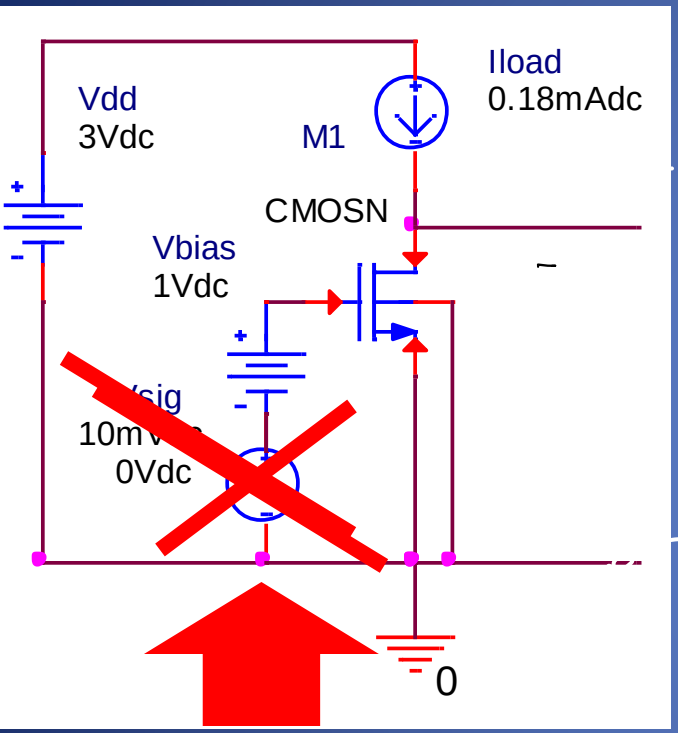


The drain current is supported by current source adjusted EXACTLY to the required value of 180 uA

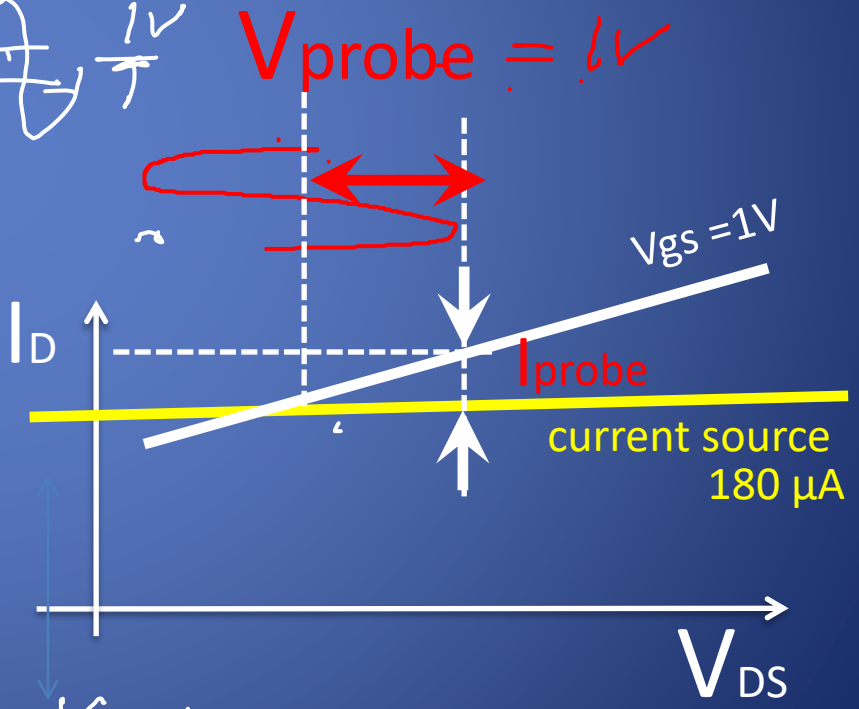


In the stage loaded with an ideal current source the slope of the MOSFET output characteristic itself defines the maximum voltage gain which can be obtained from the stage

Measurement of Output impedance



1. Input signal is disconnected.
2. Probe AC source Vprobe is connected to output of the stage.
3. Vprobe results in some AC current going to the stage output (the MOSFET drain terminal)

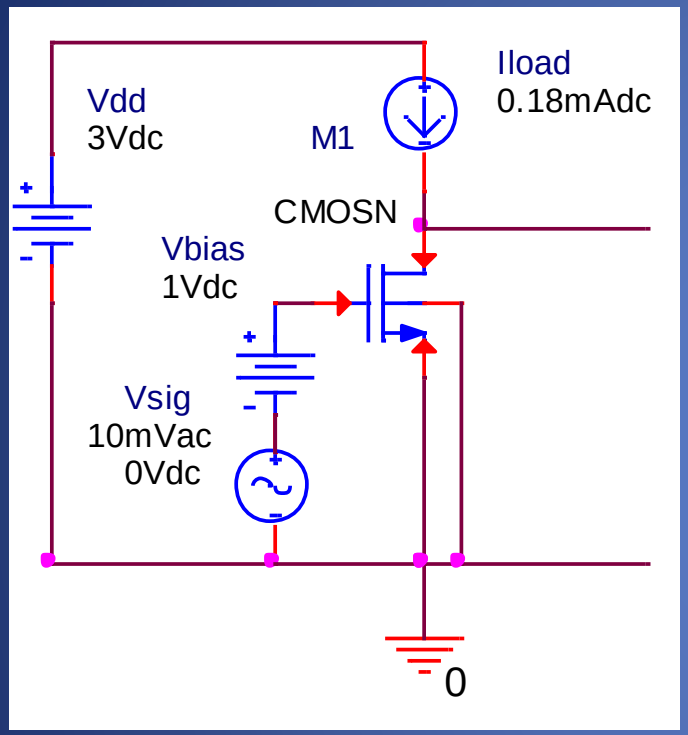


IMPORTANT: the signal source is replaced with a short circuit to convert n-MOSFET under test to a current source

$$r_o = V_{probe}/I_{probe}$$

$$r_o = \frac{V_{probe}}{I_{probe}} = \frac{1V}{10\mu A} = 100\,k\Omega$$

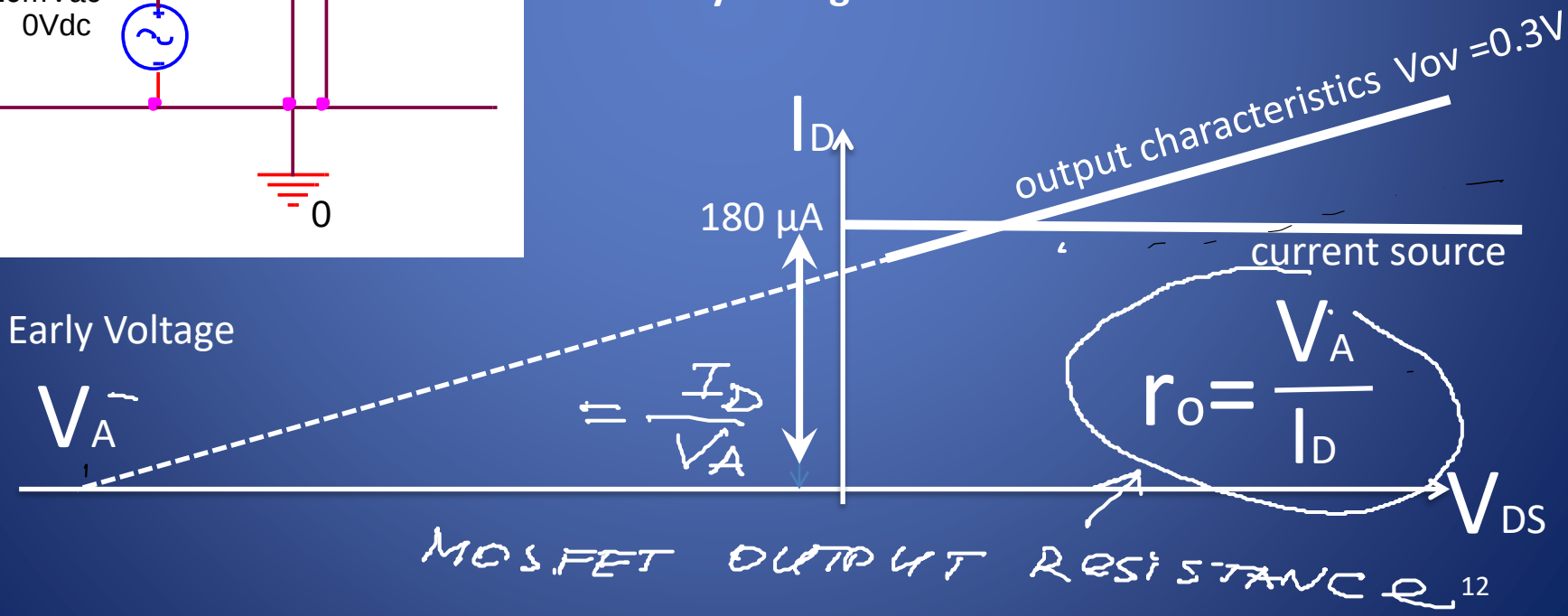
Designing MOSFET with required r_O: Early voltage V_A



The output characteristic can be approximated by a linear dependence.

Extrapolation of the line to negative range of V_{DS} defines the Early voltage

Output resistance can be estimated with a ratio of the Early voltage and the drain current



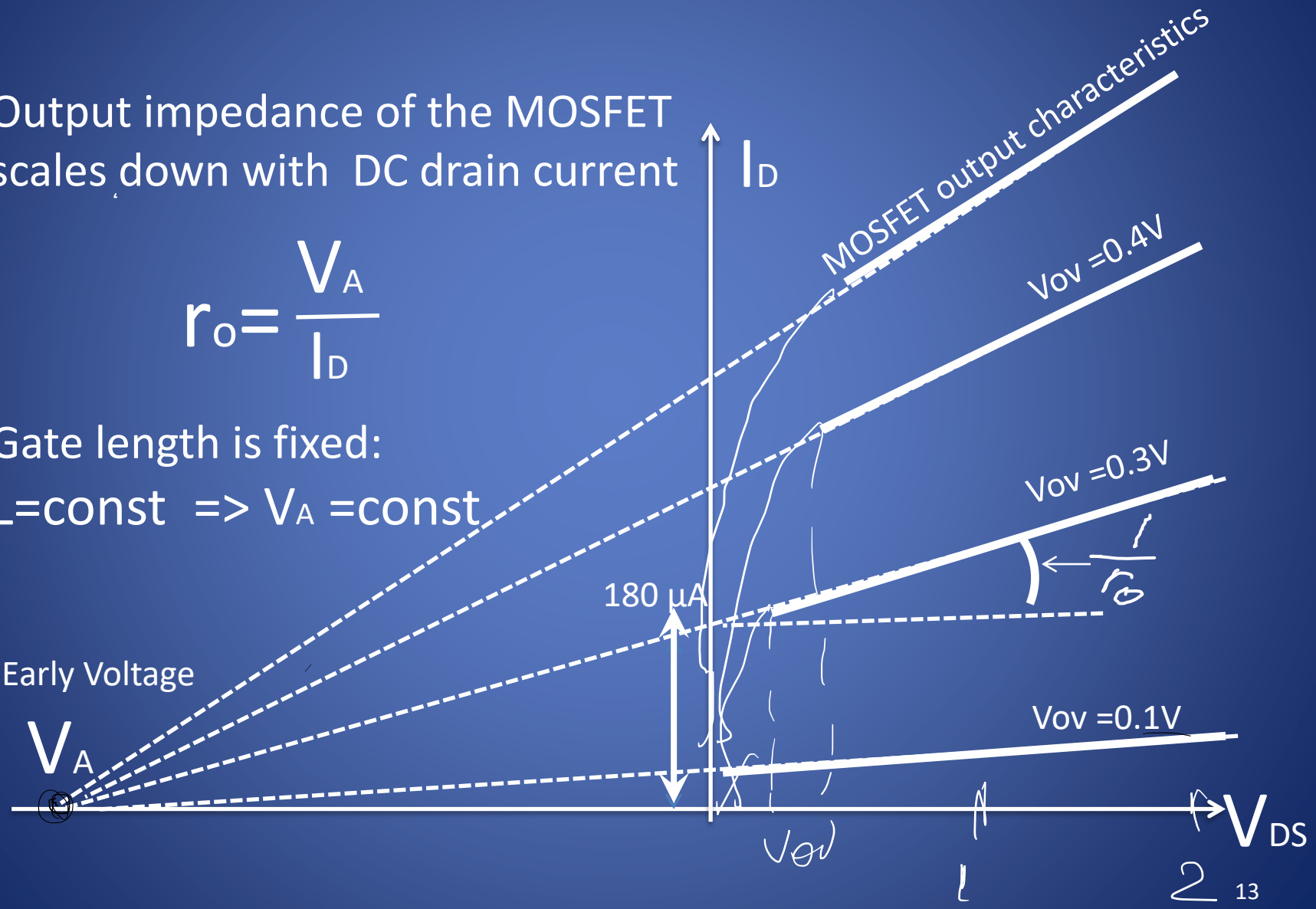
Early voltage V_A is a design parameter

Output impedance of the MOSFET scales down with DC drain current

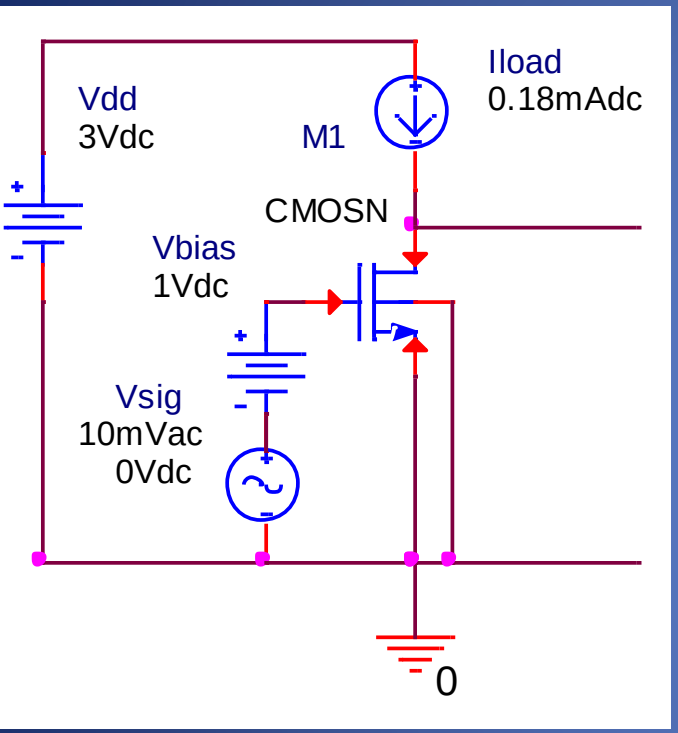
$$r_o = \frac{V_A}{I_D}$$

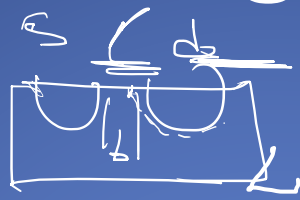
Gate length is fixed:

L=const => V_A =const



Effective gate length depends on V_{DS}



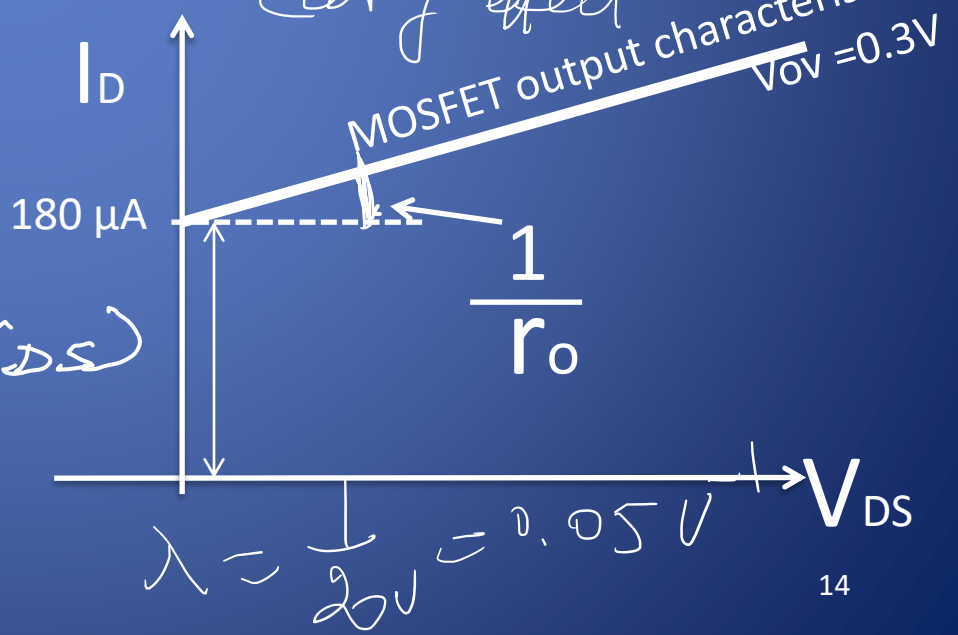


$L_{eff} \rightarrow L - \Delta L(V_{DS})$

$$I_D = \frac{1}{2} k_n' \frac{W}{L - \Delta L} V_{ov}^2$$

$$I_D = \frac{1}{2} k_n' \frac{W}{L} V_{ov}^2 \left(1 + \frac{V_{DS}}{V_A}\right)$$

Early effect



$$I_D = \frac{1}{2} k_n' \frac{W}{L} V_{ov}^2 (1 + \lambda V_{DS})$$

Lambda $\lambda = \frac{1}{V_A}$

$V_A = 20V$

$\lambda = \frac{1}{20V} = 0.05\,V$

Early voltage parameter V_A' is a process parameter

In order to increase the Early voltage V_A one can increase the gate length L

.

$$V'_A = \frac{V_A}{L} = \text{const}$$

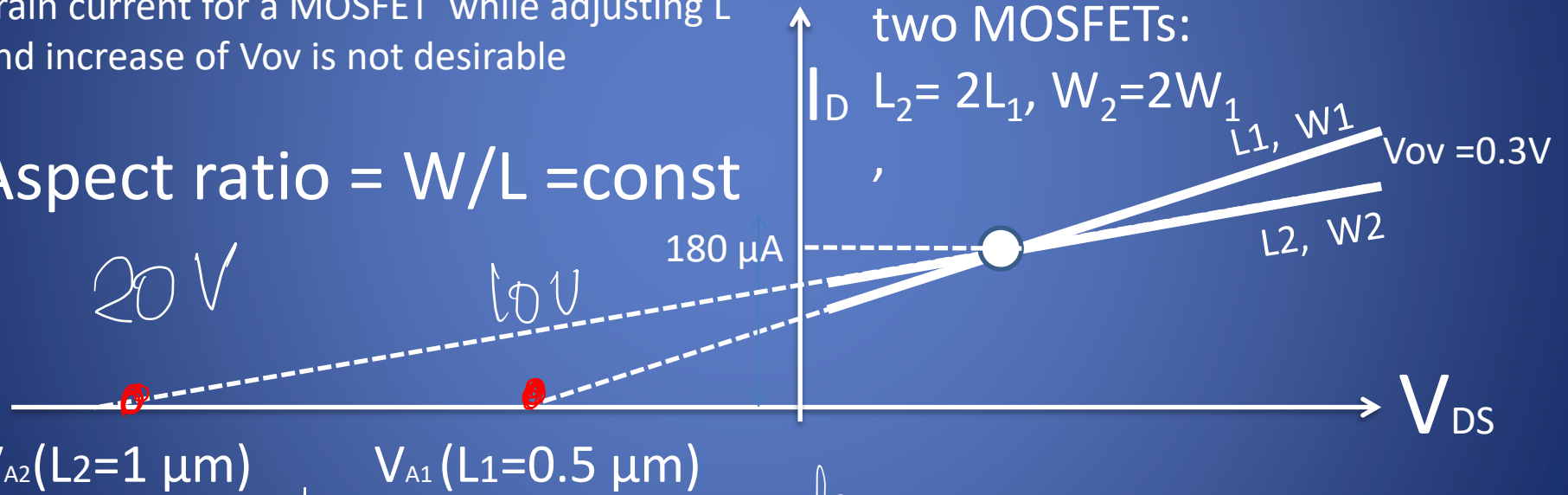
Often designs require to keep the same drain current for a MOSFET while adjusting L and increase of Vov is not desirable

Aspect ratio = W/L =const

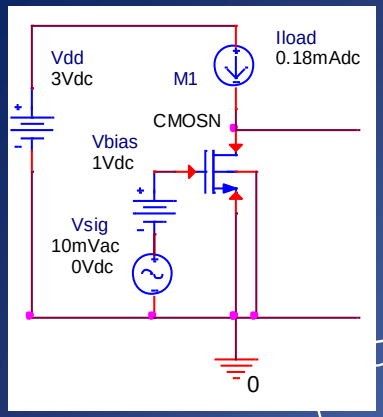
Output characteristics of two MOSFETs:

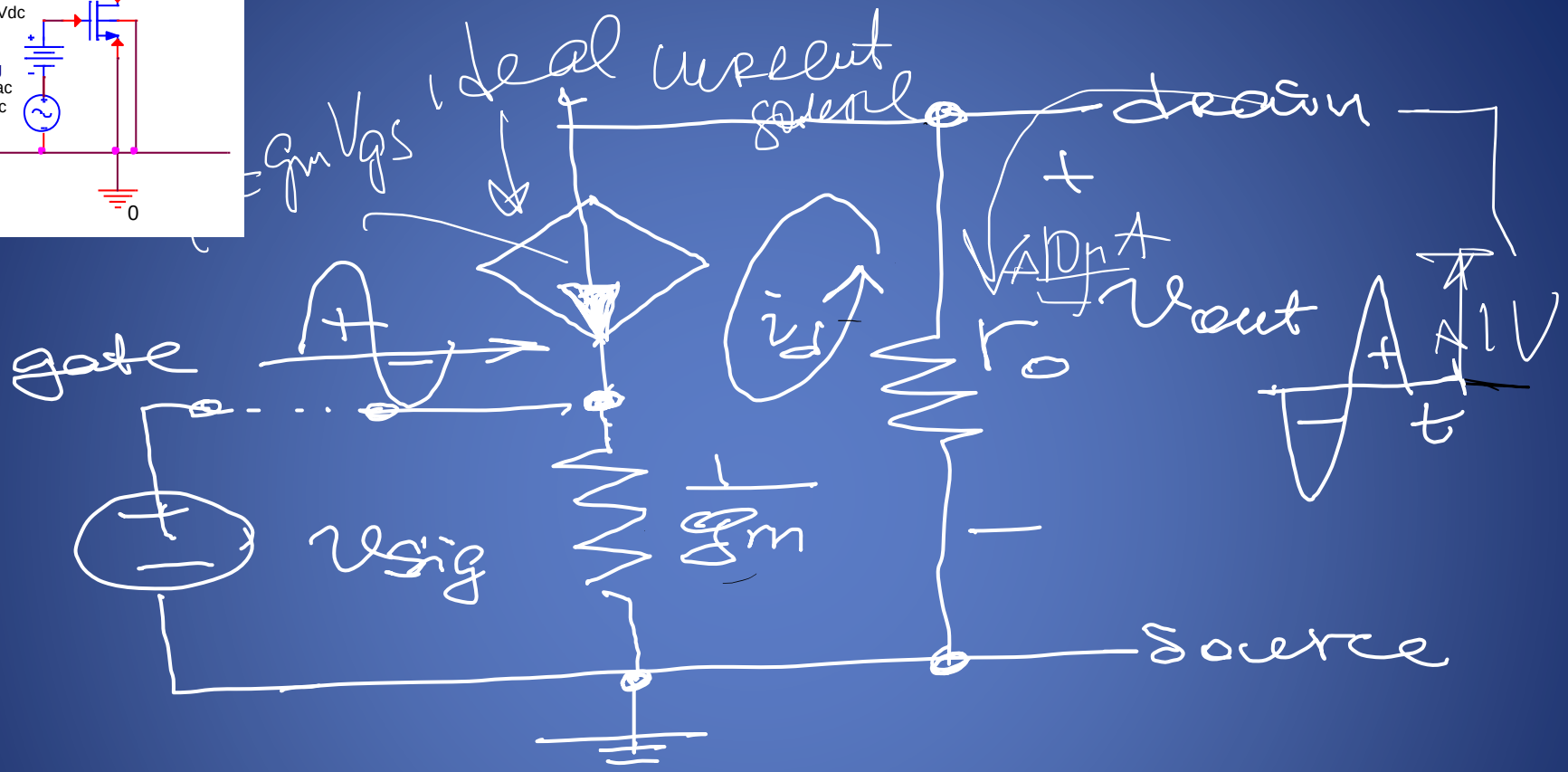
$L_2 = 2L_1$, $W_2 = 2W_1$

,



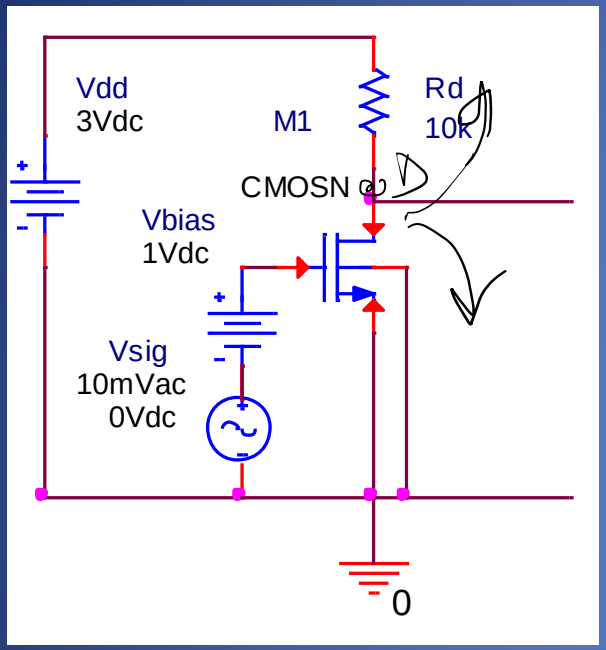
Improved small-signal model (T-model)



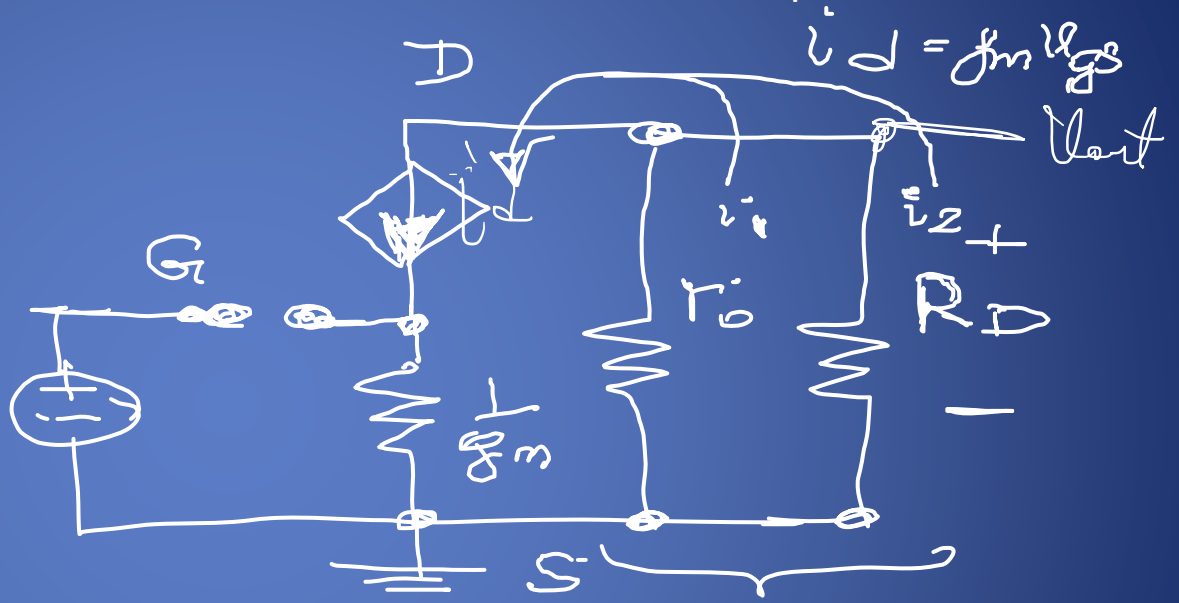


For AC signals DC voltage sources represent short circuits (i.e., V_{DD} ⇔ Ground) and DC current sources represent open circuits (no AC current can flow through them). The output voltage is measured between the drain (+) and ground (-): since the AC component of the drain current enters negative terminal of the resistor, output voltage has to have negative sign (it is indeed inverted): $V_{out} = - r_o I_d = -g_m r_o v_{sig}$.

Role of R_D in voltage gain A_v



Since Vdd⇔Ground, r_o and R_D are in parallel for AC



$$i_d = i_1 + i_2$$

$$R_{eq} = \frac{r_o \cdot R_D}{r_o + R_D}$$

$$A_v = g_m R_{eq}$$

$$R_{equiv} = (r_o \,||\, R_D)$$

$$A_v = A_o \cdot \frac{R_D}{r_o + R_D}$$

Often R_D is selected to be matching r_o: in the latter case $A_v = A_o/2$

Early voltage parameters in n- and p-MOSFETs

n-MOS

$V_{An}' = 20\,V/\mu m$

$L_n = 0.5\,\mu m$

$V_{An} = V_{An}' \cdot L_n = 10\,V$

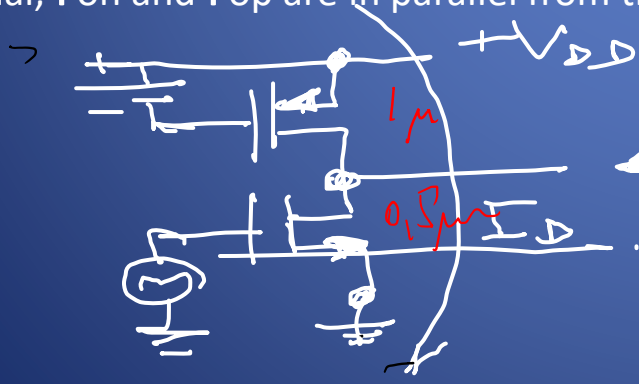
p-MOS

$V_{Ap}' = 10\,V/\mu m$

$L_p = 1\,\mu m$

$V_{Ap} = V_{Ap}' \cdot L_p = 10\,V$

Often in circuits n-MOS and p-MOS transistors are connected in a chain and therefore have the same drain current. It will be reasonable to select gate lengths for n-MOS and p-MOS transistors to have similar V_A to have n-MOS and p-MOS with similar output impedances (since Vdd⇔ Ground for AC signal, r_{on} and r_{op} are in parallel from the point of view of AC signals).



$I_D = I_n = I_p$

$r_{on} = r_{op}$

$R_{out} = r_{on} \parallel r_{op} = \frac{r_o}{2}$

$R_{out} \simeq \frac{10\,V}{0.2\,mA \cdot 2} = 25\,k\Omega$