EEO335

Spring 2024

# Delta-Sigma Modulator

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# Copy of Original Assignment

**Assignment 9 - Delta-Sigma Modulator**

This Assignment aims at verifying and expanding, with experiments and supporting simulations, your knowledge and understanding of delta-sigma modulators.

Please document each step with snapshots, pictures, and your observations. Please make visible on WaveForms the date and time fields (top left) and the serial number (bottom right) of your Analog Discovery. Also, please include this page.

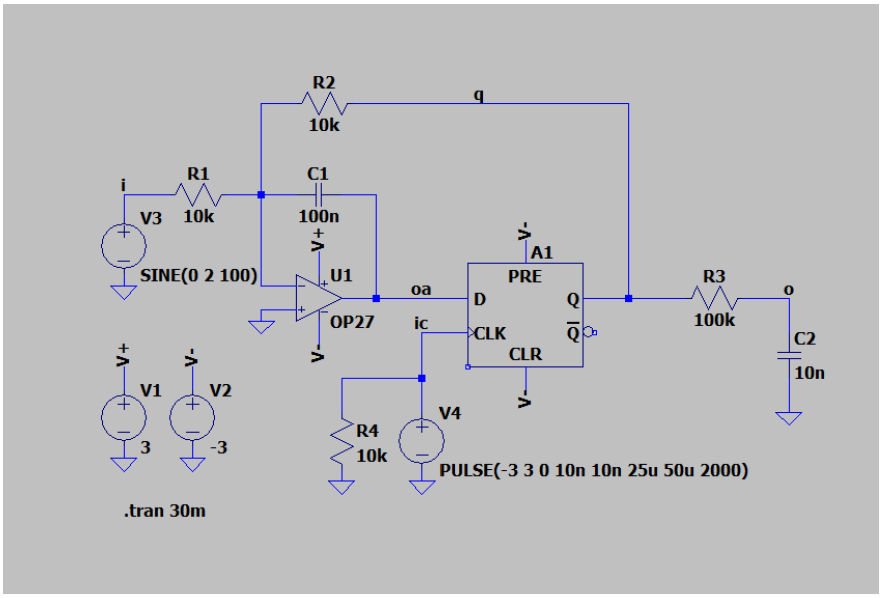


Figure 1

1) Using the simulator, design the circuit shown in Fig. 1 (**30pts**)

a) simulate and show the input and the response at the output

b) observe and report the impact of changing the clock (PULSE) frequency to 10kHz, 20kHz, 50kHz and 100kHz (keep 50% duty cycle)

c) explain in your own words how the circuit operates

Note: the DFF can be found in the Digital library, recommended settings Vhigh=3 Vlow=-3 Trise=10n Tfall=10n)

2) Build the circuit at (1) and experimentally reproduce the simulations (**70pts**)

Note1: you can use the 74LS74 or the 74HC74

Note2: pay attention to the PRE and CLR – depending on the model they can be either active-high (as in the schematics) or active-low

# Overview

In this lab, we design and analyze a delta-sigma modulator circuit using simulation software. By simulating the circuit, we observed the input-output relationship and explored the effects of varying the clock frequency. Then, we build the circuit using hardware components and replicate the experimental results. This lab reinforces our understanding of delta-sigma modulation through theoretical design and practical experimentation.

# 1 Using the simulator, design the circuit shown in Fig. 1

## a)

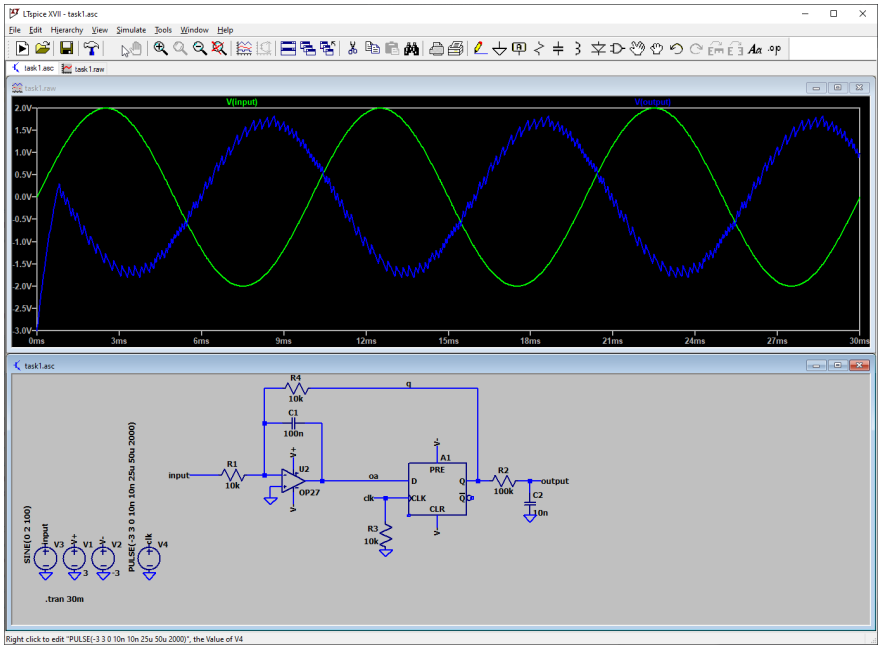


Figure 1: simulate and show the input and the response at the output

## b)

By increasing the clock frequency from 10 kHz to 20 kHz to 50 kHz and then to 100 kHz a trend can be observed. The output accuracy improves with higher clock frequencies. With lower sampling frequencies, there is more uncertainty in the measurement result.

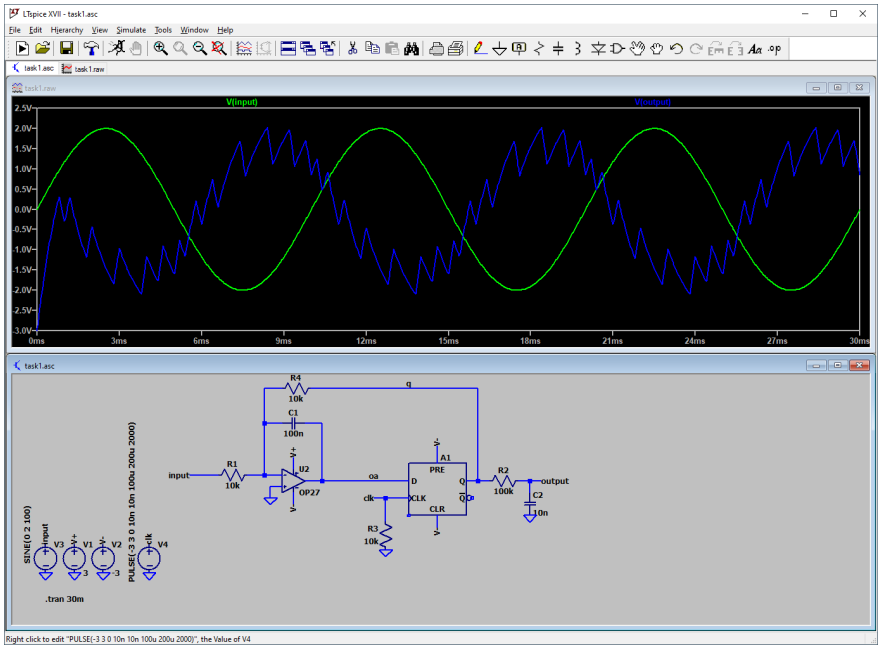


Figure 2: Simulation performance shown at 10 kHz.

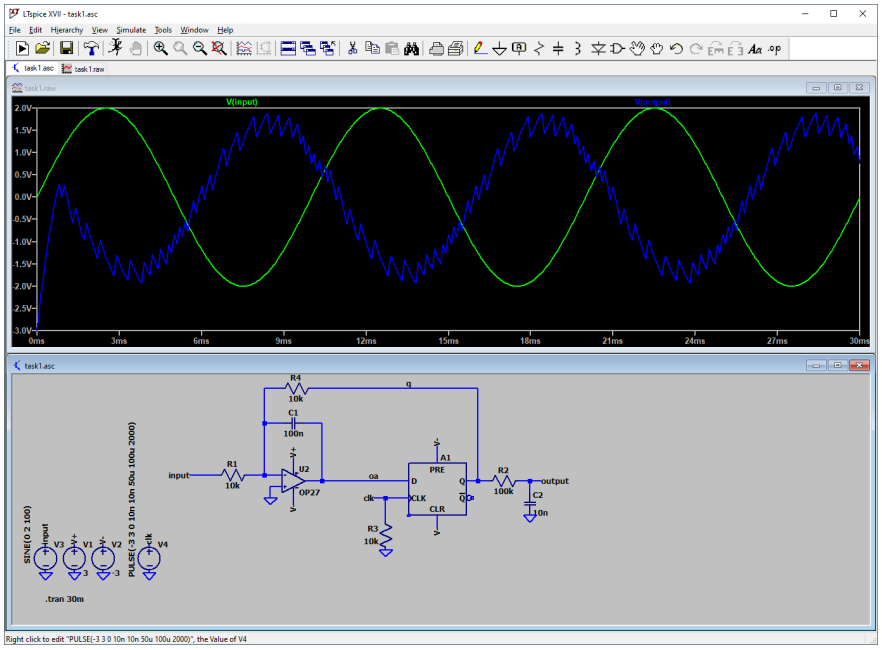


Figure 3: Simulation performance shown at 20 kHz.

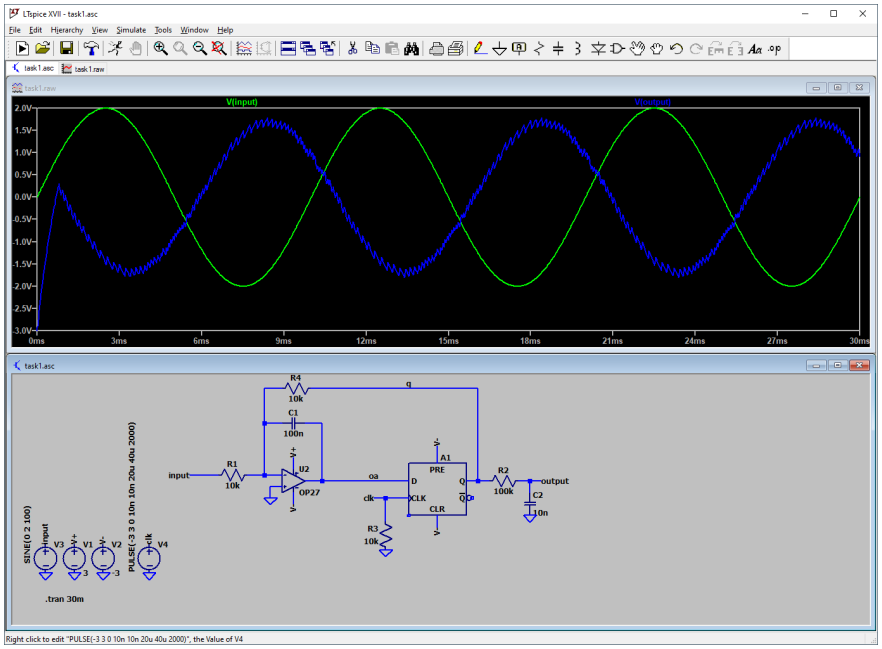


Figure 4: Simulation performance shown at 50 kHz.

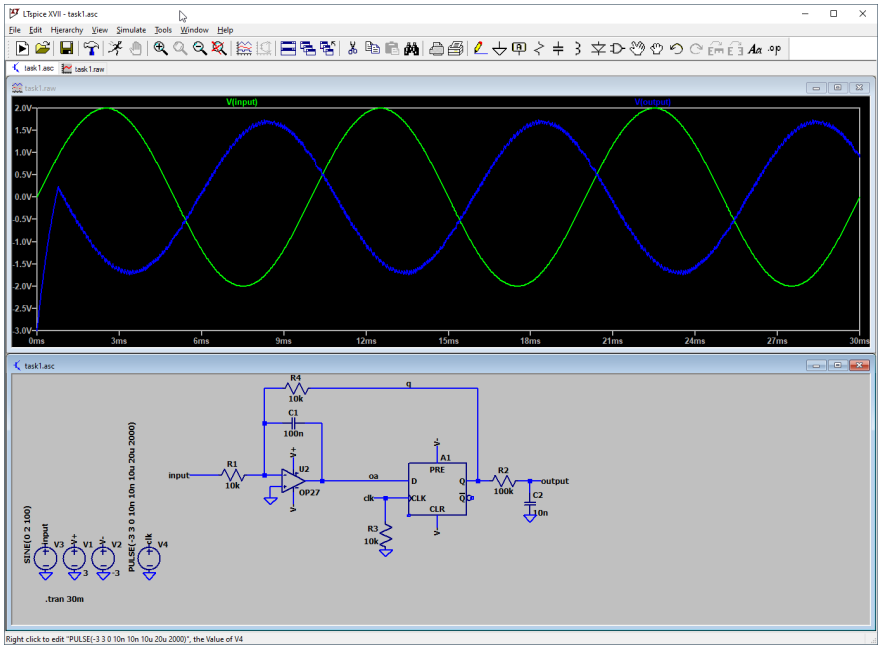


Figure 5: Simulation performance shown at 100 kHz.

## c)

A delta sigma modulator has several block functions. To form the sigma portion, the op27 op-amp and capacitor C1 form an integrator function. To form the delta portion, a difference function is formed at the negative input of the op-amp.

At the moment a clock signal arrives on the DFF clk pin, the input at D is relayed out to Q. This signal is fed back to the negative input of the opamp to calculate the difference in the input signal to output.

As described, these differences are continuously summed (integrated) at a rate proportional to the clock frequency. By increasing the number of samples, any error present becomes less significant and therefore, the system can achieve a high accuracy.

## 2 Build the circuit at (1) and experimentally reproduce the simulations

The experimental circuit comes very close to replicating the results of the simulation. The clock frequency affects the output quality in the same way as seen in the simulation.

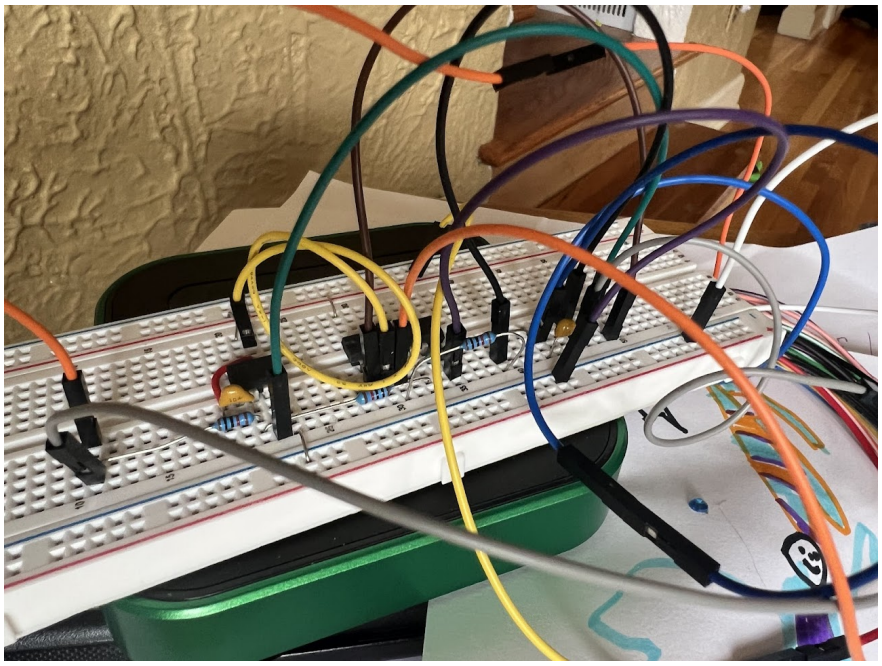

Figure 6: Photo of circuit

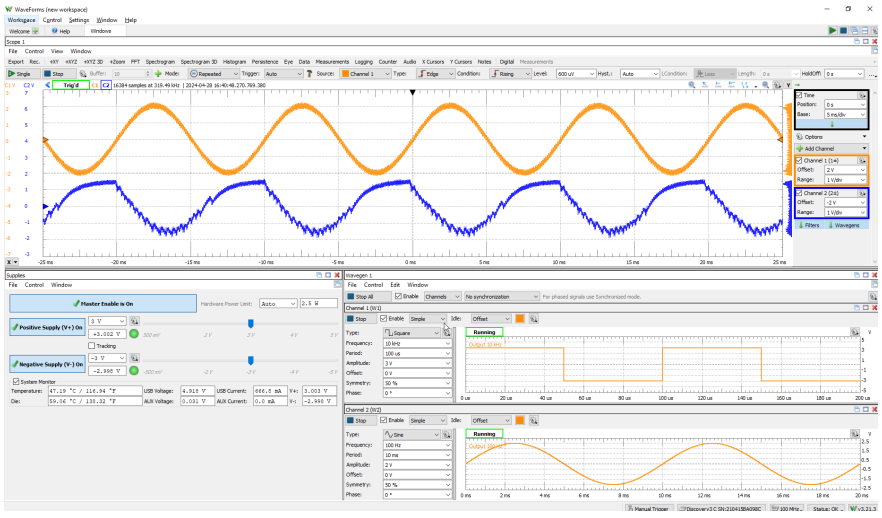

Figure 7: Experimental performance shown at 10 kHz.

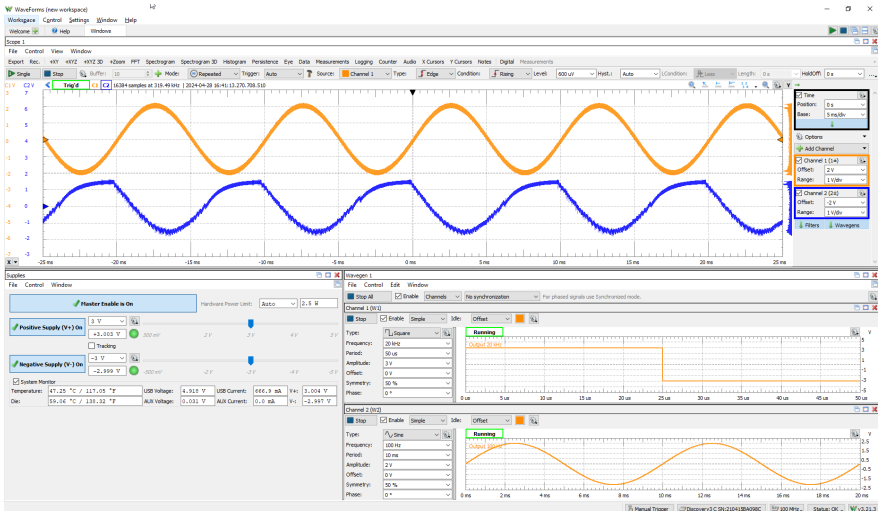

Figure 8: Experimental performance shown at 20 kHz.

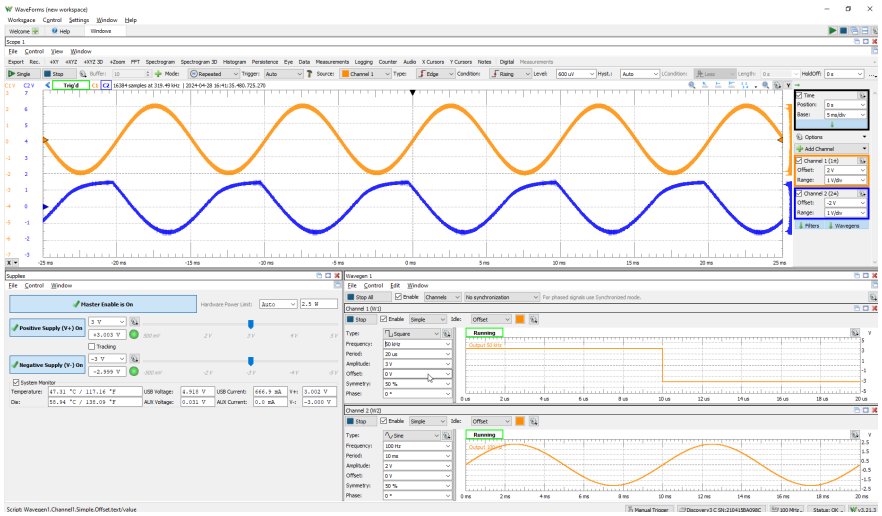

Figure 9: Experimental performance shown at 50 kHz.

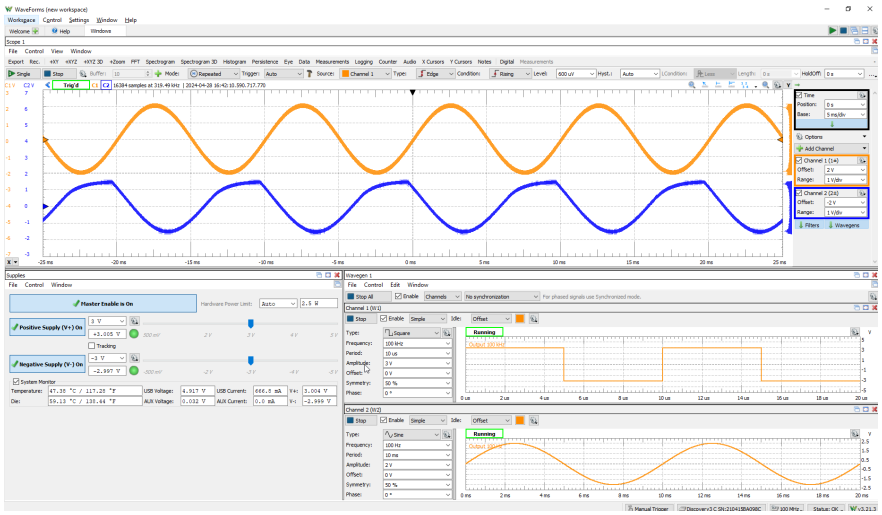

Figure 10: Experimental performance shown at 100 kHz.