EEO 352 Fall 2023 - Assignment 5 – Counters

Please document each step with snapshots of the built circuit, plots, pictures and your observations. Please include this page.

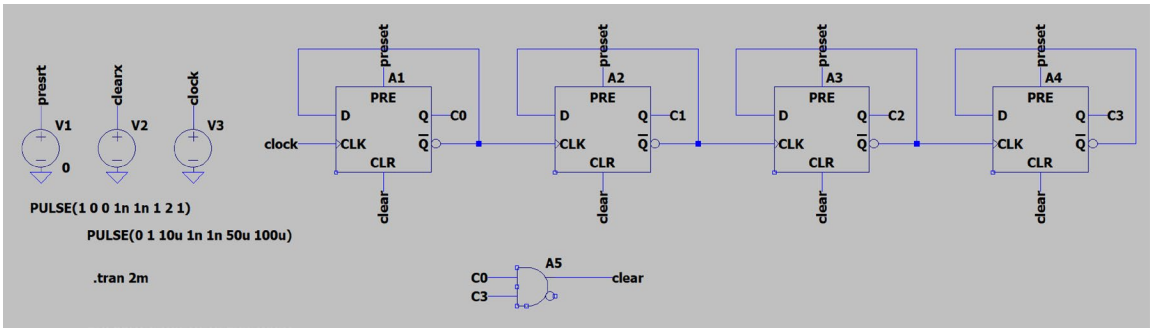

Fig.1a

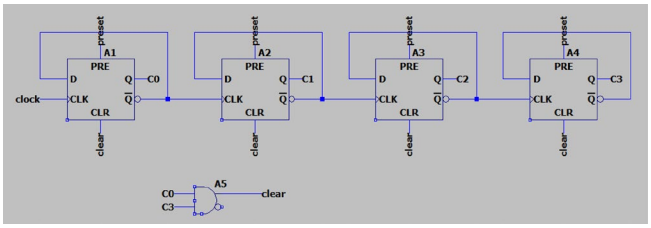

Fig.1b

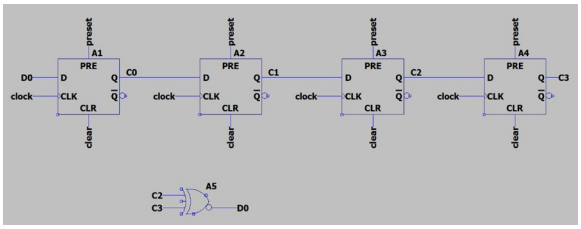

Fig.1c

1) Using the components in the Digital library, design and simulate as follows, plotting the clock and the four outputs in separate panes (**25pts**):

a) Divide-by-16 counter as shown in Fig.1a

b) Divide-by-9 counter as shown in Fig.1b

c) Pseudorandom counter as shown in Fig.1c

Note1: The LTspice ideal DFLOP triggers on the positive edge of CLK, and the PRE and CLR are active high

Note2: In order to avoid simulator convergence issues, set Trise=1ns and Tfall=1ns in all digital gates.

Note3: Use a 10kHz clock and clear all flip-flops at the beginning of the simulation.

2) Using two 74LS74, one 74LS00 and one 74LS86, build and measure the circuits at (1a), (1b) and (1c), plotting the clock on the oscilloscope and in the logic analyzer, and the four outputs in a bus, which shows the counts using the logic analyzer of the Analog Discovery (**75pts**).

Note1: Use a +5V supply and ground.

Note2: In the 74LS74 the PRE and CLR are active low: connect both to +5V

Note3: In order to start the psudorandom counter, you may need to temporarily force D of the first flip-flop high, and then move D back to the output of the XOR.