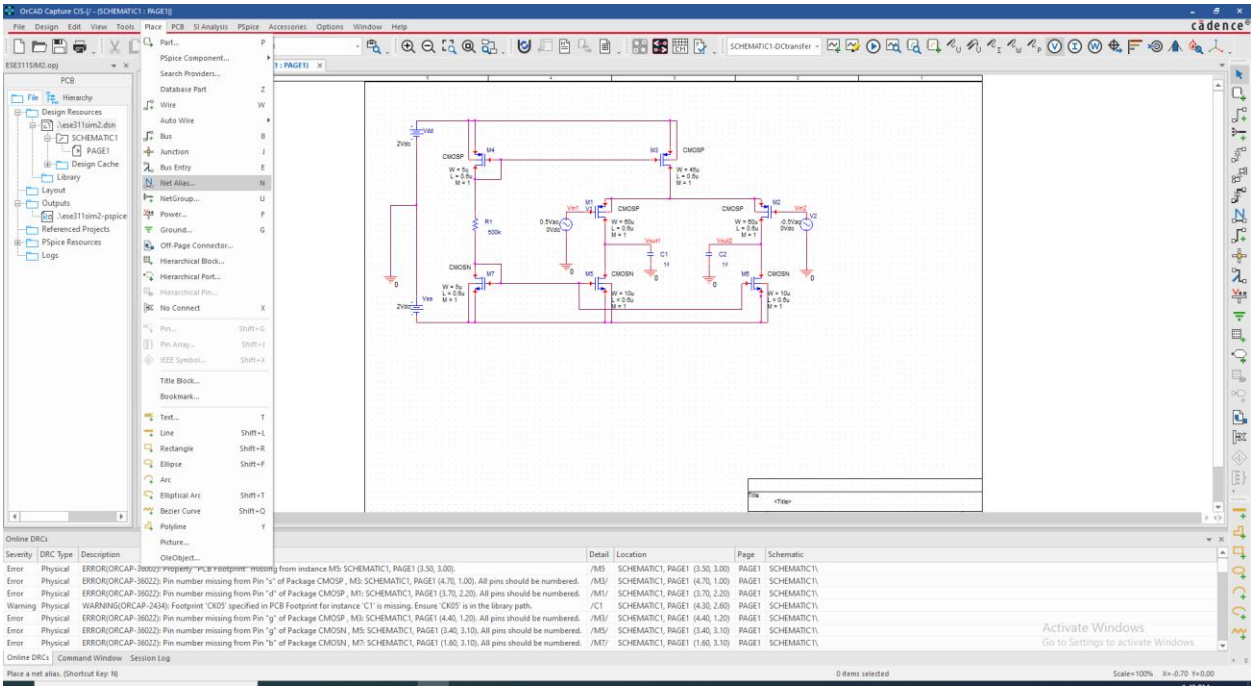
# Simulation 2 in examples

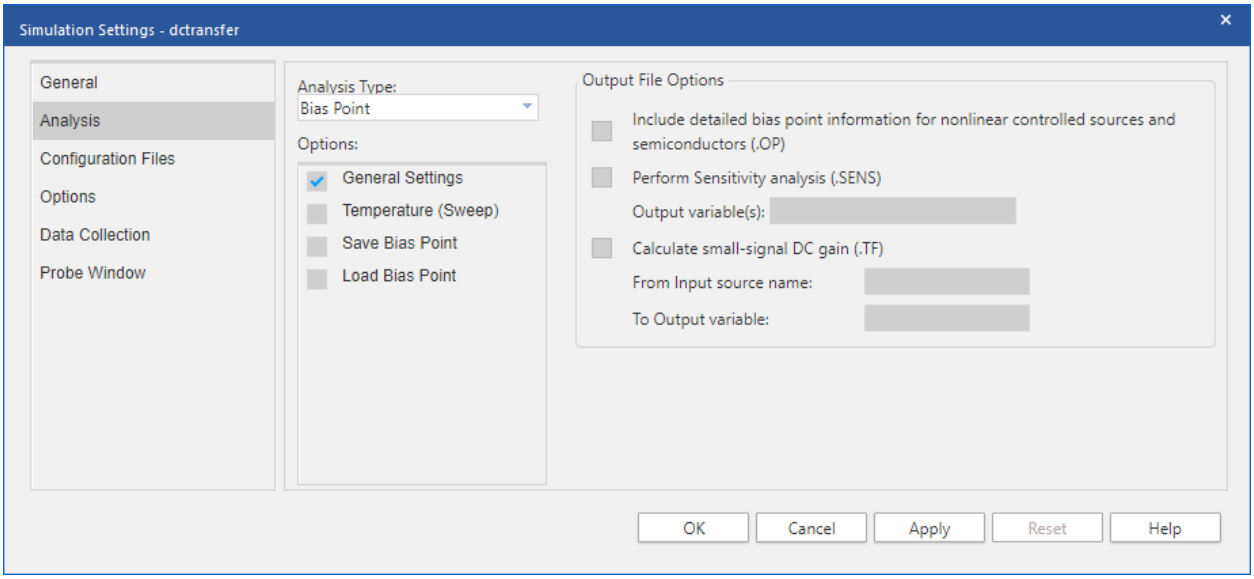
Name the nets (wires) to be used in plots: Vin1, Vin2, Vou1, Vout2:

Press N, type the name (Vou1) and place the marker on the left output wire in the schematic.

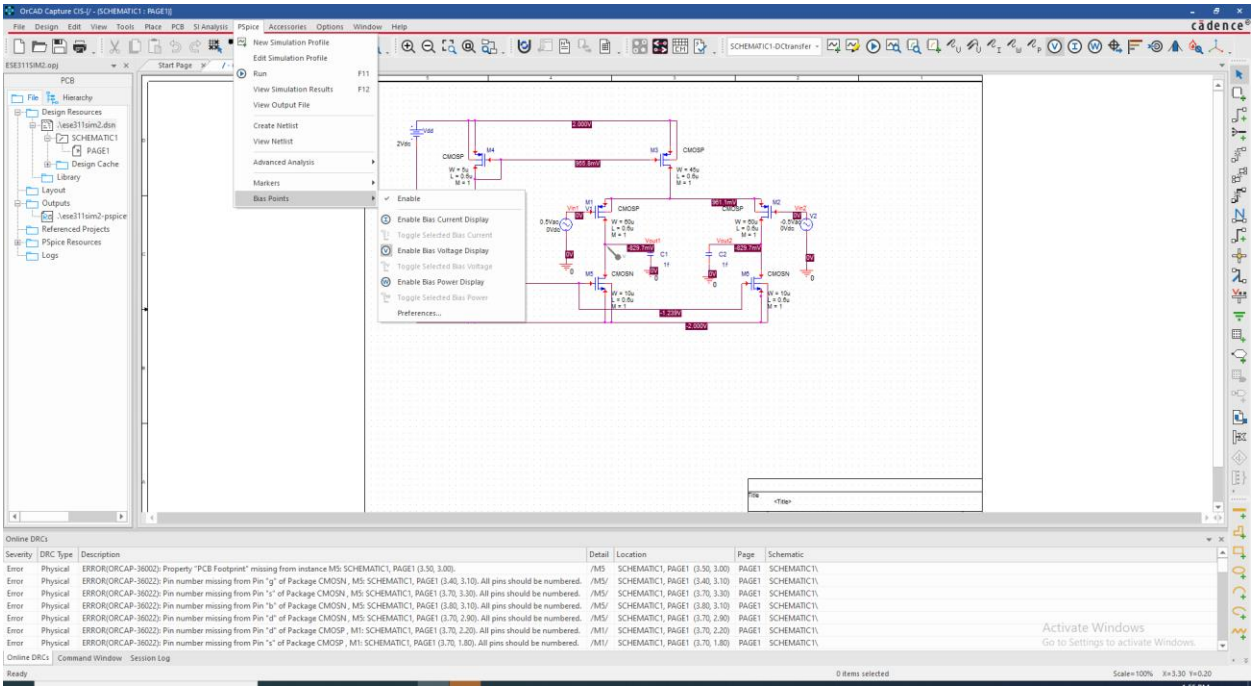
Place the same marker to the right output, the name number will be incremented automatically, it will get name Vout2.

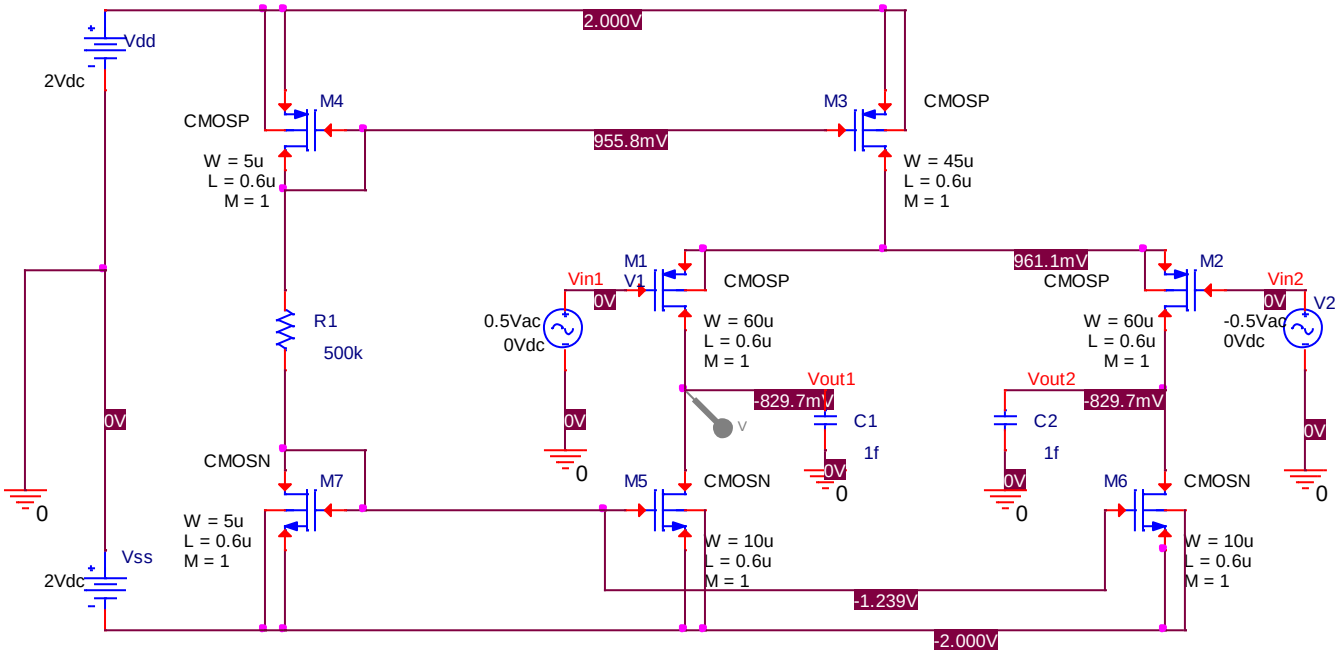


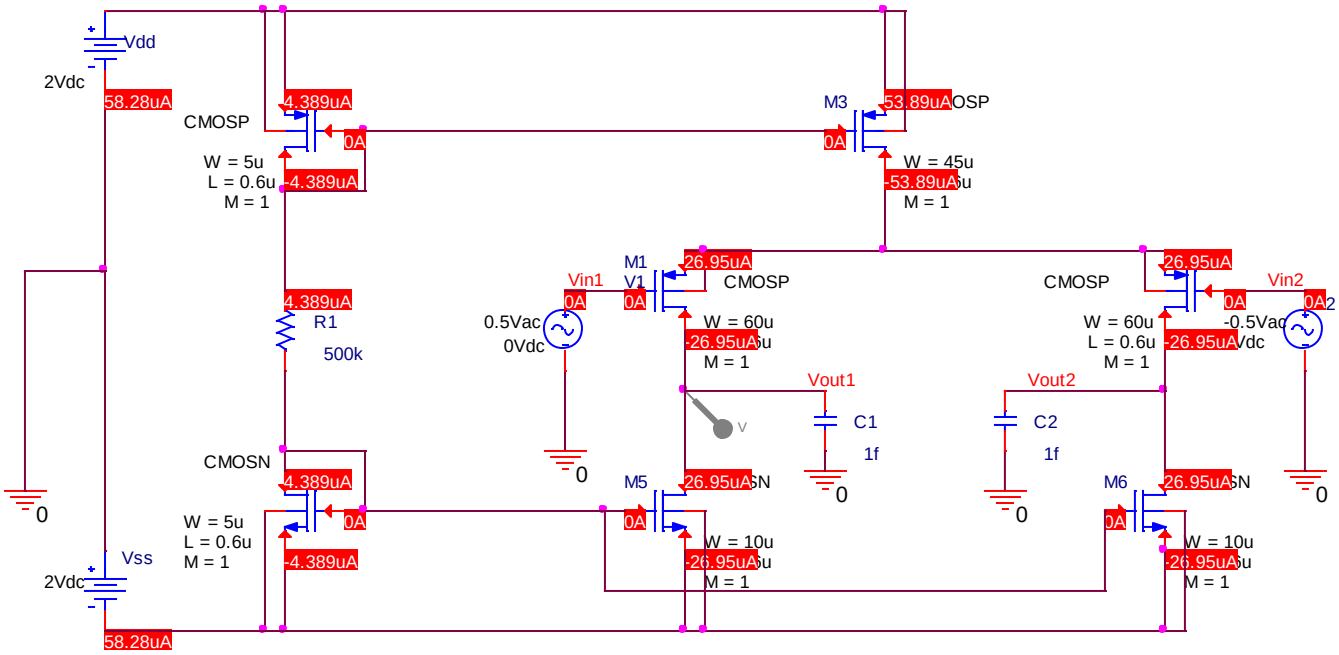
Simulate the device operating points:  Edit the simulation profile, change it to BIAS POINT.



Run simulation. The results are stored internally. Enable display of DC voltages and currents: one at a time as shown or both.






Inspect the values of DC voltages and currents:

Estimate VGS and VDS for each MOSFET subtracting the corresponding terminal voltages.

VSG1,2 = 0.96 V  is normal (above threshold Vtp),  VGS5,6 = 2-1.2= 0.77 (above threshold Vtn).

The reference current and the bias current were found to be about 4.4 uA, and 54 uA, respectively. One would expect the bias current (id3)  to be  9 times of reference current (id4) due to the ratio of W3/W4.

The actual bias current differs from expected due to difference in VSD of the PMOSFETs M3 and M4.

Main attention should be paid to the output DC voltage: Vout = -0.82V.

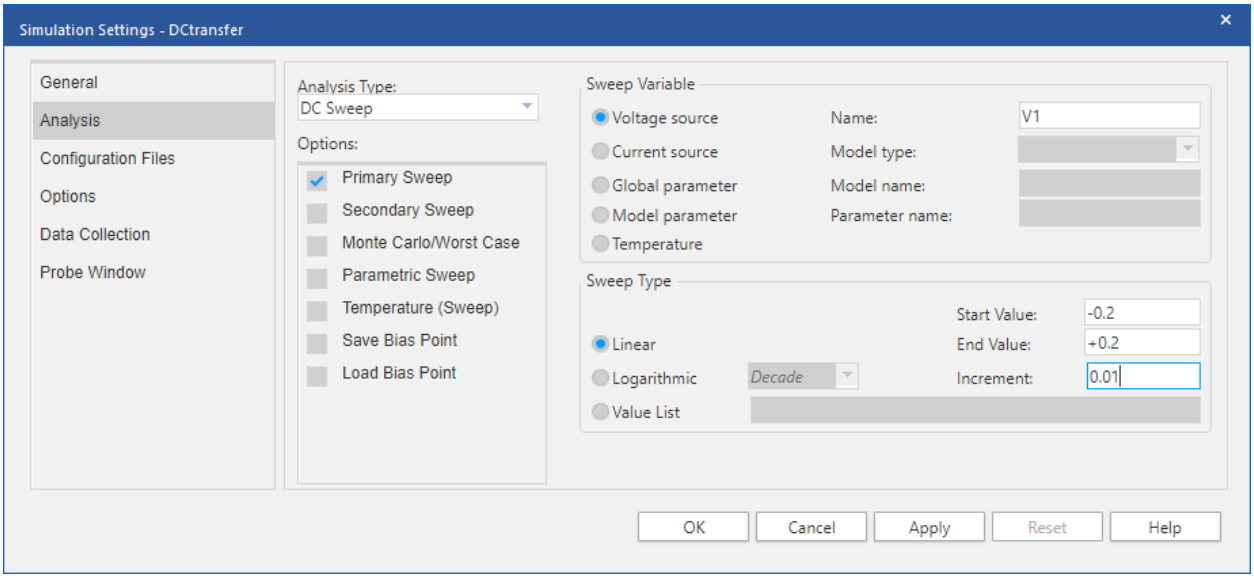
With requested selection of reference resistor R1 based on ID digits, the bias current varies  which leads to a range of possible DC voltage Vout . It is possible that the steady state value of Vout would be too high or too low so that PMOSFETs M1, M2 or NMOSFETs M, M6 operate with too small Vds close to triode region. The latter would result in a lack of voltage gain.

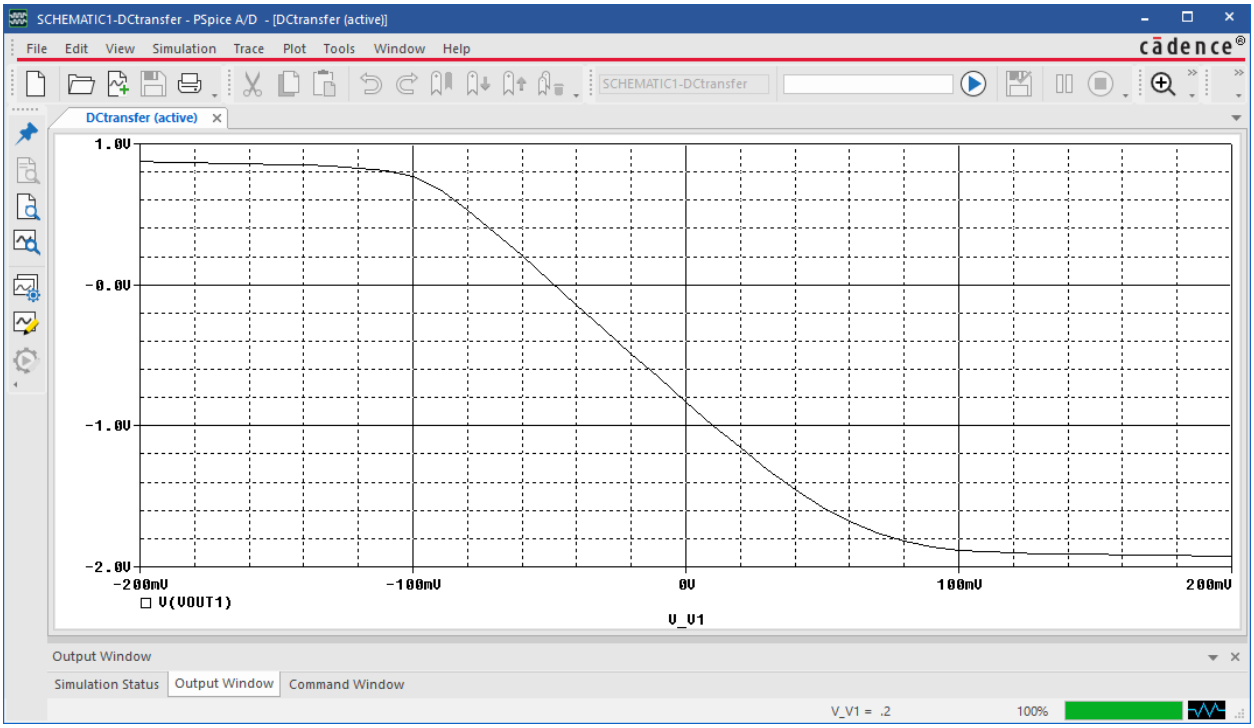
For given R1=500k the DC value of Vout was found to be within an acceptable range so that both M1 and M5 (M2 and M6) operate in the saturation region.

However, the value Vout= -0.82 V is somewhat small so that the room for decrease of Vout from the steady state value is much smaller than the room for increase of Vout. It would result in clipping of the negative half-wave of Vout with small amplitude of Vin  due to M5 or M6 entering the triode mode.  The operating point can be moved to a higher DC voltage so that a sinusoidal Vout can have greater amplitude without waveform distortion of clipping.

The possible range of Vout can be explored by simulation of the DC transfer characteristic Vout (Vin).

The amplitude of Vin should be greater than 1.4*Vov1, where Vov is overdrive voltage of transistors in the differential pair.  Due to symmetry it is sufficient to monitor Vout in one side of the differential stage.



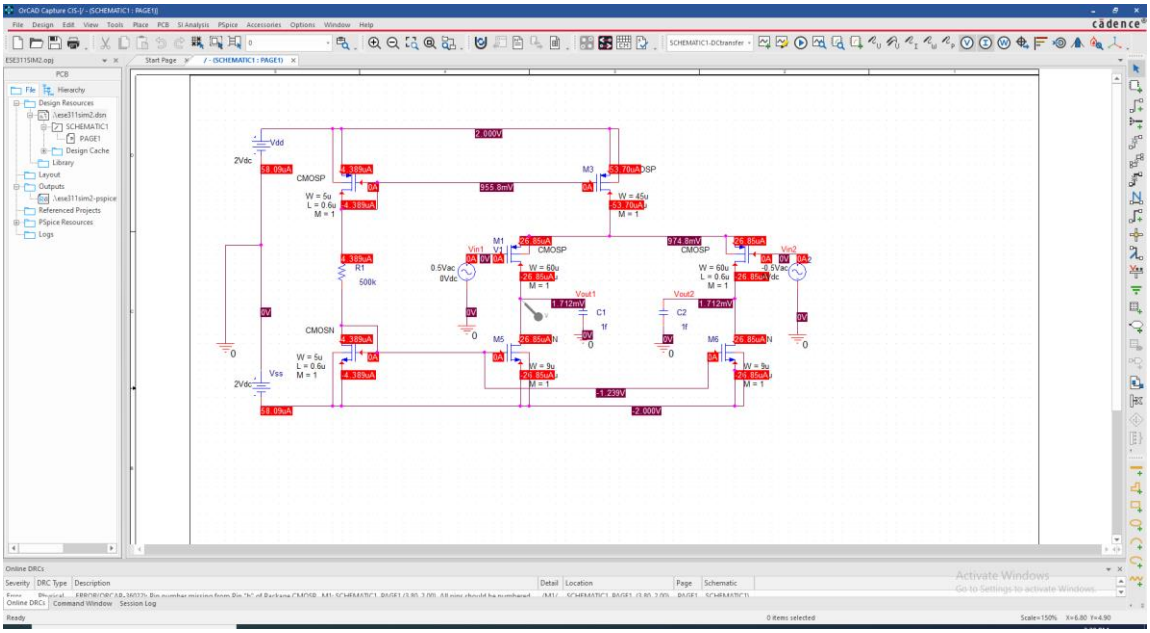

One can see than with Vin = 0 the DC output voltage is -0.82V, the same as the bias point shown in the schematic.

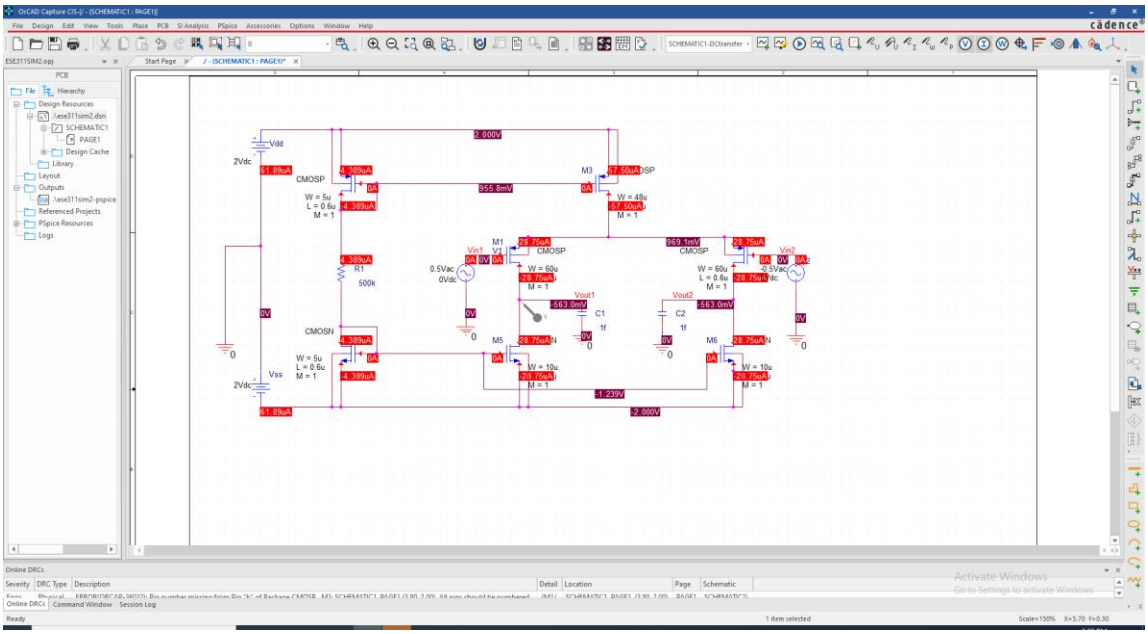
The DC transfer characteristics shows that Vout can be as low as -1.8V and as high as +0.8 V.

Thus, Vout can decrease by 1 V and increase by 1.6 V. For operation with sinusoidal signals one would like to see similar changes +/- 1.3 V possible with the steady state value of Vout =-0.5 V DC.

The adjustment of the DC operating point can be achieved with a minor change of n-MOSFET width W5=W6 or p-MOSFET widths W1=W2, or W3.

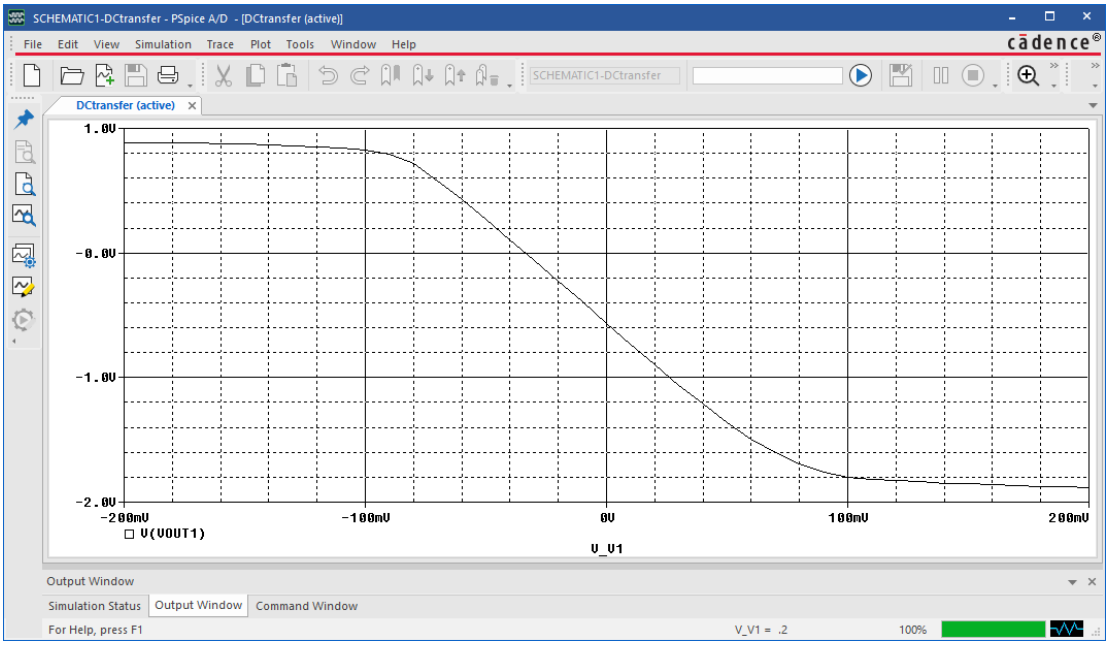
Note than the operating point is very sensitive to change of W5=W6. Technically it is easier to change W1=W2 or to allow for a minor change of the bias current with adjustment of W3.





Now the DC output voltage is much closer to -0.5V. The bias current was not changed significantly.

The updated DC  transfer characteristic shows zero  of V1 shifted to the left.

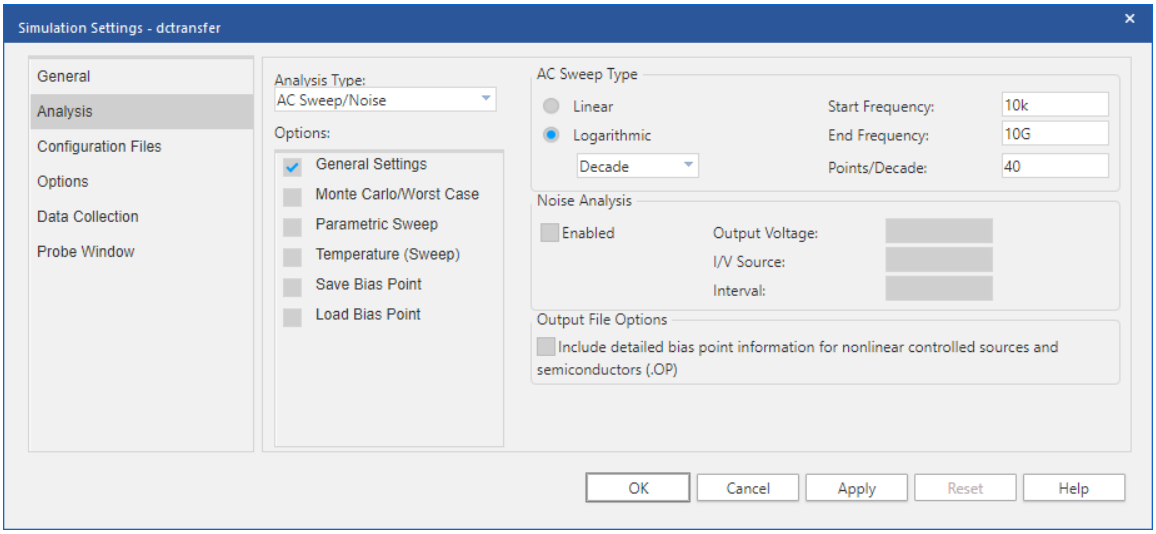



One can see that input voltage swing can be about +/- 0.1 V.

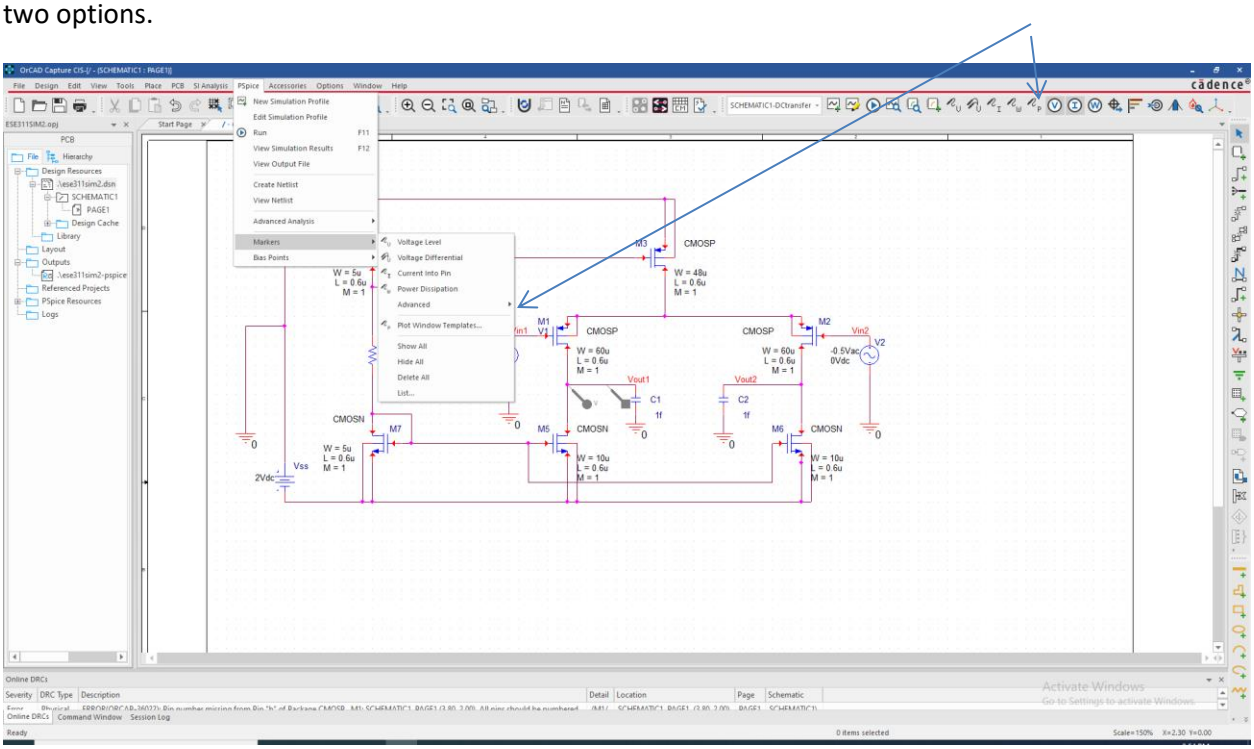
The slope of this characteristic is the AC voltage gain for single ended output Vout1: Av= Vout1/Vid, where Vid is differential voltage Vin1-Vin2.  Within the liner part of the transfer characteristic  the change of V1 by 0.1 V results in change of Vout by 1.6 V. Thus, the differential voltage gain for single ended output  is about 16 times or 24 dB.

The next step is to obtain the Bode plot for transfer function of the amplifier (voltage gain).

Edit the simulation profile as follows

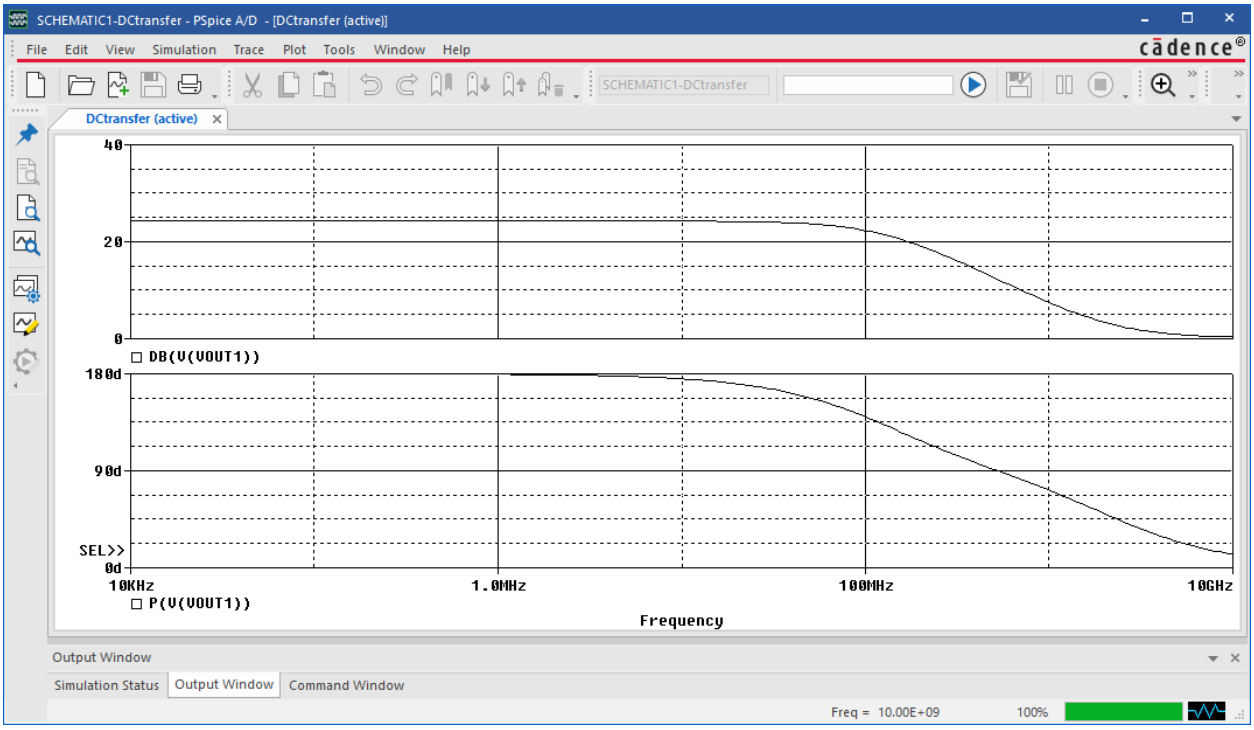


Plot windows template for Bode plot with separate plots for magnitude and phase angle. Arrows show two options.

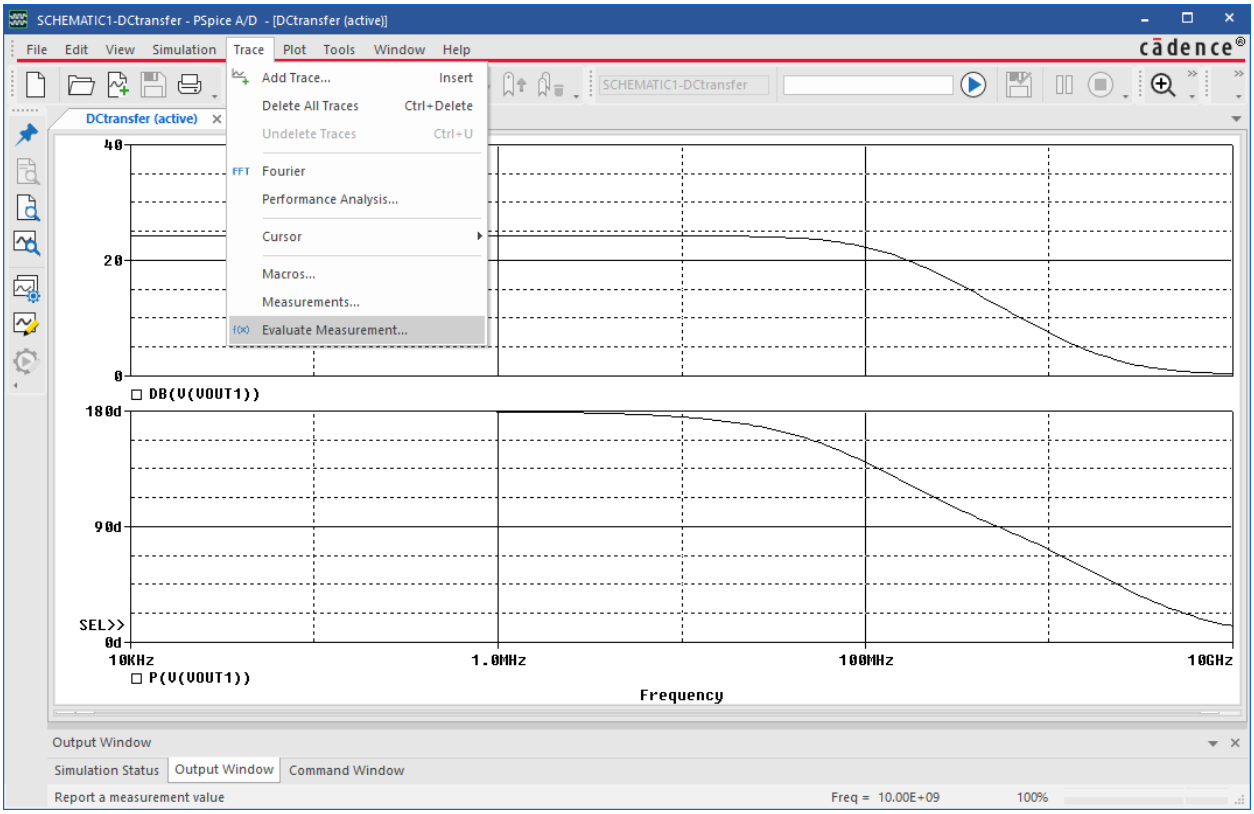



Place the Bode plot dB marker-separate to Vout1, delete the previous regular voltage probe marker.

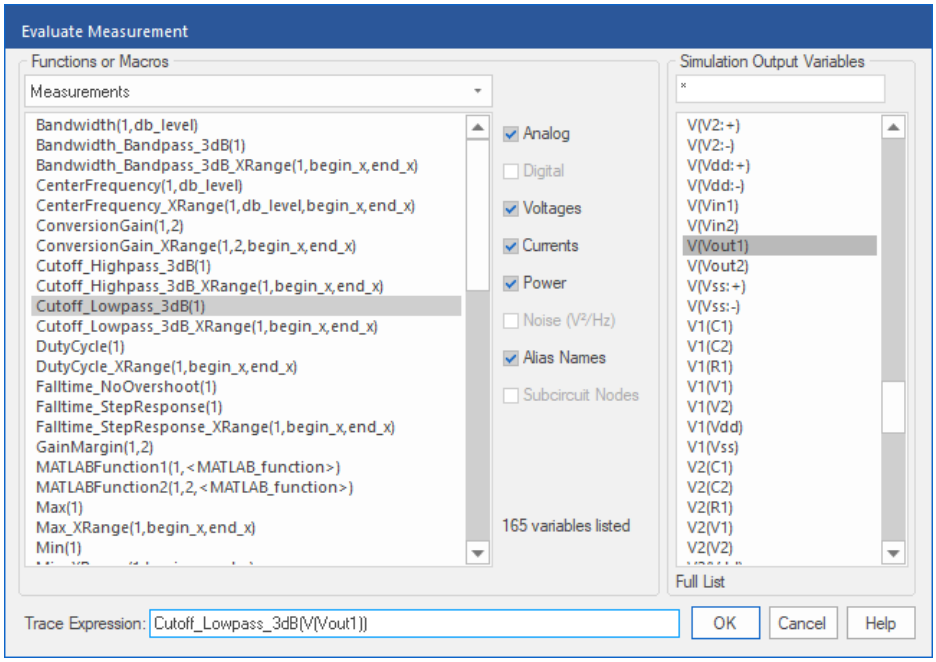
Run the simulation.



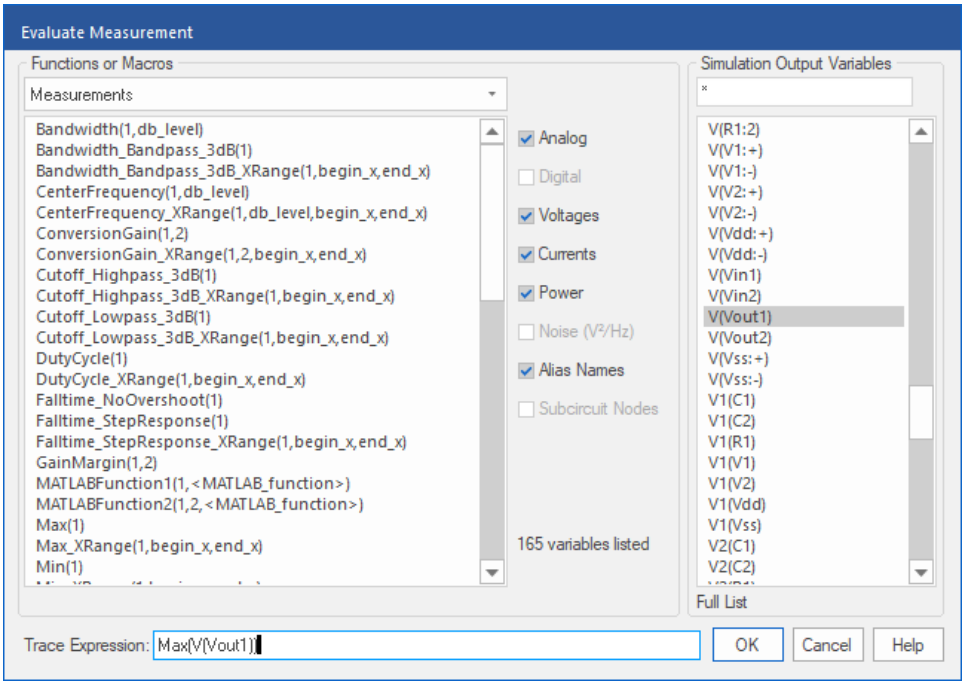

Net step is to measure the amplifier bandwidth (low pass cut-off frequency at –3dB point) with 2 clicks.



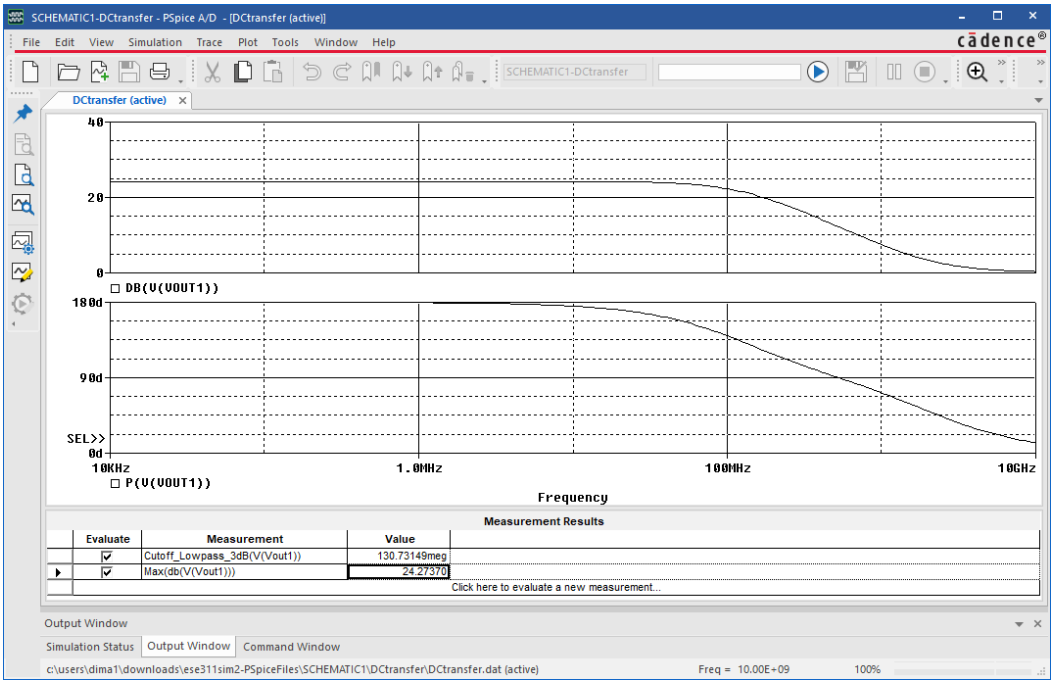
Click the function then select and click the output variable so that the variable if interest is placed into parentheses of the function.




One should get a window at the bottom of the plot with the bandwidth report. One can add an accurate DC voltage gain value.

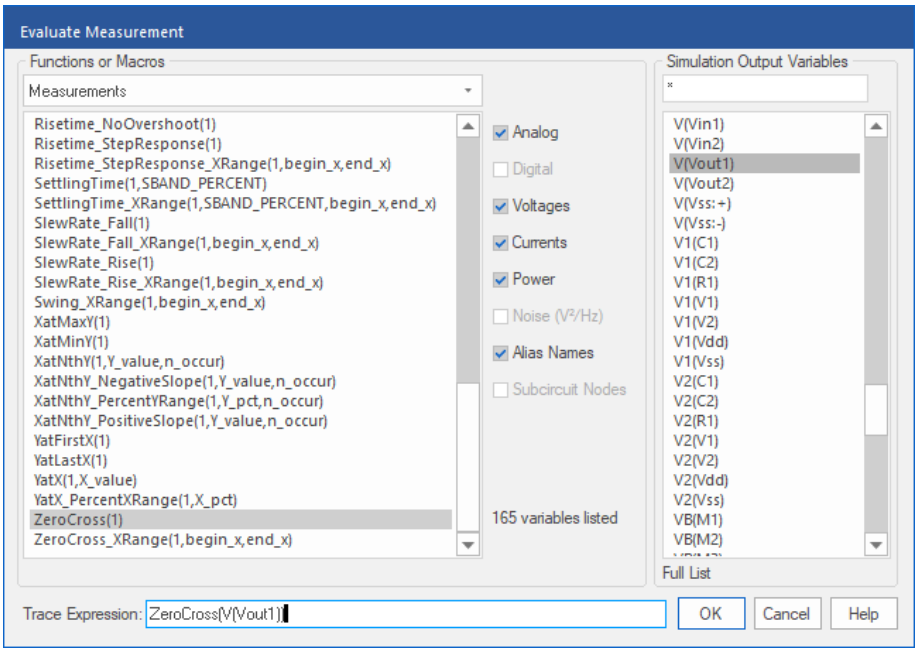


This expression  will provide the value in Volts. In order to get it in dB units, one should insert dB and parentheses as follows: Max (dB(V(Vout1))).  It would result in the following



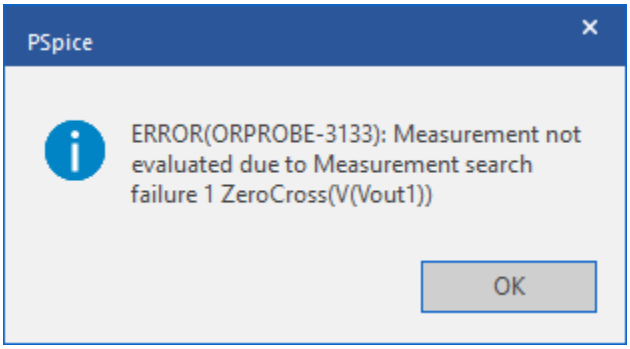

Print the Bode plot to a pdf file for incorporation to the report. Similarly obtain other Bode plots for modified circuits as requested in Sim 2 assignment.  In the circuit with greater load capacitance it was requested to find unity gain frequency  (ft) in addition to DC voltage gain and cut-off frequency.

For that one should use the following function



Note that for the circuit without external load capacitance (just a negligibly small 1 femto Farad)

requesting zero would results in an error because the voltage gain plot never crossed zero dB in the specified range.




One should see a visible crossing of the Vout response with 0 dB level in the plot in order to request zero. These parameters are extracted from simulated results so that in cases of errors in finding parameters as shown above some circuits would need to be resimulated with extension of the frequency range then the parameter can be requested again.

For the differential output the voltage gain is twice greater (+6 dB).