Assignment 9 - Delta-Sigma Modulator

This Assignment aims at verifying and expanding, with experiments and supporting simulations, your knowledge and understanding of delta-sigma modulators.

Please document each step with snapshots, pictures, and your observations. Please make visible on WaveForms the date and time fields (top left) and the serial number (bottom right) of your Analog Discovery. Also, please include this page.

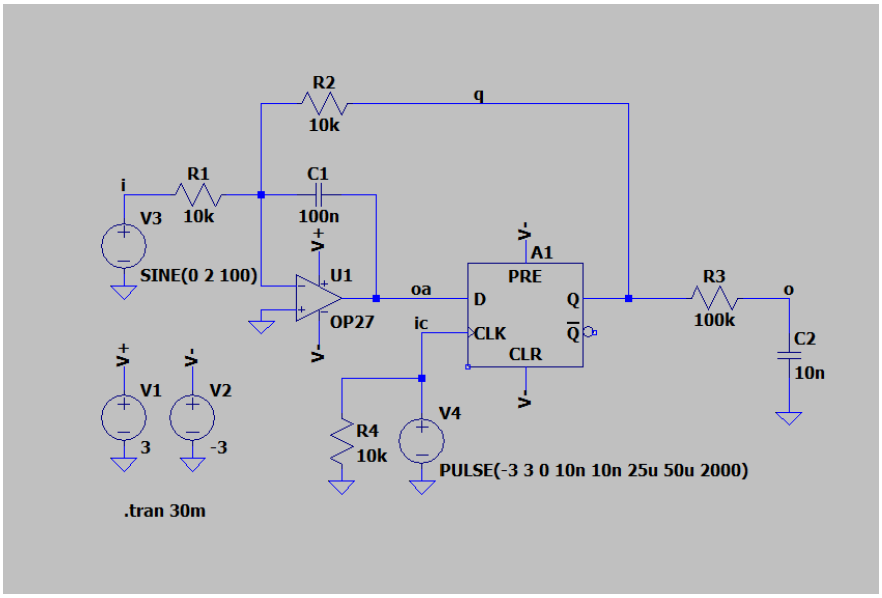

Figure 1

1) Using the simulator, design the circuit shown in Fig. 1 (**30pts**)

a) simulate and show the input and the response at the output

b) observe and report the impact of changing the clock (PULSE) frequency to 10kHz, 20kHz, 50kHz and 100kHz (keep 50% duty cycle)

c) explain in your own words how the circuit operates

Note: the DFF can be found in the Digital library, recommended settings Vhigh=3 Vlow=-3 Trise=10n Tfall=10n)

2) Build the circuit at (1) and experimentally reproduce the simulations (**70pts**)

Note1: you can use the 74LS74 or the 74HC74

Note2: pay attention to the PRE and CLR – depending on the model they can be either active-high (as in the schematics) or active-low