EEO 352 Fall 2023 - Assignment 9 – Monostables and Rectifiers - ABET

Please document each step with snapshots of the built circuit, plots, pictures and your observations. Please include this page.

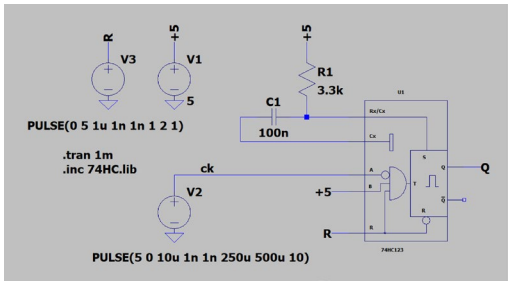

Fig.1a

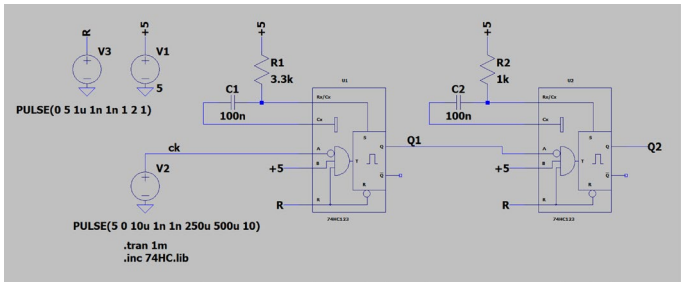

Fig.1b

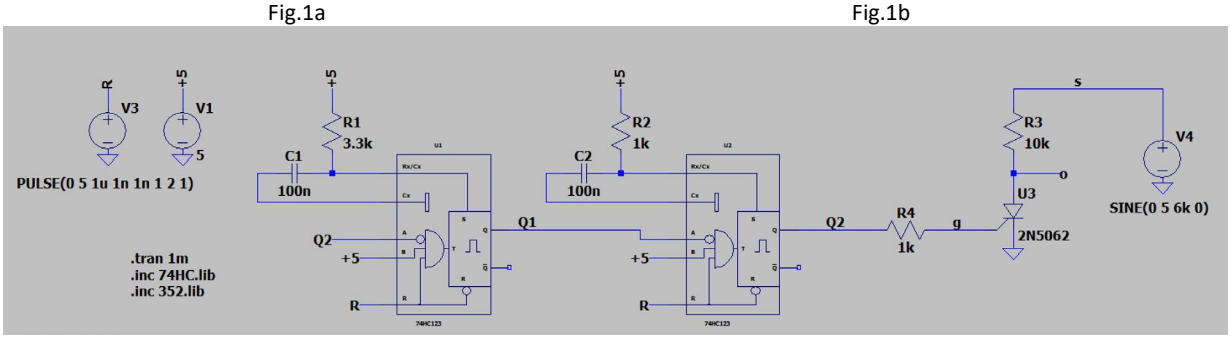

Fig.2

1) Using the 74HC123 part in the 74HC library, design and simulate as follows, plotting the clock and the Q signals in separate panes and reporting the width of the Q pulses (**10pts**):

a) Monostable as shown in Fig.1a

b) Dual monostable as shown in Fig.1b

c) Self-triggered dual monostable as at (b) but replacing the CK with Q2

Note1: you need to include the 74HC library as shown

Note2: simulations may be long, be patient

2) Using the SCR 2N5062 develop the asynchronous rectifier as shown in Fig.2 (**10pts**) (*ABET PI-21*)

a) Formulate the problem addressed by the circuit and explain how the circuit operates

b) Plotting the signals Q2, s and o

Note1: you need to include the 352 library as shown, and change the SCR Value into 2N5062 (right-click on the part)

3) Using the 74LS123 part, build and measure the circuits at (1a), (1b) and (1c), plotting CK and Q for (a), the CK and Q2 for (b) and Q1 and Q2 for (c), and reporting the width of the Q pulses (**40pts**)

Note1: Use a +5V supply and ground

Note2: In order to start (c), you may need to temporarily force R of one of the second monostable low, and then move it back to high

4) Using the SCR MCR100-6 part, build and measure the circuit at (2), plot the signals s and o, and analyze the performance (**40pts**) (*ABET PI-24*)

Note1: Verify that the circuit is self-triggering by checking the signal Q2