EEO352 Lab 9
Monostables and Rectifiers

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Copy of Original Assignment

EEO 352 Fall 2023 - Assignment 9 – Monostables and Rectifiers - ABET

Please document each step with snapshots of the built circuit, plots, pictures and your observations. Please include this page.

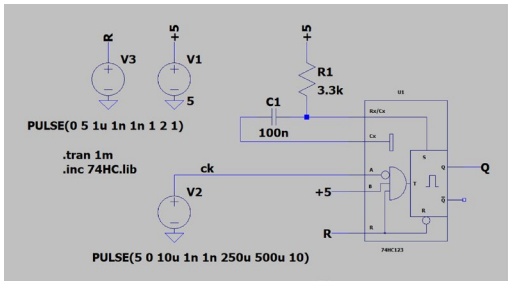

Fig.1a

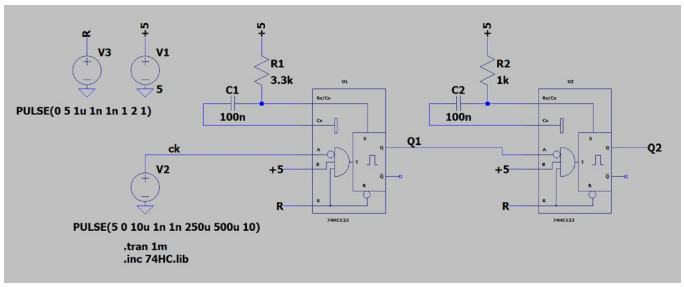

Fig.1b

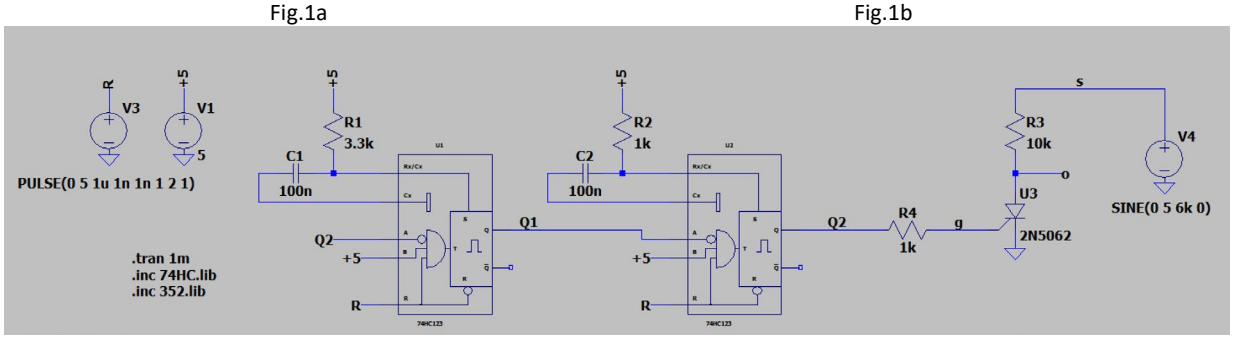

Fig.2

1) Using the 74HC123 part in the 74HC library, design and simulate as follows, plotting the clock and the Q signals in separate panes and reporting the width of the Q pulses (**10pts**):

a) Monostable as shown in Fig.1a

b) Dual monostable as shown in Fig.1b

c) Self-triggered dual monostable as at (b) but replacing the CK with Q2

Note1: you need to include the 74HC library as shown

Note2: simulations may be long, be patient

2) Using the SCR 2N5062 develop the asynchronous rectifier as shown in Fig.2 (**10pts**) (*ABET PI-21*)

a) Formulate the problem addressed by the circuit and explain how the circuit operates

b) Plotting the signals Q2, s and o

Note1: you need to include the 352 library as shown, and change the SCR Value into 2N5062 (right-click on the part)

3) Using the 74LS123 part, build and measure the circuits at (1a), (1b) and (1c), plotting CK and Q for (a), the CK and Q2 for (b) and Q1 and Q2 for (c), and reporting the width of the Q pulses (**40pts**)

Note1: Use a +5V supply and ground

Note2: In order to start (c), you may need to temporarily force R of one of the second monostable low, and then move it back to high

4) Using the SCR MCR100-6 part, build and measure the circuit at (2), plot the signals s and o, and analyze the performance (**40pts**) (*ABET PI-24*)

Note1: Verify that the circuit is self-triggering by checking the signal Q2

Summary

In this lab we perform timing control using monostable circuits and ac power control using an SCR.

1 Using the 74HC123 part in the 74HC library, design and simulate as follows, plotting the clock and the Q signals in separate panes and reporting the width of the Q pulses

a)

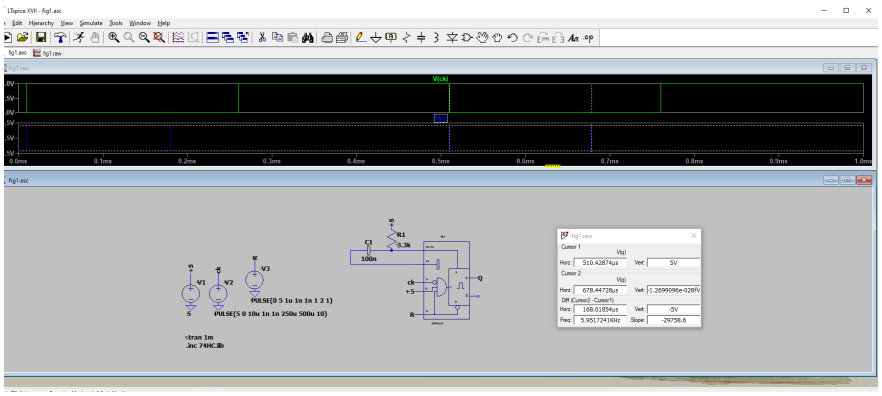

Figure 1: Q pulse width is $\approx 170\,\mu s$

b)

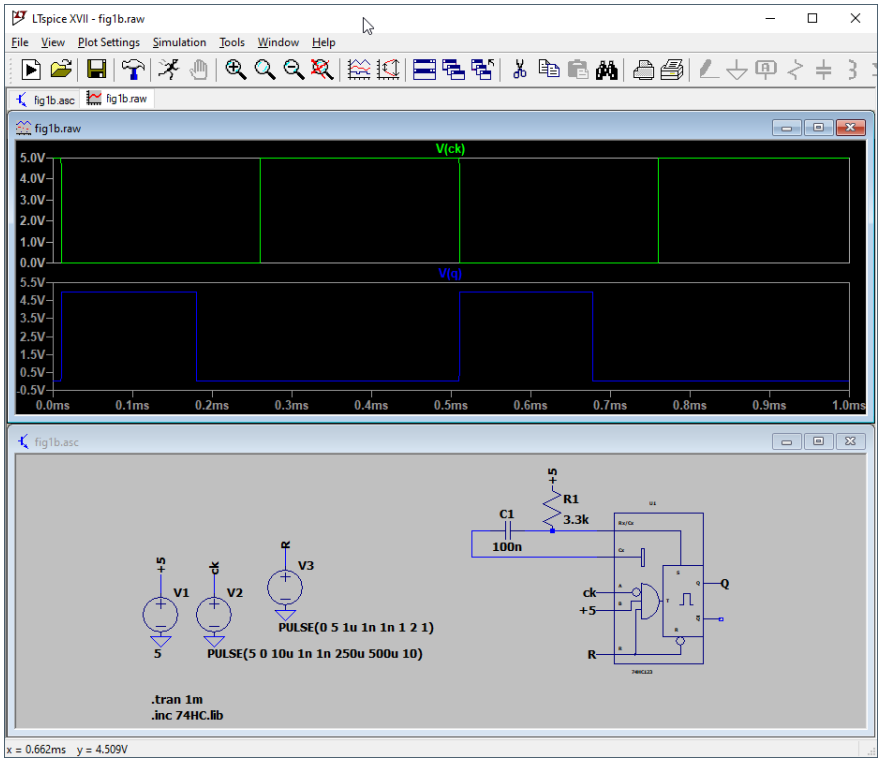

Figure 2: Q1 pulse width is $\approx 170\,\mu s$, and Q2 pulse width is $\approx 62.5\,\mu s$

c)

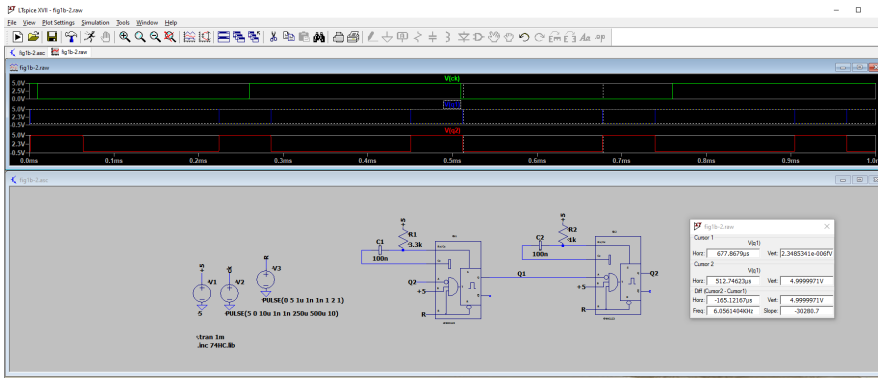

Figure 3: Q1 pulse width is $\approx 165\,\mu s$, and Q2 pulse width is $\approx 62.5\,\mu s$

2 Using the SCR 2N5062 develop the asynchronous rectifier as shown in Fig.2

a)

The two 74HC123 IC's are configured to form a self triggering monostable circuit. The output (Q2) then is a repeating square wave of fixed duty cycle. This signal is tied to the gate of an SCR. This means that

while the gate input is high, the output will be clamped to 0.6V. There is an AC signal input to the anode of an SCR - this signal will be available at the output except when the gate input is high, then the output will be clamped to 0.6V. Only the positive half of the input AC wave form can be modified.

The problem with this circuit is the lack of synchronization. Without synchronizing the self-triggering monostable circuit with the AC waveform on the anode of the SCR, the power is not able to be regulated in a meaningful way.

b)

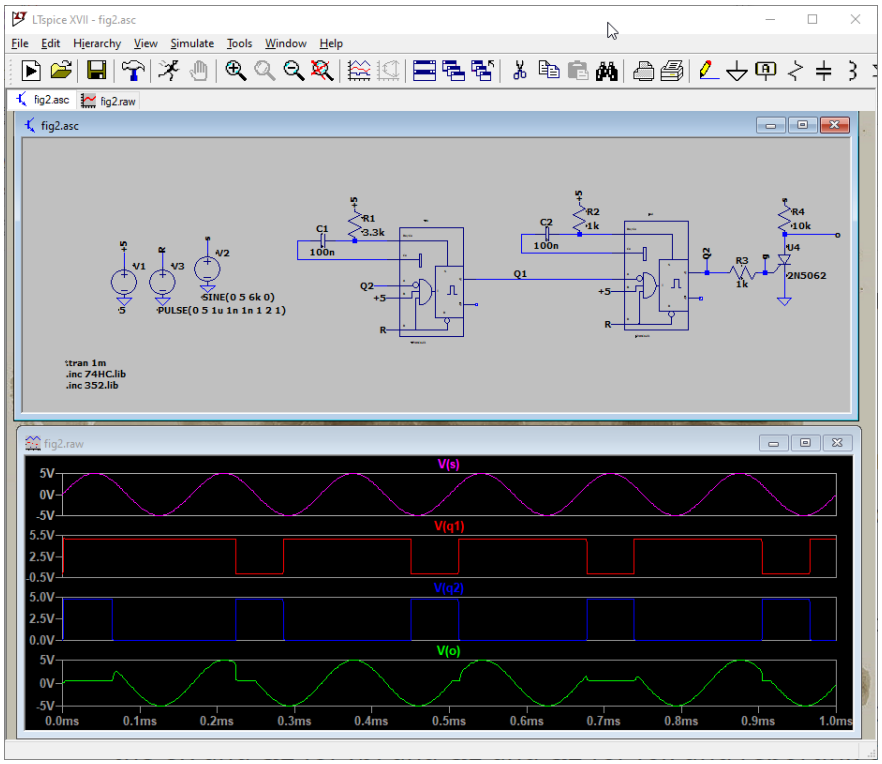

Figure 4: Asynchronous rectifier plots

3 Using the 74LS123 part, build and measure the circuits at (1a), (1b) and (1c), plotting CK and Q for (a), the CK and Q2 for (b) and Q1 and Q2 for (c), and reporting the width of the Q pulses

a)

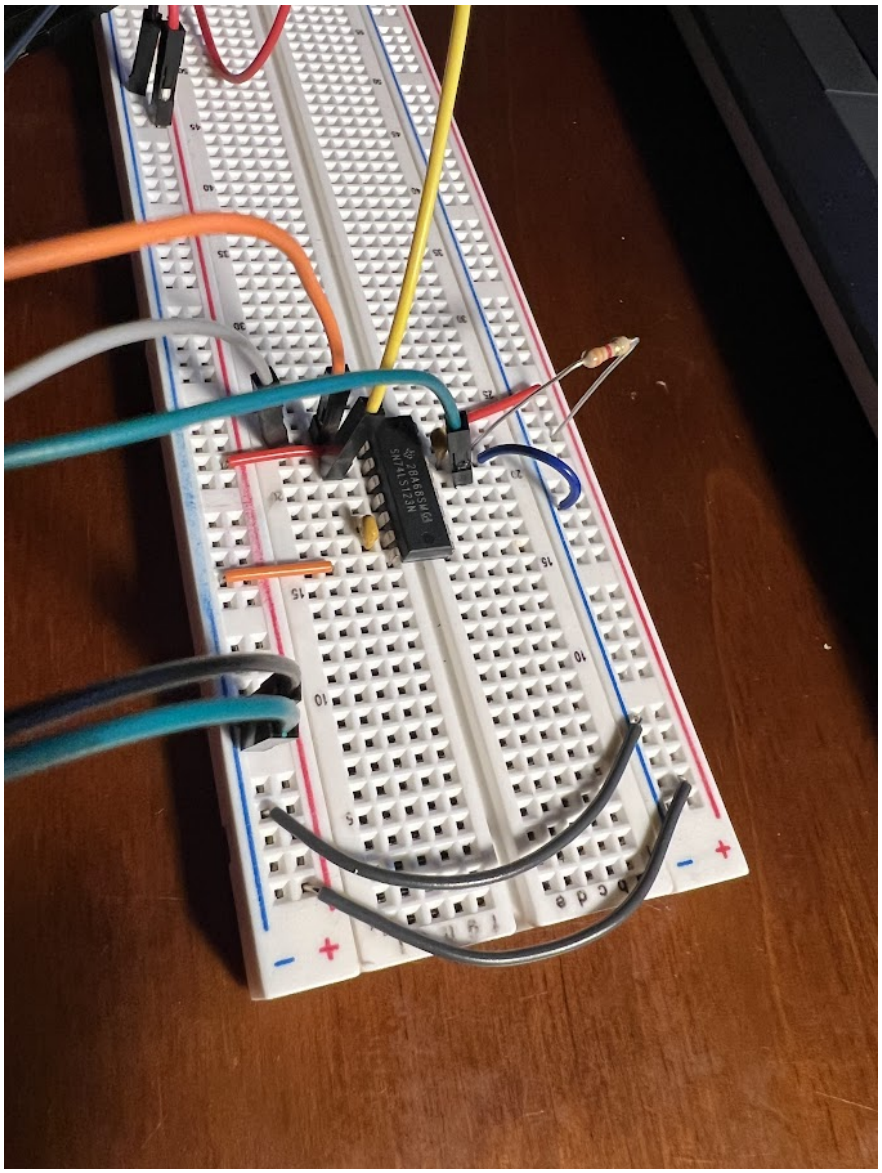

Figure 5: Test Setup

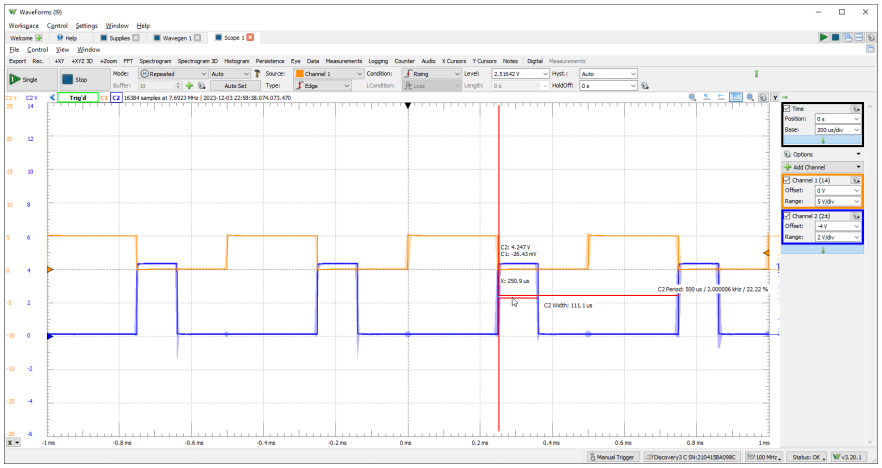

Figure 6: Waveform plots, Q = 111 µs

b)

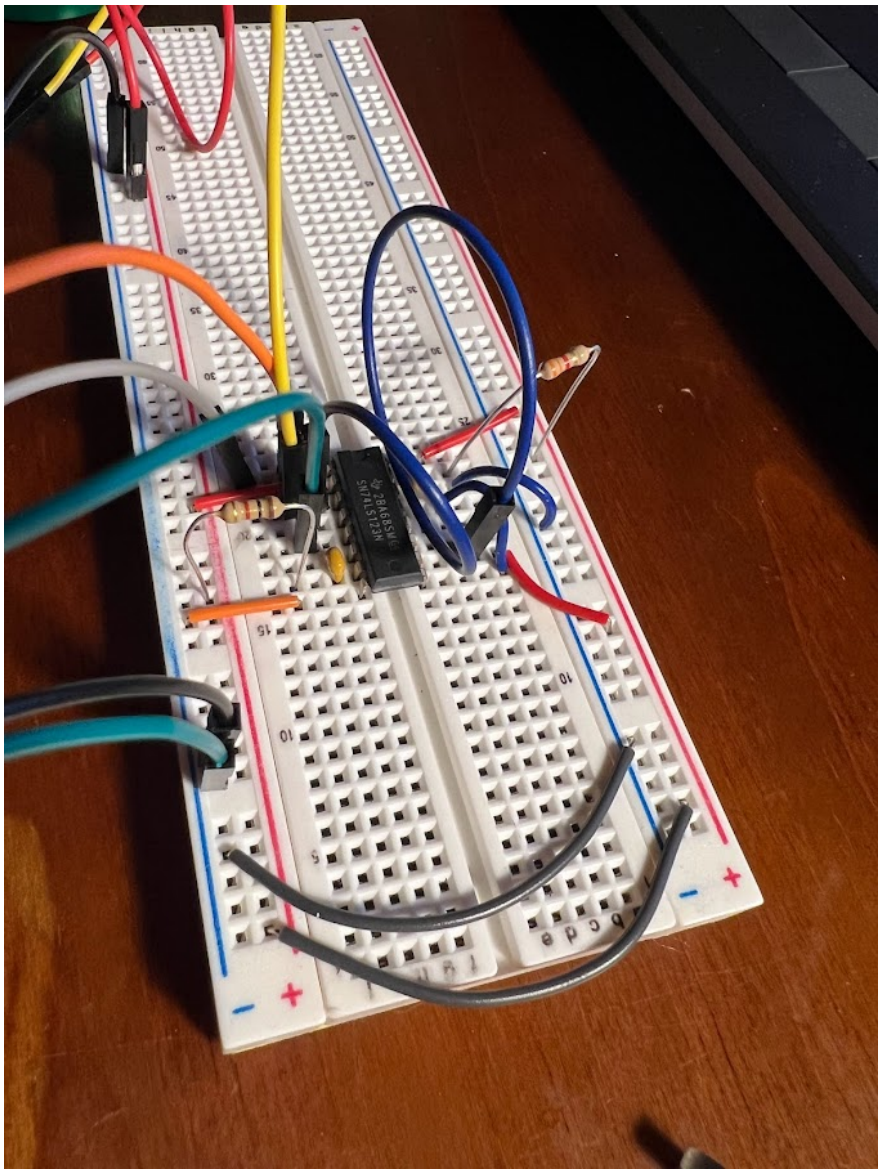

Figure 7: Test Setup

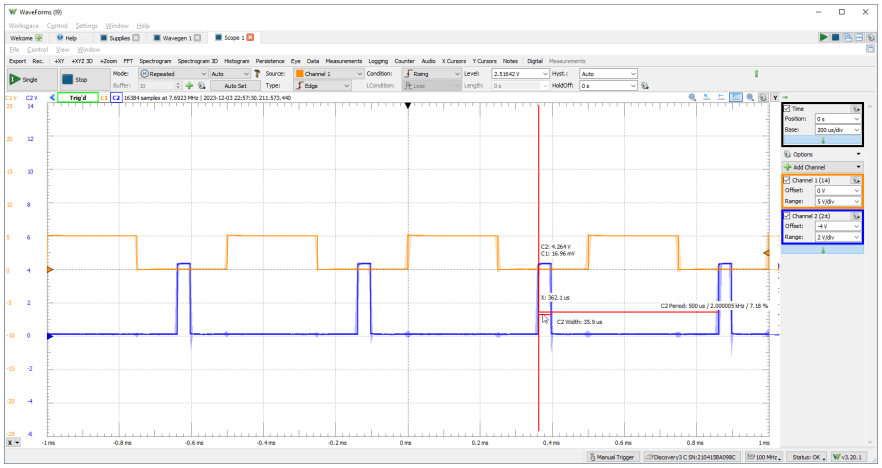

Figure 8: Waveform plots, Q2 = 36 µs

c)

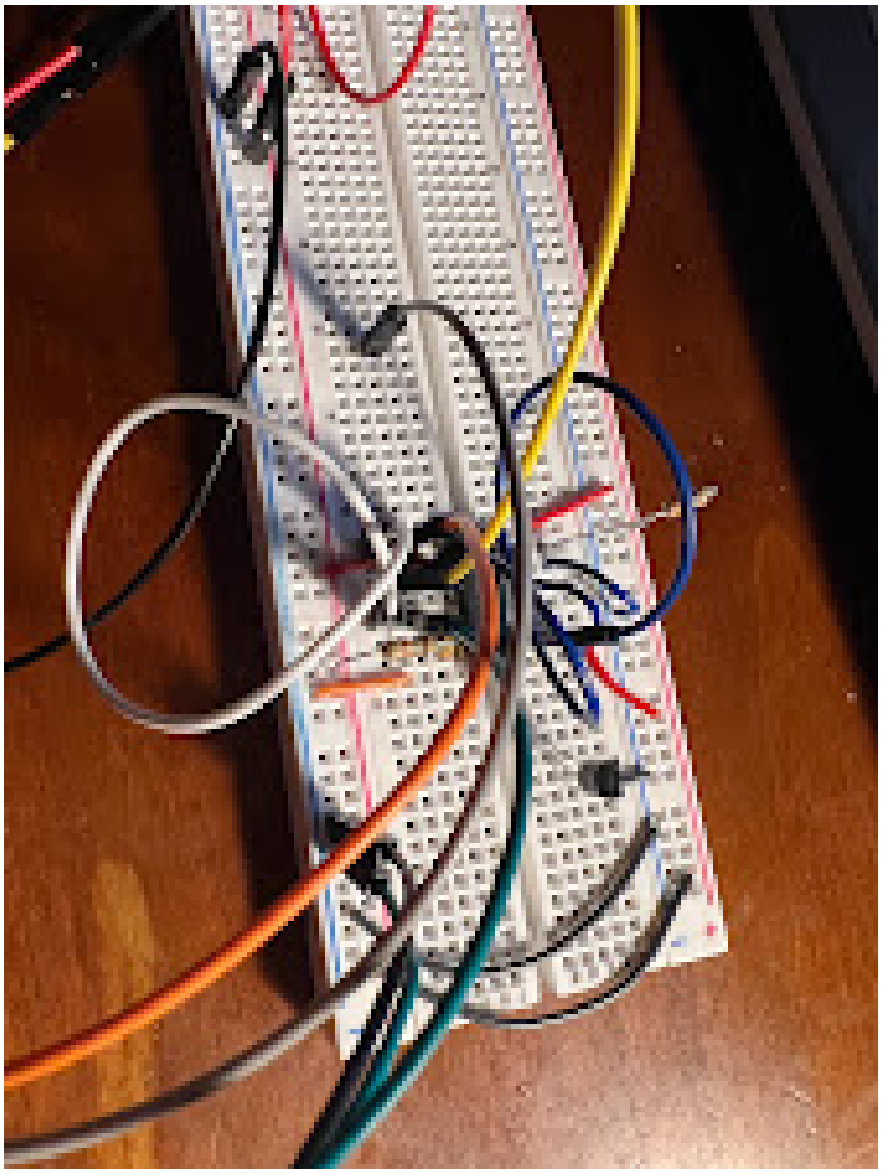

Figure 9: Test Setup

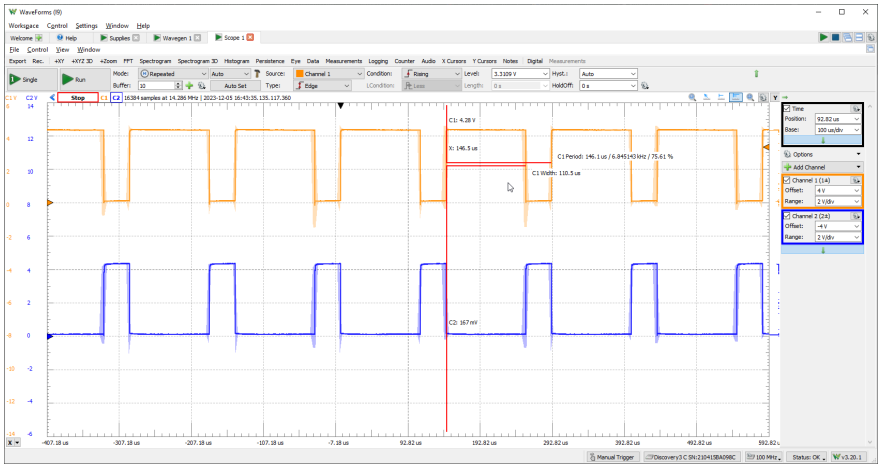

Figure 10: Waveform plots, Q1 = 110.5 µs

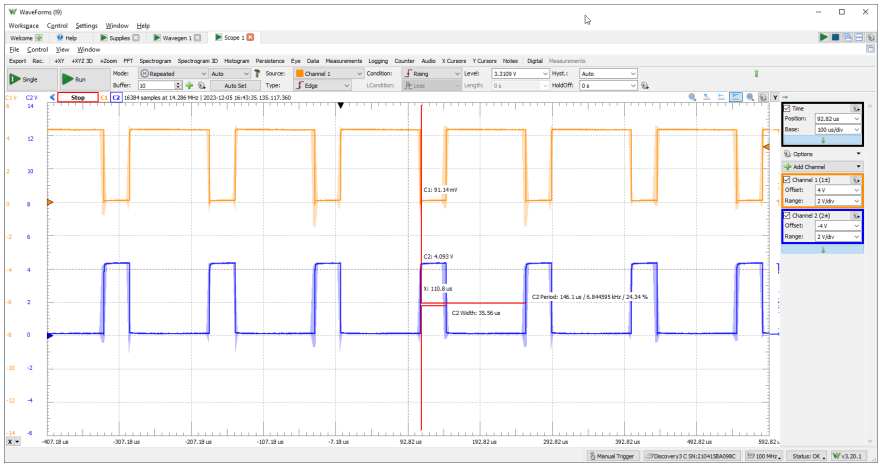

Figure 11: Waveform plots, Q2 = 35.5 µs

4 Using the SCR MCR100-6 part, build and measure the circuit at (2), plot the signals s and o, and analyze the performance

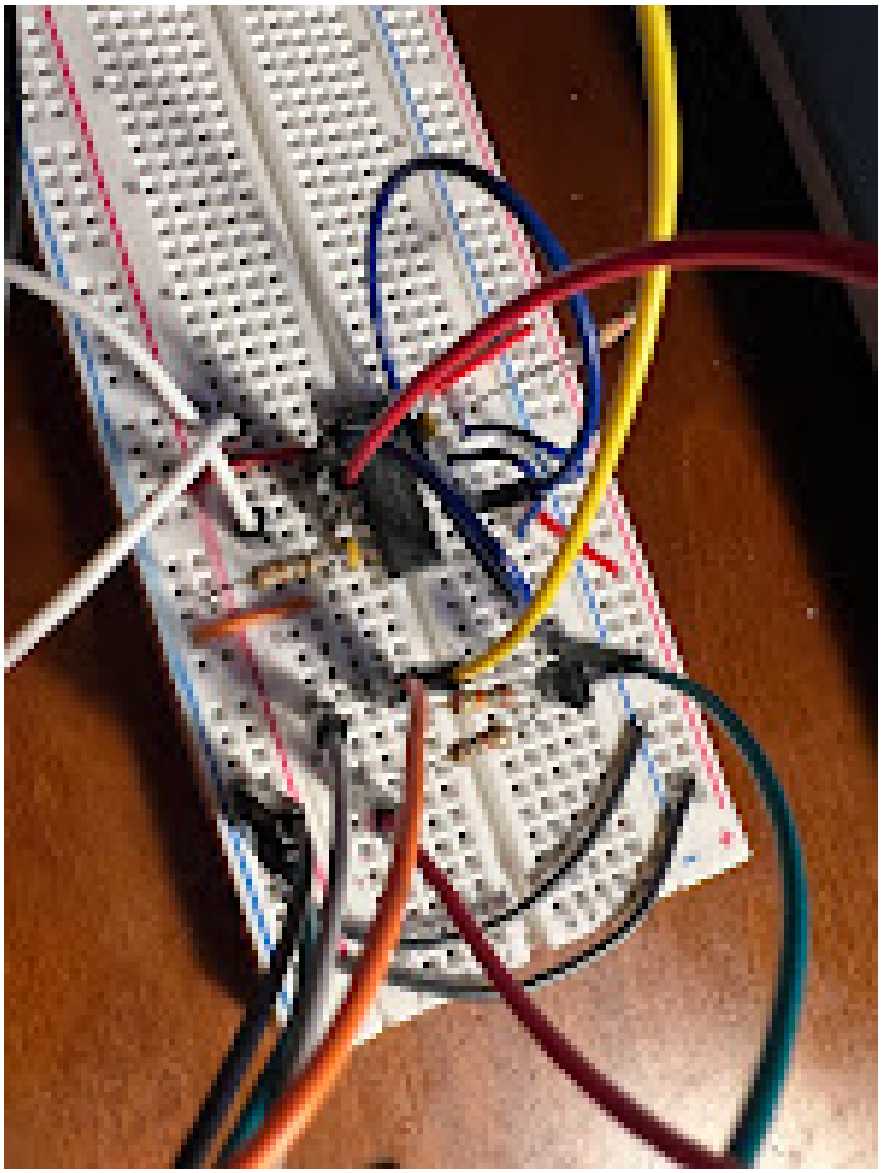

Figure 12: Test Setup

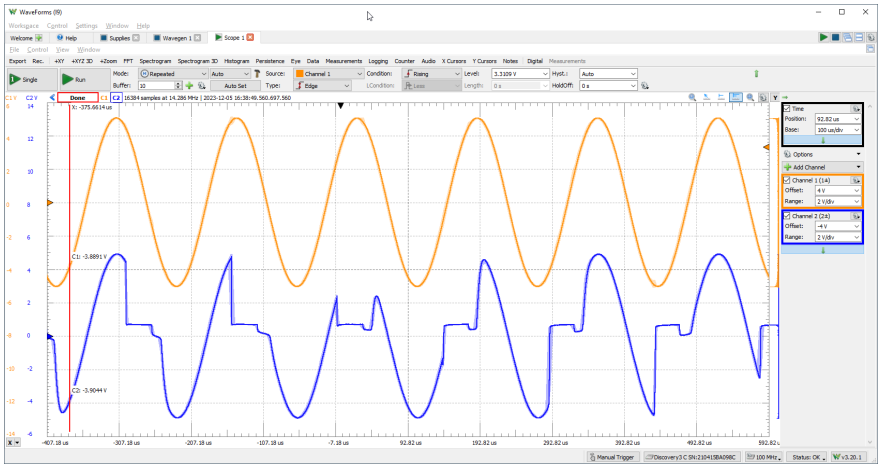

Figure 13: Waveform Plots

It can be seen from the waveform plots that the circuit has similar performance to the simulation. It appears that the lack of synchronization is still an issue preventing useful circuit operation.