Assignment 3 - Differential Amplifier

This Assignment aims at verifying and expanding, with experiments and supporting simulations, your knowledge and understanding of the input stage of the differential amplifier.

Please document each step with snapshots, pictures, and your observations. Wherever possible please include the date and time field and the AD S/N. Please include this page.

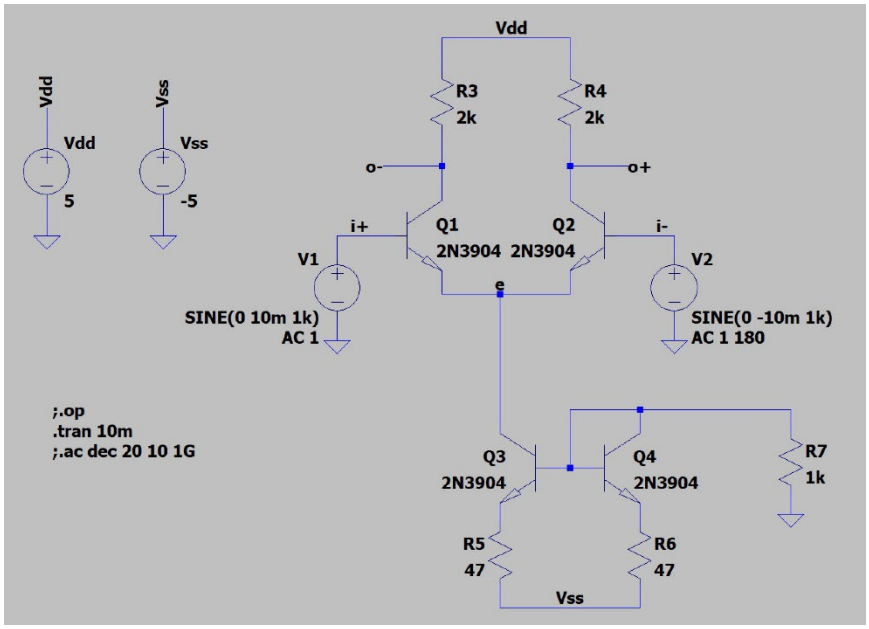

Figure 1

1) Using the simulator, design the configuration in Fig. 1 and simulate as follows (**30pts**)

a) simulate the response at Q2 collector to a 10mV, 1kHz sinusoidal input at Q1 base, simulate the frequency response and calculate the -3dB

b) simulate the response at Q2 collector to a 10mV, 1kHz sinusoidal input at Q1 base and a synchronized and in-phase 10mV, 1kHz sinusoidal input at Q2 base (i.e. a common-mode input)

c) simulate the response at Q2 collector to a 10mV, 1kHz sinusoidal input at Q1 base and a synchronized and 180deg-phase 10mV, 1kHz sinusoidal input at Q2 base (i.e. a fully-differential input), simulate the frequency response and calculate the -3dB

d) simulate the response at Q2 collector minus the response at Q1 collector (i.e. differential output) to a 10mV, 1kHz sinusoidal common-mode input

e) simulate the differential output to a 10mV, 1kHz sinusoidal fully-differential input, simulate the frequency response and calculate the -3dB

Note: You can disable a signal by setting the amplitude to 0V. You can shift 180-deg the signal (inversion) by inverting the amplitude into -10mV or by setting the phase to 180.

2) Build the circuit at (1) and experimentally reproduce all the simulations except for the frequency response of case (e) (**60pts**)

3) Explain in your own words why the configuration (d) has a much lower gain than the configuration (e) (**10pts**)