Unit 9

n-MOSFET Common-Source amplifier with p-MOSFET current source load: selection of W and L

High voltage gain requires high load impedance

p-MOSFET to replace Load resistor

Rule of thumb selection of matched impedances of nMOS (pull down) and pMOS (pull up) networks:

$r_{on} = r_{op} = r_o \Rightarrow R_{out} = r_o/2$

Matched Early voltages of nMOS and PMOS devices

$V_{an} = V_{ap}$

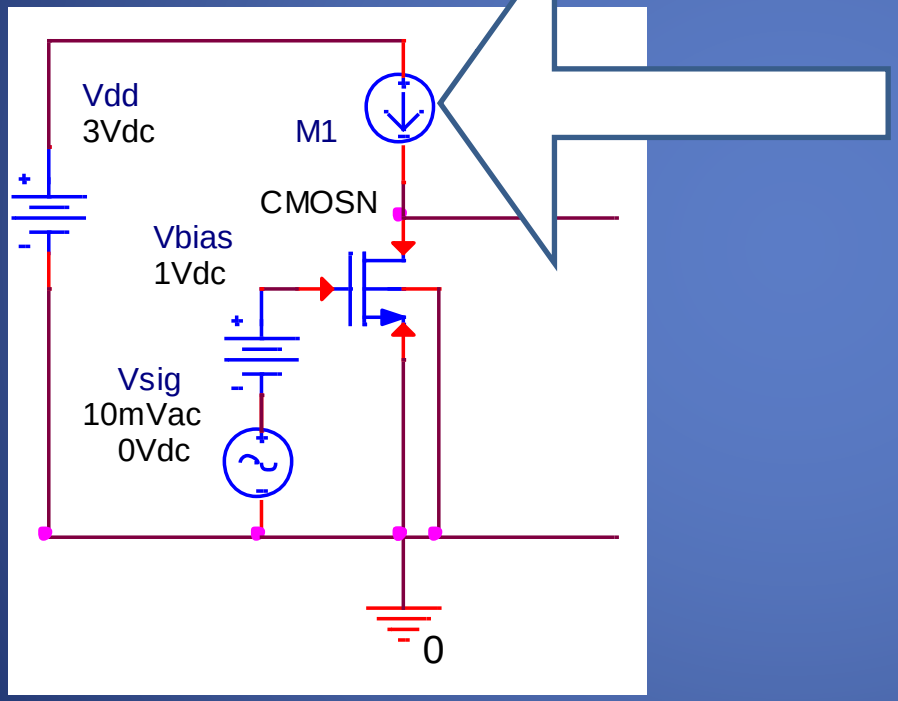
$L_p = 2 \times L_n$

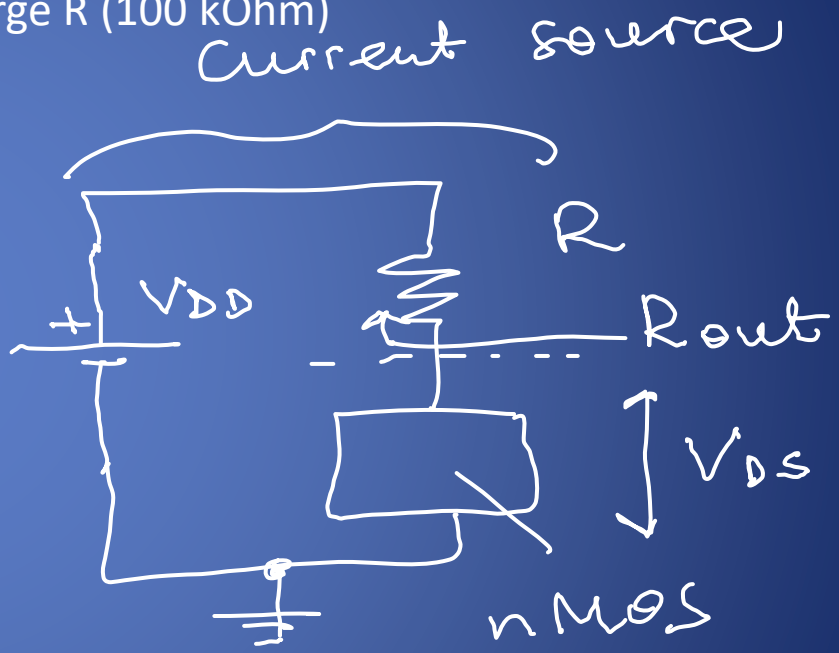
pMOSFET gate length doubled compared to that for nMOSFET

A good current source has large R_{out}, it can be obtained with large V_{DD} and large R

Target: generation of 200 uA DC
(ideally independent from output voltage)

Possible solution: large V_{DD} (20V DC) in series with large R (100 kOhm)





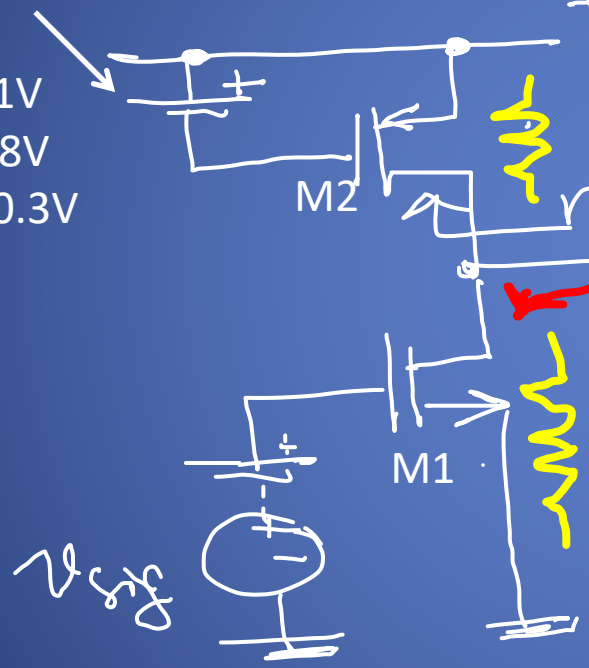
n-MOSFET stage loaded with a large R =100 kOhm would have large AC voltage gain: $A_v = g_m R$ = 1.2 mA/V x 100 kOhm = 120

n-MOS stage loaded with p-MOS current source

$|A_v| = g_m \cdot R_{out}$

Vbias = |Vtp| + |Vovp| = const

suppose
Vbias =1.1V
|Vtp|= 0.8V
|Vovp|= 0.3V



$r_{op} = V_{Ap}/I_D$ is an output resistance of p-MOSFET

$r_{on} = V_{an}/I_D$ is an output resistance of n-MOSFET

n

The voltage gain for AC signal is limited by the equivalent output resistance (R_{out}) defined by connected in parallel r_{on} and r_{op} Why in parallel? V_{DD} is a constant voltage source, in small signal equivalent circuit V_{DD} represents a short circuit.
For AC signal DC source V_{DD} is equivalent to ground.

Selection of gate length L for p-MOSFET

since Rout = $r_{on}||r_{op}$, ideally, we would like to see $r_{op} >> r_{on}$,

The latter would require a pMOSFET with a long gate length Lp
and a very wide pMOSFET Wp, respectively (for given overdrive voltage Vovp)

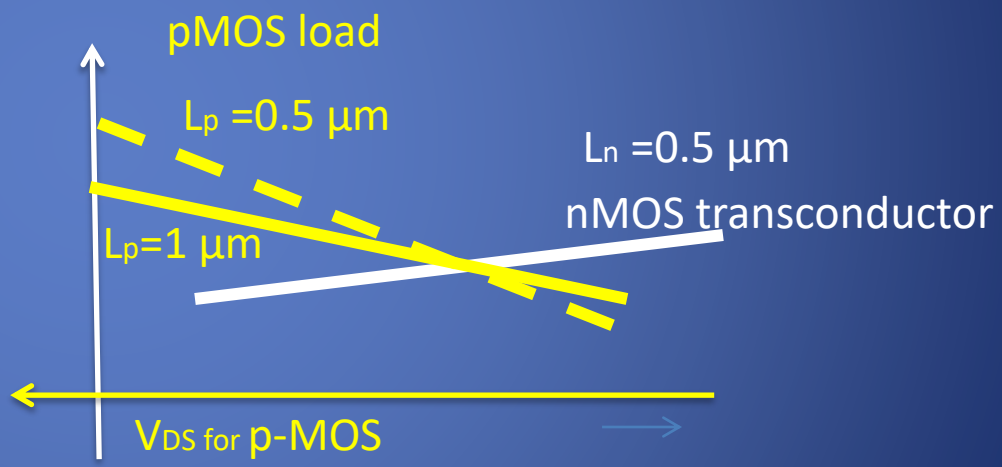
One can select $r_{on} = r_{op}$ for a reasonable width Wp.

Both nMOS and pMOS have the same DC current $I_{Dn} = I_{Dp} = I_D$, therefore

$$V_{An} = V_{Ap}$$

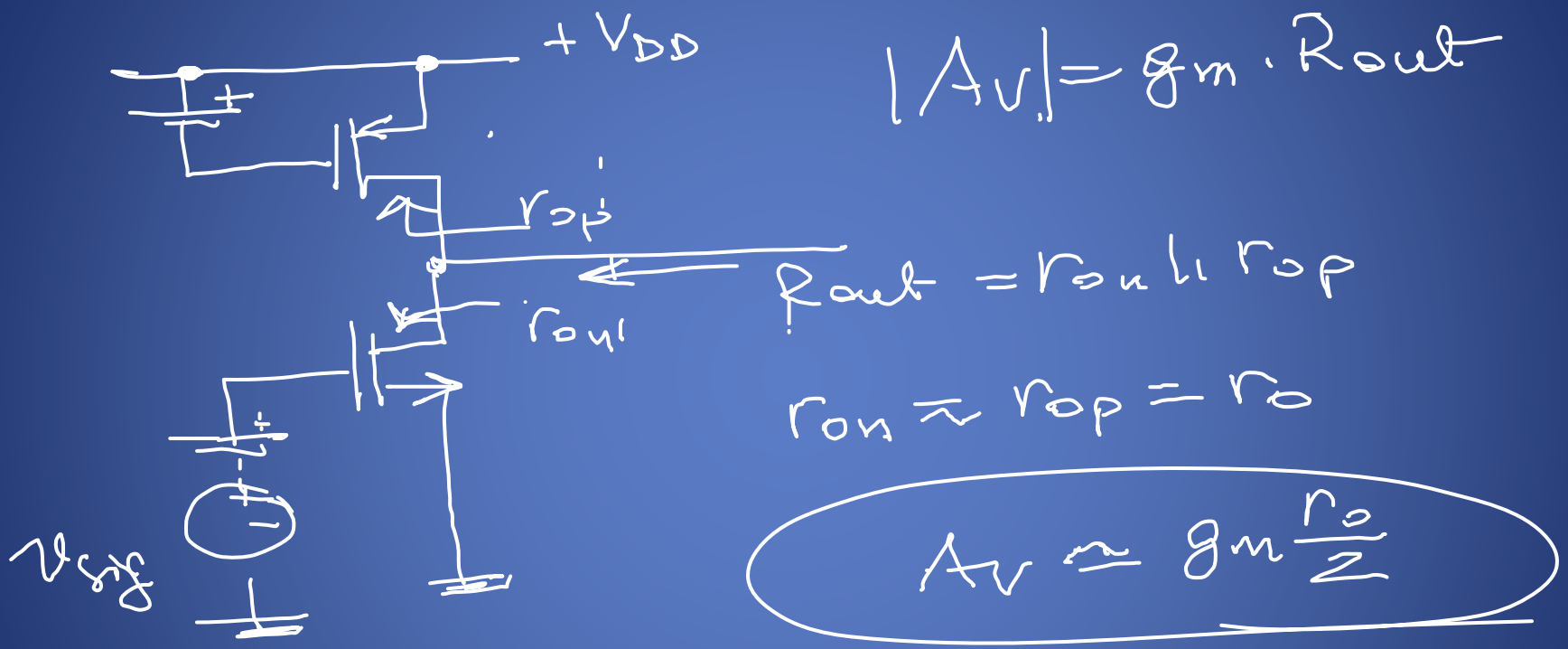
$$\Downarrow$$

$$L_p = 2\,L_n$$



The gate length of p-MOS in the current source is selected to be ~twice greater than L for the amplifying n-MOS transistor to compensate for relatively small Early voltage parameter of p-MOS V'_{Ap} = 10 V/um compared to that for n-MOS V'_{An} = 20 V/um.

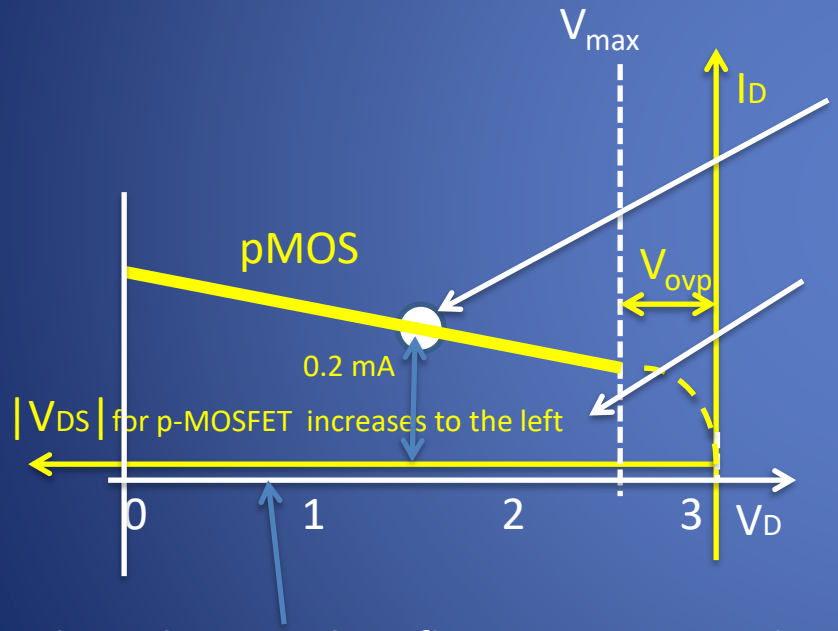
Selection of $r_{op} = r_{on}$ is a good compromise which combines a respectfully-high voltage gain of $A_0/2$ with a not-too-wide p-MOSFET



In the case of $r_{op} << r_{on}$, the voltage gain would be limited by a small r_{op} , not good. Meeting condition $r_{op} >> r_{on}$ implies large Lp which leads to large W for the given drain current and overdrive voltage. This would be a too expensive solution due to large p-MOSFET size. Selection of the design parameters for matching output resistances ($r_{op} = r_{on}$) is a reasonable compromise which achieves both moderate voltage gain (only twice smaller than Ao) and moderate W of the p-MOSFET load.

p-MOSFET current source as n-MOSFET load in the voltage gain stage

The LOAD LINE represents an output characteristic of p-MOSFET with high load resistance for AC signal



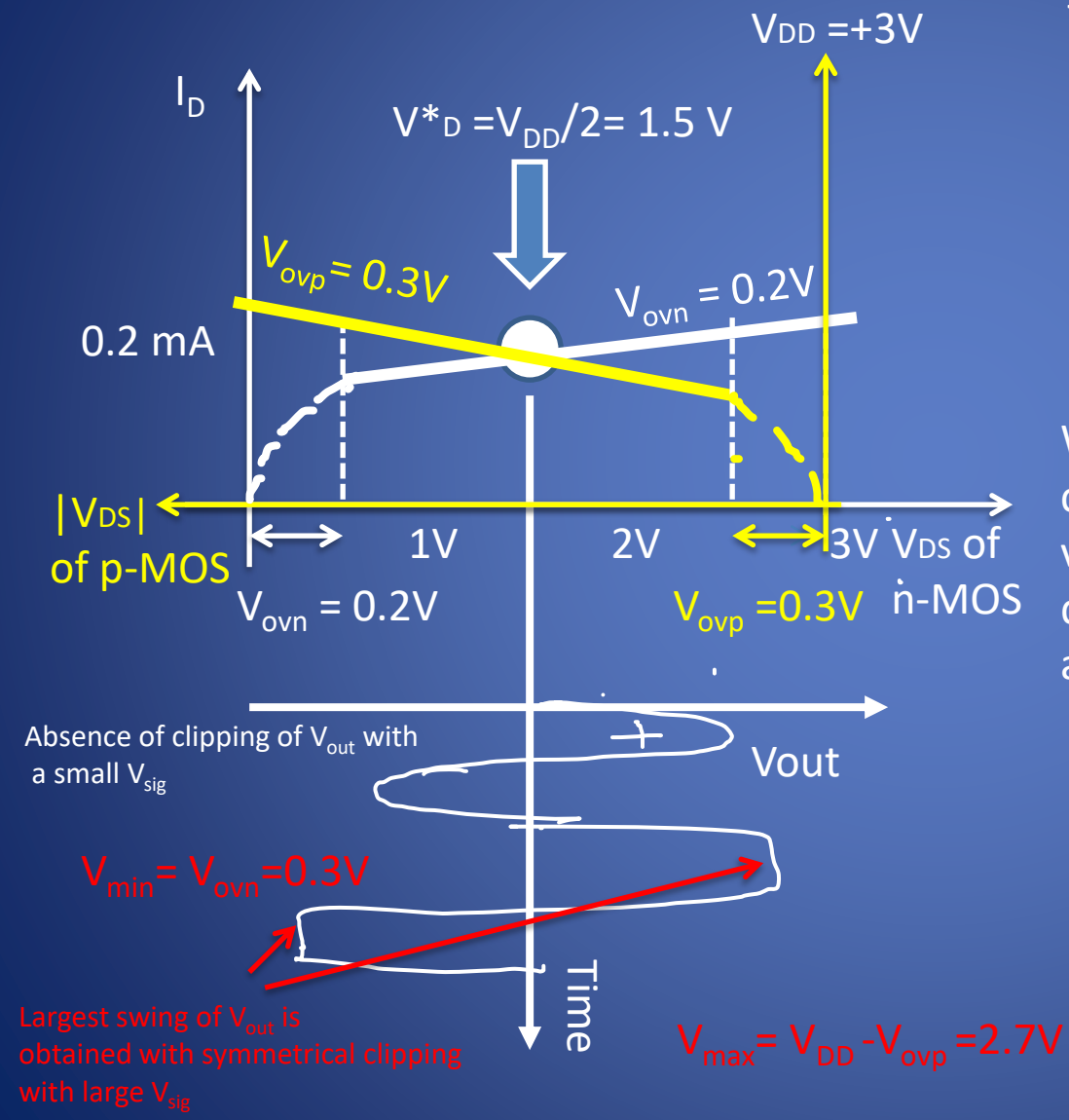
Operating point or quiescent (Q)-point):
V^*_D =1.5V, I_D*= 200 uA

The maximum output voltage (peak) Vout max is smaller than V_{DD} by the p-MOSFET overdrive voltage V_{ovp}

$Vout_{max} = Vdd - Vovp = 3 - 0.3 = 2.7$ V

The voltage scale reflects V_D measured with respect to ground
V_D increases to the right from 0 to V_{DD} = +3V DC.

DC Operating point and selection of the pMOSFET bias (Vgs and Vov, respectively)



The stage operating point (V_D*, Id*) is defined by intersection of the output characteristics of n-MOS and p-MOS devices. The optimal position of the operating point is $V_D^* = V_{DD}/2$ for the maximum amplitude of undistorted output voltage.

With small slopes of the output characteristics, the operating point is very sensitive to selection of MOSFET design parameters: Vovn , Vovp, as well as W and L.

Selection of the aspect ratio for p-MOS

by default $I_{Dn}=I_{dp}$

Requesting symmetrical clipping of the output voltage implies $V_{ovn} = V_{ovp}$
It would lead to a very wide p-MOSFET

$$W_p = (k'n/k'p)*(V'_{An}/V'_{Ap}) *W_n = 6\ W_n$$

$$\frac{K_n'}{K_p'} = 3 \qquad \frac{|V_{An}'|}{V_{Ap}'} = 2$$

A wide p-MOSFET current source would take too much area,
and would create a large capacitive load for n-MOSFET stage

For given DC current, W changes as a square of Vov. V_{ovp} can be moderately increased (x1.4 times) for significant (x2 times) decrease of Wp.

The width of p-MOSFET would be reasonably wider than that of n-MOSFET: $W_p = 3\ W_n$ realized with matched output resistances of n-MOS and p-MOS transistors ($L_p = 2*L_n$)

Summary of (most important) expressions

Selection of overdrive voltage and DC bias voltage:

$Vov = V_{GS} - Vt \rightarrow V_{GS}$

Transconductance and selection of DC bias current:

$g_m = 2I_D/Vov \rightarrow I_D$

Output resistance and gate length:

$r_o = V_A/I_D = (V'_A * L)/I_D \rightarrow L$

Aspect ratio and MOSFET width:

$(W/L) = (2I_D)/ (k' * Vov^2) \rightarrow W$

High output resistance r_o can be realized with a long gate length L
The long gate length L implies a large mosfet width W

K'p < k'n → for moderate width of p-MOSFET (and other reasons TBD) one selects Vovp > Vovn

Summary of (most important) process and design parameters

Process parameters	Design parameters
1. Threshold voltages V_{tn} = 0.7 V, V_{tp} = -0.8 V	V_{ovn} = 0.2 V, $\lvert V_{ovp} \rvert$ = 0.3 V
2. Process transconductance parameters k_n'= 200 uA/V^2 , k_p'= 70 uA/V^2	DC bias current: I_D
	Gate lengths: L_n, L_p
3. Early voltage parameters V_{An}'= 20 V/um, V_{Ap}'= 10 V/um	Gate widths: W_n, W_p