



EEO311

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# Analysis of the common-source differential stage

*Pete Mills*  
*ID: 115009163*

Associate Professor  
Dmitri DONETSKI

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# Copy of Original Assignment

EEO311

## Simulation assignment 2

### Analysis of the common-source differential stage

#### 1. Objectives

- Simulation of DC transfer characteristic of amplifiers, selection of MOSFET DC operating point.
- Simulation of AC response of gain stages. Determination of DC voltage gain for single -ended and differential outputs, cut-off (-3dB) and unity-gain frequencies.
- Evaluation of the effects of bias current, capacitive load, and input source impedance on AC response.

#### 2. Description of the amplifier

The differential-in differential-out amplifier shown in Figure 1 operates on capacitive load  $C1, C2$  from voltage source  $V_{id} = V1 - V2$  with internal resistance  $R_{sig} = R1 + R2$ . The differential input voltage of 1 V AC was split into two halves so that numerical value of the output voltage represents the differential voltage gain. The output voltage is taken as  $V_{out} = V_{out1} - V_{out2}$ .

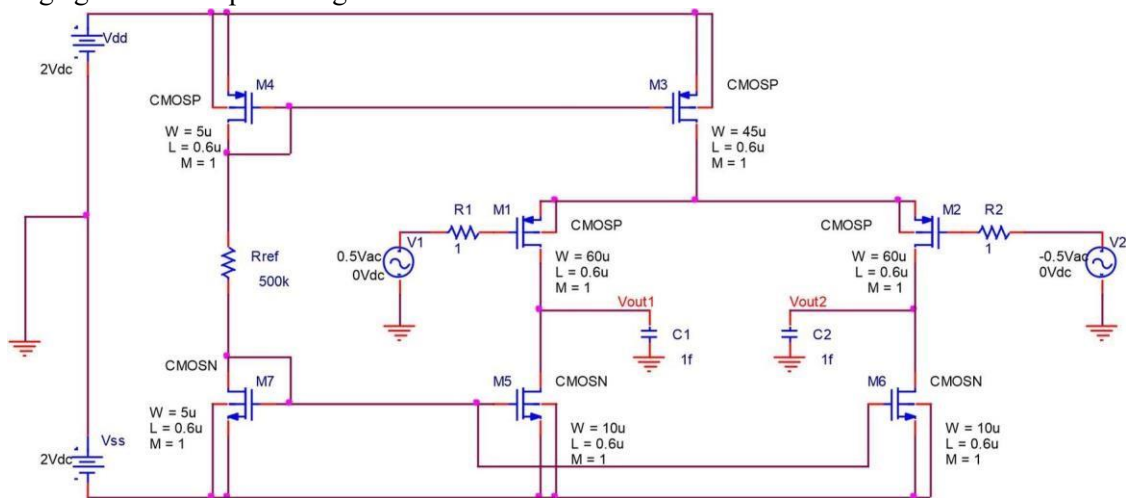


Figure 1. Schematic of the PMOSFET differential stage loaded with NMOSFET current sink.

The bias current of the PMOSFET differential pair  $M1, M2$  is defined by reference current through  $R_{ref}$  and the ratio of PMOSFET widths  $W3/W4$ . A large width of  $M1, M2$  ( $W1 = W2 = 60\mu$ ) was selected for a large voltage gain. Note that for PMOSFETs n-well (body, the 4<sup>th</sup> terminal) can be connected to the source terminal as shown for  $M1, M2$ . Parameters of the current source load (the sink  $M5, M6$  with  $W5=W6=10\mu$ ) were selected to obtain the DC voltage at the drains of  $M1, M2$  to be near  $-0.5V$  to allow for a large swing of  $V_{out}$  in both positive and negative directions from the steady state value (operating point). The width of  $M4$  and  $M7$  (diodes) is  $5\mu$ . The gate length of all devices is  $0.6\mu$ . The stage is powered from a bipolar DC source  $V_{dd}=2V$ ,  $V_{ss}=-2V$ .

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### 3. Assignment

- a) Enter the amplifier schematic in OrCAD (Figure 1) with MOSFET dimensions as shown. At this time use negligibly small values for  $R_1=R_2=1\text{ Ohm}$  and  $C_1=C_2=1\text{ fF}$  (later on these values will be increased to evaluate the impact of these parameters on frequency response of the amplifier). The value of reference resistor  $R_{\text{ref}}$  has to be selected with the last 3 digits of your ID number in kOhm. Take  $R_{\text{ref}}$  as the 3-digits of your ID number if it is above 500. In other case, add 500 to your 3digit number to make  $R_{\text{ref}}$  anywhere in 500k to 1 MOhm range.

- b) Simulate the operating points (DC bias). Inspect DC voltages and currents. The DC voltage at the drain of M1, M2 should be in -0.2 V...- 0.8 V range.

Ideally one would like to see  $V_{\text{out}}$  in the range from -0.4 to -0.6 V DC near the middle of the linear part of the DC transfer characteristic. For that simulate the DC transfer characteristic  $V_{\text{out1}}$  (V1) and inspect it. Without significant change of DC bias current, the DC output voltage could be adjusted by changing width M5, M6. Due to small width of NMOSFETs, it would be convenient to change  $W_1=W_2$  or fine tune out DC with change of  $W_3$  since the bias current was not specified. Copy both the final schematic with DC voltages and current displayed and the DC transfer characteristic to the report file.

- c) Obtain the magnitude and phase responses of the voltage gain for  $V_{\text{out1}}$  for the circuit with  $R_1$ ,  $R_2$ ,  $C_1$ ,  $C_2$  as shown in Figure 1. The suggested frequency range for AC analysis is 10 kHz to 10 GHz. Obtain the Bode plot with both magnitude in dB and phase responses, determine accurate values of the -3 dB cut-off frequency and the voltage gain in dB for single ended output. Copy the Bode plot to the report. Estimate the gain-bandwidth product for this case in GHz.

- d) Increase the capacitive load to  $C_1 = C_2 = 100\text{ fF}$ . It models the amplifier load due to input (gate to source) capacitance of the 2<sup>nd</sup> stage (not shown). Obtain the Bode plot for this case and determine the -3 dB cut-off frequency and the unity gain frequency (frequency for 0 dB gain). Estimate the gain-bandwidth product for this case.

- e) Increase the bias current by scaling down the value of the reference resistor by a factor in the range from 3 to 4 (your choice). Simulate the operating points (bias), display DC voltages and currents. Adjust MOSFET widths (M3, for example) to obtain  $V_{\text{out}}$  DC at the drains of M1, M2 approximately in the middle of the DC transfer characteristic. Copy the final schematic with DC voltages and current displayed, the DC transfer characteristic to the report. Simulate the Bode plot and determine the DC gain (gain at low frequencies), the -3 dB cut-off and unity gain frequencies. Estimate the gain-bandwidth product for this case.

- f) Increase resistances to  $R_1 = R_2 = 100\text{ kOhm}$ . These are to model the input signal source internal resistance. Simulate the Bode plot for this case, determine the -3 dB cut-off and unity gain frequencies for the amplifier. Examine the Bode plot and identify two poles: the pole created by the input signal source resistance and the effective input capacitance of the PMOSFET stage due to Miller effect and the pole due to the stage output resistance and load capacitance. Estimate the frequencies of the poles from the plot (approximately).

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- g) Summarize the data for 3 cases (3d, 3e, 3f) in a table. Include the bias current (drain current of M3), voltage gain for single ended and differential output cases, -3 dB bandwidth, gain-bandwidth product and unity gain frequency (where applicable).

### 4. Bonus

With completion of the bonus assignment a 50 % will be added to Sim 2 score. Obtain the following dependences for the PMOSFET with gate length  $L = 0.6 \mu\text{m}$ :

- a) DC drain current per unit gate width versus  $V_{gs}$ , use decimal log scale for the drain current. Obtain the plot of  $I_d(V_{gs})$  in the range from 0.4 to 1.2 V (absolute values) with a 0.01 V increment at a constant  $V_{ds} = 1.5\text{V}$  (absolute value), plot it in the decimal log scale to reveal the exponential dependence of the subthreshold current on  $V_{gs}$  and determine the slope in reciprocal V. Estimate the value of  $V_{gs}$  increment in mV required to change  $I_d$  by an order of magnitude in the subthreshold region.
- b) Transconductance over drain current ( $g_m/I_d$ ) versus  $V_{gs}$  for the above conditions. One can obtain it as a derivative of natural logarithm of drain current versus  $V_{gs}$ . Simulate the PMOSFET transfer characteristic, plot  $d(\log(I_d))$ . The plot shows that one can obtain high voltage gain in a region of small  $V_{gs}$  with small bias current at the expense of MOSFET width and the device capacitances, respectively. For given gate length, parameter  $g_m/I_d$  reflects maximum voltage gain which can be realized.
- c) Identify the operating regimes of the PMOSFET (weak, moderate or strong inversion) in your circuit for both DC bias current values. Operation in the region of moderate inversion is often desirable as it allows to realize both high voltage gain and wide bandwidth. Increase of the bias current and selection of higher  $V_{gs}$  are selected if greater gain-bandwidth product is required when time constants are limited by MOSFET parasitic capacitances ( $C_{gs}$ ,  $C_{gd}$ ).
- d) Estimate the PMOSFET transconductance of M1, M2 for the case with greater bias current from the plot  $g_m/I_d$ . Calculate the amplifier gain -bandwidth product (unity gain frequency for the response with a single-pole) from estimates of  $g_m$  and output load capacitance. The load capacitance is obtained by sum of  $C_1 = 100 \text{ fF}$  and  $C_{gd1} + C_{gd5}$ . Estimate the gate to drain capacitances assuming  $C_{ox} = 4 \text{ fF}/\mu\text{m}^2$  and a 10 % overlap of the gate and drain regions. Compare the gain-bandwidth product values obtained by simulation and by estimate from  $g_m$  and capacitive load.

### 5. Report

The report should include a brief description of the project goals, copies of amplifier schematics for 3 cases including DC potentials and currents, all simulated plots, evaluated parameters presented in a table, discussion of observed trends, estimates of pole frequencies by visual inspection of Bode plots and a brief summary.

# Overview

In simulation 2 our primary objective is to observe how changes in mosfet construction parameters can influence a design. Here we made adjustments to mosfets used in the implementation of a differential amplifier. By making adjustments to the width parameter and current mirror reference resistor we are able to tune the amplifier to improve efficiency and minimize distortion.

## 1 Assignment

### 1.1 Part A

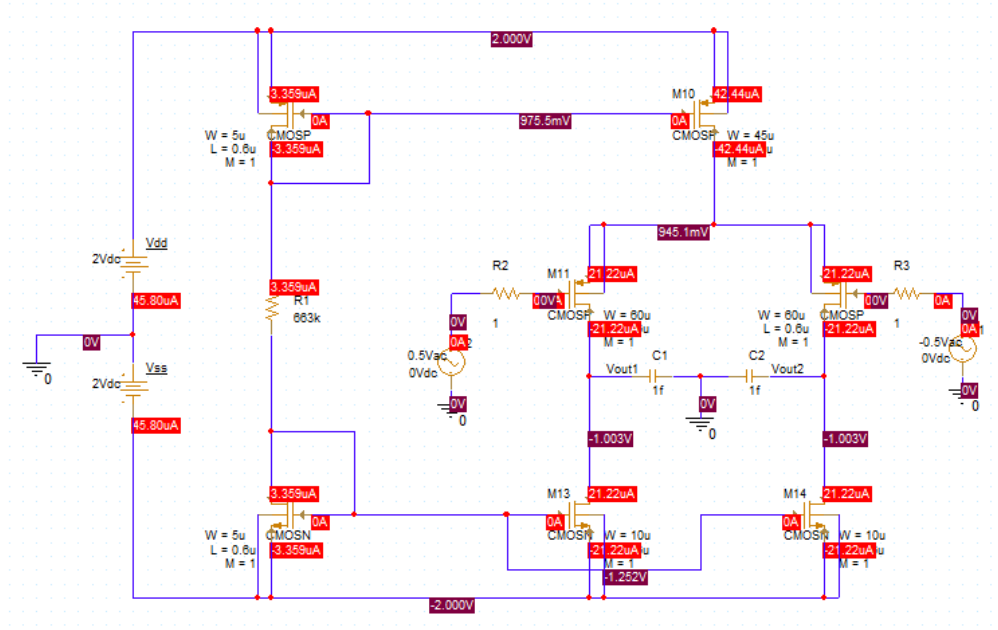


Figure 1: Bias point simulation with reference current resistor value set to  $663k\Omega$ .

## 1.2 Part B

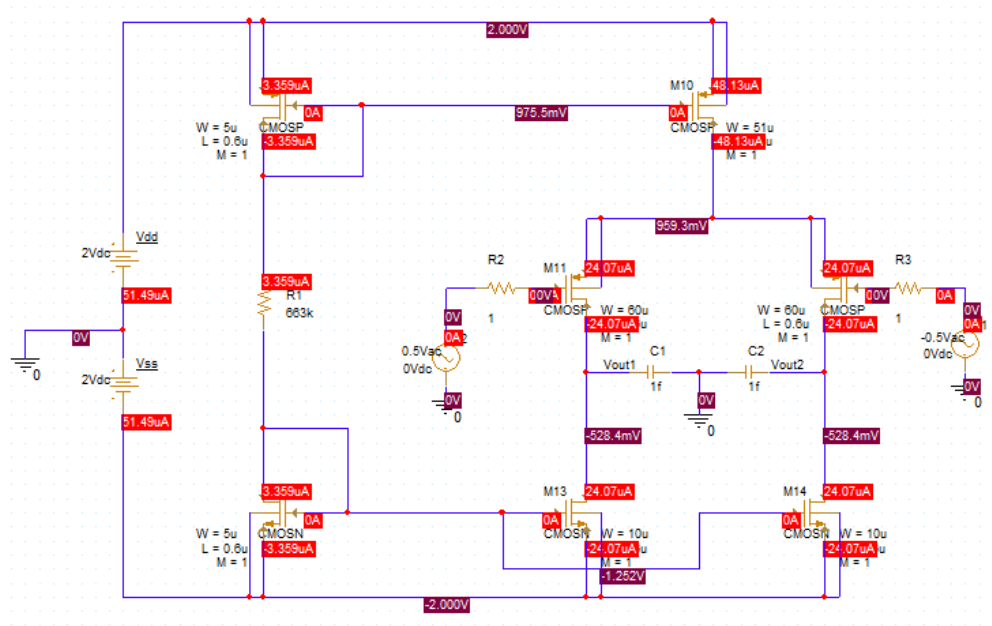


Figure 2: M10 width changed to 51  $\mu\text{m}$ .

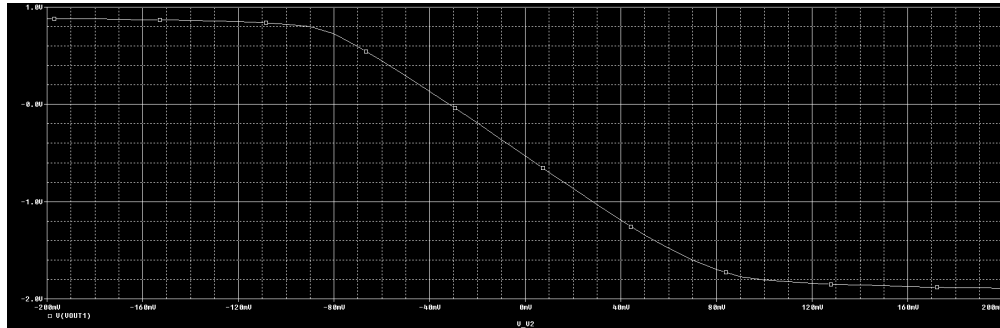


Figure 3: DC Transfer characteristic for Vout1 reveals a range  $\approx -90\text{mV}$  to  $100\text{mV}$ .

1.3 Part C

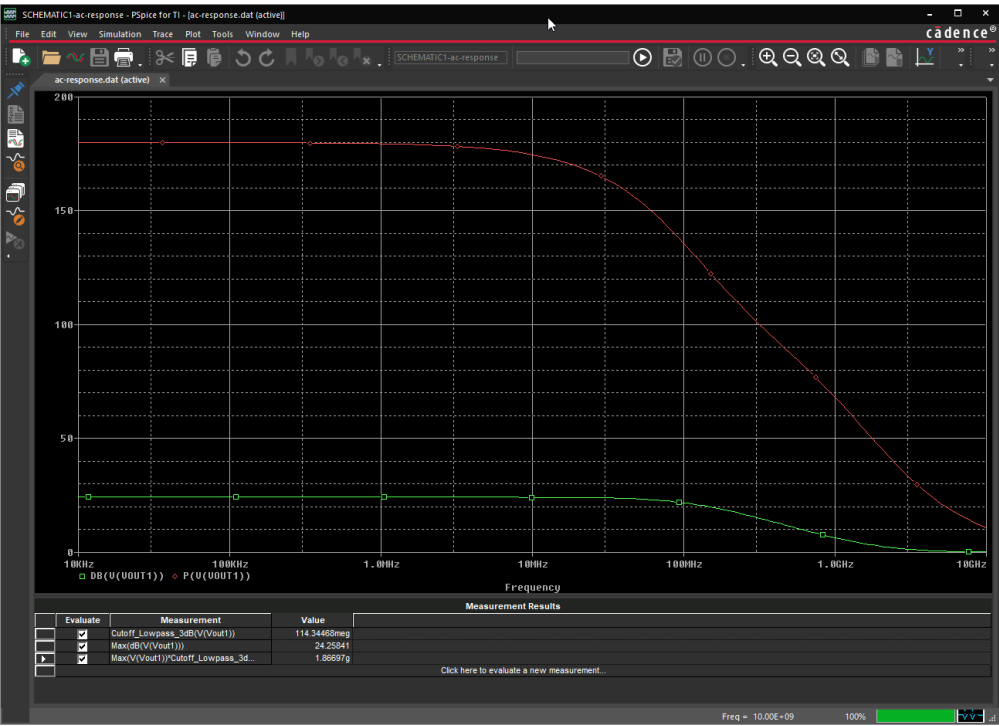


Figure 4: Cutoff frequency: 114.3 MHz. Gain: 24.3. GBP: 1.87 GHz.

## 1.4 Part D

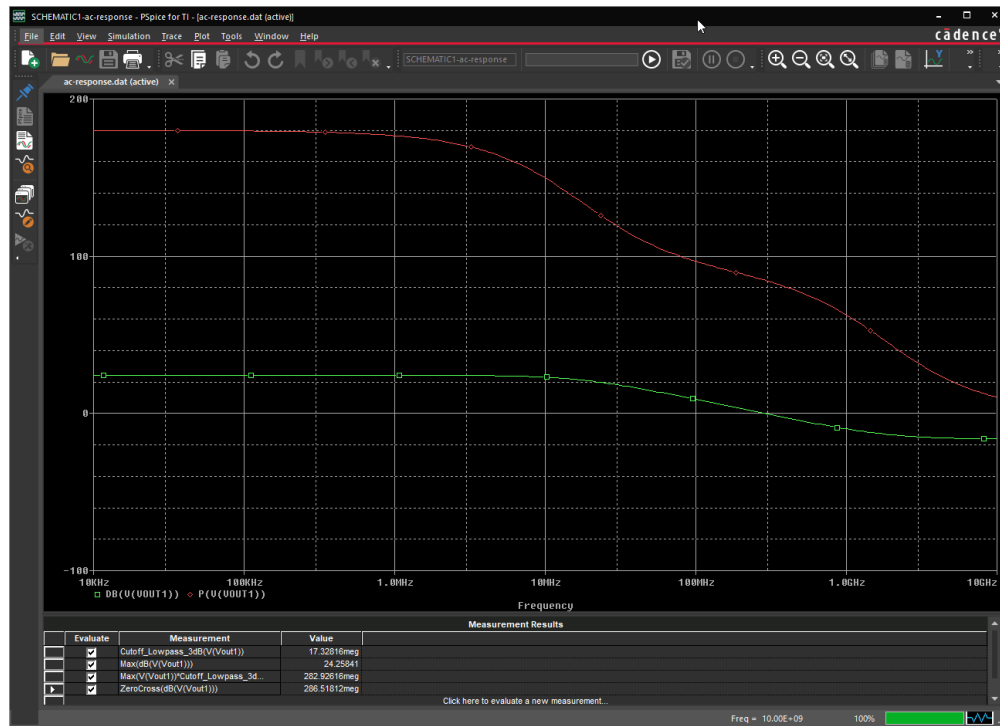


Figure 5: Cutoff frequency: 17.3 MHz. Gain: 24.3. GBP: 282.9 GHz. Unity Gain: 286.5 MHz



## 1.5 Part E



Figure 6: DC transfer characteristic.

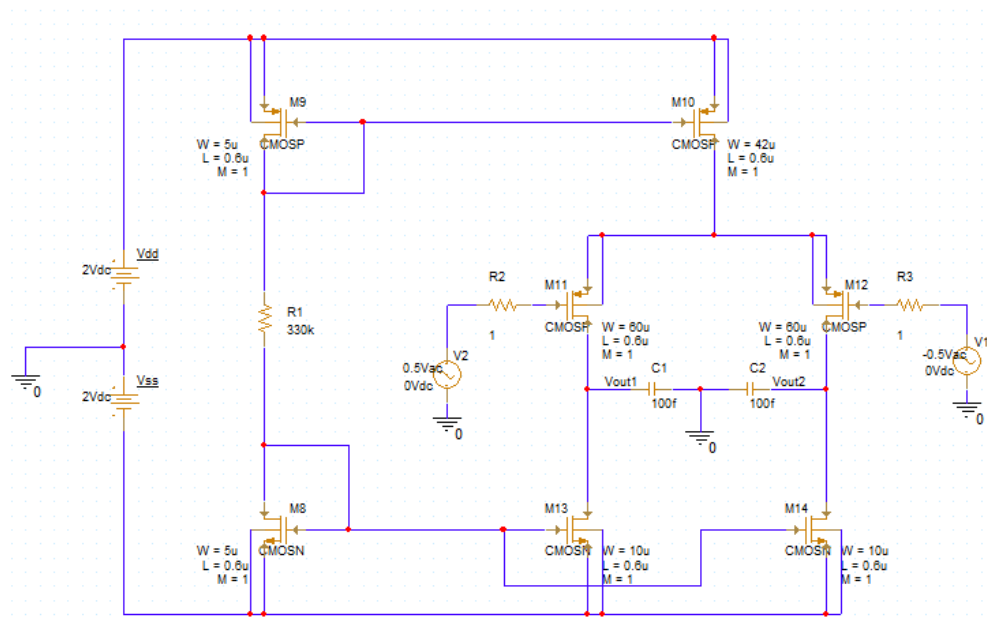


Figure 7: Schematic

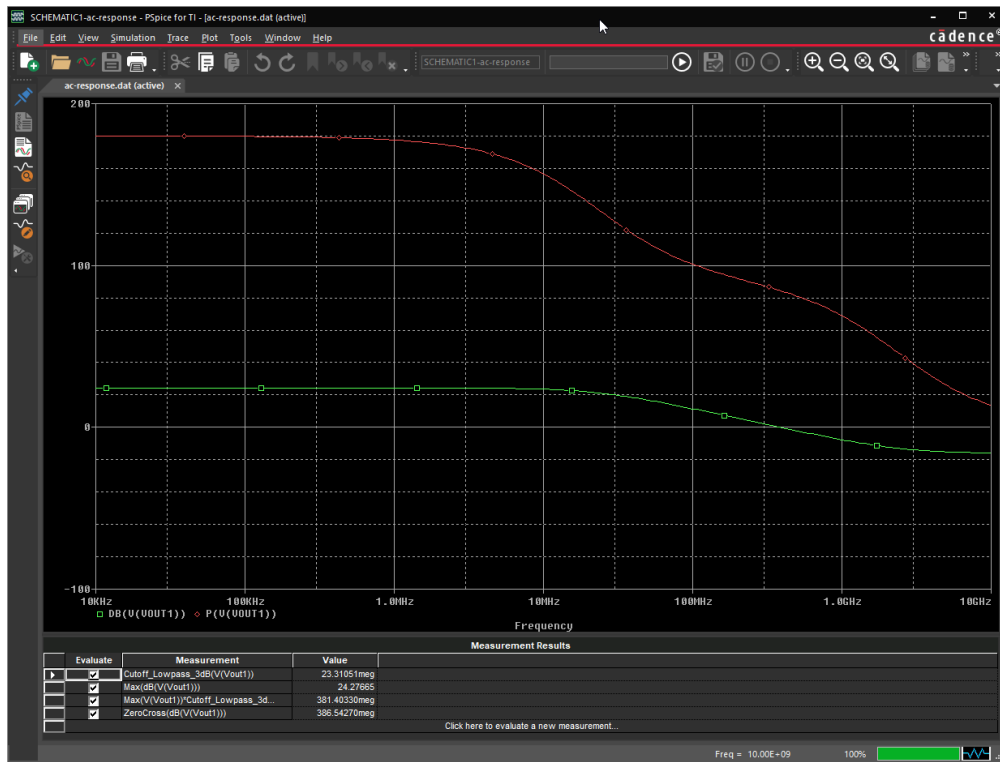


Figure 8: Cutoff frequency: 23.3 MHz. Gain: 24.3. GBP: 381.4 GHz. Unity Gain: 386.5 MHz

## 1.6 Part F

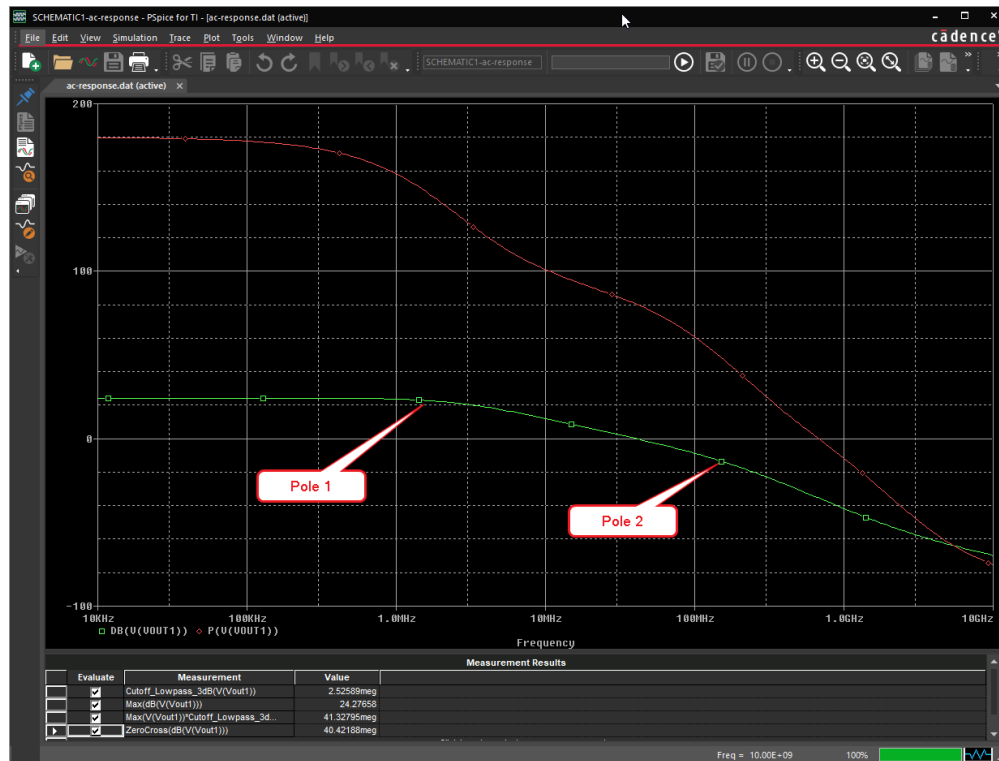


Figure 9: Cutoff frequency: 2.5 MHz. Unity Gain: 40.4 MHz, Pole 1: 2.5 MHz, Pole 2: 200 MHz

## 1.7 Part G

Table 1: Simulation Data Summary

Case	Bias Current	Gain (SE)	Gain (DO)	Bandwidth	GBP	Unity Gain
3D	48.1 $\mu$ A	24.3	32.5	17.3 MHz	282.9 GHz	286.5 MHz
3E	48.1 $\mu$ A	24.3	32.7	23.3 MHz	381.4 GHz	386.5 MHz
3F	71.3 $\mu$ A	24.3	32.7	2.5 MHz	41.3 MHz	40.4 MHz

## 2 Bonus

I will return to complete if time permits.