EEO352 Lab 5
Counters

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Copy of Original Assignment

EEO 352 Fall 2023 - Assignment 5 – Counters

Please document each step with snapshots of the built circuit, plots, pictures and your observations. Please include this page.

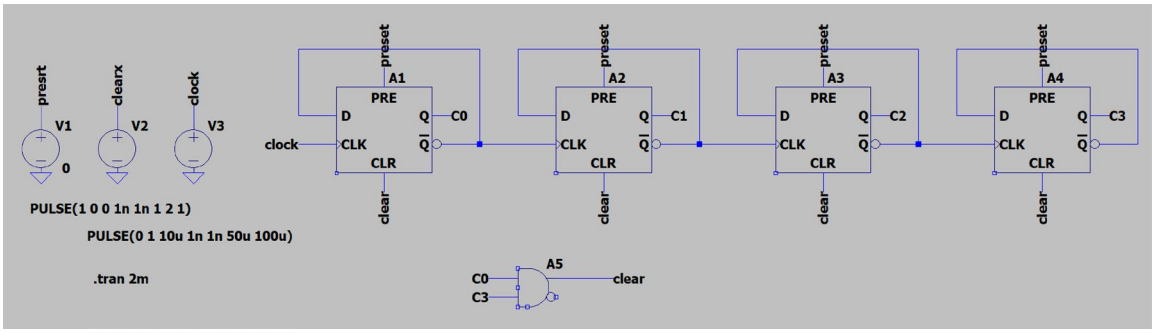

Fig.1a

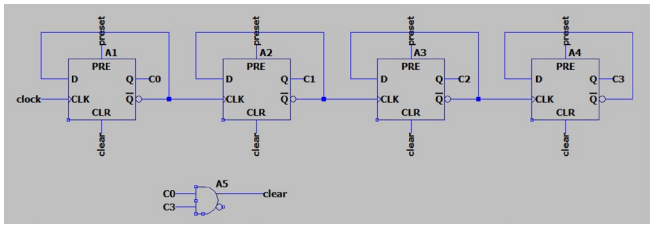

Fig.1b

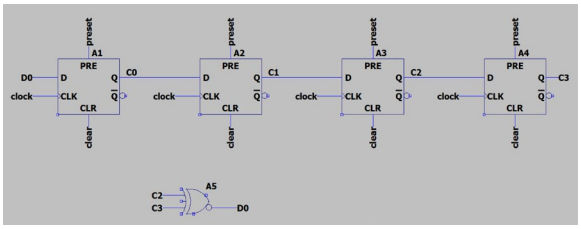

Fig.1c

1) Using the components in the Digital library, design and simulate as follows, plotting the clock and the four outputs in separate panes (**25pts**):

a) Divide-by-16 counter as shown in Fig.1a

b) Divide-by-9 counter as shown in Fig.1b

c) Pseudorandom counter as shown in Fig.1c

Note1: The LTspice ideal DFLOP triggers on the positive edge of CLK, and the PRE and CLR are active high

Note2: In order to avoid simulator convergence issues, set Trise=1ns and Tfall=1ns in all digital gates.

Note3: Use a 10kHz clock and clear all flip-flops at the beginning of the simulation.

2) Using two 74LS74, one 74LS00 and one 74LS86, build and measure the circuits at (1a), (1b) and (1c), plotting the clock on the oscilloscope and in the logic analyzer, and the four outputs in a bus, which shows the counts using the logic analyzer of the Analog Discovery (**75pts**).

Note1: Use a +5V supply and ground.

Note2: In the 74LS74 the PRE and CLR are active low: connect both to +5V

Note3: In order to start the psudorandom counter, you may need to temporarily force D of the first flip-flop high, and then move D back to the output of the XOR.

Summary

In this lab we built frequency division circuits and a pseudorandom counter. To implement these circuits we used the following IC's.

- 74LS74 D-FF
- 74LS00 Quad 2-Input NAND Gate
- 74LS86 Quad 2-Input Exclusive-OR Gate

There are several differences between the LTspice special function/mixed mode simulation devices and the actual CMOS components we prototyped. This required a different approach to specifying the circuit in LTspice vs on the breadboard.With the differences identified and accounted for, the simulation produced results identical to the real world experiment.

The divide by 16 circuit is a straight forward implementation of 2^n frequency division. Whereas the divide by 9 circuit required a different approach. Here we made a binary counter, then NAND a reset/clear signal when the binary value is equal to decimal 9.For my implementation of the pseudorandom counter it was necessary for me to start the DFF by taking DO high before reattaching to the output of the XOR. This procedure was described in the lab instructions.

1 Design and Simulate

a)

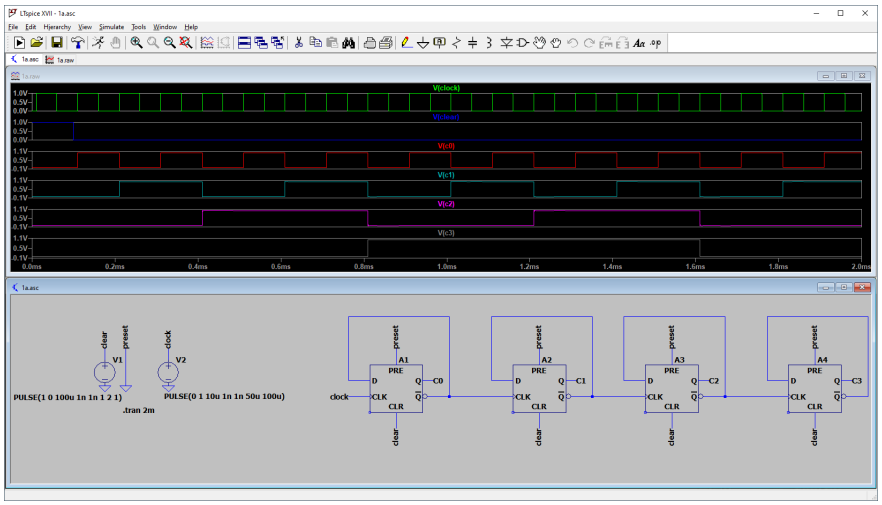

Figure 1: Divide by 16 circuit

b)

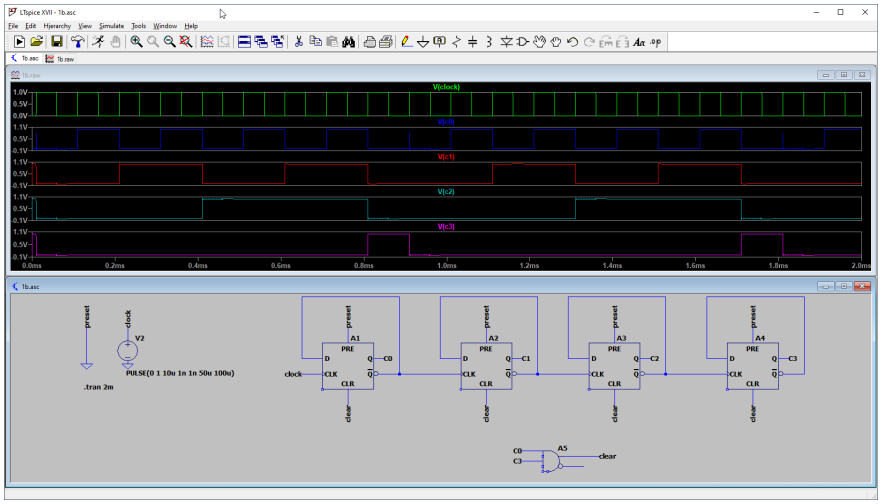

Figure 2: Divide by 9 circuit. Note the asymmetrical duty cycle.

c)

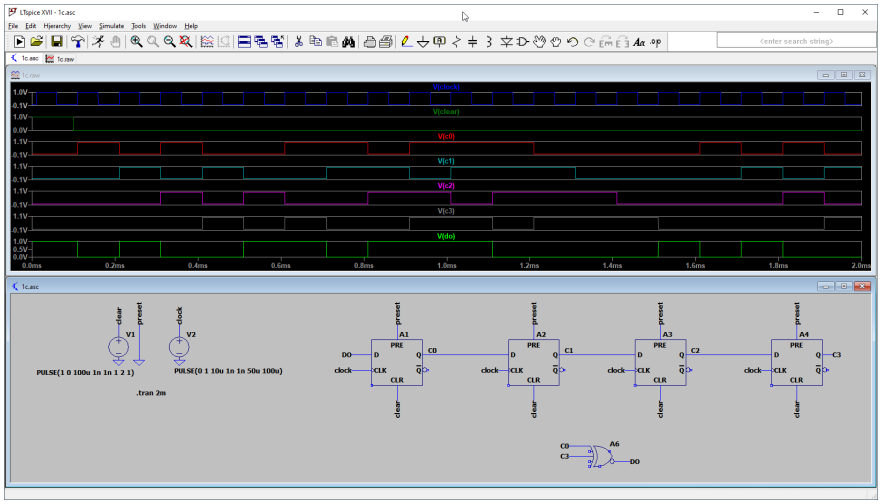

Figure 3: Pseudo random generator

2 Build and Measure

a)

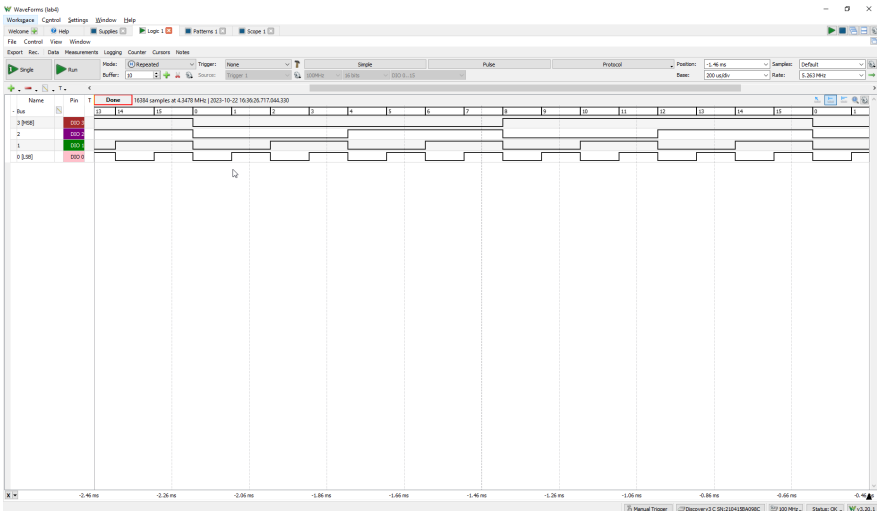

Figure 4: Divide by 16 analysis

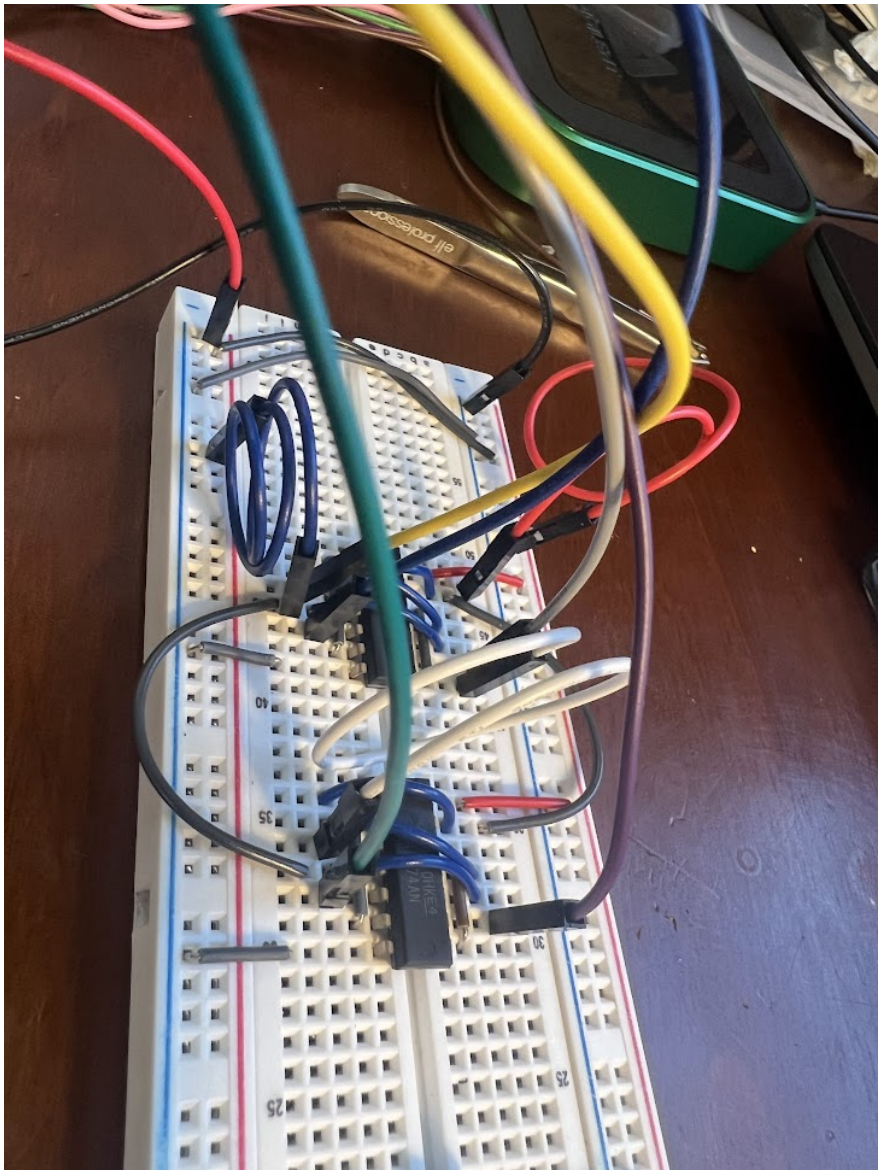

Figure 5: Divide by 16 prototype circuit photo

b)

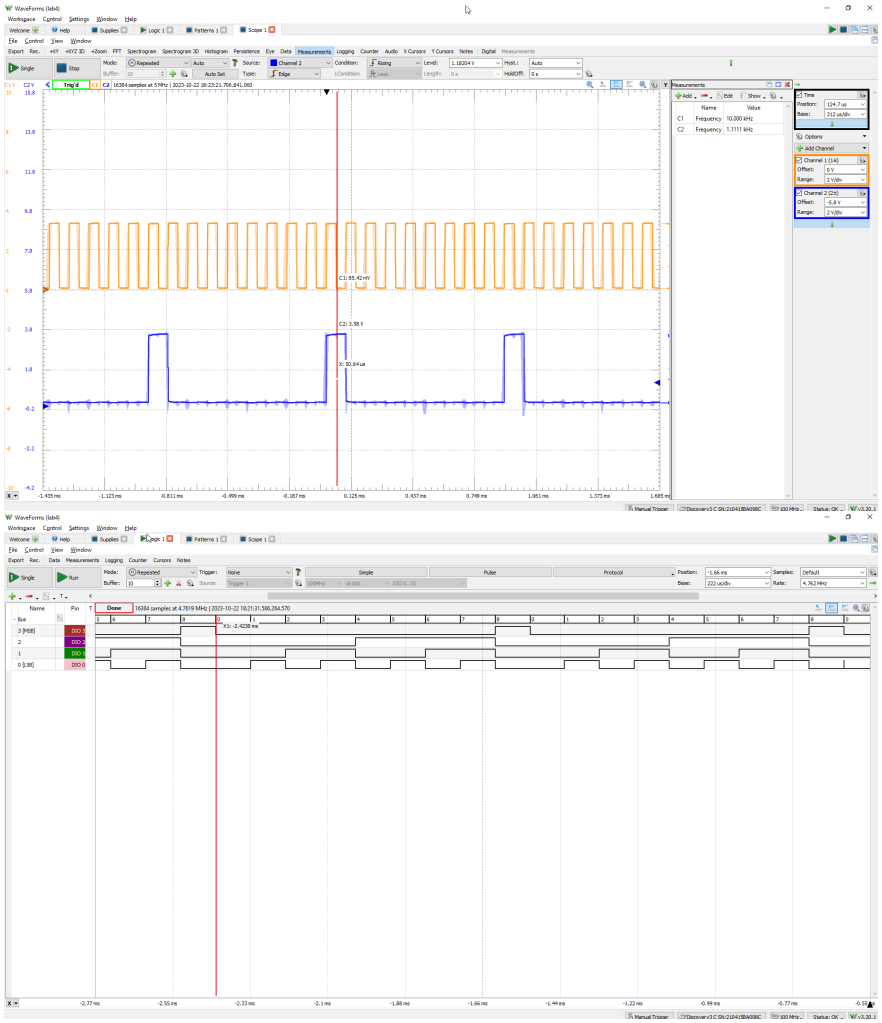

Figure 6: Divide by 9 analysis

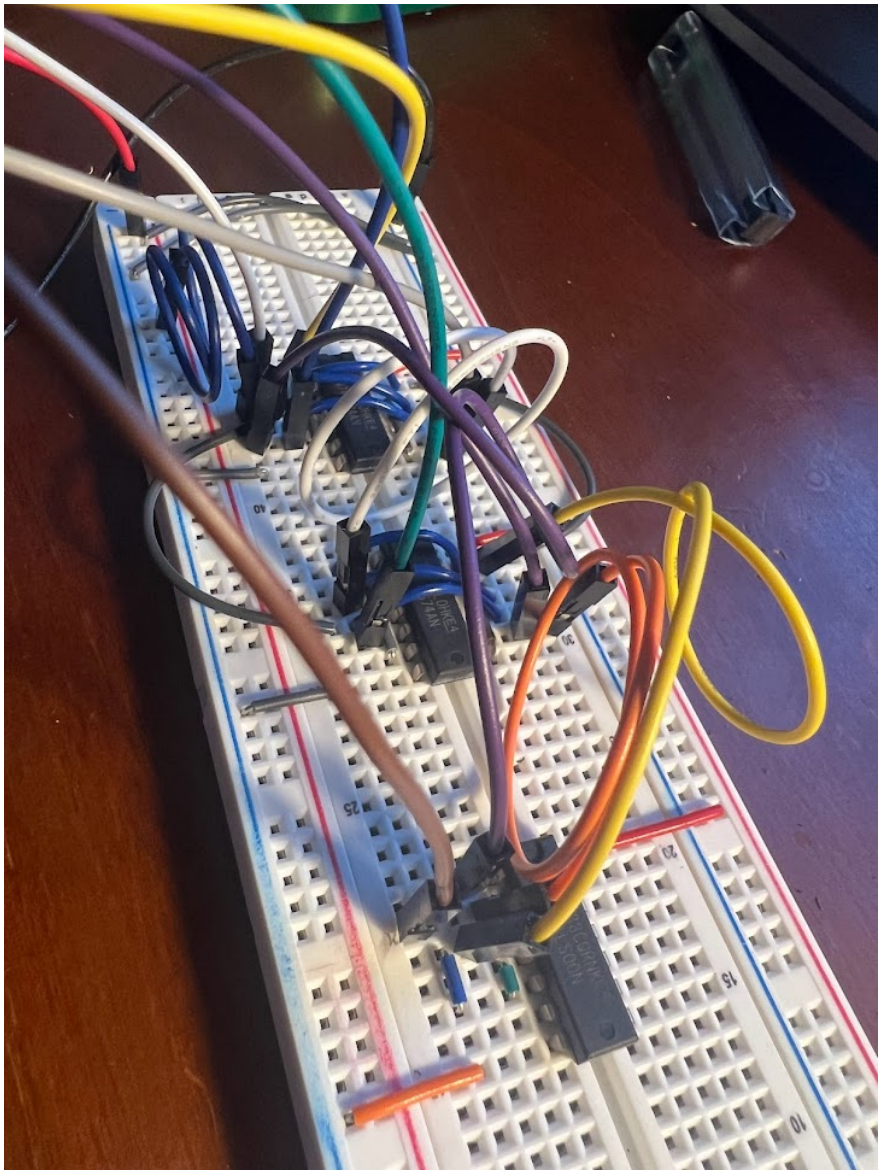

Figure 7: Divide by 9 prototype circuit photo

c)

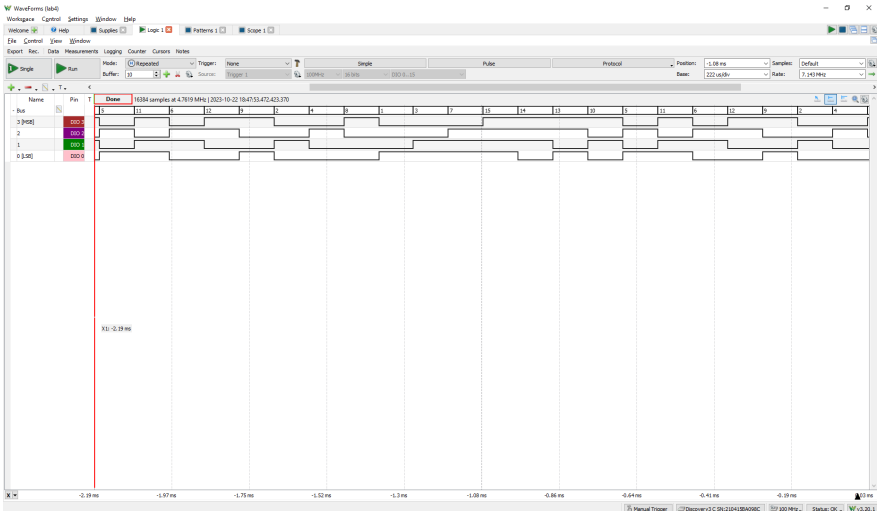

Figure 8: Pseudorandom counter analysis

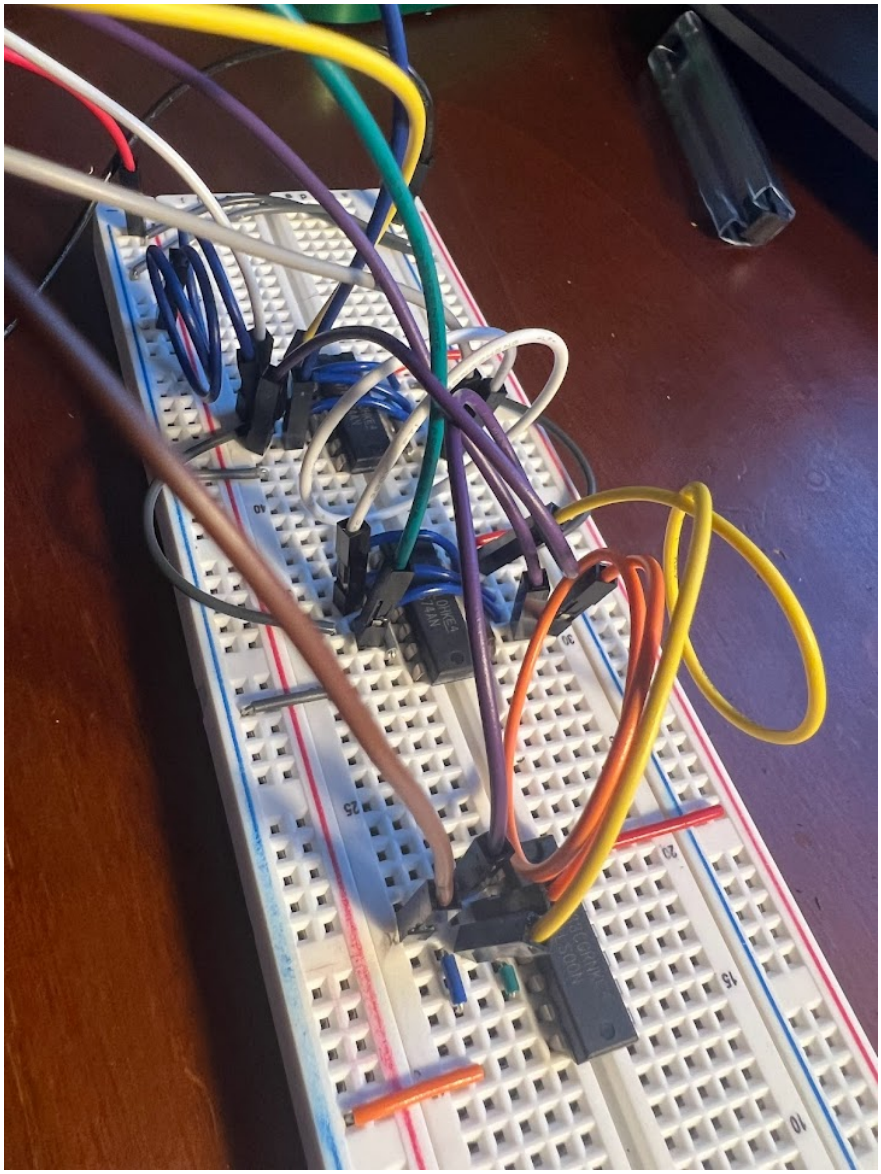

Figure 9: Pseudorandom counter prototype circuit photo