Homework 8

Common-source amplifier A and Cascode amplifier B operate on a 100 fF load capacitance C1=C2= C_load =100 fF. Circuit B was obtained by incorporation of the common-gate stage M3 to circuit A. All devices are biased to operate in the saturation region with the same transconductance gm = 1 mA/V. The MOSFET output resistances and Cgs and Cgd capacitances are as follows:

ro_n = ro1 = ro3 = 100 kOhm, ro_p = ro2 = 50 kOhm

Cgs_n = 20 fF, Cgs_p = 60 fF, Cgd_n = 5 fF, Cgd_p = 15 fF.

Consider a two-pole frequency response formed by two time constants:

a) output resistance Rout seen by C_load and the total capacitive load C_load + Cgd_n + Cgd_p.
b) input signal source resistance R1=R2 =Rsig =100 kOhm and the capacitance seen by Rsig at the gate of M1.

Note that in Amplifier B the Miller capacitance was reduced compared to that in Amplifier A due to reduction of the voltage gain of M1. Assignment:

1. Calculate the DC voltage gain, the time constants forming two poles and the pole frequencies. Estimate the – 3dB bandwidth for amplifiers A and B. Complete the table in the next page.
2. Sketch the amplitude and phase responses of the voltage gain for amplifiers A and B on the provided Bode plot template. Note that inverting amplifiers have a 180 deg phase shift at low frequencies.

Upload a copy of page 2 to BSpace for grading.

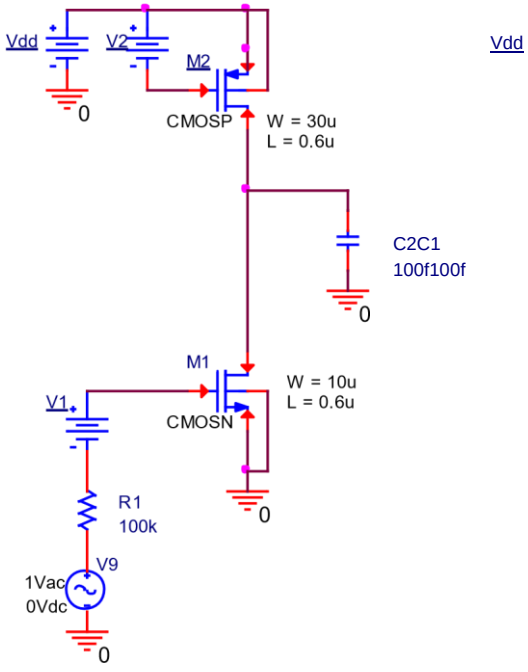

Figure A

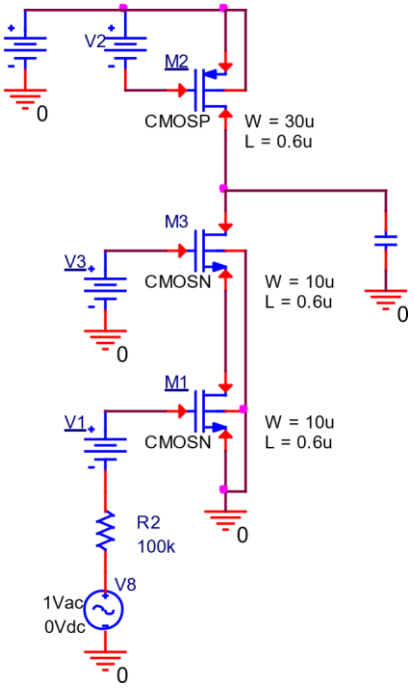

Figure B

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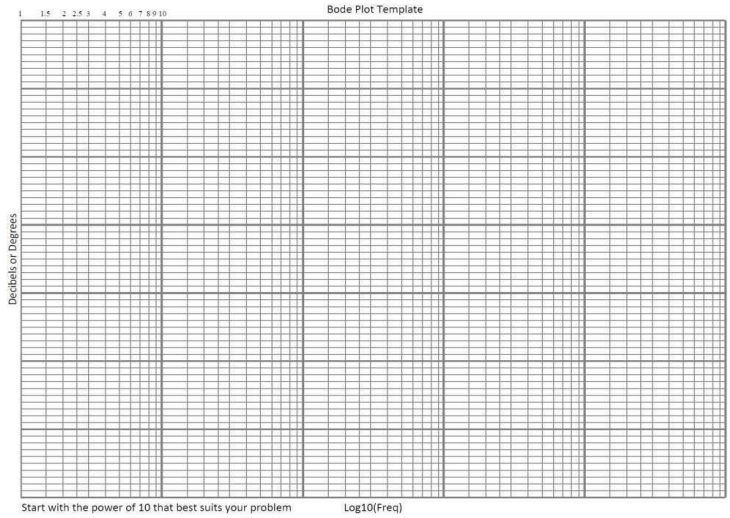
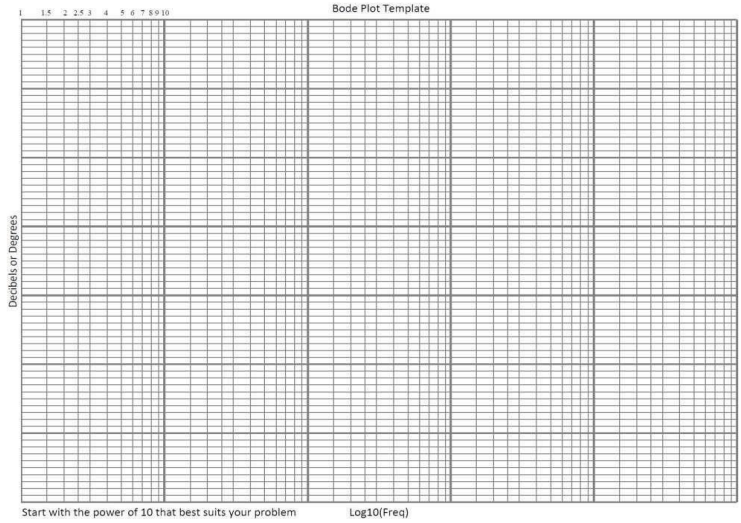
1 . Amplitude responses of the voltage gain for amplifiers A and B.



Phase responses for amplifiers A and B.



2. DC voltage gain, pole frequencies and bandwidth for the amplifiers

	A	B
DC voltage gain, dB		
1st pole frequency (MHz)		
2nd pole frequency (MHz)		
Bandwidth at -3 dB point (MHz)		