EEO353 Lab 4
Multi-Stage Amplifier Project - ABET

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Copy of Original Assignment

Assignment 4 - Multi-Stage Amplifier Project - ABET

This Assignment aims at verifying and expanding, with design, simulations and measurements, your creativity and your knowledge and understanding of the differential amplifier circuit.

This is a Project: you must design and build your circuit starting from specifications and constraints.

Please document each step with snapshots, pictures, and your observations. Wherever possible please include the date and time field and the AD S/N. Please include this page.

1) Using the simulator, design and simulate a multi-stage amplifier using the following specifications and constraints (**50pts**) *(ABET PI-21,PI-22,PI-23)*:

- Use NPN and PNP BJTs (recommended 2N3904, 2N3906)
- Use three supplies: +5V, -5V, 0V
- Use BJTs only in each stage, including loads and current sources (no resistors allowed) except for current biasing circuits (i.e. use resistors and BJTs only to generate the bias voltages for the loads and current sources of the amplifier)
- First stage: differential with current < 5mA
- Second stage: common-base to realize, with the output of the first stage, a cascode stage with current < 1mA
- Third stage: emitter follower with current < 10mA
- Gain > 5,000
- Gain-bandwidth product > 10MHz
- Single dominant pole (compensated if needed for stability)

2) Using the simulator, design and simulate a non-inverting amplifier with gain ~10 by applying a negative feedback network to the multi-stage amplifier developed in task 1 (i.e. used as operational amplifier) (**25pts**)

a) Simulate the response to a 100mV, 10kHz sinusoidal input, simulate the transfer function and calculate the -3dB
b) Apply and offset to the sinusoidal input in order to have an average ~0V at the output; explain why the offset is needed

3) Build the circuit at (2) and experimentally reproduce the simulations (**100pts**) *(ABET PI-24)*

Helpful hints:

- Use small resistors at the differential inputs in order to minimize the offset from the Base currents
- Consider using a BJT mirror for the loads of the differential stage
- Filter all supplies to 0V with tens to hundreds of µF
- Filter all bias voltages to 0V (especially the base of the cascode) with tens to hundreds of µF
- Add compensation to the gain node if needed for stability
- BJTs can get damaged: if needed, you can check the PN junctions by using the multimeter in diode or resistance mode

4) Suggest ways to improve beyond specifications the performance of the amplifier at (1) (**25pts**) *(ABET PI-25)*

Summary

In this laboratory experiment, we began with the design and simulation of a multi-stage amplifier tailored to meet specific performance criteria and component constraints. Following the initial design, we proceeded to adjust the circuit to create a variant with reduced gain. Subsequently, we further refined this second amplifier to address issues related to output offset voltage.

Transitioning from simulation to practical implementation, we constructed the lower-gain BJT amplifier and conducted measurements, the same as those performed during the simulation phase.

Concluding our practical endeavors, we are tasked with providing recommendations for enhancing the circuit's performance and functionality. These suggestions aim to refine the amplifier's characteristics beyond the initial specifications, offering avenues for optimization.

1 Using the simulator, design and simulate a multi-stage amplifier using the following specifications and constraints

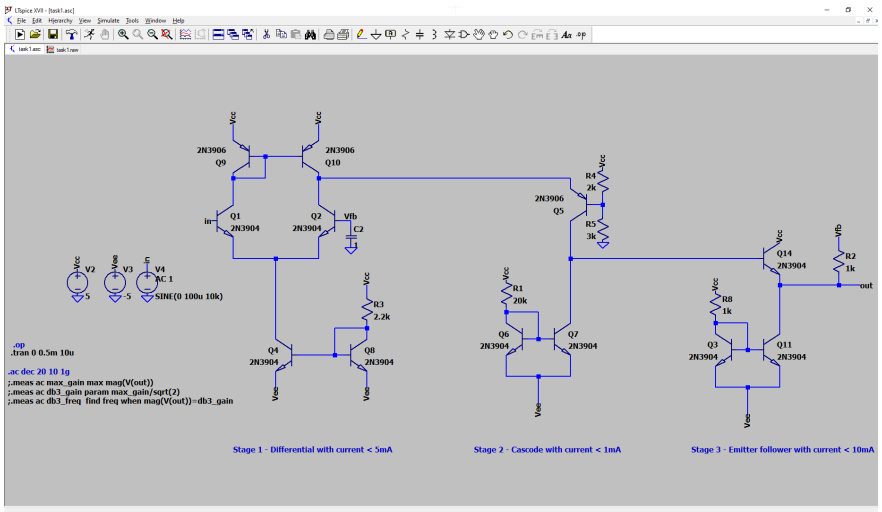

Figure 1: Schematic

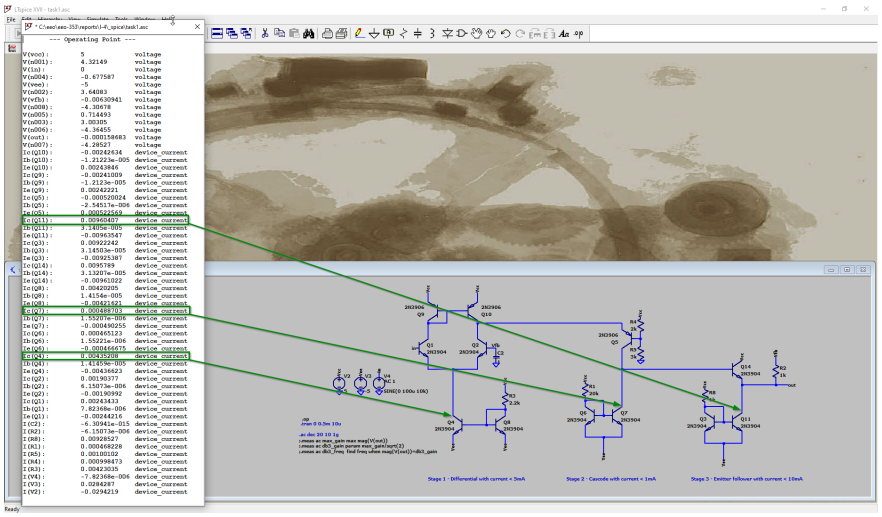

Figure 2: DC Operating Points showing compliance with stage current requirements.

b)

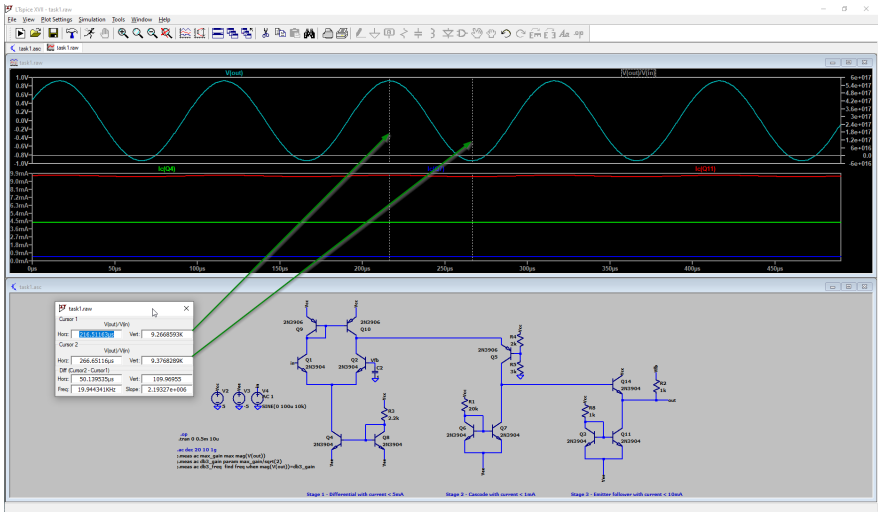

Figure 3: Transient Response showing total gain exceeding the required minimum.

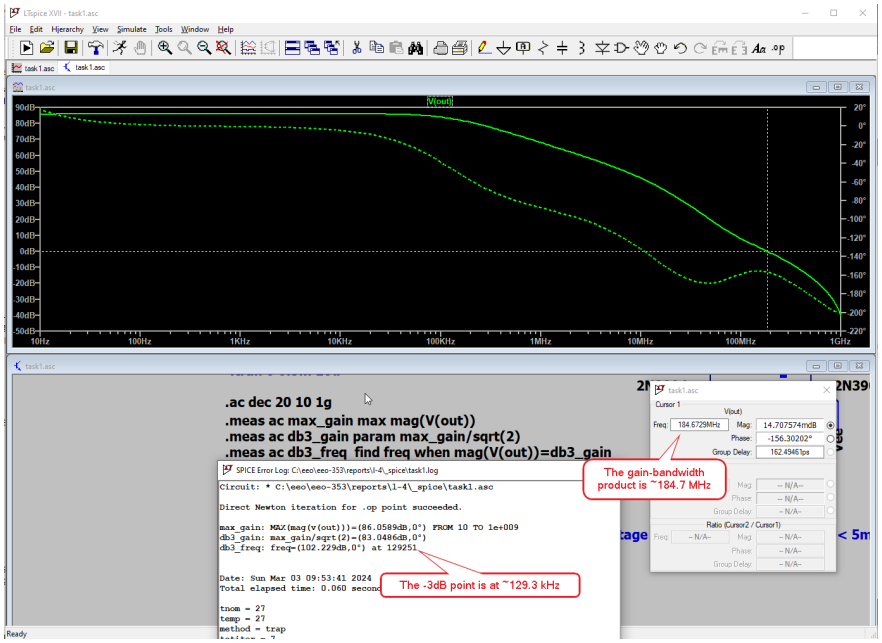

Figure 4: AC Analysis showing both the $-3\,\mathrm{dB}$ frequency and the Gain-Bandwidth product.

2 Using the simulator, design and simulate a non-inverting amplifier with gain ≈ 10 by applying a negative feedback network to the multi-stage amplifier developed in task 1

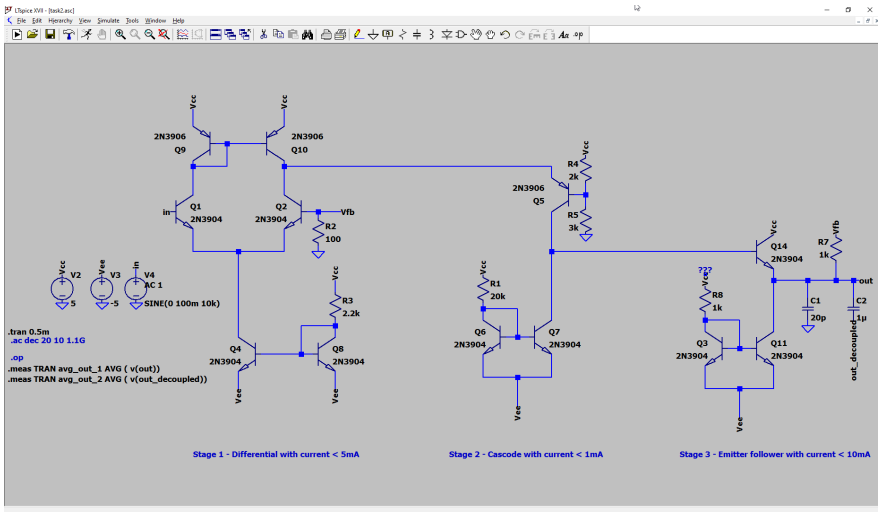

Figure 5: Schematic

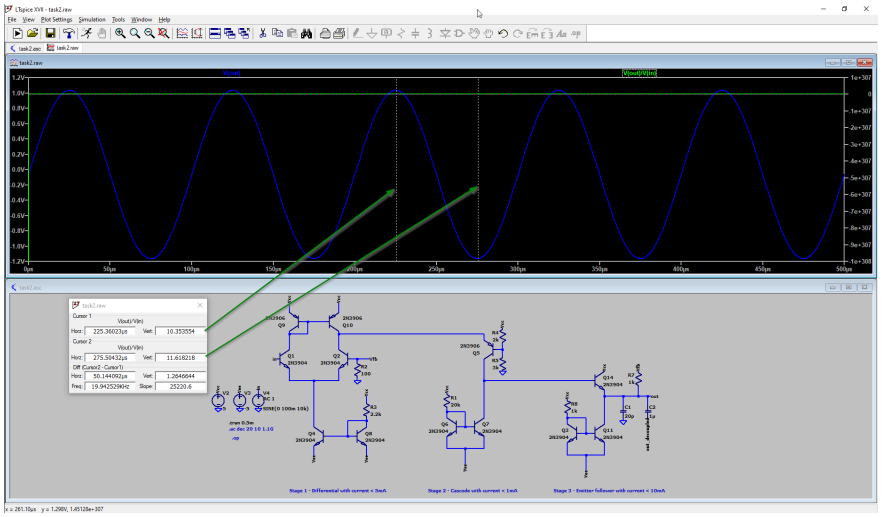

Figure 6: Transient analysis showing an average system gain.

a)

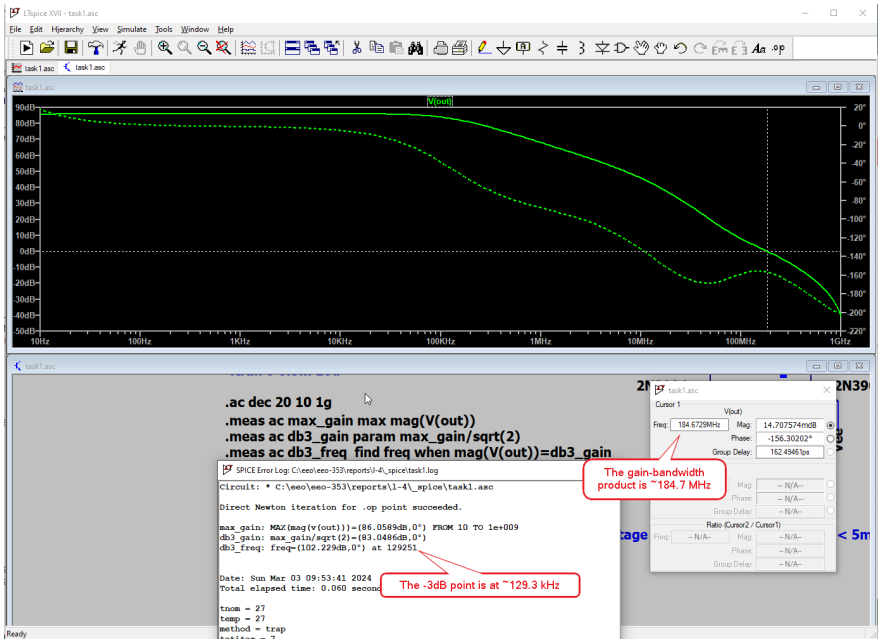

Figure 7: AC Analysis showing both the $-3\,\mathrm{dB}$ frequency and the Gain-Bandwidth product.

b)

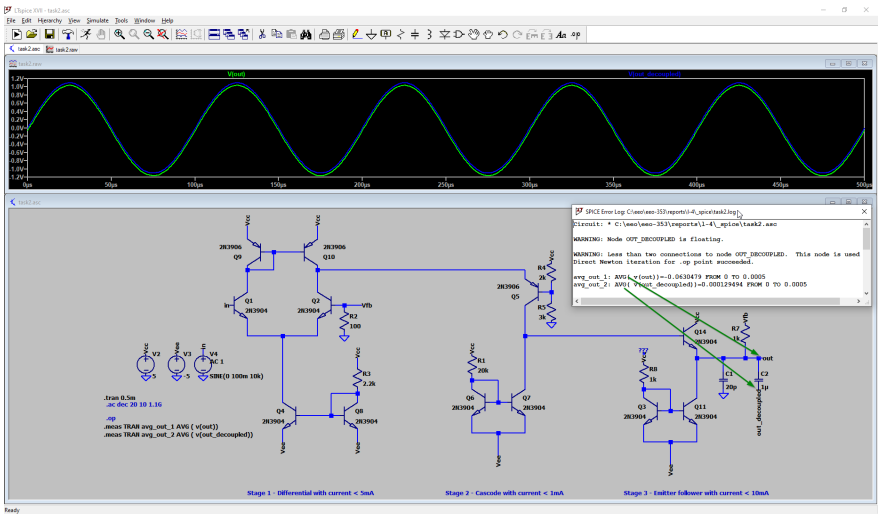

Figure 8: Transient Analysis showing the effect of a bypass capacitor to strip the DC component from the output signal

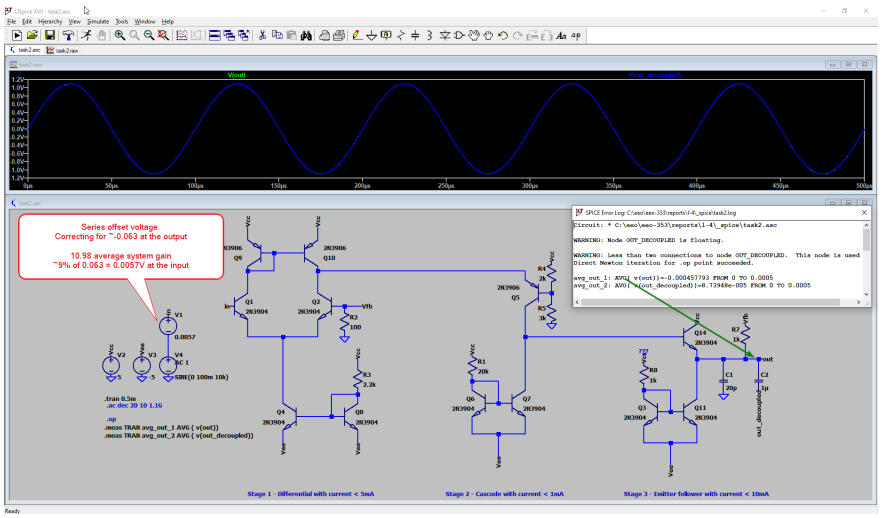

Figure 9: Alternative approach to compensating for the DC offset on the output signal. A gain-corrected series voltage.

The offset adjustment is needed to ensure that the amplifier operates at its desired DC operating point. By applying an offset to the sinusoidal input such that the average output is approximately 0V, we effectively bias the amplifier to its quiescent point. This biasing is essential for maintaining linearity, stability, and minimizing distortion in the amplifier circuit. Without proper biasing, the amplifier may exhibit distortion and operate inefficiently. Therefore, adjusting the input offset is necessary to set the amplifier's DC operating point accurately and ensure specified performance.

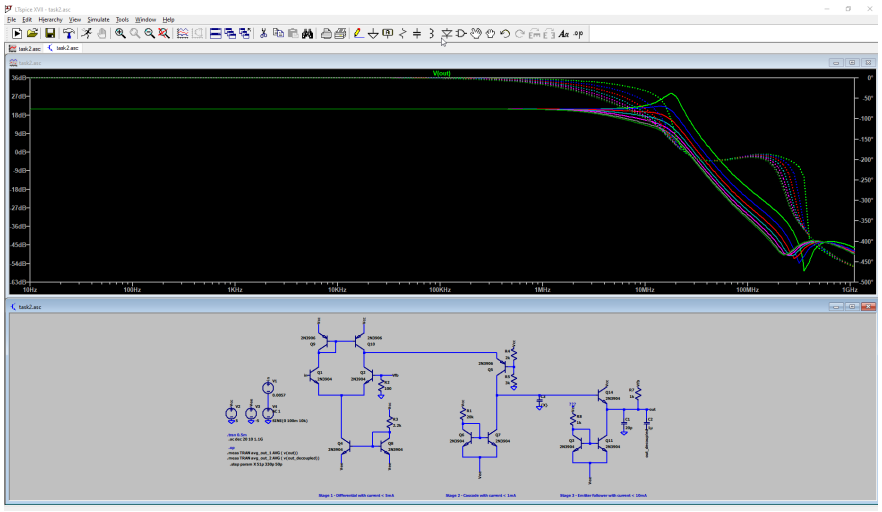

Figure 10: Sweeping the gain capacitor suggests a 150 pF would smooth out a bunp in the frequency response without overdamping the response.

A suggestion from professor led to the investigation above.

3 Build the circuit at (2) and experimentally reproduce the simulations

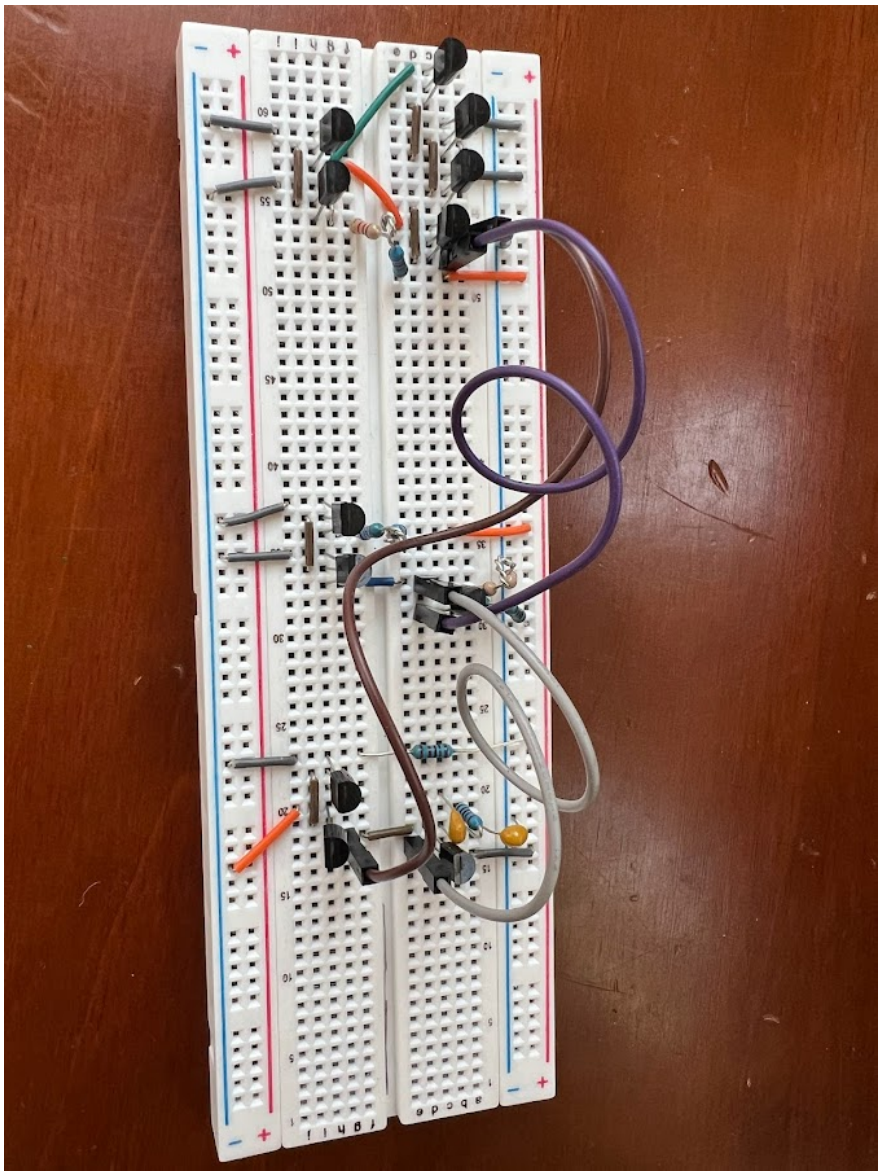

Figure 11: Circuit layout

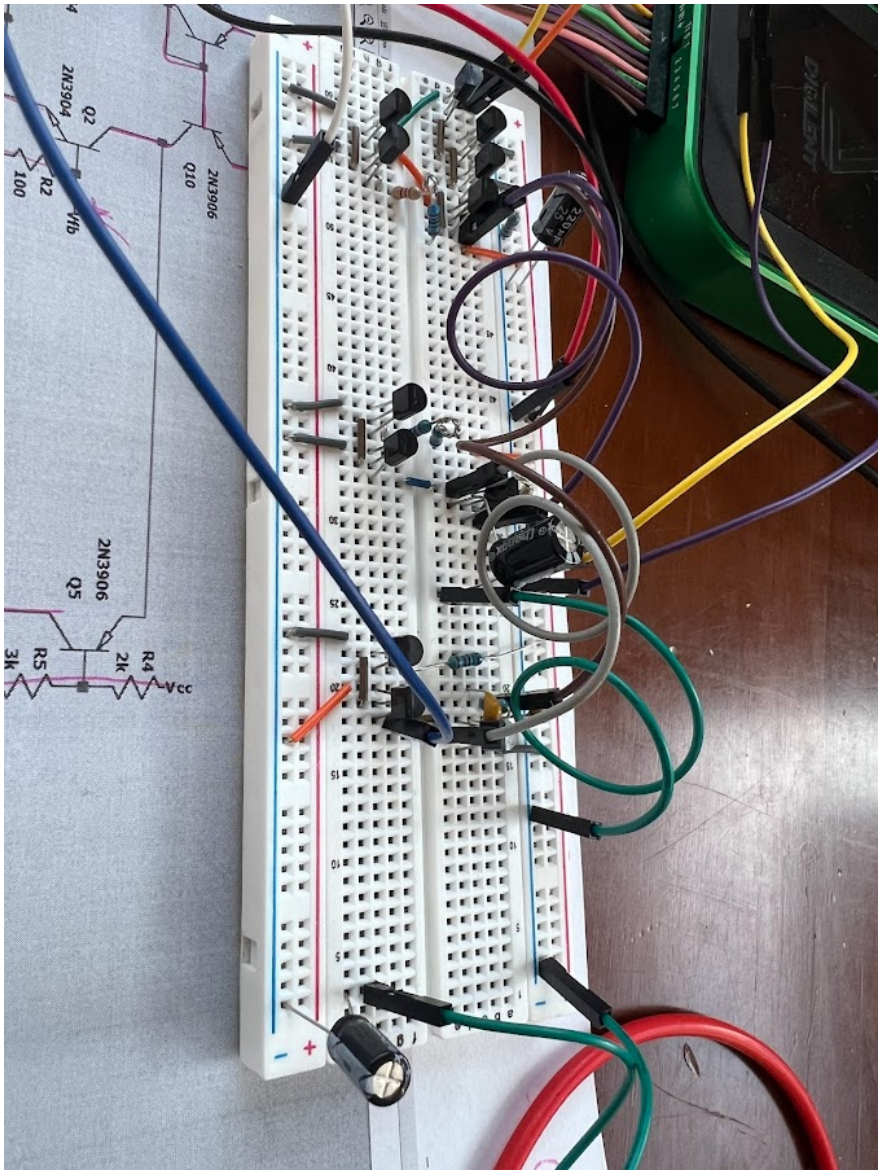

Figure 12: Adding filter caps as suggested in the instructions.

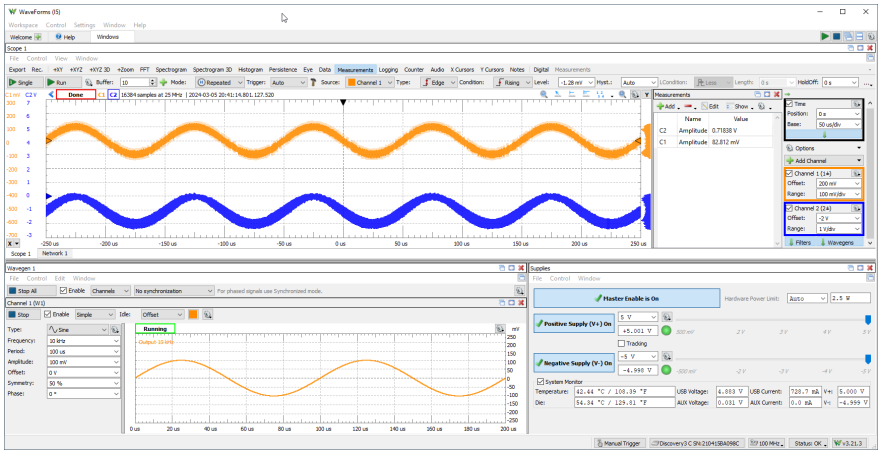

Figure 13: Oscilloscope measurements showing a system gain of about 10.

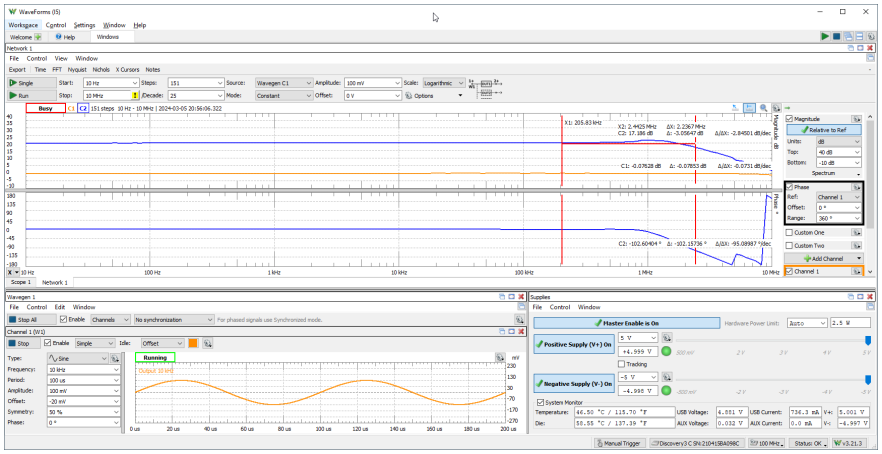

Figure 14: Network analysis showing the $-3\,\mathrm{dB}$.

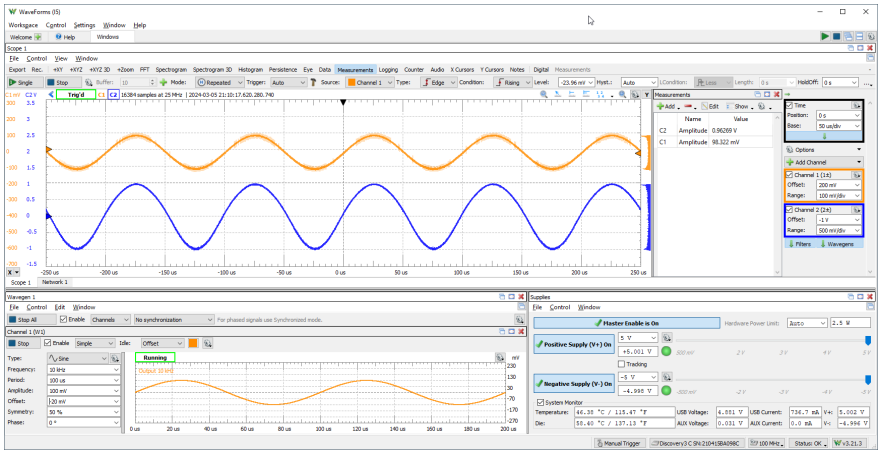

Figure 15: Compensating for the DC offset on the output signal.A DC offset to the input signal.

4 Suggest ways to improve beyond specifications the performance of the amplifier at (1)

Improving the physical layout and assembly of the circuit onto a printed circuit board (PCB) can have significant benefits. By carefully designing the layout, we can enhance noise immunity, reduce parasitic capacitances, and minimize crosstalk between different circuit components. Incorporating a ground plane into the PCB design further aids in minimizing signal interference and improving overall signal integrity.

Furthermore, employing shielded input wiring with the shield connected to ground at one end helps to effectively reduce noise within the system, ensuring cleaner signal transmission. Equally important is the implementation of proper power supply regulation to maintain stable operating conditions.

In addition to layout considerations, selecting higher precision passive components with superior thermal characteristics can greatly enhance the stability and accuracy of the circuit. Utilizing matched BJT pairs also contributes to temperature stability, ensuring consistent circuit performance across varying environmental conditions.

Finally, employing optimization techniques such as sweep parameters or Monte Carlo simulations as well as worst-case-analysis during component selection enables fine-tuning of values for noise reduction and performance optimization within each amplifier stage.