EEO352 Lab 7
Field Effect Transistors (FETs)

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November 15, 2023

Copy of Original Assignment

EEO 352 Fall 2023 - Assignment 7 – Field Effect Transistors (FETs) - ABET

Please document each step with snapshots of the built circuit, plots, pictures and your observations. Please include this page.

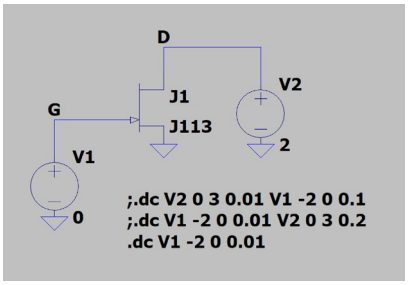

Fig.1

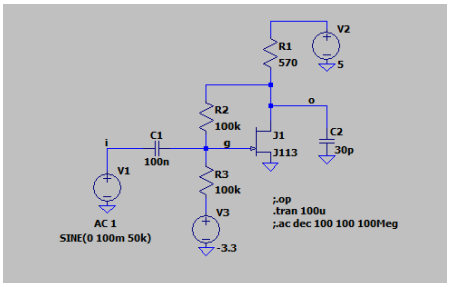

Fig.2

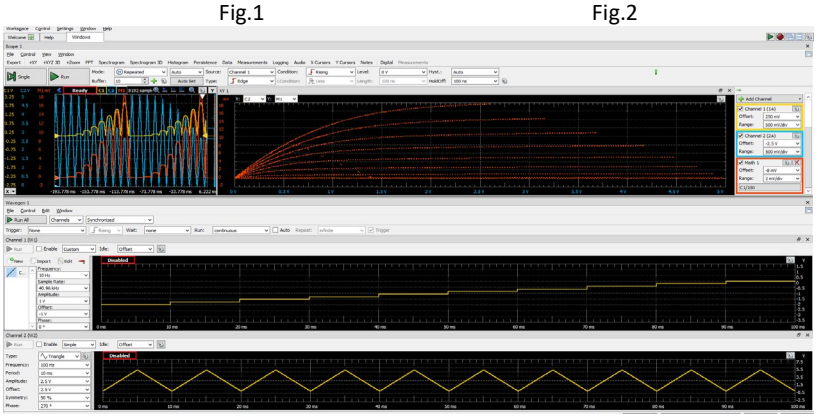

Fig.3

1) Using the n-channel JFET J113 (pick from njf) as in Fig1 simulate and plot the following (**25pts**):

a) Drain current Id vs Vds (range 0V to 3V) with parametric Vgs (-2V to 0V in 100mV steps)

a) Drain current Id vs Vgs (range -2V to 0V) with parametric Vds (0V to 3V in 200mV steps)

c) Drain current Id vs Vgs (range -2V to 0V) at Vds=2V, and extrapolate the Vgs at Id=5mA

d) Derivative (d(.)) of the drain current Id vs Vgs (range -2V to 0V) at Vds=2V, and extrapolate the transconductance at Id=5mA

Note1: the 30pF capacitor emulates the oscilloscope capacitive load (i.e. not required in experimental)

2) Using the n-channel JFET J113, one 570Ω resistor at the drain, and one 100kΩ and one 47kΩ to bias the gate, design the amplifier in Fig.2 and simulate and plot the following (**25pts**):

a) Simulate the response to 50kHz 100mV sinusoidal signal (plot in separate panes) and extrapolate gain

b) Frequency response, extrapolating the gain and -3dB bandwidth without and with the 30pF load

3) Using the n-channel JFET J113 and one 100Ω resistor at the drain, build and plot (**75pts**) *(ABET PI-71,PI-72,PI-73)*:

a) Drain current Id vs Vds (range 0V to 3V) with parametric Vgs (see example in Fig.3)

b) Drain current Id vs Vgs (range -2V to 0V) for Vds>2V, and extract the Vgs and the gm at Id=5mA

3) Explain how the tools operating on voltages allow measuring currents and plotting the desired curves

Hint1: search for "Semiconductor Curve Tracer With the Analog Discovery 2"

Hint2: for (b) use W1 Triangle Amp=1V, Off=-1V at Gate

4) Build and measure the amplifier in Fig.2 and plot the following (**75pts**):

a) Measure the response to 50kHz 100mV sinusoidal signal and extract gain

b) Frequency response, extracting the gain and the -3dB bandwidth

Summary

In this lab we simulated and built circuits around the J113 JFET. We measured properties of the device in spice simulation and in physical experiments. We also built an amplifier and analyzed the performance. For the most part the experiment closely tracked the results in the simulation. One place there was signifigant difference was in section 4. In the physical experiment vs the simulation, the gain was measured to be 3x less. Also, I was not able to operate the network analyzer up near 90 MHz as the simulation suggested would be necessary for measuring the -3 dB point. This looks to be a limitation of the Analog Discovery 3 hardware.

There were some small differences in the experiment vs the simulation when measuring $V_{gs}@I_d = 5\,\text{mA}$, however these are likely close enough to be considered part tolerance or setup deviation.

1 Circuit 1 Tasks

a)

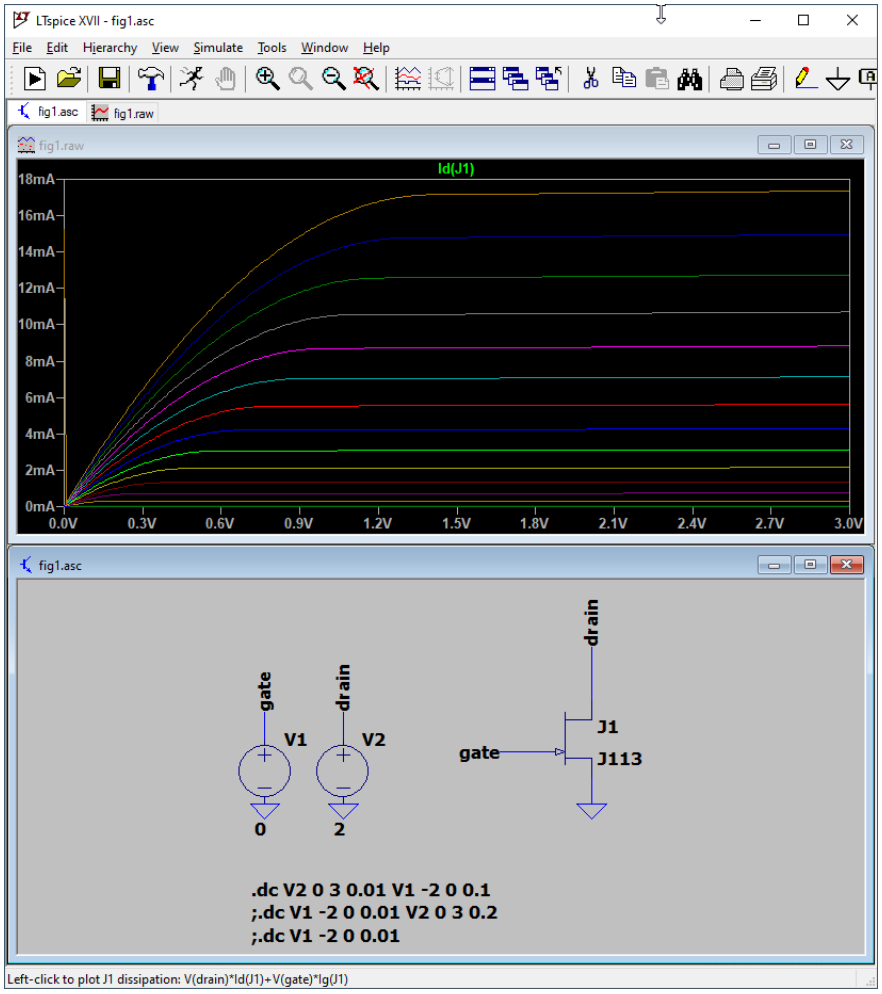

Figure 1: Drain current Id vs Vds (range 0V to 3V) with parametric Vgs (-2V to 0V in 100mV steps)

b)

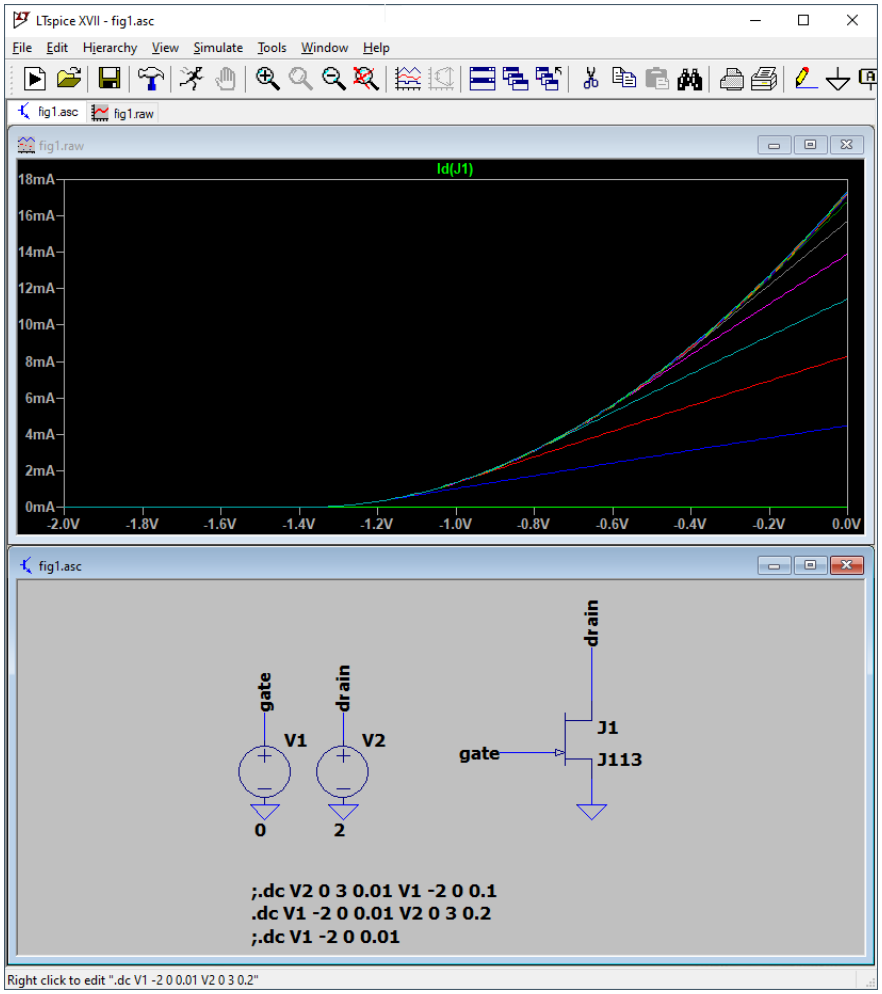

Figure 2: Drain current Id vs Vgs (range -2V to 0V) with parametric Vds (0V to 3V in 200mV steps)

c)

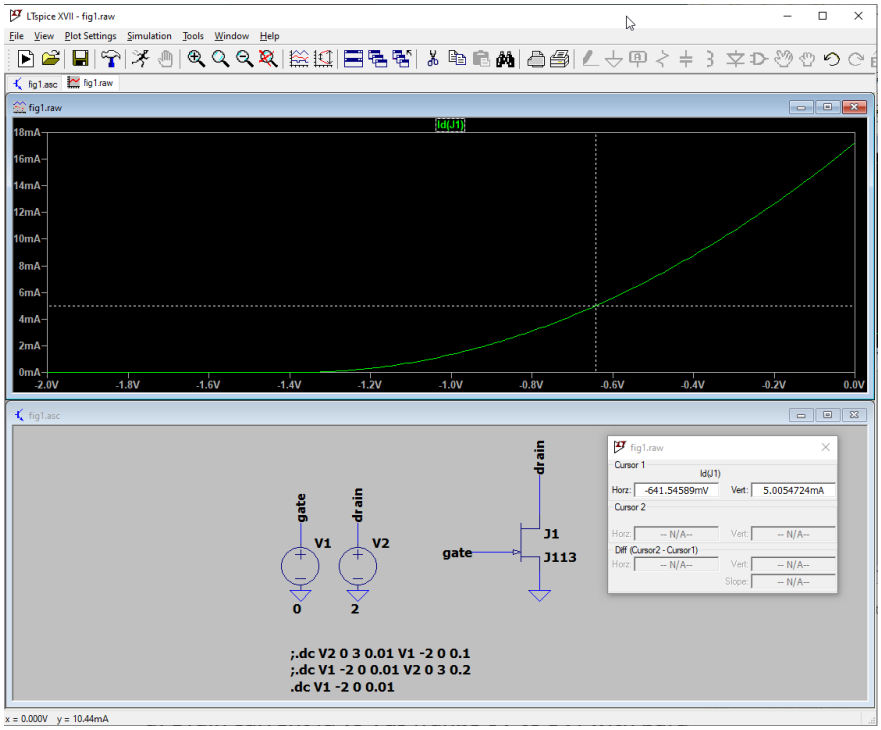

Figure 3: Drain current Id vs Vgs (range -2V to 0V) at Vds=2V, and extrapolate the Vgs at Id=5mA

V_{gs} @ $I_d = 5\,\text{mA}$ is $-641.55\,\text{mV}$.

d)

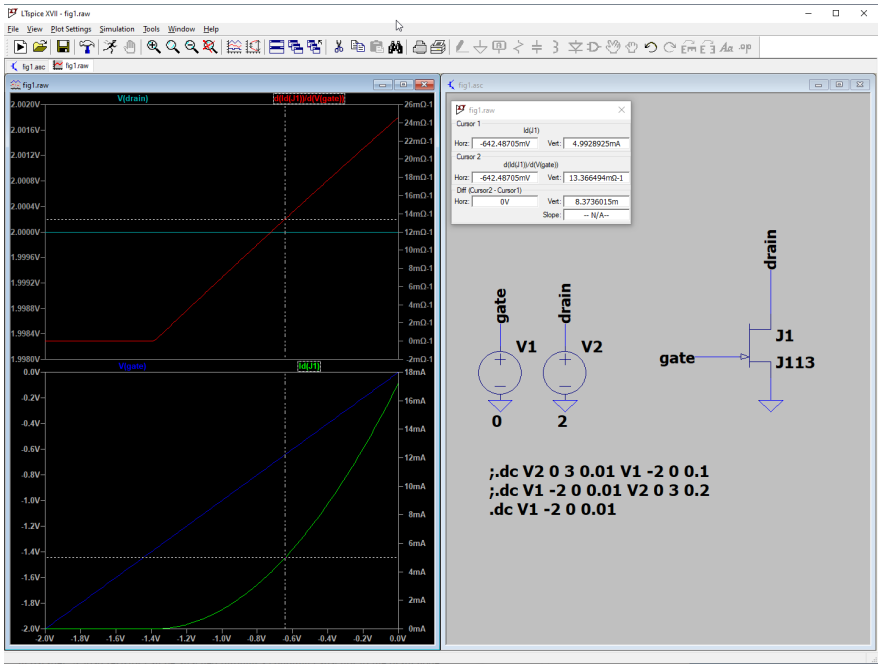

Figure 4: Derivative (d(.)) of the drain current Id vs Vgs (range -2V to 0V) at Vds=2V, and extrapolate the transconductance at Id=5mA

The transconductance g_m is found to be 13.366 mΩ @ Id = 5 mA

2 Circuit 2 Tasks

a)

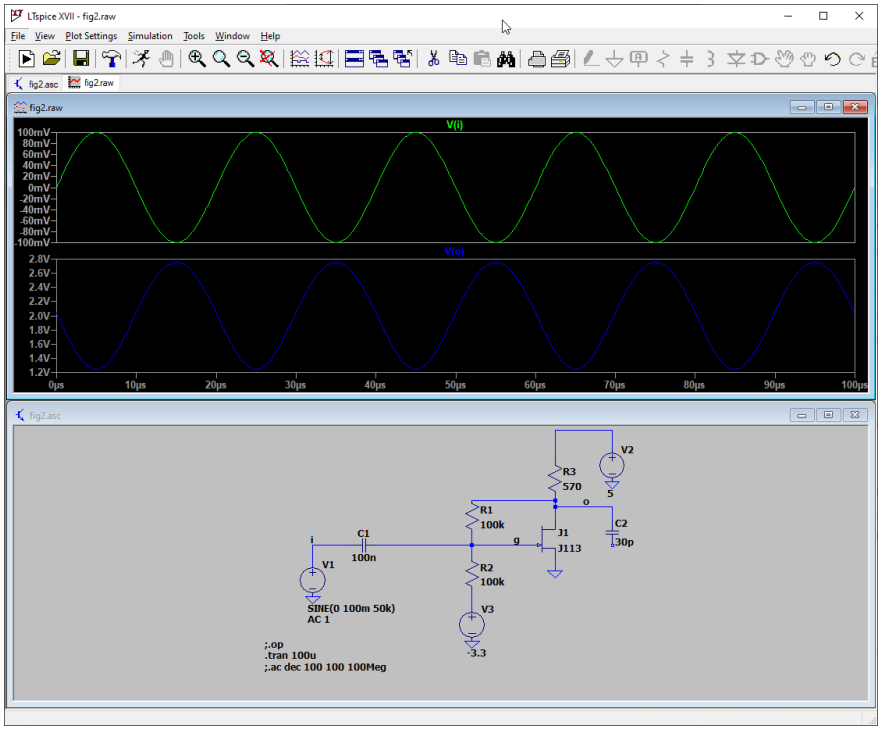

Figure 5: Simulate the response to 50kHz 100mV sinusoidal signal (plot in separate panes) and extrapolate gain

The input amplitude is 100 mV pp and output amplitude is 1.5 V pp, centered about 2.0 V, therefore the gain is 15.

b)

Frequency response, extrapolating the gain and -3dB bandwidth without and with the 30pF load

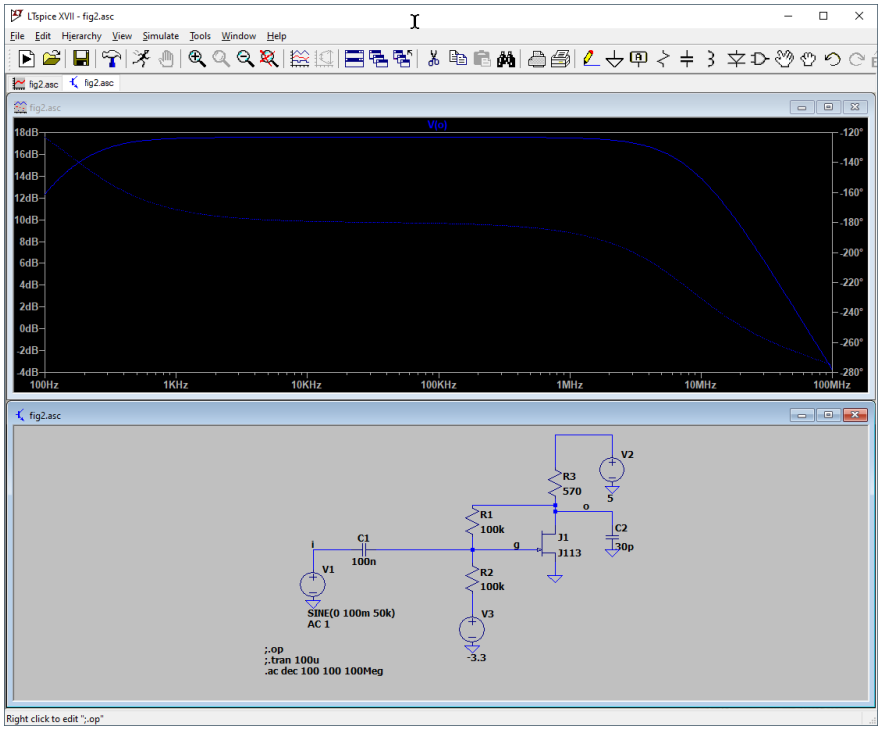

Figure 6: Frequency analysis overview

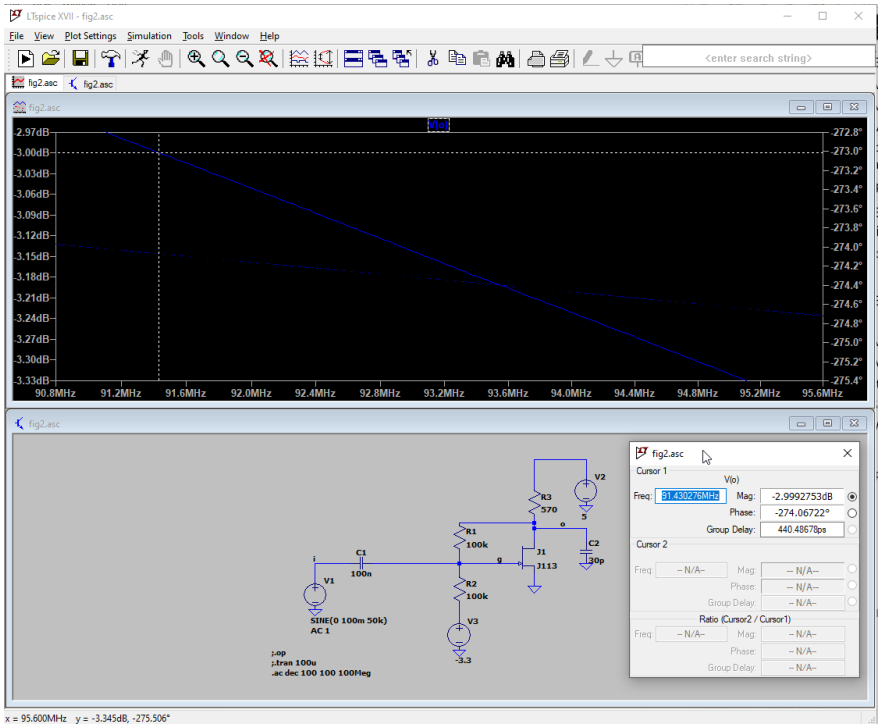

Figure 7: The $-3\,\mathrm{dB}$ point is found at $91.43\,\mathrm{MHz}$

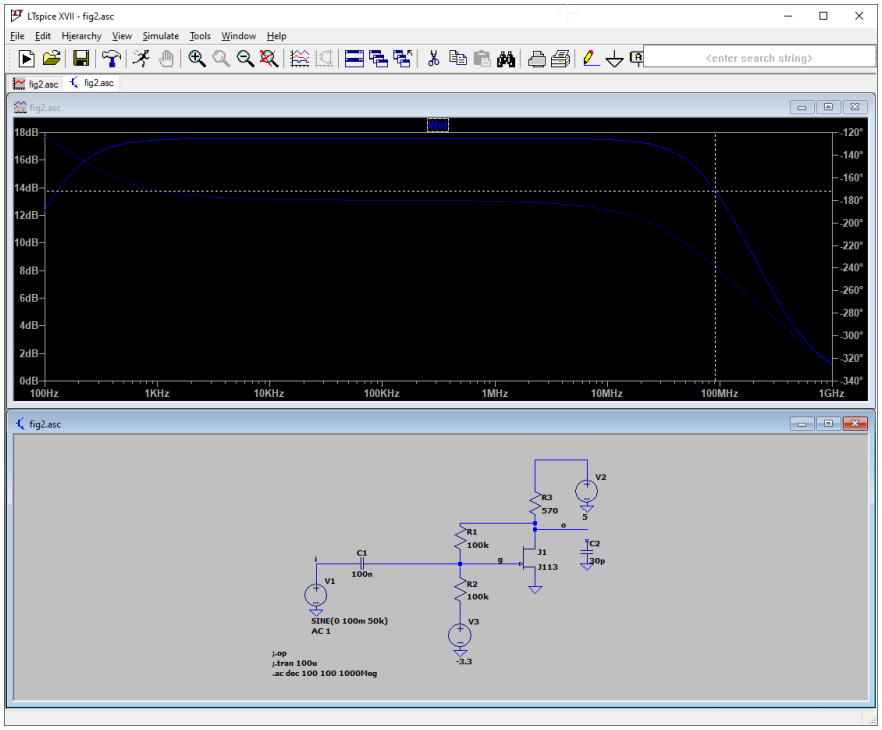

Figure 8: Without 30 pF output capacitance there is no −3 dB point.

3 Build and Measure

a)

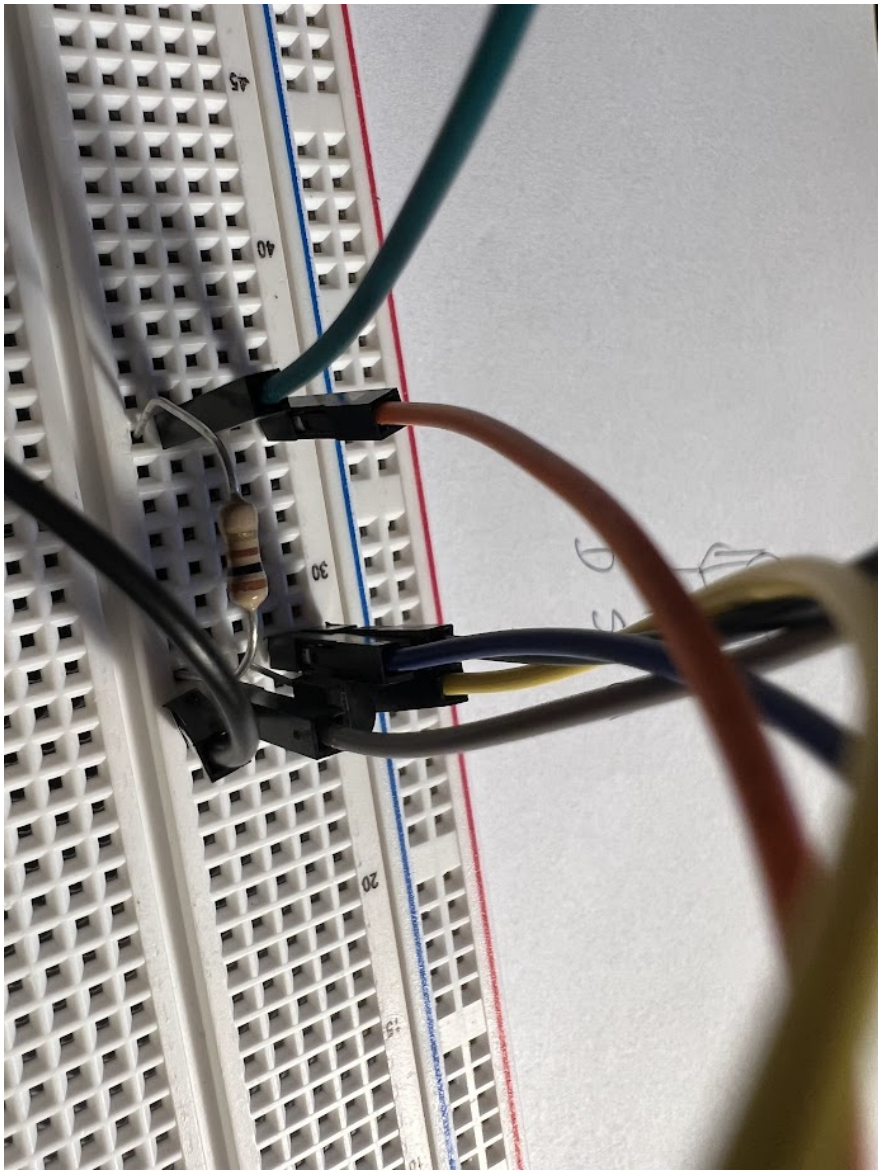

Figure 9: Test Setup

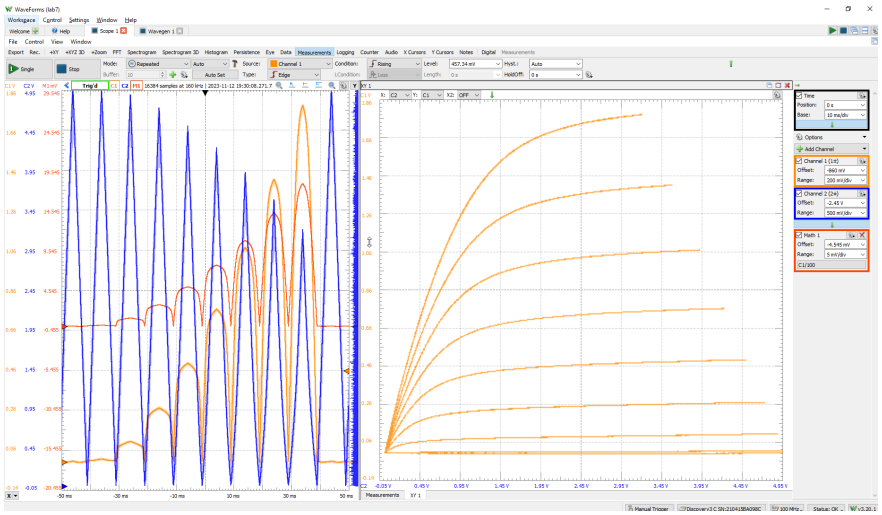

Figure 10: Drain current Id vs Vds (range 0V to 3V) with parametric Vgs (see example in Fig.3)

b)

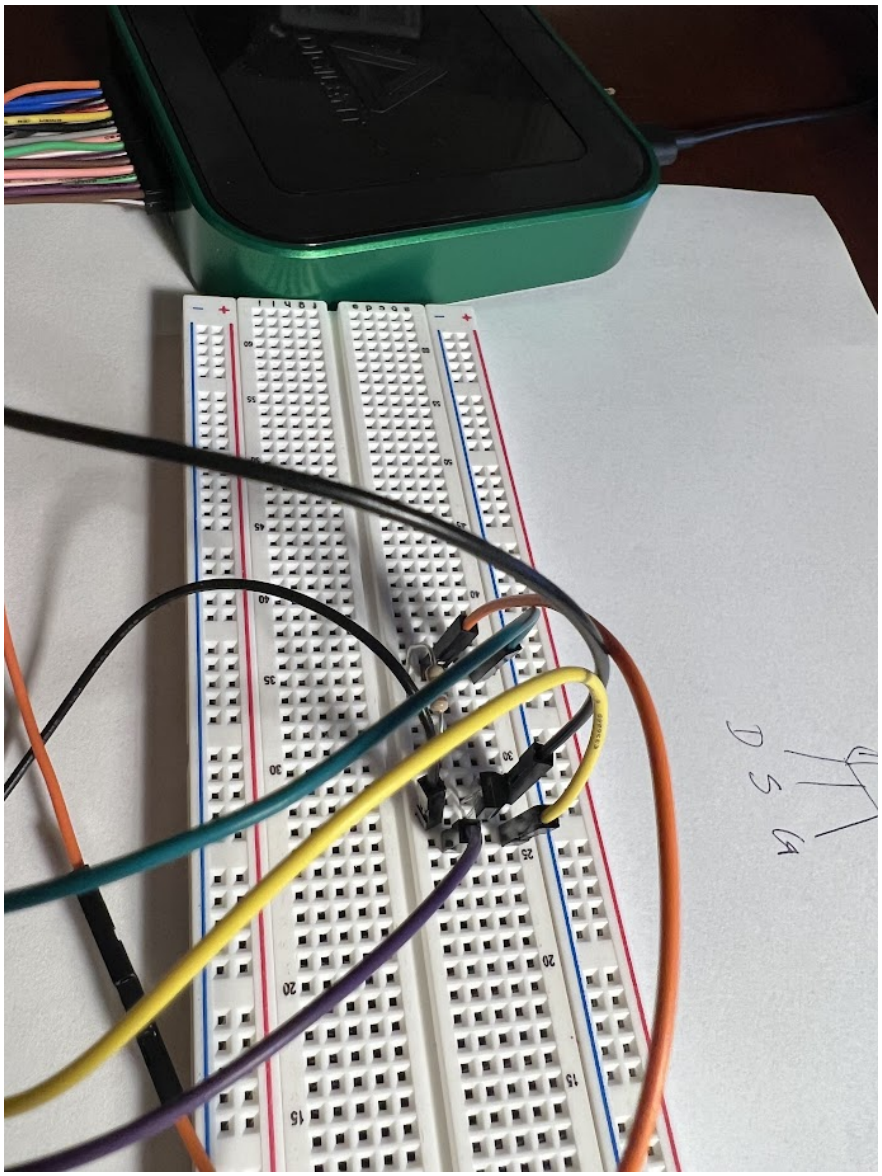

Figure 11: Test Setup

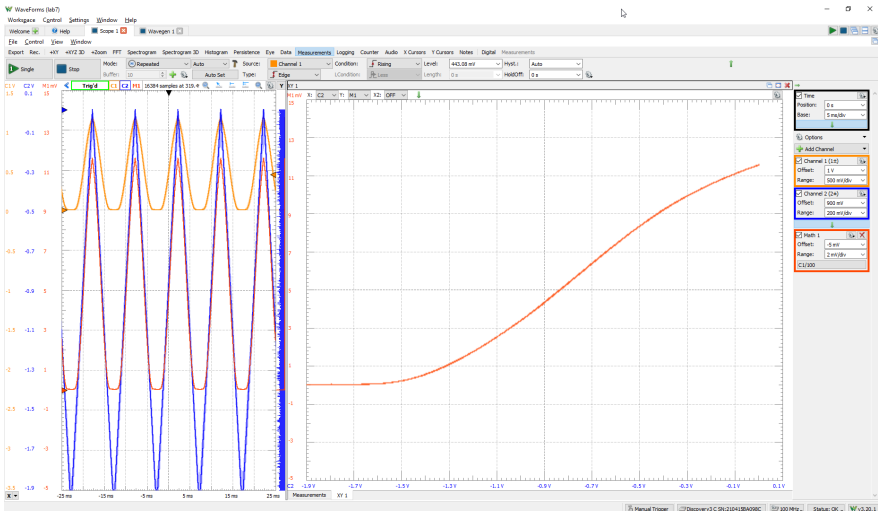

Figure 12: Drain current Id vs Vgs (range -2V to 0V) for Vds¿2V, and extract the Vgs and the gm at Id=5mA

- At $I_d = 5\,\text{mA}$, $V_{gs} \approx 850\,\text{mV}$

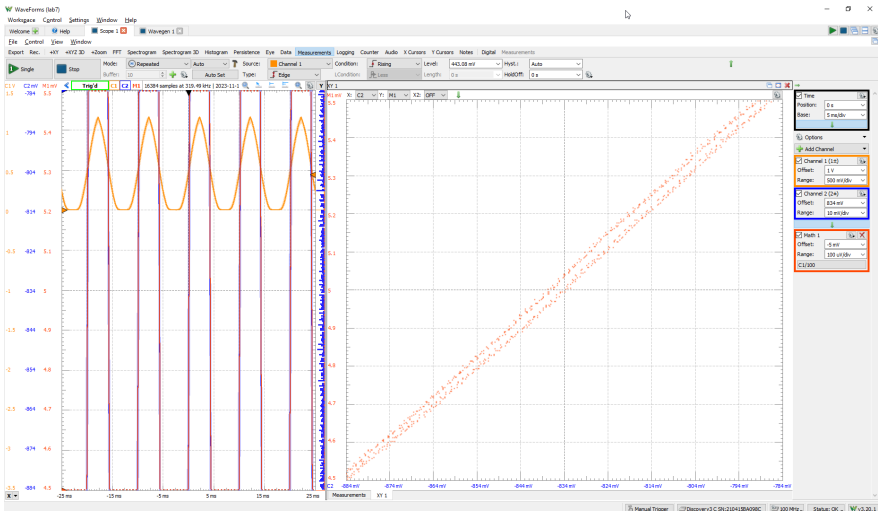

Figure 13: Zooming in to see $\Delta I_d = 0.2\,\text{mA}$ and $\Delta V_{gs} = 20\,\text{mV}$

- At $I_d = 5\,\text{mA}$, $gm \approx 10\,\text{m}\Omega$

3)

Explain how the tools operating on voltages allow measuring currents and plotting the desired curves.

A: We are able to plot currents by using a resistor in series with the current signal which allows us to read an analog voltage proportional to the current in the circuit. Using Ohm's law the actual current can be determined using the voltagemeasured and the known resistance of the resistor selected.

4)

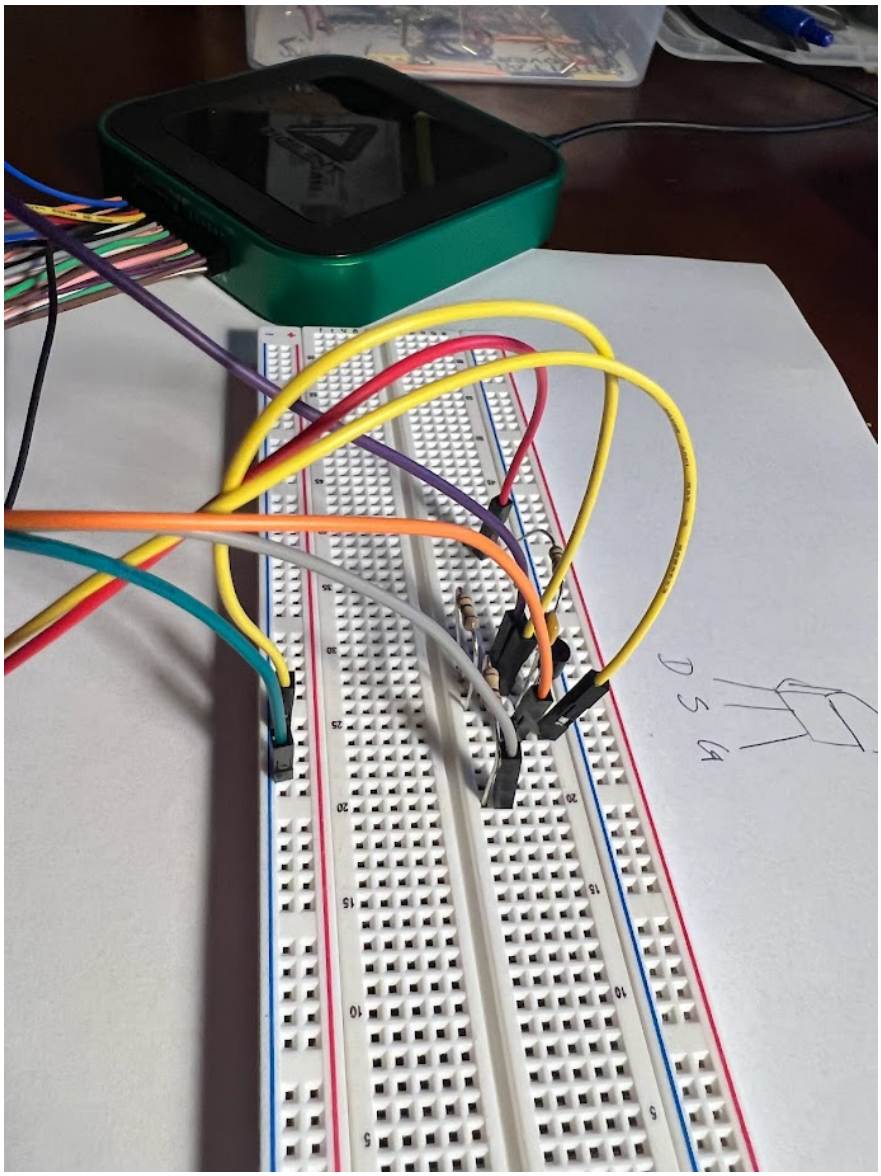

Figure 14: Test Setup

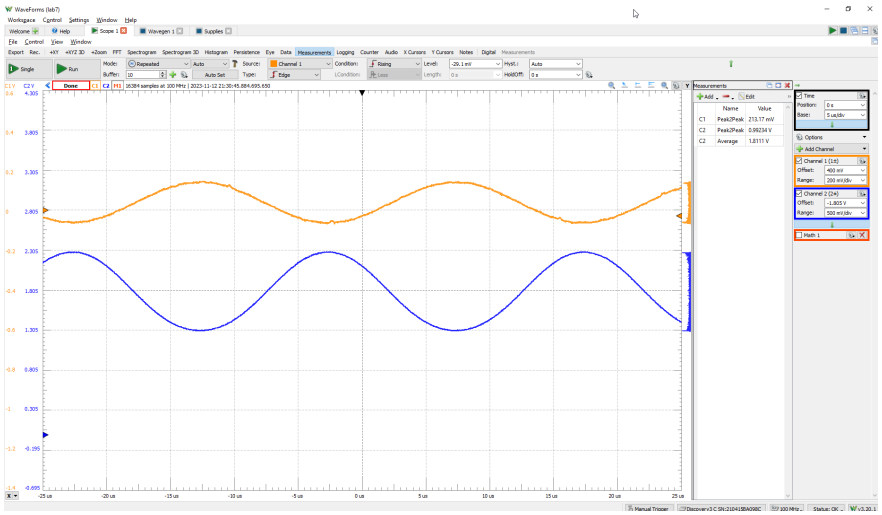

Figure 15: Measure the response to 50kHz 100mV sinusoidal signal and extract gain

The gain is calculated to be 4.65.

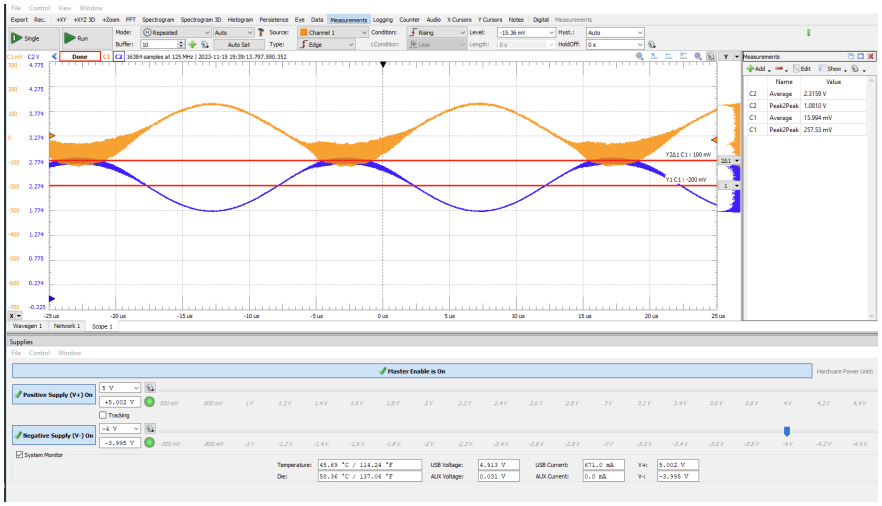

Figure 16: Based on feedback from the Professor I change V3 to $-3.5\,\mathrm{V}$, then the gain increased to 8.6. Lowering V3 further did not increase the gain, but seems to cause noise on the lower half of the input sine wave. The output amplitude was observed to be around $2.23\,\mathrm{V}$ max.

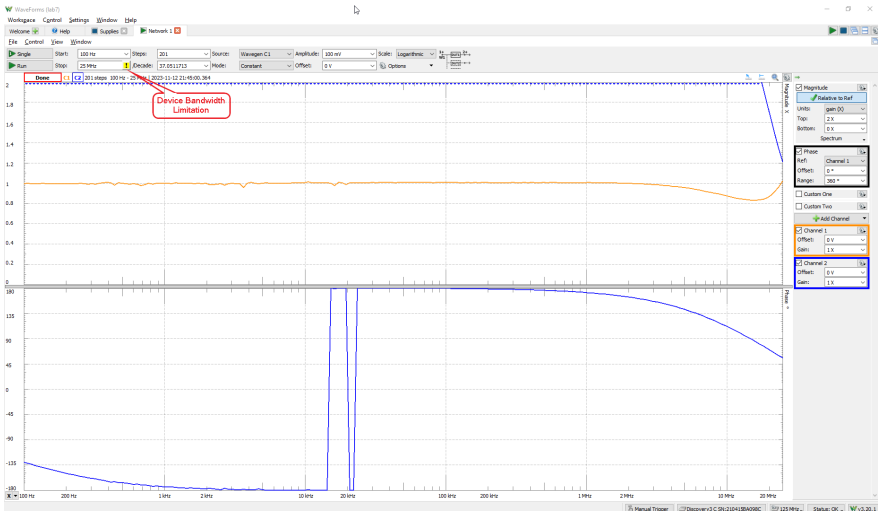

Figure 17: Frequency response, extracting the gain and the -3dB bandwidth

The Digilent Waveforms application indicated a bandwith limitation. It appears that the max bandwidth is less than 25 MHz. This is 4x lower that what the simulation shows the -3 dB point to be.