1 Overview

A controller to drive a 4 digits 7 segments display over SPI bus. The controller can set up the luminosity and shut-down the display.

The “PIC16F54 7 segments display”:

- 2 x LTD5250 2 Digits
- 1 x PIC16F54 Micro-Controller
- 1 x 74HC595 Shift Register
- 4 x 2N7002 Transistors

2 Features

- SPI bus
- Disable/Enable
- Dimming
- 4 characters

3 Schematic

The schematic[1] and the gerber[2] files

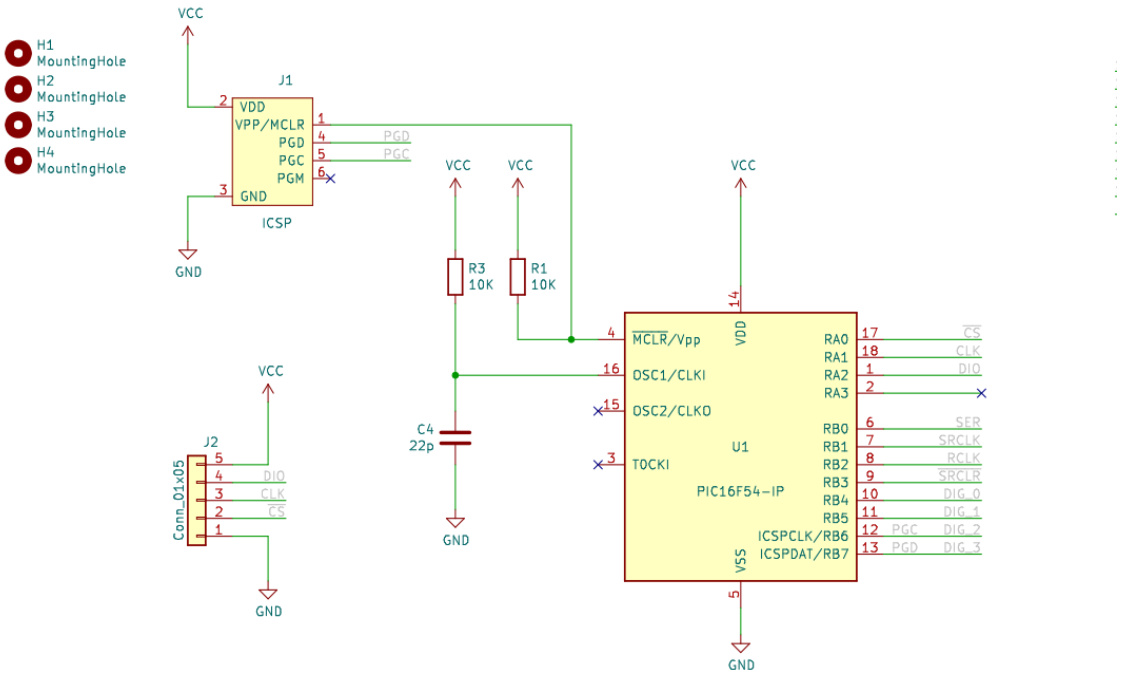

Figure 1: Schematic MCU

[1] documents/images/ltd5250-schematic.pdf
[2] documents/gerber.zip

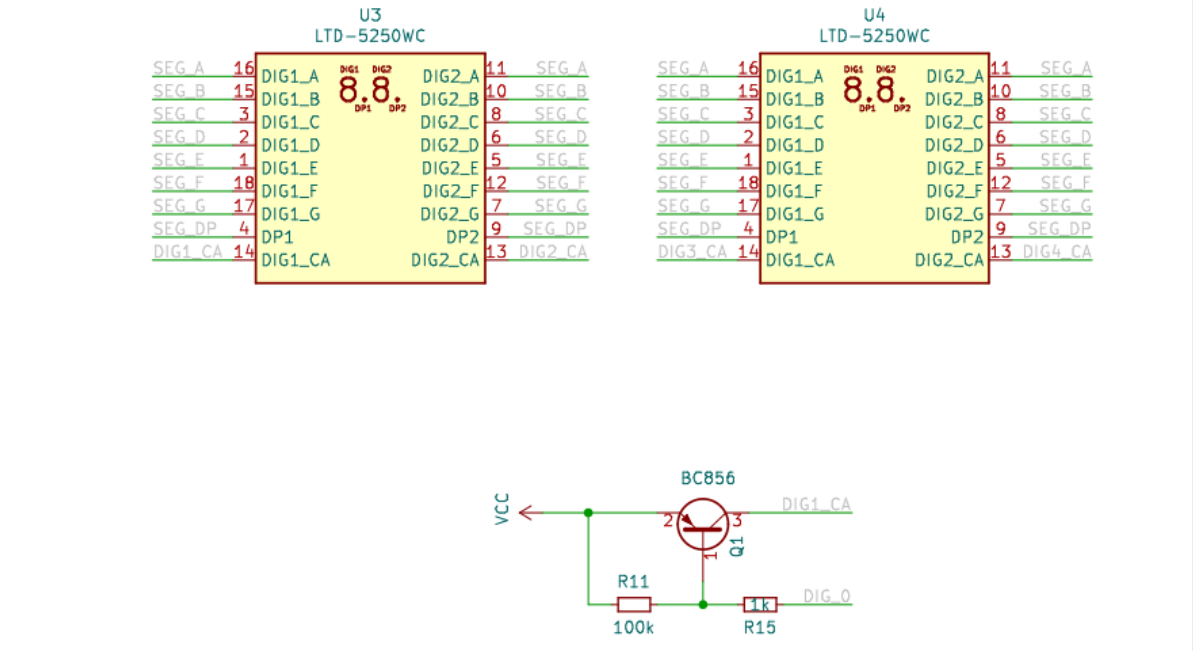

Figure 2: Schematic Seven-Segments

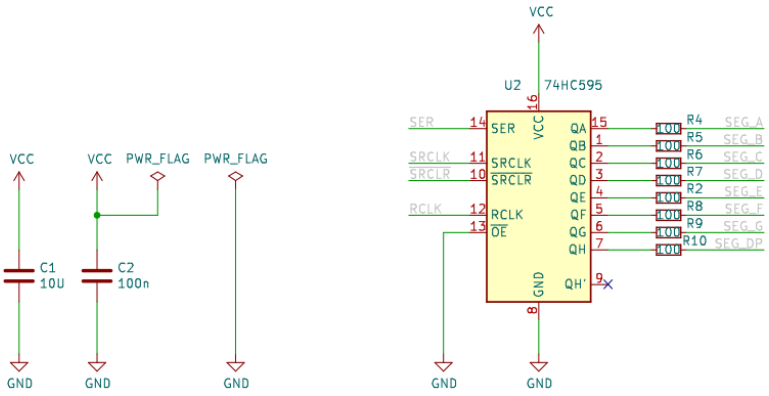

Figure 3: Schematic Programmer and Header

4 SPI Protocol

4.1 Byte Timing

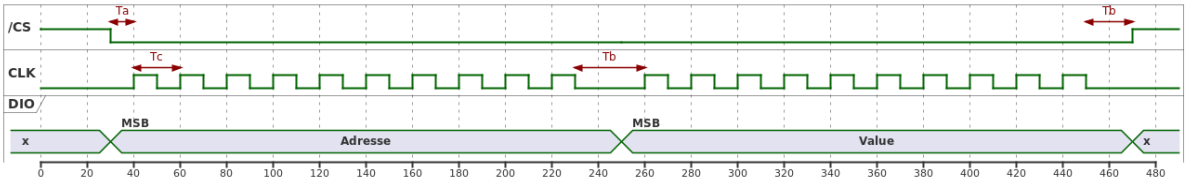

Figure 4: Master Write “0” Slot

Address: 1.Byte of the command, determines which register to be updated.
Value: 2.Byte of the command, the value to be updated.

Table 1: Bit Timing

Symbol	Description	Min	Typ	Max	Unit
Ta	Enable	144	450	360	us
Tb	Time to read	380	500	720	us
Tc	Time to new bit	144	1500	7500	us
Td	Time to new bit	144	1500	7500	us

Ta: Start of new bit
Tb: Time between start of EN and the remote sample the DIO
Tc: Time the remote spend wait for new Data, this should be bigger than the minimum allowed time for EN
Td: Time the remote spend wait for new Data, this should be bigger than the minimum allowed time for EN

4.2 Registers

Table 2: Driver Registers

Adresse	Description	Default
0x00	Option	0x0F
0x01	Digit 1	0x01
0x02	Digit 2	0x03
0x03	Digit 3	0x07

Adresse	Description	Default
0x04	Digit 4	0x0F

4.2.1 Option Register Bit Assignement

This register acts as setting register.

Table 3: Option Register

Option	7	6	5	4	3	2	1	0
Description	SLEEP	EN	EN	DIM4	DIM3	DIM2	DIM1	DIM0
Default	0	0	0	0	1	1	1	1

DIM<4-0>: Dimmer, '0b0000' is full power and '0b1111' is dark.

EN: Writing '1' to this position will power off the segments. All segments are off, but the controller is still running.

SLEEP: The controller go in sleep. Can only be restart push the MCLR pin down. All registers will be reset to theirs default value.

4.2.2 Digit x Register Bit Assignement

Registers describing the segments that should light on. Writing '1' to a position will light on this segments.

Table 4: Digit Register Bit Assignement

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DP	G	F	E	D	C	B	A

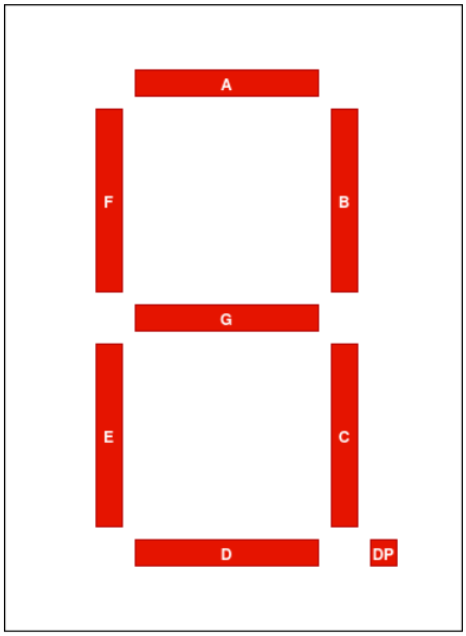

Figure 5: Seven Segments

5 Firmware

5.1 Shift Register State-Machine

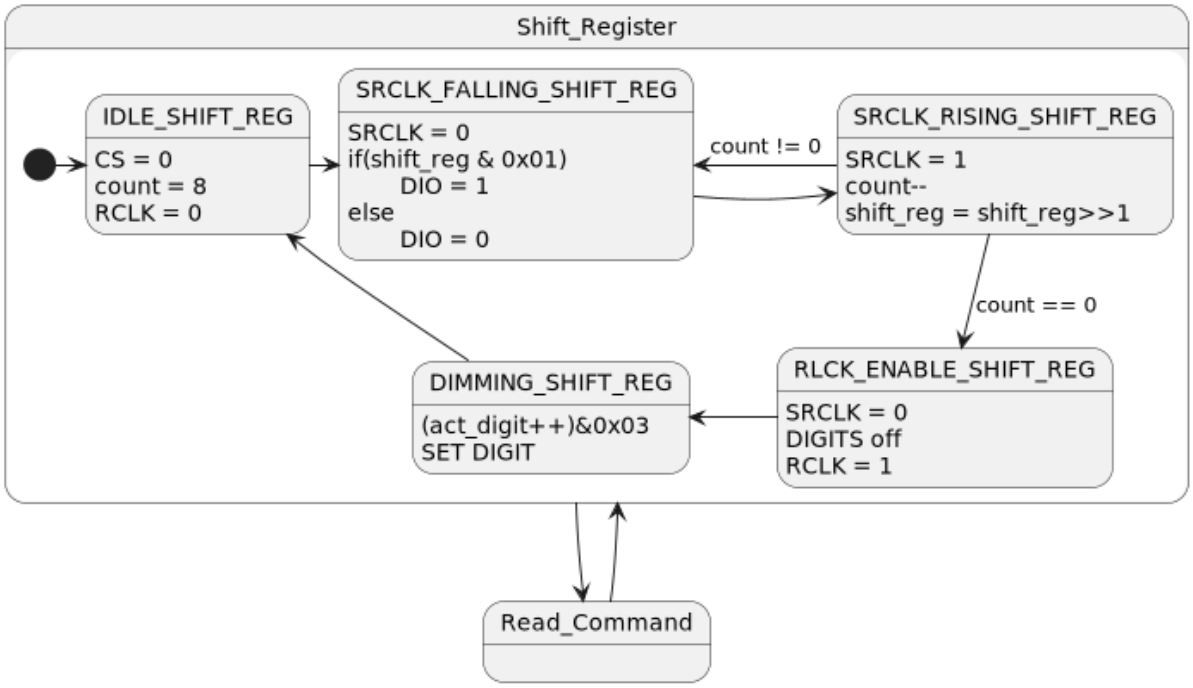

Figure 6: Shift Register State-Machine

5.2 Read Command State-Machine

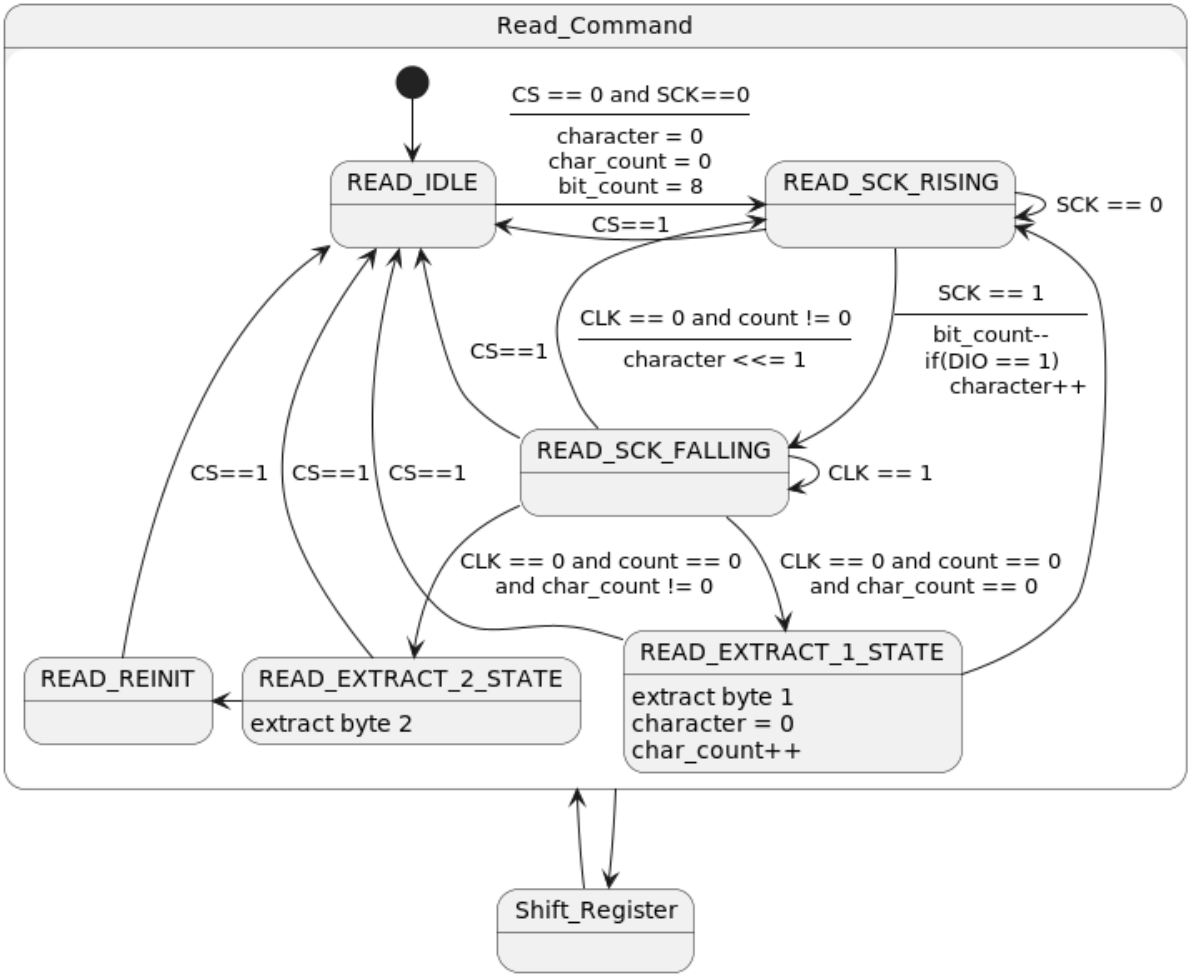

Figure 7: Read Command State-Machine