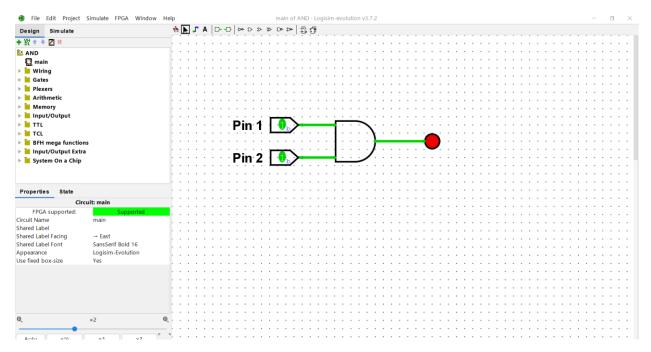
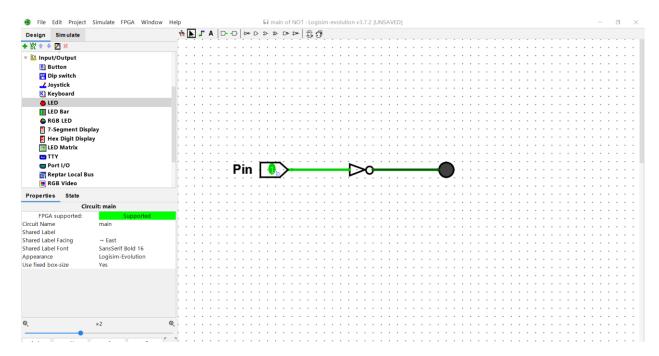
I - AND



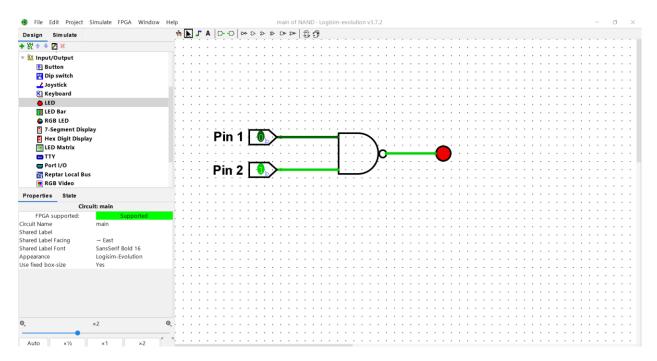
Pin 1	Pin 2 Output	
0	0	0
0	1	0
1	0	0
1	1	1

II - NOT



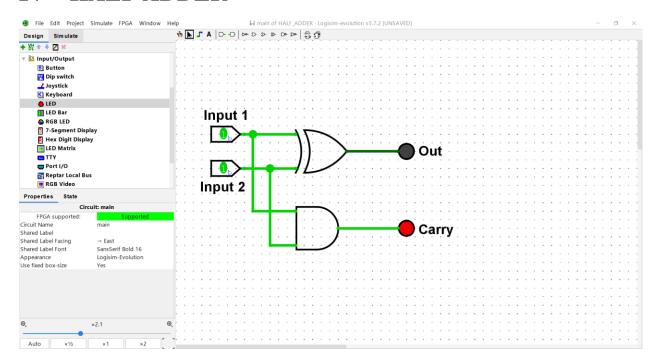
Pin	Output
0	1
1	0

III - NAND



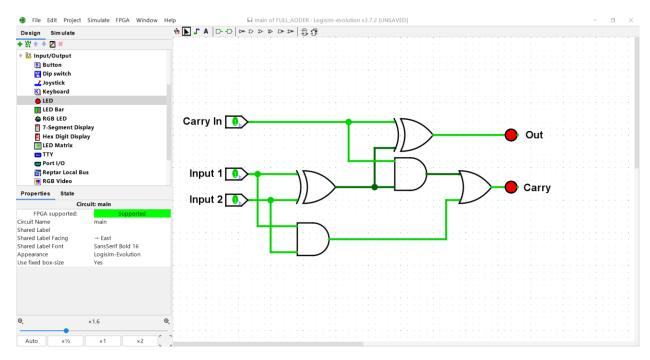
Pin 1	Pin 2	Output	
0	0	1	
0	1	1	
1	0	1	
1	1	0	

IV - HALF ADDER



Input 1	Input 2	Output	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

V – FULL ADDER



Input 1	Input 2	Carry In	Sum Output	Carry Output
0	0	0	0	0
0	0	1	1	0
1	0	0	1	0
1	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	1	0	0	1
1	1	1	1	1