实验八 加减可控计数器及其应用

1．使用 Quartus Prime 软件设计加减可控十进制计数器。

控制信号主要有：

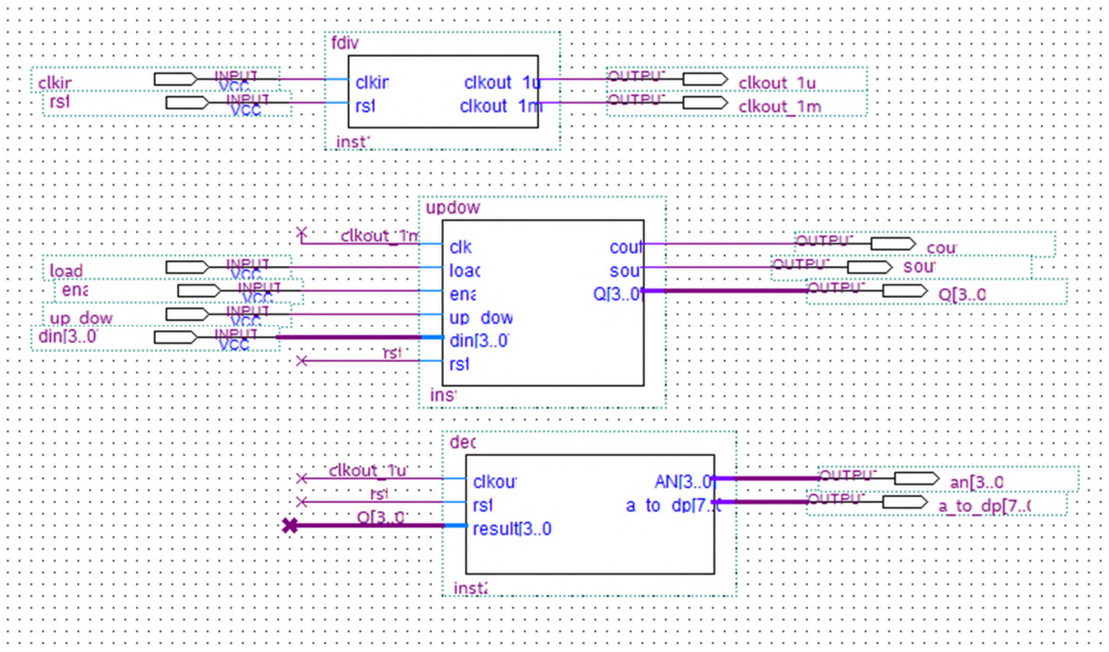
（1）复位信号 rst：异步复位，高电平清零；

（2）数据加载信号 load：同步加载，低电平加载数据；

（3）使能信号 ena：同步使能，高电平使能；

（4）加减可控信号 updown:同步加减可控，高电平递增计数，低电平递减计数。

1. 顶层文件



2. 计数器模块代码

```
module updown(clk,load,ena,cout,sout,up_down,Q,din,rst);
input load,ena,clk,rst,up_down;
input [3:0] din;
wire load,rst,up_down;
output  cout,sout;
output reg [3:0] Q;



always @(posedge clk or posedge rst )
if (rst==1)//异步清零，高电平清零
     Q<=0;
else
begin
   if (!load)//同步预置，低电平加载数据
       Q<=din;
```

```
    else
      begin
        if (ena)//同步使能，高电平使能
          begin
            if (up_down==1&&Q==9)
              Q<=0;
            else if (up_down==0&&Q==0)
              Q<=9;
            else//同步加减可控，高电平递增计数，低电平递减计数。
             begin
              if (up_down==1) //加计数
                 Q<=Q+1;
               else           //减计数
                Q<=Q-1;
             end
          end
        else
          Q<=Q;
         end
end

 assign cout=((rst==0)&&(up_down==1)&&(load==1)&&(ena==1)&&(Q==9)) ? 1:0;
 assign sout=((rst==0)&&(up_down==0)&&(load==1)&&(ena==1)&&(Q==0)) ? 1:0;
endmodule
```

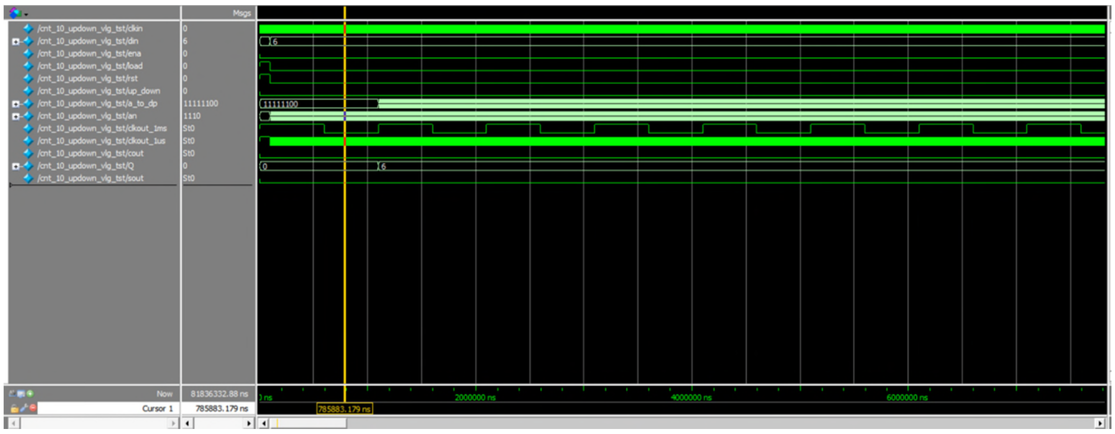
3. 测试文件代码

```
`timescale 1 ns/ 1 ps
module cnt_10_updown_vlg_tst();
// constants
// general purpose registers
//reg eachvec;
// test vector input registers
reg clkin;
reg [3:0] din;
reg ena;
reg load;
reg rst;
reg up_down;
// wires
wire [7:0]  a_to_dp;
wire [3:0]  an;
wire clkout_1ms;
wire clkout_1us;
wire cout;
wire [3:0]  Q;
wire sout;

// assign statements (if any)
cnt_10_updown i1 (
// port map - connection between master ports and signals/registers
    .a_to_dp(a_to_dp),
    .an(an),
    .clkin(clkin),
    .clkout_1ms(clkout_1ms),
    .clkout_1us(clkout_1us),
    .cout(cout),
    .din(din),
    .ena(ena),
    .load(load),
    .Q(Q),
    .rst(rst),
    .sout(sout),
    .up_down(up_down)
);
initial
begin
// code that executes only once
// insert code here --> begin
clkin=0;
rst=1;
ena=0;
load=1;
up_down=0;
din=0;
#100000
rst=0;
load=0;
din=6;
#10000000
ena=1;
load=1;
#10000000
up_down=1;
#100000
up_down=0;
#10000000
up_down=1;
```

```
// --> end
$display("Running testbench");
end
always
// optional sensitivity list
// @(event1 or event2 or .... eventn)
begin
// code executes for every event on sensitivity list
// insert code here --> begin
  #10 clkin=~clkin;
//@eachvec;
// --> end
end
endmodule
```

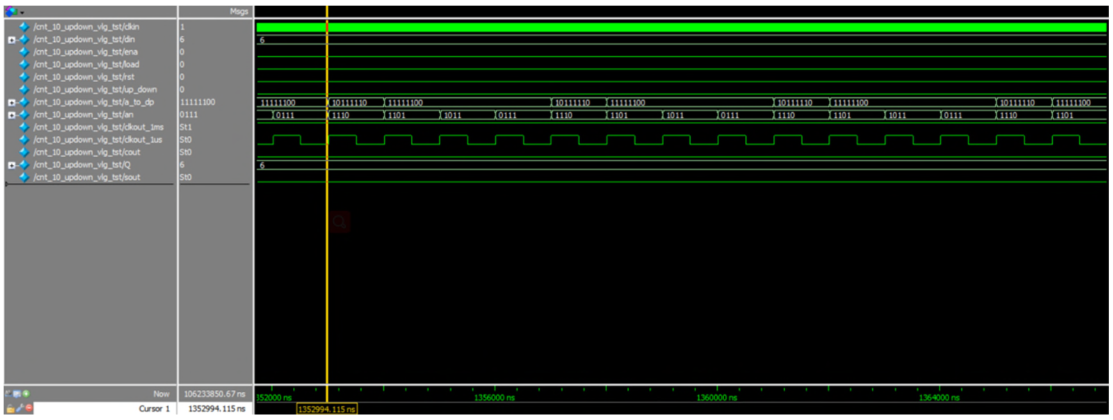
4.　仿真波形：

复位有效时 rst=1;



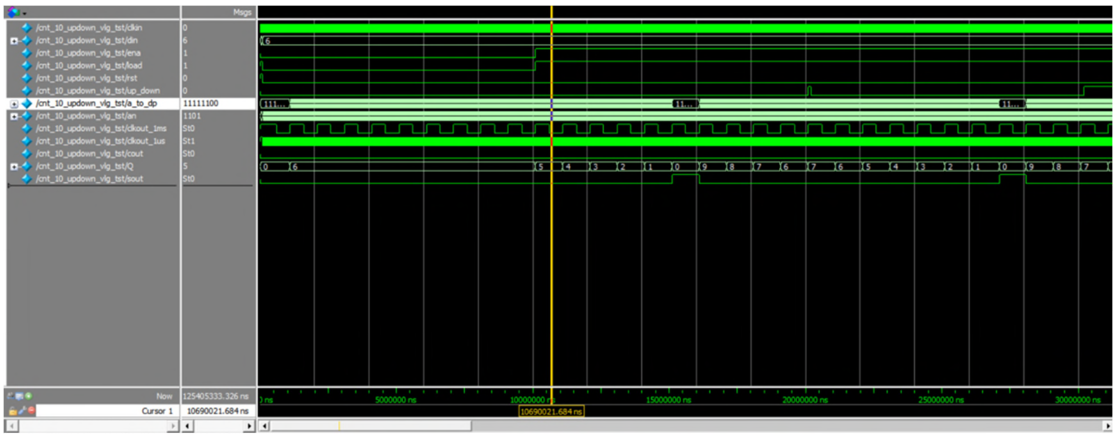
Msgs
/cnt_10_updown_vlg_tst/clkin 0
/cnt_10_updown_vlg_tst/din 6
/cnt_10_updown_vlg_tst/ena 0
/cnt_10_updown_vlg_tst/load 0
/cnt_10_updown_vlg_tst/rst 0
/cnt_10_updown_vlg_tst/up_down 0
/cnt_10_updown_vlg_tst/a_to_dp 11111100
/cnt_10_updown_vlg_tst/an 1110
/cnt_10_updown_vlg_tst/clkout_1ms St0
/cnt_10_updown_vlg_tst/clkout_1us St0
/cnt_10_updown_vlg_tst/cout St0
/cnt_10_updown_vlg_tst/Q 0
/cnt_10_updown_vlg_tst/sout St0
Now 81836332.88 ns
Cursor 1 785883.179 ns
2000000 ns
4000000 ns
6000000 ns

数据加载有效时 rst=0;load=0;din=6;



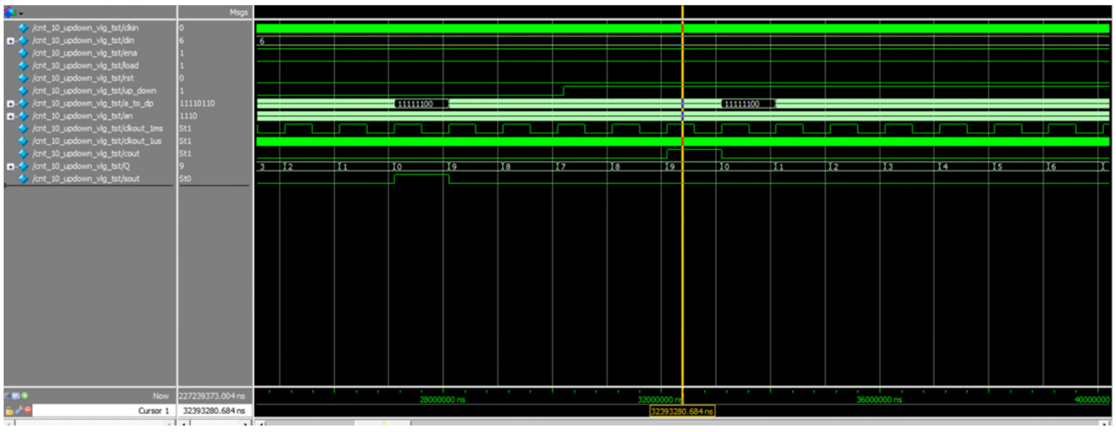
Msgs
/cnt_10_updown_vlg_tst/clkin 1
/cnt_10_updown_vlg_tst/din 6
/cnt_10_updown_vlg_tst/ena 0
/cnt_10_updown_vlg_tst/load 0
/cnt_10_updown_vlg_tst/rst 0
/cnt_10_updown_vlg_tst/up_down 0
/cnt_10_updown_vlg_tst/a_to_dp 11111100
/cnt_10_updown_vlg_tst/an 0111
/cnt_10_updown_vlg_tst/clkout_1ms St1
/cnt_10_updown_vlg_tst/clkout_1us St0
/cnt_10_updown_vlg_tst/cout St0
/cnt_10_updown_vlg_tst/Q 6
/cnt_10_updown_vlg_tst/sout St0
Now 106233850.67 ns
Cursor 1 1352994.115 ns
1356000 ns
1360000 ns
1364000 ns

使能有效时 rst=0;load=1;ena=1;

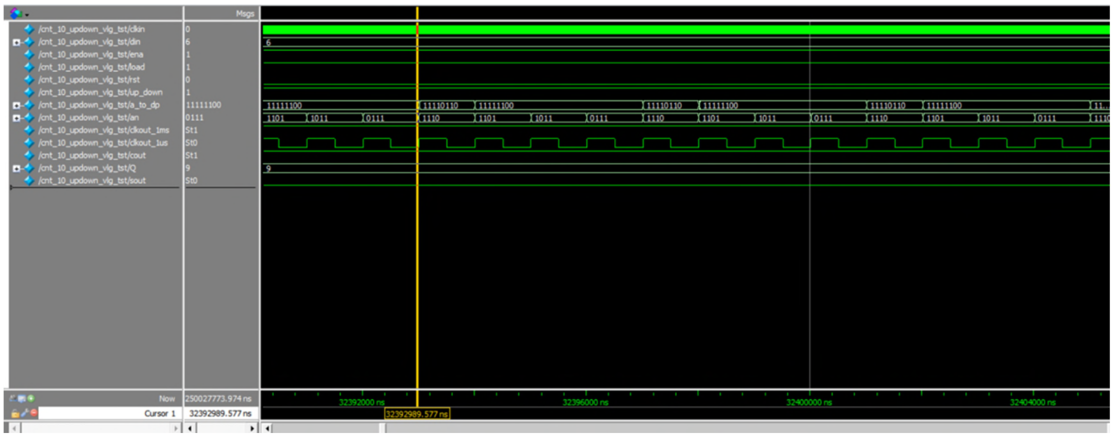


```
/cnt_10_updown_vlg_tst/clkin        0
/cnt_10_updown_vlg_tst/din          6
/cnt_10_updown_vlg_tst/ena          1
/cnt_10_updown_vlg_tst/load         1
/cnt_10_updown_vlg_tst/rst          0
/cnt_10_updown_vlg_tst/up_down      0
/cnt_10_updown_vlg_tst/a_to_dp      11111100
/cnt_10_updown_vlg_tst/an           1101
/cnt_10_updown_vlg_tst/clkout_1ms   St0
/cnt_10_updown_vlg_tst/clkout_1us   St1
/cnt_10_updown_vlg_tst/cout         St0
/cnt_10_updown_vlg_tst/Q            5
/cnt_10_updown_vlg_tst/sout         St0
Now        125405333.326 ns
Cursor 1   10690021.684 ns
```

递增计数 cout 为 1 时 rst==0, up_down==1, load==1, ena==1, Q=9

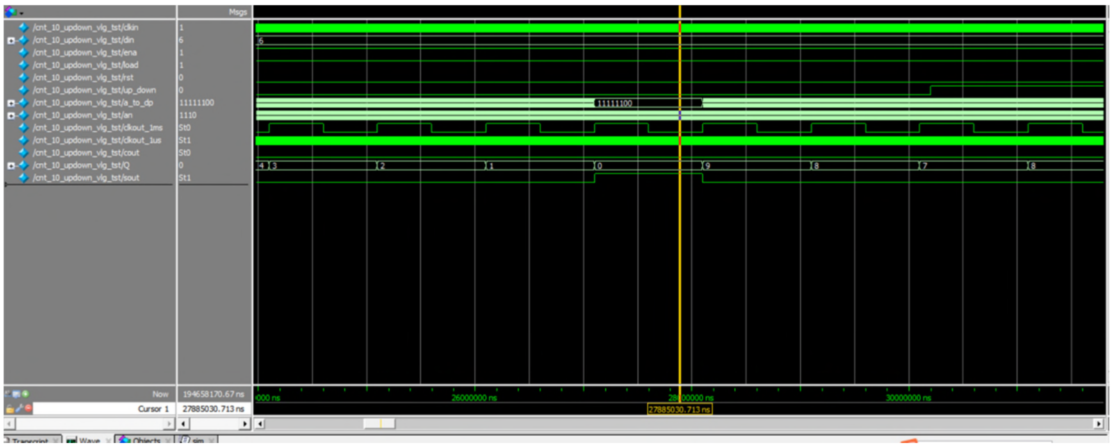


```
/cnt_10_updown_vlg_tst/clkin        0
/cnt_10_updown_vlg_tst/din          6
/cnt_10_updown_vlg_tst/ena          1
/cnt_10_updown_vlg_tst/load         1
/cnt_10_updown_vlg_tst/rst          0
/cnt_10_updown_vlg_tst/up_down      1
/cnt_10_updown_vlg_tst/a_to_dp      11110110
/cnt_10_updown_vlg_tst/an           1110
/cnt_10_updown_vlg_tst/clkout_1ms   St1
/cnt_10_updown_vlg_tst/clkout_1us   St1
/cnt_10_updown_vlg_tst/cout         St1
/cnt_10_updown_vlg_tst/Q            9
/cnt_10_updown_vlg_tst/sout         St0
Now        227239373.004 ns
Cursor 1   32393280.684 ns
```



```
/cnt_10_updown_vlg_tst/clkin        0
/cnt_10_updown_vlg_tst/din          6
/cnt_10_updown_vlg_tst/ena          1
/cnt_10_updown_vlg_tst/load         1
/cnt_10_updown_vlg_tst/rst          0
/cnt_10_updown_vlg_tst/up_down      1
/cnt_10_updown_vlg_tst/a_to_dp      11111100
/cnt_10_updown_vlg_tst/an           0111
/cnt_10_updown_vlg_tst/clkout_1ms   St1
/cnt_10_updown_vlg_tst/clkout_1us   St0
/cnt_10_updown_vlg_tst/cout         St1
/cnt_10_updown_vlg_tst/Q            9
/cnt_10_updown_vlg_tst/sout         St0
Now        250027773.974 ns
Cursor 1   32392989.577 ns
```

递减计数 sout 为 1 时, rst==0, up_down==0, load==1, ena==1, Q=0


Msgs
/cnt_10_updown_vlg_tst/clkin 1
/cnt_10_updown_vlg_tst/din 6
/cnt_10_updown_vlg_tst/ena 1
/cnt_10_updown_vlg_tst/load 1
/cnt_10_updown_vlg_tst/rst 0
/cnt_10_updown_vlg_tst/up_down 0
/cnt_10_updown_vlg_tst/a_to_dp 11111100
/cnt_10_updown_vlg_tst/an 1110
/cnt_10_updown_vlg_tst/clkout_1ms St0
/cnt_10_updown_vlg_tst/clkout_1us St1
/cnt_10_updown_vlg_tst/cout St0
/cnt_10_updown_vlg_tst/Q 0
/cnt_10_updown_vlg_tst/sout St1
Now 194658170.67 ns
Cursor 1 27885030.713 ns
26000000 ns
30000000 ns
27885030.713 ns

2．使用 Quartus Prime 软件设计加减可控十六进制计数器。

控制信号主要有：

（1）复位信号 rst：异步复位，高电平清零；

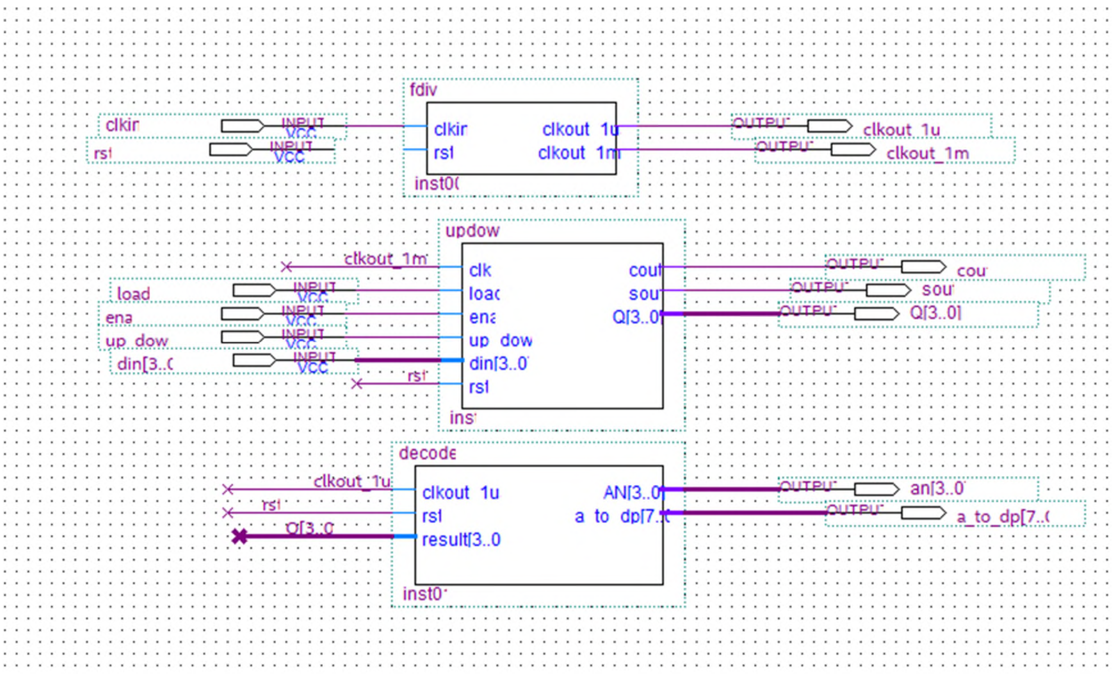
（2）数据加载信号 load：异步加载，低电平加载数据；

（3）使能信号 ena：同步使能，高电平使能；

（4）加减可控信号 updown:同步加减可控，高电平递增计数，低电平递减计数。

实验结论

1.　顶层文件：截完整的 BDF 图。



2.　计数器模块代码

```
module updown(clk,load,ena,cout,sout,up_down,Q,din,rst);
input load,ena,clk,rst,up_down;
input [3:0] din;
output cout,sout;
output reg [3:0] Q;

always @(posedge clk or posedge rst or negedge load )
if (rst==1)//异步清零，高电平清零
     Q<=0;
else
begin
if (!load)//异步预置，低电平加载数据
       Q<=din;
else
 begin
if (ena)//同步使能，高电平使能
 begin
 if (up_down==1&&Q==15)
        Q<=0;
 else if (up_down==0&&Q==0)
         Q<=15;
 else//同步加减可控，高电平递增计数，低电平递减计数。
 begin
 if (up_down==1) //加计数
      Q<=Q+1;
 else           //减计数
      Q<=Q-1;
   end
  end
 else
    Q<=Q;
 end
end

assign cout=((rst==0)&&(up_down==1)&&(load==1)&&(ena==1)&&(Q==15)) ? 1:0;
assign sout=((rst==0)&&(up_down==0)&&(load==1)&&(ena==1)&&(Q==0)) ? 1:0;
endmodule
```

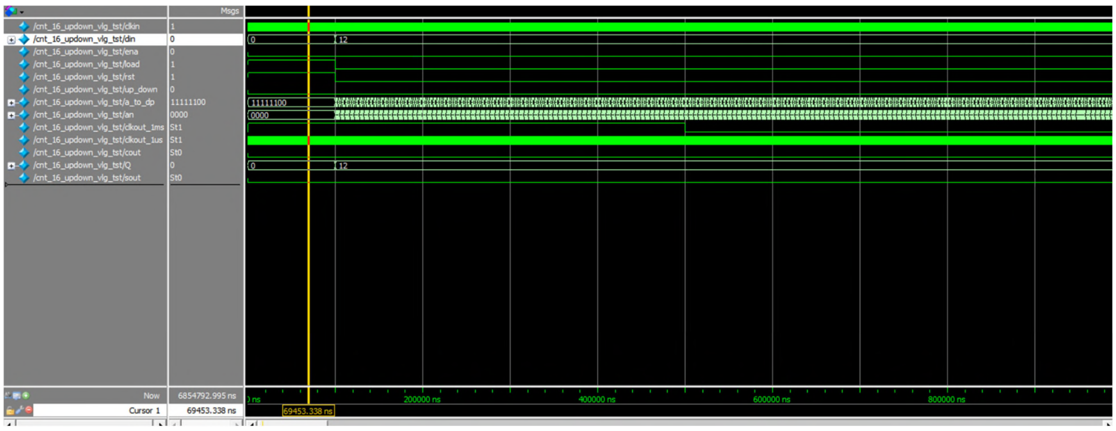
3. 测试文件代码

```
`timescale 1 ns/ 1 ps
module cnt_16_updown_vlg_tst();
// constants
// general purpose registers
//reg eachvec;
// test vector input registers
reg clkin;
reg [3:0] din;
reg ena;
reg load;
reg rst;
reg up_down;
// wires
wire [7:0]  a_to_dp;
wire [3:0]  an;
wire clkout_1ms;
wire clkout_1us;
wire cout;
wire [3:0]  Q;
wire sout;

// assign statements (if any)
cnt_16_updown i1 (
// port map - connection between master ports and signals/registers
    .a_to_dp(a_to_dp),
    .an(an),
    .clkin(clkin),
    .clkout_1ms(clkout_1ms),
    .clkout_1us(clkout_1us),
    .cout(cout),
    .din(din),
    .ena(ena),
    .load(load),
    .Q(Q),
    .rst(rst),
    .sout(sout),
    .up_down(up_down)
);
initial
begin
// code that executes only once
// insert code here --> begin
clkin=0;
rst=1;
ena=0;
load=1;
up_down=0;
din=0;
#100000
rst=0;
load=0;
din=12;
#10000000
```

```
ena=1;
load=1;
#100000000
up_down=1;
// --> end
$display("Running testbench");
end
always
// optional sensitivity list
// @(event1 or event2 or .... eventn)
begin
// code executes for every event on sensitivity list
// insert code here --> begin
  #10 clkin=~clkin;
//@eachvec;
// --> end
end
endmodule
```

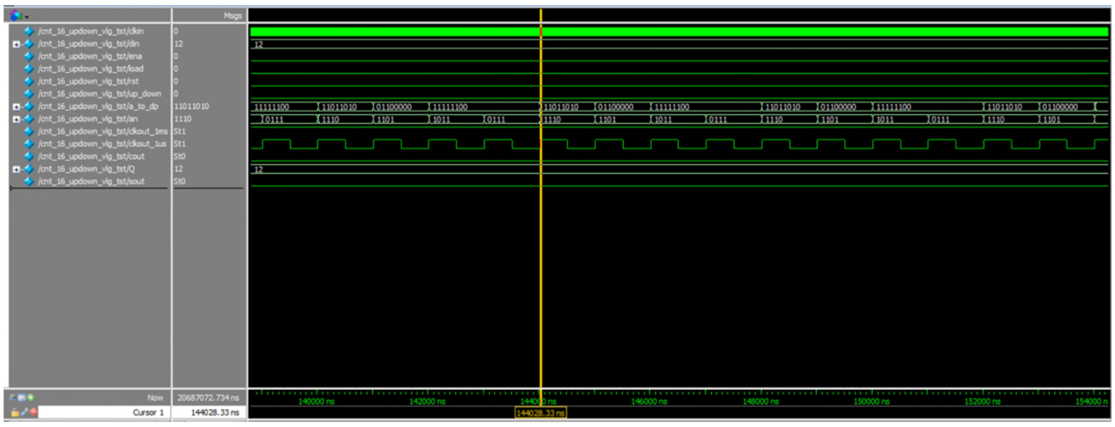
4. 仿真波形

复位有效时 rst=1;



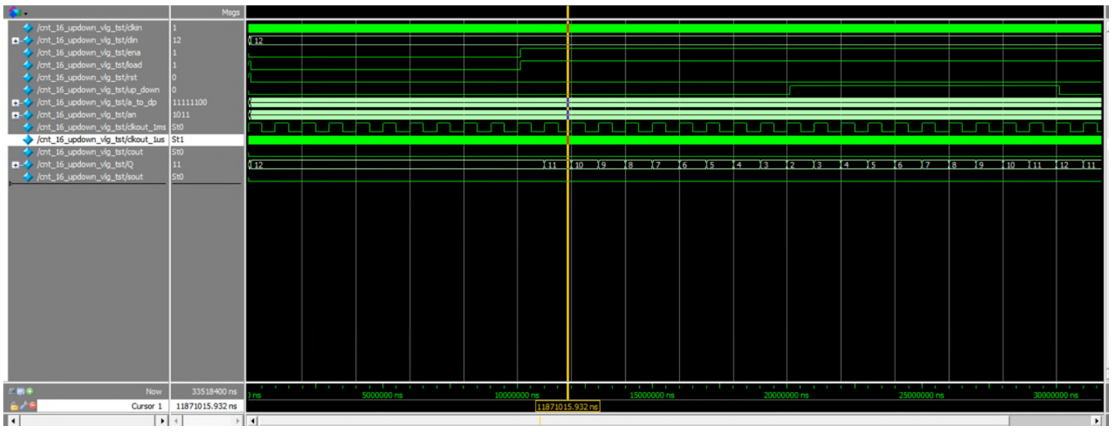
	Msgs
/cnt_16_updown_vlg_tst/clkin	1
/cnt_16_updown_vlg_tst/din	0
/cnt_16_updown_vlg_tst/ena	0
/cnt_16_updown_vlg_tst/load	1
/cnt_16_updown_vlg_tst/rst	1
/cnt_16_updown_vlg_tst/up_down	0
/cnt_16_updown_vlg_tst/a_to_dp	11111100
/cnt_16_updown_vlg_tst/an	0000
/cnt_16_updown_vlg_tst/clkout_1ms	St1
/cnt_16_updown_vlg_tst/clkout_1us	St1
/cnt_16_updown_vlg_tst/cout	St0
/cnt_16_updown_vlg_tst/Q	0
/cnt_16_updown_vlg_tst/sout	St0
Now	6854792.995 ns
Cursor 1	69453.338 ns

数据加载有效时 rst=0;load=0;din=12;



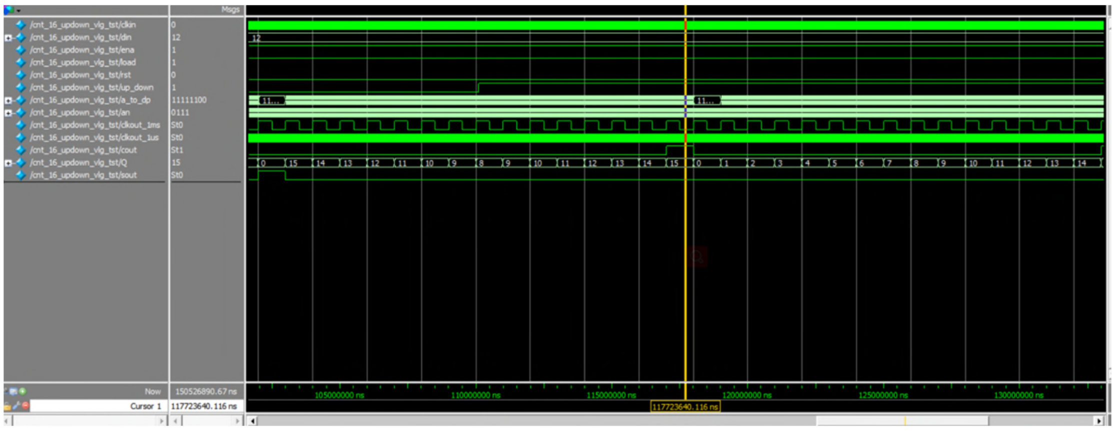
	Msgs
/cnt_16_updown_vlg_tst/clkin	0
/cnt_16_updown_vlg_tst/din	12
/cnt_16_updown_vlg_tst/ena	0
/cnt_16_updown_vlg_tst/load	0
/cnt_16_updown_vlg_tst/rst	0
/cnt_16_updown_vlg_tst/up_down	0
/cnt_16_updown_vlg_tst/a_to_dp	11011010
/cnt_16_updown_vlg_tst/an	1110
/cnt_16_updown_vlg_tst/clkout_1ms	St1
/cnt_16_updown_vlg_tst/clkout_1us	St1
/cnt_16_updown_vlg_tst/cout	St0
/cnt_16_updown_vlg_tst/Q	12
/cnt_16_updown_vlg_tst/sout	St0
Now	20687072.734 ns
Cursor 1	144028.33 ns

使能有效时 rst=0;load=1;ena=1;

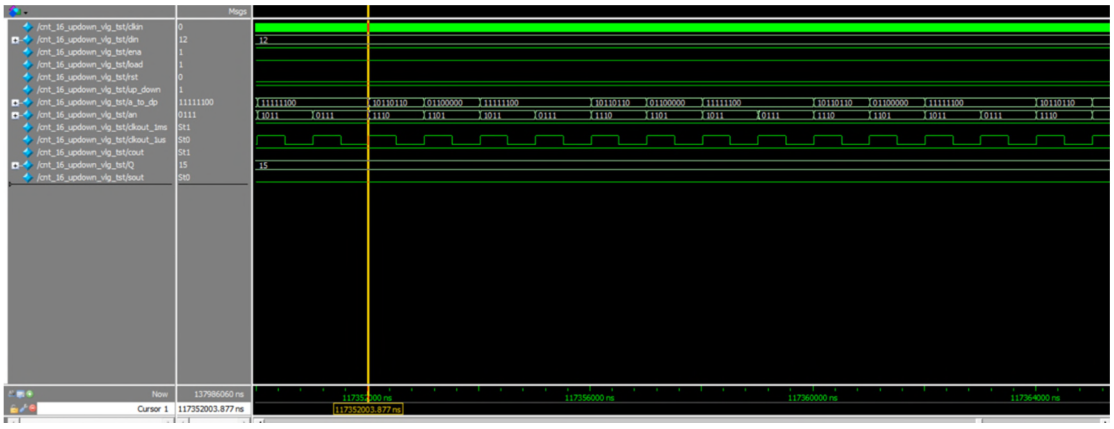


```
/cnt_16_updown_vlg_tst/clkin       1
/cnt_16_updown_vlg_tst/din         12
/cnt_16_updown_vlg_tst/ena         1
/cnt_16_updown_vlg_tst/load        1
/cnt_16_updown_vlg_tst/rst         0
/cnt_16_updown_vlg_tst/up_down     0
/cnt_16_updown_vlg_tst/a_to_dp     11111100
/cnt_16_updown_vlg_tst/an          1011
/cnt_16_updown_vlg_tst/clkout_1ms  St0
/cnt_16_updown_vlg_tst/clkout_1us  St1
/cnt_16_updown_vlg_tst/cout        St0
/cnt_16_updown_vlg_tst/Q           11
/cnt_16_updown_vlg_tst/sout        St0
Now       33518400 ns
Cursor 1  11871015.932 ns
```

递增计数 cout 为 1 时 rst==0,up_down==1,load==1,ena==1,Q=15

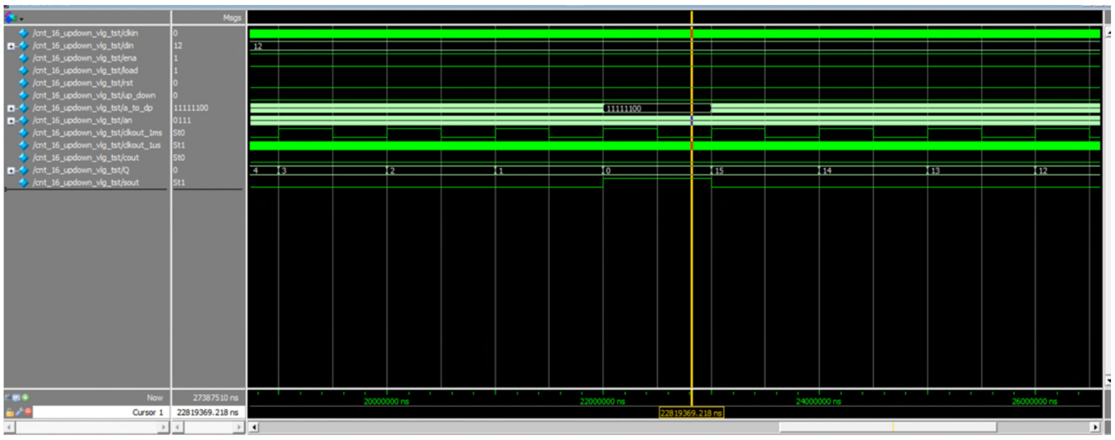


```
/cnt_16_updown_vlg_tst/clkin       0
/cnt_16_updown_vlg_tst/din         12
/cnt_16_updown_vlg_tst/ena         1
/cnt_16_updown_vlg_tst/load        1
/cnt_16_updown_vlg_tst/rst         0
/cnt_16_updown_vlg_tst/up_down     1
/cnt_16_updown_vlg_tst/a_to_dp     11111100
/cnt_16_updown_vlg_tst/an          0111
/cnt_16_updown_vlg_tst/clkout_1ms  St0
/cnt_16_updown_vlg_tst/clkout_1us  St0
/cnt_16_updown_vlg_tst/cout        St1
/cnt_16_updown_vlg_tst/Q           15
/cnt_16_updown_vlg_tst/sout        St0
Now       150526890.67 ns
Cursor 1  117723640.116 ns
```



```
/cnt_16_updown_vlg_tst/clkin       0
/cnt_16_updown_vlg_tst/din         12
/cnt_16_updown_vlg_tst/ena         1
/cnt_16_updown_vlg_tst/load        1
/cnt_16_updown_vlg_tst/rst         0
/cnt_16_updown_vlg_tst/up_down     1
/cnt_16_updown_vlg_tst/a_to_dp     11111100
/cnt_16_updown_vlg_tst/an          0111
/cnt_16_updown_vlg_tst/clkout_1ms  St1
/cnt_16_updown_vlg_tst/clkout_1us  St0
/cnt_16_updown_vlg_tst/cout        St1
/cnt_16_updown_vlg_tst/Q           15
/cnt_16_updown_vlg_tst/sout        St0
Now       137986060 ns
Cursor 1  117352003.877 ns
```

递减计数 sout 为 1 时,rst==0,up_down==0,load==1,ena==1,Q==0



Msgs
/cnt_16_updown_vlg_tst/clkin 0
/cnt_16_updown_vlg_tst/din 12
/cnt_16_updown_vlg_tst/ena 1
/cnt_16_updown_vlg_tst/load 1
/cnt_16_updown_vlg_tst/rst 0
/cnt_16_updown_vlg_tst/up_down 0
/cnt_16_updown_vlg_tst/a_to_dp 11111100
/cnt_16_updown_vlg_tst/an 0111
/cnt_16_updown_vlg_tst/clkout_1ms St0
/cnt_16_updown_vlg_tst/clkout_1us St1
/cnt_16_updown_vlg_tst/cout St0
/cnt_16_updown_vlg_tst/Q 0
/cnt_16_updown_vlg_tst/sout St1
Now 27387510 ns
Cursor 1 22819369.218 ns
20000000 ns
22000000 ns
24000000 ns
26000000 ns
22819369.218 ns

3．使用 Quartus Prime 软件设计加减可控双十进制计数器。

控制信号主要有：

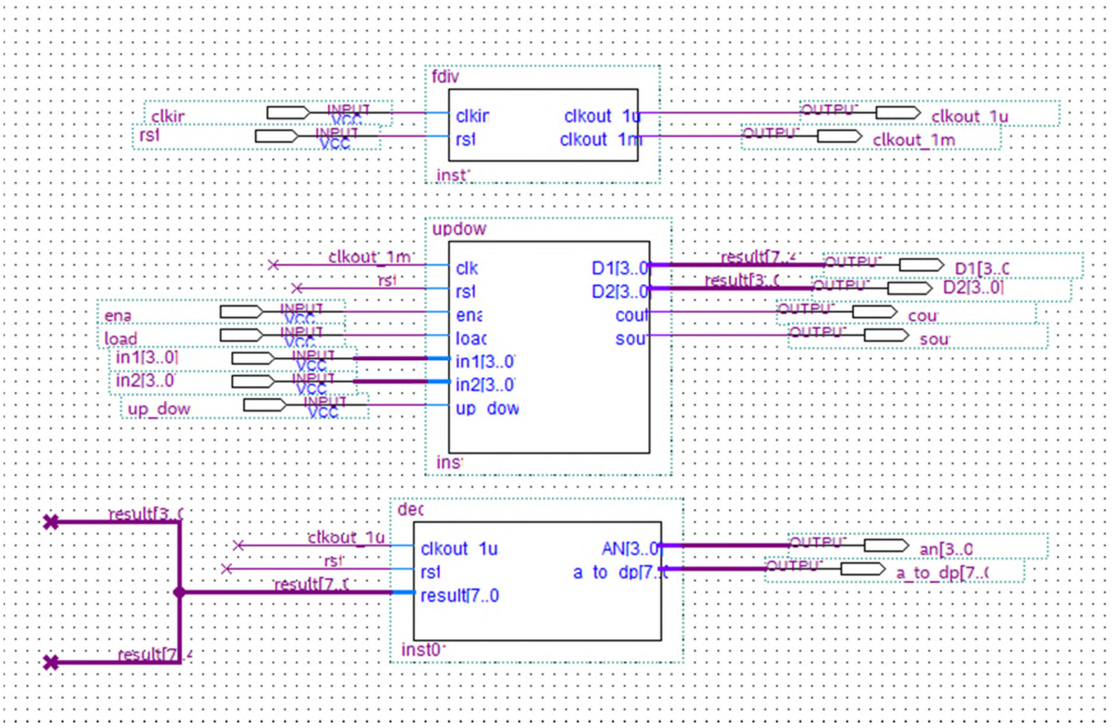
（1）复位信号 rst：异步复位，高电平清零；

（2）数据加载信号 load：异步加载，低电平加载数据；

（3）使能信号 ena：同步使能，高电平使能；

（4）加减可控信号 updown:同步加减可控，高电平递增计数，低电平递减计数。

1.　顶层文件



2.　计数器模块代码

```
module updown(clk,rst,ena,load,in1,in2,D1,D2,cout,sout,up_down);
input up_down,clk,rst,load,ena;
input [3:0] in1,in2;
output reg [3:0] D1,D2;
output cout,sout;

always @ ( posedge clk or posedge rst  or negedge load)
  if (rst)//异步清零，高电平清零
     begin
      D1<=0;
      D2<=0;
     end
  else
     begin
       if (!load) //异步加载，低电平加载数据
          begin
          D1<=in1;
          D2<=in2;
          end
       else
             begin
              if (ena) //同步使能，高电平使能
             begin
                if (up_down==1)//加计数
                   begin
                    if ((D1==9)&&(D2==9))//当输入为 99，输出变为 0.
                             begin
                              D1<=0;
                              D2<=0;
                             end
                    else if (D2==9)//当输入个位为 9，则输出十位加一，个位为 0.
                      begin
                     D1<=D1+1;
                     D2<=0;
                     end
                   else        //当输入为其他情况，则输出十位不变，个位加一.
                             begin
                               D1<=D1;
                              D2<=D2+1;
                             end
                      end
                else //减计数
                      begin
                    if ((D1==0)&&(D2==0)) //当输入等于 0，则输出变为 99.
                                begin
                                 D1<=9;
                                 D2<=9;
                                end
                    else if (D2==0)      //当输入个位等于 0，则输出的十位减一，个位为 9.
                            begin
                             D2<=9;
                             D1<=D1-1;
                            end
                     else             //当输入为其他情况，则输出十位不变，个位减一
                            begin
                            D2<=D2-1;
                            D1<=D1;
                            end
                      end
                  end
              else  //当不使能时，输出保持不变
               begin
                 D1<=D1;
                 D2<=D2;
               end
              end
        end

 assign cout=((rst==0)&&(up_down==1)&&(load==1)&&(ena==1)&&((D1==9)&&(D2==9))) ? 1:0;
 assign sout=((rst==0)&&(up_down==0)&&(load==1)&&(ena==1)&&((D1==0)&&(D2==0))) ? 1:0;
endmodule
```

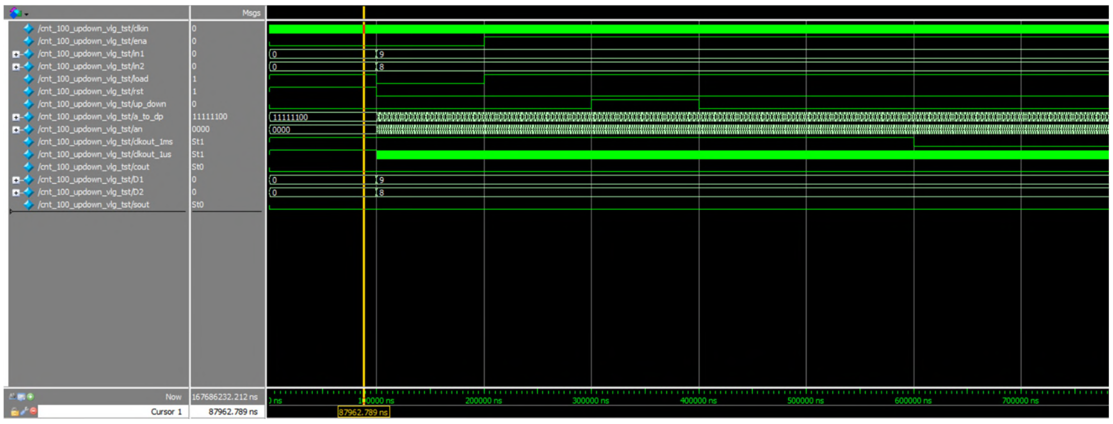
3. 测试文件代码

```
`timescale 1 ns/ 1 ps
module cnt_100_updown_vlg_tst();
// constants
// general purpose registers
//reg eachvec;
// test vector input registers
reg clkin;
reg ena;
reg [3:0] in1;
reg [3:0] in2;
reg load;
reg rst;
reg up_down;
// wires
wire [7:0]  a_to_dp;
wire [3:0]  an;
wire clkout_1ms;
wire clkout_1us;
wire cout;
wire [3:0]  D1;
wire [3:0]  D2;
wire sout;

// assign statements (if any)
cnt_100_updown i1 (
// port map - connection between master ports and signals/registers
    .a_to_dp(a_to_dp),
    .an(an),
    .clkin(clkin),
    .clkout_1ms(clkout_1ms),
    .clkout_1us(clkout_1us),
    .cout(cout),
    .D1(D1),
    .D2(D2),
    .ena(ena),
    .in1(in1),
    .in2(in2),
    .load(load),
    .rst(rst),
    .sout(sout),
    .up_down(up_down)
);
initial
begin
// code that executes only once
// insert code here --> begin
clkin=0;
rst=1;
ena=0;
load=1;
up_down=0;
in1=0;
in2=0;
ena=0;
#100000
rst=0;
load=0;
in1=9;
in2=8;
#100000
ena=1;
load=1;
```

```
#100000
up_down=1;
#10000000
up_down=0;
// --> end
$display("Running testbench");
end
always
// optional sensitivity list
// @(event1 or event2 or .... eventn)
begin
// code executes for every event on sensitivity list
// insert code here --> begin
  #10 clkin=~clkin;
//@eachvec;
// --> end
end
endmodule
```

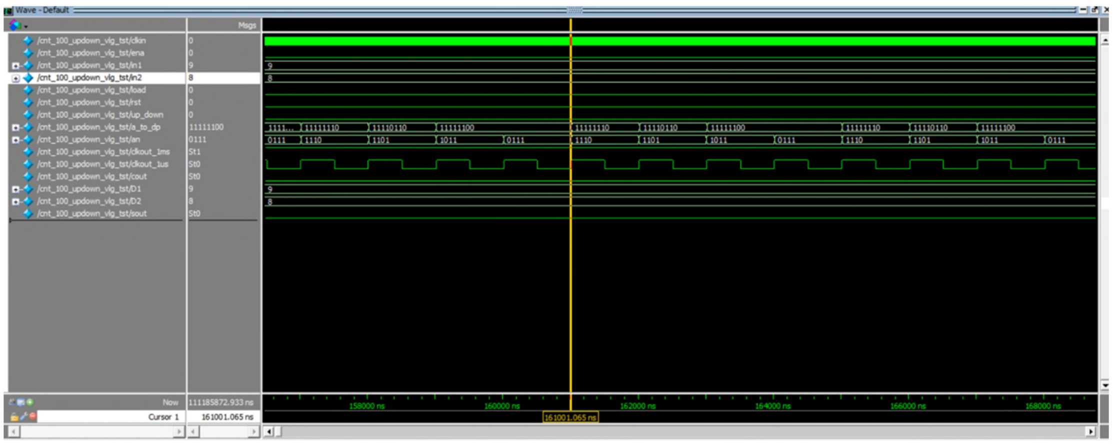
4. 仿真波形：

复位有效时 rst=1;



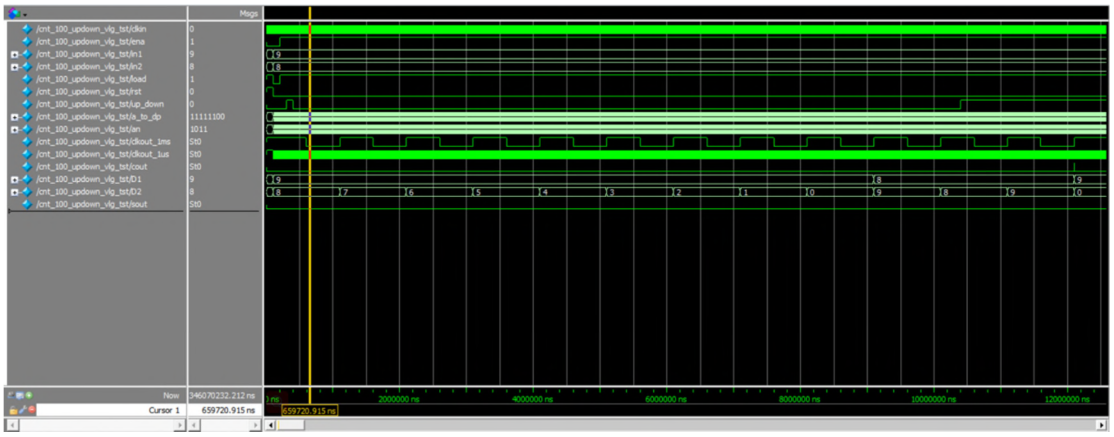
```
/cnt_100_updown_vlg_tst/clkin        0
/cnt_100_updown_vlg_tst/ena          0
/cnt_100_updown_vlg_tst/in1          0
/cnt_100_updown_vlg_tst/in2          0
/cnt_100_updown_vlg_tst/load         1
/cnt_100_updown_vlg_tst/rst          1
/cnt_100_updown_vlg_tst/up_down      0
/cnt_100_updown_vlg_tst/a_to_dp      11111100
/cnt_100_updown_vlg_tst/an           0000
/cnt_100_updown_vlg_tst/clkout_1ms   St1
/cnt_100_updown_vlg_tst/clkout_1us   St1
/cnt_100_updown_vlg_tst/cout         St0
/cnt_100_updown_vlg_tst/D1           0
/cnt_100_updown_vlg_tst/D2           0
/cnt_100_updown_vlg_tst/sout         St0
Now       167686232.212 ns
Cursor 1  87962.789 ns
```

数据加载有效时 rst=0;load=0;in1=9;in2=8;



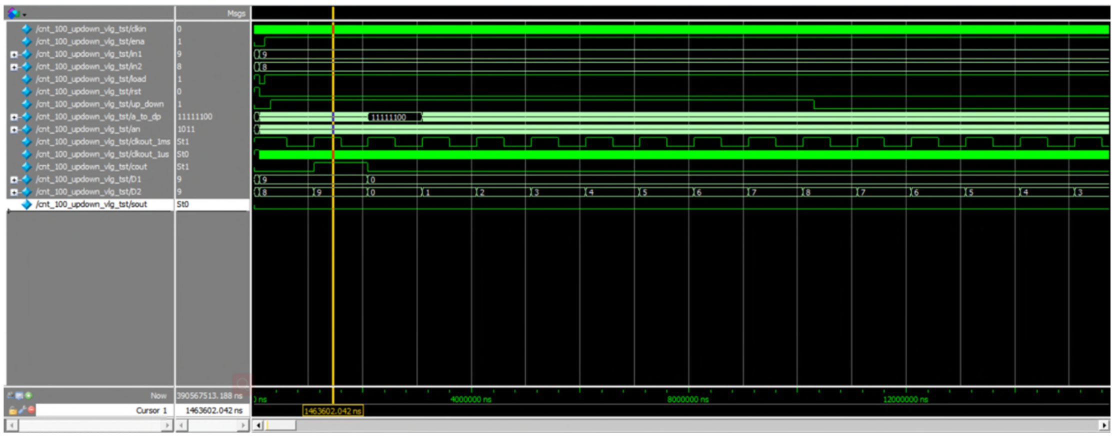
```
/cnt_100_updown_vlg_tst/clkin        0
/cnt_100_updown_vlg_tst/ena          0
/cnt_100_updown_vlg_tst/in1          9
/cnt_100_updown_vlg_tst/in2          8
/cnt_100_updown_vlg_tst/load         0
/cnt_100_updown_vlg_tst/rst          0
/cnt_100_updown_vlg_tst/up_down      0
/cnt_100_updown_vlg_tst/a_to_dp      11111100
/cnt_100_updown_vlg_tst/an           0111
/cnt_100_updown_vlg_tst/clkout_1ms   St1
/cnt_100_updown_vlg_tst/clkout_1us   St0
/cnt_100_updown_vlg_tst/cout         St0
/cnt_100_updown_vlg_tst/D1           9
/cnt_100_updown_vlg_tst/D2           8
/cnt_100_updown_vlg_tst/sout         St0
Now       111185872.933 ns
Cursor 1  161001.065 ns
```

使能有效时 rst=0;load=1;ena=1;

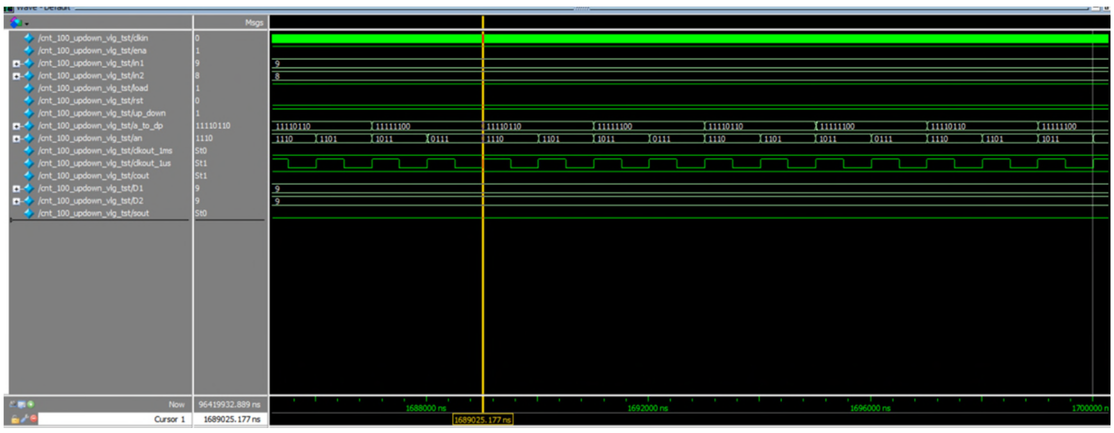


```
/cnt_100_updown_vlg_tst/clkin        0
/cnt_100_updown_vlg_tst/ena          1
/cnt_100_updown_vlg_tst/in1          9
/cnt_100_updown_vlg_tst/in2          8
/cnt_100_updown_vlg_tst/load         1
/cnt_100_updown_vlg_tst/rst          0
/cnt_100_updown_vlg_tst/up_down      0
/cnt_100_updown_vlg_tst/a_to_dp      11111100
/cnt_100_updown_vlg_tst/an           1011
/cnt_100_updown_vlg_tst/clkout_1ms   St0
/cnt_100_updown_vlg_tst/clkout_1us   St0
/cnt_100_updown_vlg_tst/cout         St0
/cnt_100_updown_vlg_tst/D1           9
/cnt_100_updown_vlg_tst/D2           8
/cnt_100_updown_vlg_tst/sout         St0
Now        346070232.212 ns
Cursor 1   659720.915 ns
```

递增计数 cout 为 1 时 rst==0,up_down==1,load==1,ena==1,D1==9,D2==9

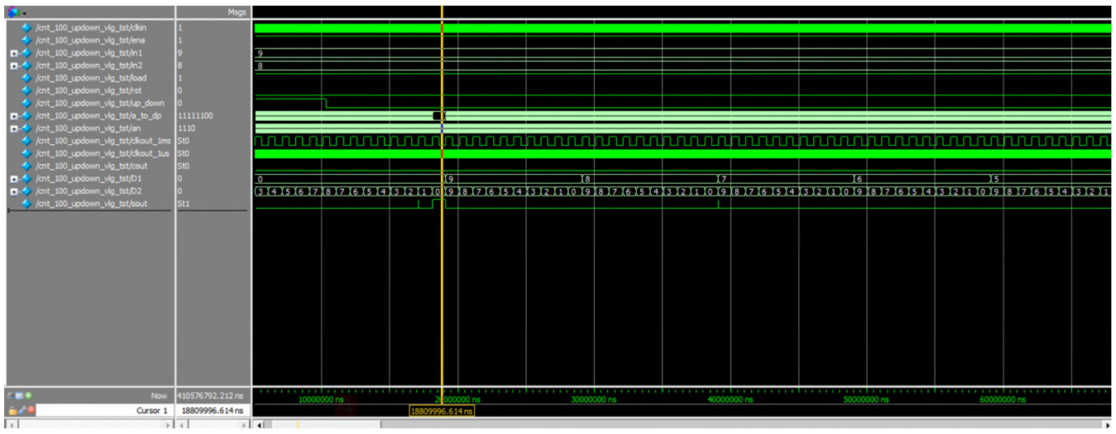


```
/cnt_100_updown_vlg_tst/clkin        0
/cnt_100_updown_vlg_tst/ena          1
/cnt_100_updown_vlg_tst/in1          9
/cnt_100_updown_vlg_tst/in2          8
/cnt_100_updown_vlg_tst/load         1
/cnt_100_updown_vlg_tst/rst          0
/cnt_100_updown_vlg_tst/up_down      1
/cnt_100_updown_vlg_tst/a_to_dp      11111100
/cnt_100_updown_vlg_tst/an           1011
/cnt_100_updown_vlg_tst/clkout_1ms   St1
/cnt_100_updown_vlg_tst/clkout_1us   St0
/cnt_100_updown_vlg_tst/cout         St1
/cnt_100_updown_vlg_tst/D1           9
/cnt_100_updown_vlg_tst/D2           9
/cnt_100_updown_vlg_tst/sout         St0
Now        390567513.188 ns
Cursor 1   1463602.042 ns
```



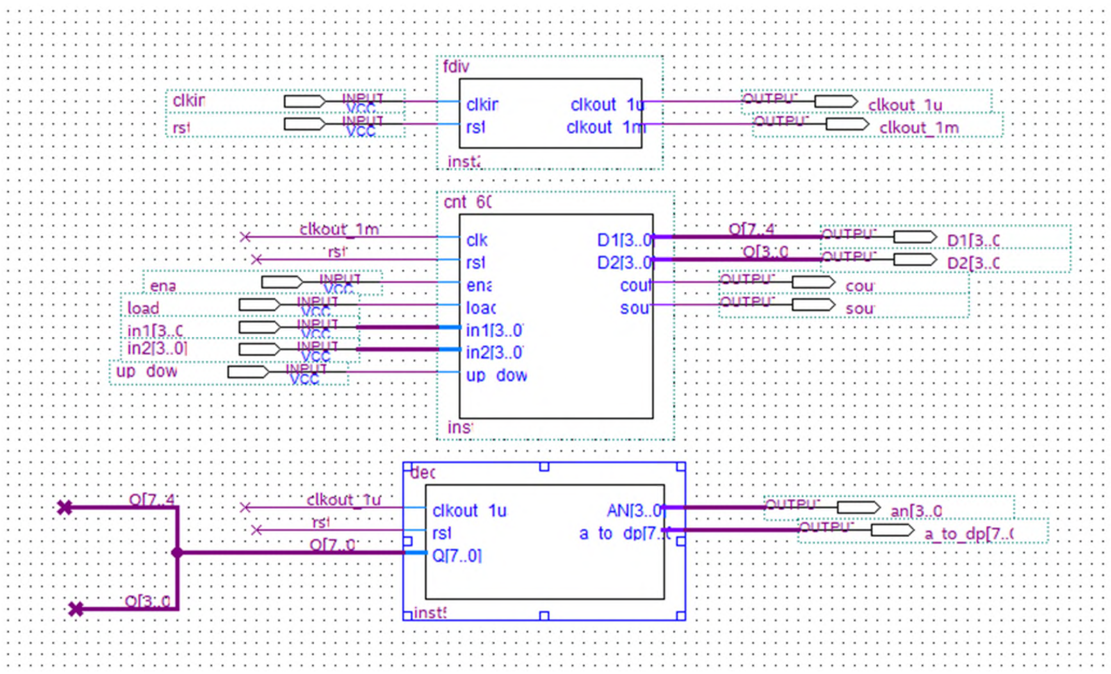
```
/cnt_100_updown_vlg_tst/clkin        0
/cnt_100_updown_vlg_tst/ena          1
/cnt_100_updown_vlg_tst/in1          9
/cnt_100_updown_vlg_tst/in2          8
/cnt_100_updown_vlg_tst/load         1
/cnt_100_updown_vlg_tst/rst          0
/cnt_100_updown_vlg_tst/up_down      1
/cnt_100_updown_vlg_tst/a_to_dp      11110110
/cnt_100_updown_vlg_tst/an           1110
/cnt_100_updown_vlg_tst/clkout_1ms   St0
/cnt_100_updown_vlg_tst/clkout_1us   St1
/cnt_100_updown_vlg_tst/cout         St1
/cnt_100_updown_vlg_tst/D1           9
/cnt_100_updown_vlg_tst/D2           9
/cnt_100_updown_vlg_tst/sout         St0
Now        96419932.889 ns
Cursor 1   1689025.177 ns
```

递减计数 sout 为 1 时,rst==0,up_down==0,load==1,ena==1,D1==0,D2==0


Msgs
/cnt_100_updown_vlg_tst/clkin 1
/cnt_100_updown_vlg_tst/ena 1
/cnt_100_updown_vlg_tst/in1 9
/cnt_100_updown_vlg_tst/in2 8
/cnt_100_updown_vlg_tst/load 1
/cnt_100_updown_vlg_tst/rst 0
/cnt_100_updown_vlg_tst/up_down 0
/cnt_100_updown_vlg_tst/a_to_dp 11111100
/cnt_100_updown_vlg_tst/an 1110
/cnt_100_updown_vlg_tst/clkout_1ms St0
/cnt_100_updown_vlg_tst/clkout_1us St0
/cnt_100_updown_vlg_tst/cout St0
/cnt_100_updown_vlg_tst/D1 0
/cnt_100_updown_vlg_tst/D2 0
/cnt_100_updown_vlg_tst/sout St1
Now 410576792.212 ns
Cursor 1 18809996.614 ns

4.　　实验扩展部分：加减可控 60 进制计数器的设计（秒表）

1.　顶层文件



2.　计数器模块代码

```
module cnt_60(clk,rst,ena,load,D1,D2,in1,in2,cout,sout,up_down);
input up_down,clk,rst,load,ena;
input [3:0] in1,in2;
output reg [3:0] D1,D2;
output cout,sout;

always @ ( posedge clk or posedge rst  or negedge load)
if (rst)//异步清零，高电平清零
   begin
    D1<=0;
    D2<=0;
   end
else
  begin
  if (!load) //异步加载，低电平加载数据
   begin
    D1<=in1;
    D2<=in2;
    end
   else
    begin
      if (ena) //同步使能，高电平使能
       begin
         if (up_down==1)//加计数
          begin
          if ((D1==5)&&(D2==9))//当输入为 59，则输出变为 0.
             begin
               D1<=0;
               D2<=0;
            end
           else if (D2==9)//当输入个位为 9，则输出十位加一，个位为 0.
             begin
             D1<=D1+1;
              D2<=0;
             end
                else        //当输入为其他情况，则输出十位不变，个位加一.
                    begin
                     D1<=D1;
                     D2<=D2+1;
                   end
                  end
    else //减计数
    begin
    if ((D1==0)&&(D2==0)) //当输入等于 0，则输出变为 59.
     begin
    D1<=5;
     D2<=9;
     end
    else if (D2==0)      //当输入个位等于 0，则输出的十位减一，个位为 9.
      begin
       D2<=9;
       D1<=D1-1;
     end
     else             //当输入为其他情况，则输出十位不变，个位减一
```

```
         begin
        D2<=D2-1;
       D1<=D1;
       end
        end
   end
    else//当使能端为 0 时，输出保持不变；
       begin
         D1<=D1;
         D2<=D2;
        end
      end
    end

  assign cout=((rst==0)&&(up_down==1)&&(load==1)&&(ena==1)&&((D1==5)&&(D2==9))) ? 1:0;
  assign sout=((rst==0)&&(up_down==0)&&(load==1)&&(ena==1)&&((D1==0)&&(D2==0))) ? 1:0;
endmodule
```

3. 测试文件代码

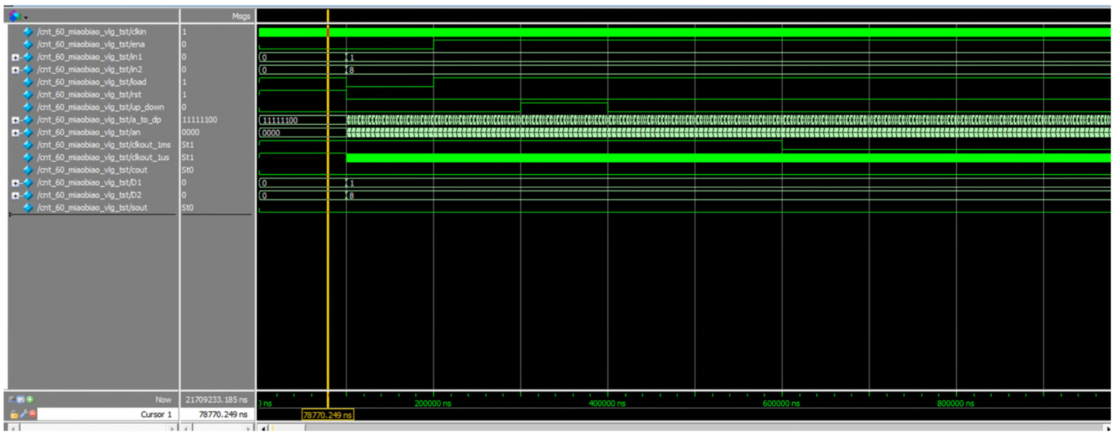
```
`timescale 1 ns/ 1 ps
module cnt_60_miaobiao_vlg_tst();
// constants
// general purpose registers
//reg eachvec;
// test vector input registers
reg clkin;
reg ena;
reg [3:0] in1;
reg [3:0] in2;
reg load;
reg rst;
reg up_down;
// wires
wire [7:0]  a_to_dp;
wire [3:0]  an;
wire clkout_1ms;
wire clkout_1us;
wire cout;
wire [3:0]  D1;
wire [3:0]  D2;
wire sout;

// assign statements (if any)
```

```
cnt_60_miaobiao i1 (
// port map - connection between master ports and signals/registers
    .a_to_dp(a_to_dp),
    .an(an),
    .clkin(clkin),
    .clkout_1ms(clkout_1ms),
    .clkout_1us(clkout_1us),
    .cout(cout),
    .D1(D1),
    .D2(D2),
    .ena(ena),
    .in1(in1),
    .in2(in2),
    .load(load),
    .rst(rst),
    .sout(sout),
    .up_down(up_down)
);
initial
begin
// code that executes only once
// insert code here --> begin
clkin=0;
rst=1;
ena=0;
load=1;
up_down=0;
in1=0;
in2=0;
ena=0;
#100000
rst=0;
load=0;
in1=1;
in2=8;
#100000
ena=1;
load=1;
#10000000
up_down=1;
#100000000
up_down=0;
// --> end
$display("Running testbench");
```

```
end
always
// optional sensitivity list
// @(event1 or event2 or .... eventn)
begin
// code executes for every event on sensitivity list
// insert code here --> begin
  #10 clkin=~clkin;
//@eachvec;
// --> end
end
endmodule
```

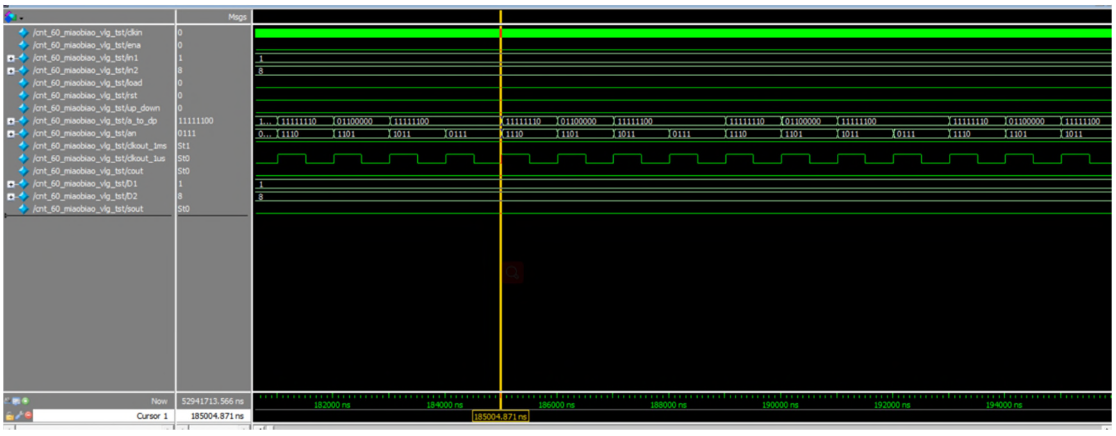
4.　仿真波形：

复位有效时 rst=1;



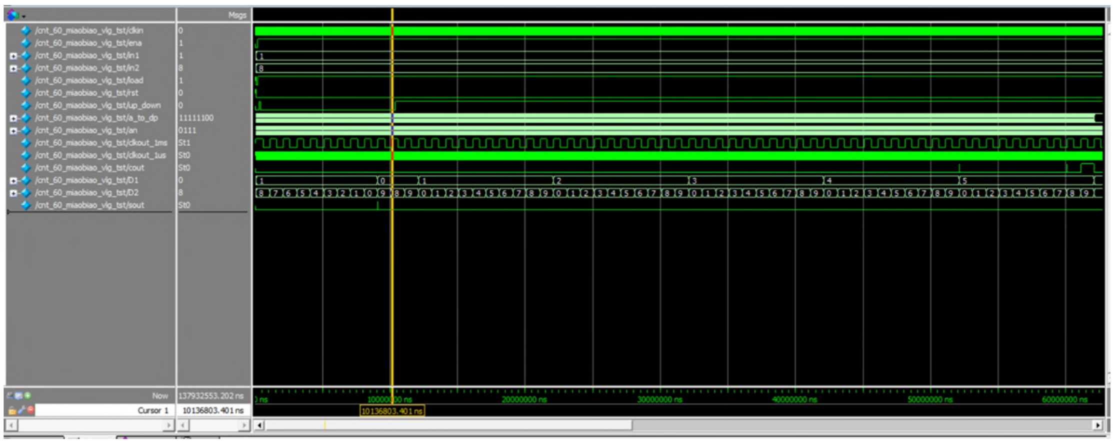
```
/cnt_60_miaobiao_vlg_tst/clkin       1
/cnt_60_miaobiao_vlg_tst/ena         0
/cnt_60_miaobiao_vlg_tst/in1         0
/cnt_60_miaobiao_vlg_tst/in2         0
/cnt_60_miaobiao_vlg_tst/load        1
/cnt_60_miaobiao_vlg_tst/rst         1
/cnt_60_miaobiao_vlg_tst/up_down     0
/cnt_60_miaobiao_vlg_tst/a_to_dp     11111100
/cnt_60_miaobiao_vlg_tst/an          0000
/cnt_60_miaobiao_vlg_tst/clkout_1ms  St1
/cnt_60_miaobiao_vlg_tst/clkout_1us  St1
/cnt_60_miaobiao_vlg_tst/cout        St0
/cnt_60_miaobiao_vlg_tst/D1          0
/cnt_60_miaobiao_vlg_tst/D2          0
/cnt_60_miaobiao_vlg_tst/sout        St0
Now       21709233.185 ns
Cursor 1  78770.249 ns
```

数据加载有效时数据加载有效时 rst=0;load=0;in1=1;in2=8;



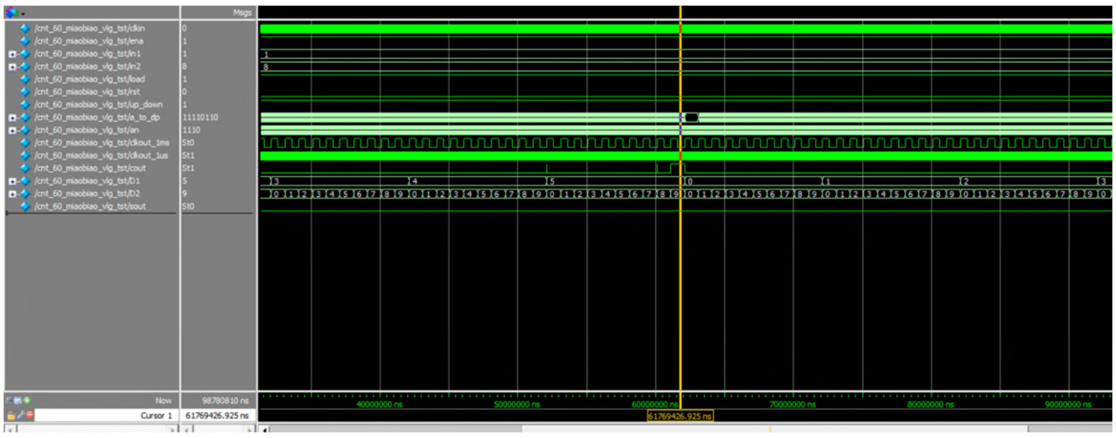
```
/cnt_60_miaobiao_vlg_tst/clkin       0
/cnt_60_miaobiao_vlg_tst/ena         0
/cnt_60_miaobiao_vlg_tst/in1         1
/cnt_60_miaobiao_vlg_tst/in2         8
/cnt_60_miaobiao_vlg_tst/load        0
/cnt_60_miaobiao_vlg_tst/rst         0
/cnt_60_miaobiao_vlg_tst/up_down     0
/cnt_60_miaobiao_vlg_tst/a_to_dp     11111100
/cnt_60_miaobiao_vlg_tst/an          0111
/cnt_60_miaobiao_vlg_tst/clkout_1ms  St1
/cnt_60_miaobiao_vlg_tst/clkout_1us  St0
/cnt_60_miaobiao_vlg_tst/cout        St0
/cnt_60_miaobiao_vlg_tst/D1          1
/cnt_60_miaobiao_vlg_tst/D2          8
/cnt_60_miaobiao_vlg_tst/sout        St0
Now       52941713.566 ns
Cursor 1  185004.871 ns
```

使能有效时 rst=0;load=1;ena=1;

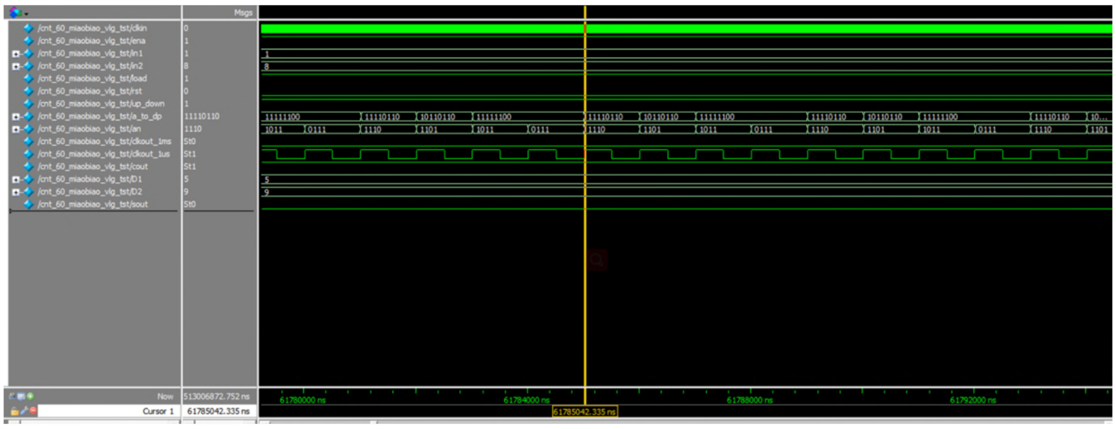


```
/cnt_60_miaobiao_vlg_tst/clkin        0
/cnt_60_miaobiao_vlg_tst/ena          1
/cnt_60_miaobiao_vlg_tst/in1          1
/cnt_60_miaobiao_vlg_tst/in2          8
/cnt_60_miaobiao_vlg_tst/load         1
/cnt_60_miaobiao_vlg_tst/rst          0
/cnt_60_miaobiao_vlg_tst/up_down      0
/cnt_60_miaobiao_vlg_tst/a_to_dp      11111100
/cnt_60_miaobiao_vlg_tst/an           0111
/cnt_60_miaobiao_vlg_tst/clkout_1ms   St1
/cnt_60_miaobiao_vlg_tst/clkout_1us   St0
/cnt_60_miaobiao_vlg_tst/cout         St0
/cnt_60_miaobiao_vlg_tst/D1           0
/cnt_60_miaobiao_vlg_tst/D2           8
/cnt_60_miaobiao_vlg_tst/sout         St0
Now        137932553.202 ns
Cursor 1   10136803.401 ns
```

递增计数 cout 为 1 时 rst==0,up_down==1,load==1,ena==1,D1==5,D2==9

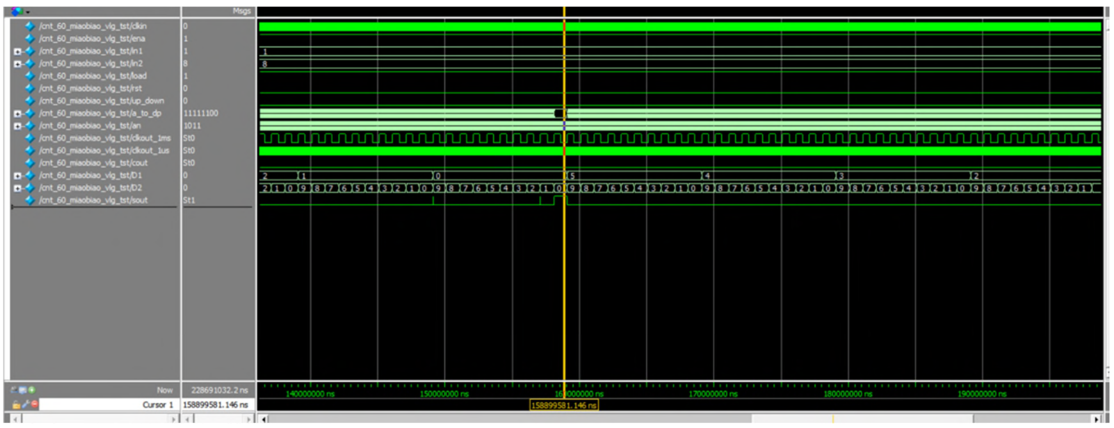


```
/cnt_60_miaobiao_vlg_tst/clkin        0
/cnt_60_miaobiao_vlg_tst/ena          1
/cnt_60_miaobiao_vlg_tst/in1          1
/cnt_60_miaobiao_vlg_tst/in2          8
/cnt_60_miaobiao_vlg_tst/load         1
/cnt_60_miaobiao_vlg_tst/rst          0
/cnt_60_miaobiao_vlg_tst/up_down      1
/cnt_60_miaobiao_vlg_tst/a_to_dp      11110110
/cnt_60_miaobiao_vlg_tst/an           1110
/cnt_60_miaobiao_vlg_tst/clkout_1ms   St0
/cnt_60_miaobiao_vlg_tst/clkout_1us   St1
/cnt_60_miaobiao_vlg_tst/cout         St1
/cnt_60_miaobiao_vlg_tst/D1           5
/cnt_60_miaobiao_vlg_tst/D2           9
/cnt_60_miaobiao_vlg_tst/sout         St0
Now        98780810 ns
Cursor 1   61769426.925 ns
```



```
/cnt_60_miaobiao_vlg_tst/clkin        0
/cnt_60_miaobiao_vlg_tst/ena          1
/cnt_60_miaobiao_vlg_tst/in1          1
/cnt_60_miaobiao_vlg_tst/in2          8
/cnt_60_miaobiao_vlg_tst/load         1
/cnt_60_miaobiao_vlg_tst/rst          0
/cnt_60_miaobiao_vlg_tst/up_down      1
/cnt_60_miaobiao_vlg_tst/a_to_dp      11110110
/cnt_60_miaobiao_vlg_tst/an           1110
/cnt_60_miaobiao_vlg_tst/clkout_1ms   St0
/cnt_60_miaobiao_vlg_tst/clkout_1us   St1
/cnt_60_miaobiao_vlg_tst/cout         St1
/cnt_60_miaobiao_vlg_tst/D1           5
/cnt_60_miaobiao_vlg_tst/D2           9
/cnt_60_miaobiao_vlg_tst/sout         St0
Now        513006872.752 ns
Cursor 1   61785042.335 ns
```

递减计数 sout 为 1 时,rst==0,up_down==0,load==1,ena==1,D1==0,D2==0



```
                                              Msgs
/cnt_60_miaobiao_vlg_tst/clkin                0
/cnt_60_miaobiao_vlg_tst/ena                  1
/cnt_60_miaobiao_vlg_tst/in1                  1
/cnt_60_miaobiao_vlg_tst/in2                  8
/cnt_60_miaobiao_vlg_tst/load                 1
/cnt_60_miaobiao_vlg_tst/rst                  0
/cnt_60_miaobiao_vlg_tst/up_down              0
/cnt_60_miaobiao_vlg_tst/a_to_dp              11111100
/cnt_60_miaobiao_vlg_tst/an                   1011
/cnt_60_miaobiao_vlg_tst/clkout_1ms           St0
/cnt_60_miaobiao_vlg_tst/clkout_1us           St0
/cnt_60_miaobiao_vlg_tst/cout                 St0
/cnt_60_miaobiao_vlg_tst/D1                   0
/cnt_60_miaobiao_vlg_tst/D2                   0
/cnt_60_miaobiao_vlg_tst/sout                 St1

                                 Now          228691032.2 ns
                            Cursor 1          158899581.146 ns
```