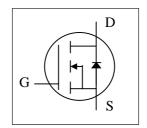
Halogen-Free Product



N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- ▼ 100% R_q & UIS Test
- **▼** Simple Drive Requirement
- **▼** Fast Switching Characteristic
- **▼** RoHS Compliant & Halogen-Free

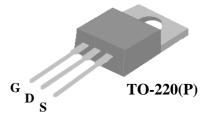


BV _{DSS}	100V
R _{DS(ON)}	$\mathbf{3.88m}\Omega$

Description

XP10N3R8 series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-220 package is widely preferred for all commercial-industrial through hole applications. The low thermal resistance and low package cost contribute to the worldwide popular package.



Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	<u>+</u> 20	V
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V ⁴ (Silicon Limited)	132	Α
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V ⁴ (Package Limited)	130	Α
I _D @T _C =100°C	Drain Current, V _{GS} @ 10V	83.5	Α
I _{DM}	Pulsed Drain Current ¹	520	Α
P _D @T _C =25°C	Total Power Dissipation	125	W
P _D @T _A =25°C	Total Power Dissipation	2	W
E _{AS}	Single Pulse Avalanche Energy ³	211	mJ
T _{STG}	Storage Temperature Range	-55 to 150	$^{\circ}\!\mathbb{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}\!\mathbb{C}$

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	1	°C/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient	62	°C/W



Electrical Characteristics@T_j=25°C(unless otherwise specified)

Parameter	Test Conditions	Min.	Тур.	Max.	Units
Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	100	-	-	V
Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =60A	-	ı	3.88	mΩ
Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_{D}=250uA$	2	-	4	V
Forward Transconductance	V_{DS} =5V, I_{D} =60A	-	100	-	S
Drain-Source Leakage Current	V _{DS} =80V, V _{GS} =0V	-	-	25	uA
Gate-Source Leakage	V _{GS} = <u>+</u> 20V, V _{DS} =0V	-	-	<u>+</u> 0.1	uA
Total Gate Charge⁵	I _D =60A	-	85	136	nC
Gate-Source Charge ⁵	V _{DS} =50V	-	21	-	nC
Gate-Drain ("Miller") Charge⁵	V _{GS} =10V	-	35	-	nC
Turn-on Delay Time ⁵	V _{DS} =50V	-	20	-	ns
Rise Time ⁵	I _D =60A	-	107	-	ns
Turn-off Delay Time ⁵	$R_G=6\Omega$	-	63	-	ns
Fall Time ⁵	V _{GS} =10V	-	200	-	ns
Input Capacitance ⁵	V _{GS} =0V	-	4100	6560	pF
Output Capacitance ⁵	V _{DS} =80V	-	620	-	pF
Reverse Transfer Capacitance ⁵	f=1.0MHz	-	20	-	pF
Gate Resistance	f=1.0MHz	-	2	4	Ω
	Drain-Source Breakdown Voltage Static Drain-Source On-Resistance ² Gate Threshold Voltage Forward Transconductance Drain-Source Leakage Current Gate-Source Leakage Total Gate Charge ⁵ Gate-Drain ("Miller") Charge ⁵ Turn-on Delay Time ⁵ Rise Time ⁵ Turn-off Delay Time ⁵ Fall Time ⁵ Input Capacitance ⁵ Reverse Transfer Capacitance ⁵	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	$\begin{array}{cccccccccccccccccccccccccccccccccccc$

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
V_{SD}	Forward On Voltage ²	I _S =60A, V _{GS} =0V	-	-	1.3	V
t _{rr}	Reverse Recovery Time ⁵	I _S =60A, V _{GS} =0V,	-	65	-	ns
Q _{rr}	Reverse Recovery Charge ⁵	dl/dt=100A/µs	-	100	-	nC

Notes:

- 1. Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Starting T_i =25°C , V_{DD} =50V , L=0.1mH , R_G =25 Ω , V_{GS} =10V
- 4. Package limitation current is 130A.
- 5. Guaranteed by design.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT, AUTOMOTIVE OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

XSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

XSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE

RELIABILITY, FUNCTION OR DESIGN.



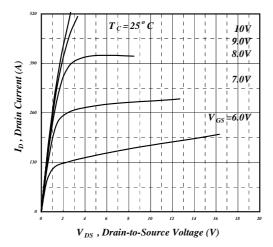


Fig 1. Typical Output Characteristics

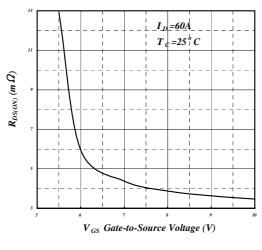


Fig 3. On-Resistance v.s. Gate Voltage

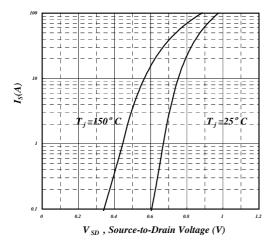


Fig 5. Forward Characteristic of Reverse Diode

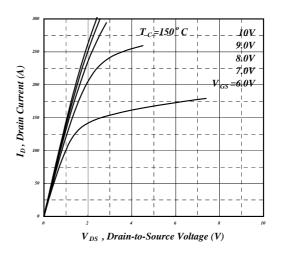


Fig 2. Typical Output Characteristics

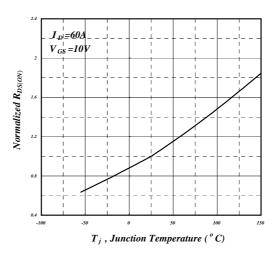


Fig 4. Normalized On-Resistance v.s. Junction Temperature

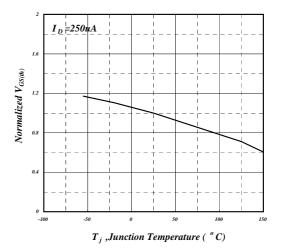


Fig 6. Gate Threshold Voltage v.s.
Junction Temperature



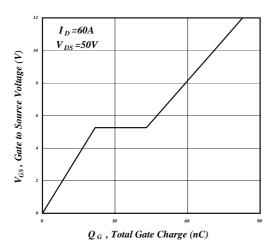


Fig 7. Gate Charge Characteristics

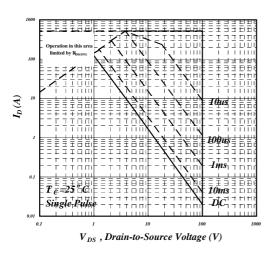


Fig 9. Maximum Safe Operating Area

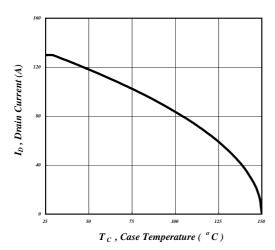


Fig 11. Drain Current v.s. Case Temperature

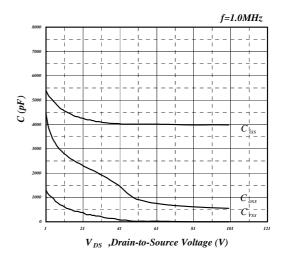


Fig 8. Typical Capacitance Characteristics

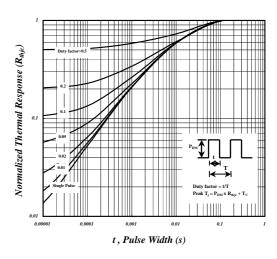


Fig 10. Effective Transient Thermal Impedance

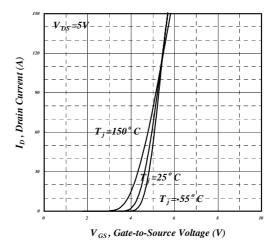


Fig 12. Transfer Characteristics



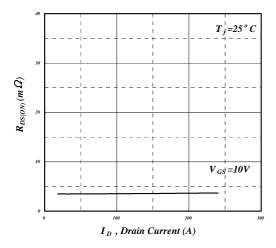


Fig 13. Typ. Drain-Source on State Resistance

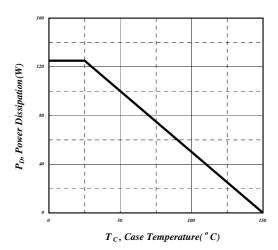
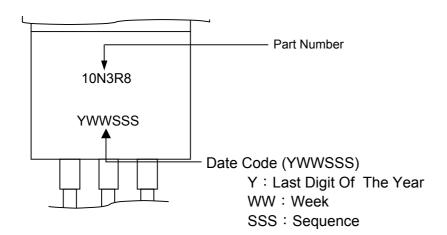


Fig 14. Total Power Dissipation

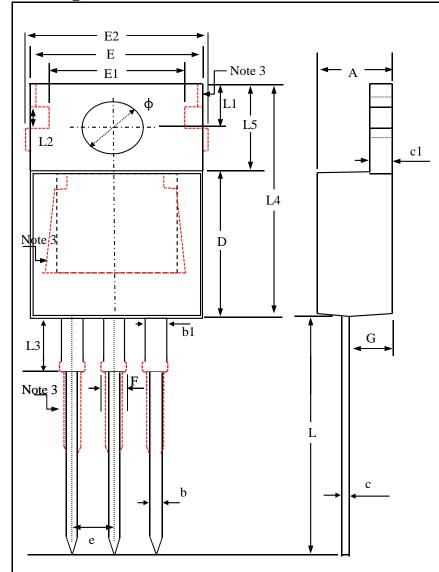


MARKING INFORMATION





Package Outline: TO-220



SYMBOLS	Millimeters			
STABOLS	MIN	NOM	MAX	
A	4.20	4.50	4.80	
b	0.60	0.80	1.00	
b1	1.10	1.38	1.80	
c	0.30	0.48	0.65	
c1	1.10	1.30	1.50	
Е	9.70	10.00	10.40	
E1	7.40	8.30	9.20	
e		2.54 (ref.))	
L	12.70	13.60	14.50	
L1	2.50	2.75	3.00	
L2	1.00	1.40	1.80	
L3	2.60	3.35	4.10	
L4	14.30	15.15	16.00	
L5	6.00	6.40	6.80	
φ	3.40	3.70	4.00	
D	8.30	8.85	9.40	
F	1.20	1.41	1.85	
G	2.20	2.60	3.00	
E2	_	_	11.50	

Note:

- 1.All Dimensions Are in Millimeters.
- 2.Dimension Does Not Include Mold Protrusions.
- 3. Thermal PAD and Pin contour is for reference, it may has little difference by option.



TO-220 FOOTPRINT:

