MOSFET - Power, N-Channel
100 V, 4.2 mΩ, 201 A

NTB004N10G

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX (Note 1)
100 V	4.2 mΩ @ 10 V	201 A

Features
- Low $R_{DS(on)}$
- High Current Capability
- Wide SOA
- These Devices are Pb−Free and are RoHS Compliant

Applications
- Hot Swap in 48 V Systems

MAXIMUM RATINGS (T_J = 25°C Unless otherwise specified)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	100	V
Gate−to−Source Voltage − Continuous			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$	Steady State	T_C = 25°C	I_D	201	A
		T_C = 100°C		142	
Power Dissipation $R_{\theta JC}$	Steady State	T_C = 25°C	P_D	340	W
Pulsed Drain Current	t_p = 10 μs		I_{DM}	3002	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	283	A
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 50 Vdc, V_{GS} = 10 Vdc, $I_{L(pk)}$ = 102 A, L = 0.1 mH, R_G = 25 Ω)			E_{AS}	520	mJ
Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 Seconds			T_L	260	°C

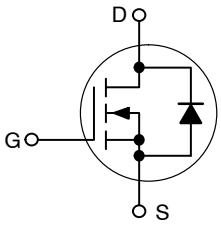
THERMAL RESISTANCE RATINGS

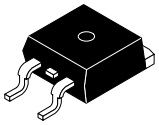
Parameter	Symbol	Max	Unit
Junction−to−Case (Drain) Steady State	$R_{\theta JC}$	0.44	°C/W
Junction−to−Ambient (Note 1)	$R_{\theta JA}$	62.5	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).

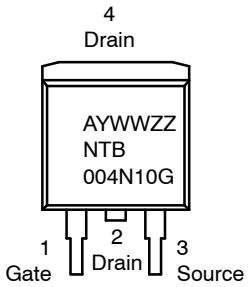
N−Channel





D²PAK
CASE 418AJ
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Site Code
Y = Year Code
WW = Week Code
ZZ = 2−digit Assembly Lot Code
NTB004N10G = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless otherwise specified)

Characteristics	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		100			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				83.2		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 80 V	T_J = 25°C			1.0	μA
			T_J = 150°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 500 μA		2.0	2.8	4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(th)}/T_J$				−10.5		mV/°C
Drain−to−Source On−Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 100 A	T_J = 25°C		3.4	4.2	mΩ
			T_J = 175°C		6.82		mΩ
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 100 A			70		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{iss}	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz			11900		pF
Output Capacitance	C_{oss}				1170		
Reverse Transfer Capacitance	C_{rss}				147		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 50 V, I_D = 100 A			175		nC
Threshold Gate Charge	$Q_{G(TH)}$				32		
Gate−to−Source Charge	Q_{GS}				67.3		
Gate−to−Drain Charge	Q_{GD}				40.8		
Plateau Voltage	V_{GP}				6.0		V
Gate Resistance	R_G	V_{OSC} = 100 mV, V_{GS} = 0 V, f = 1 MHz			0.445		Ω
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DD} = 50 V, I_D = 100 A, R_G = 4.7 Ω			43		ns
Rise Time	t_r				64.5		
Turn−Off Delay Time	$t_{d(off)}$				84.7		
Fall Time	t_f				30		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	I_S = 100 A	T_J = 25°C		0.9	1.2	V
			T_J = 125°C		0.77		
Reverse Recovery Time	t_{rr}	V_{GS} = 0 V, I_S = 100 A, dI_{SD}/dt = 100 A/μs			76.6		ns
Charge Time	t_a				46.4		
Discharge Time	t_b				30.2		
Reverse Recovery Charge	Q_{RR}				157		nC

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

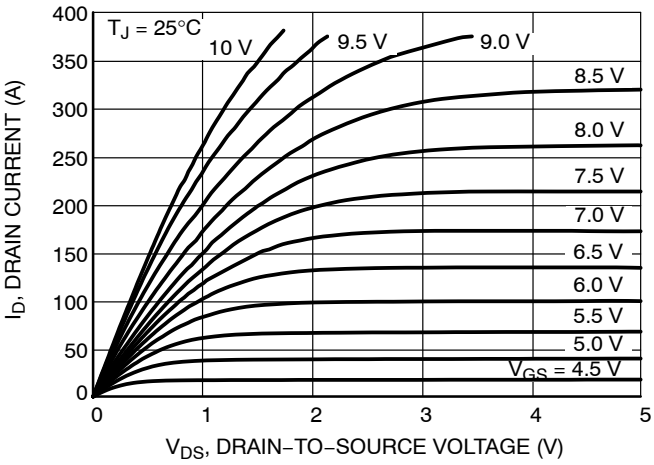


Figure 1. On−Region Characteristics

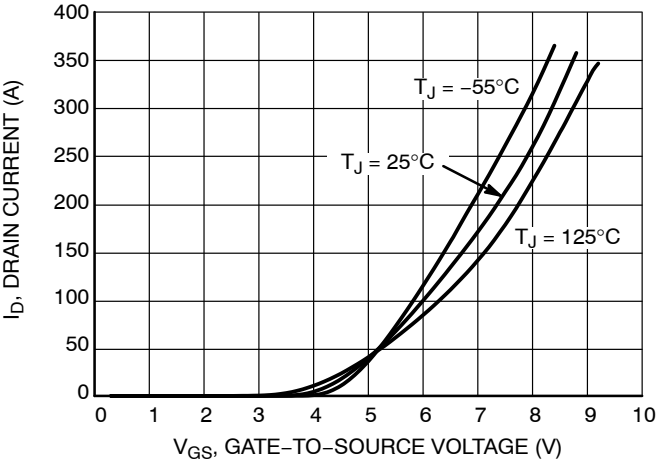


Figure 2. Transfer Characteristics

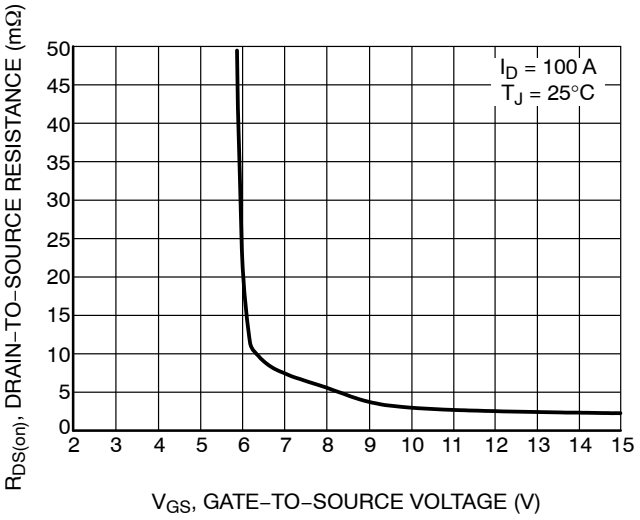


Figure 3. On−Region versus Gate Voltage

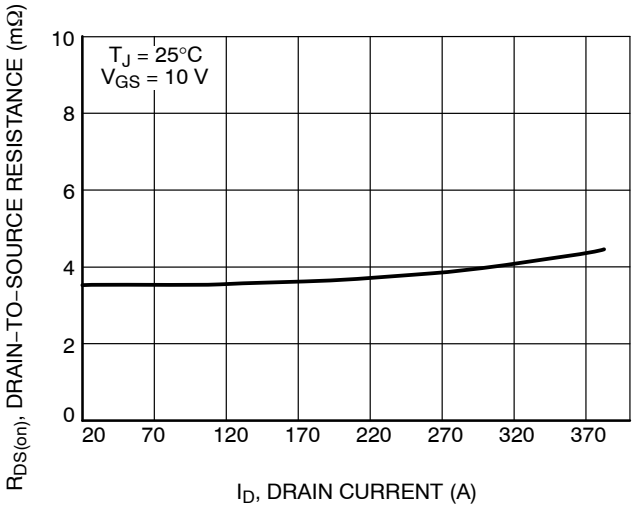


Figure 4. On−Region versus Drain Current and Gate Voltage

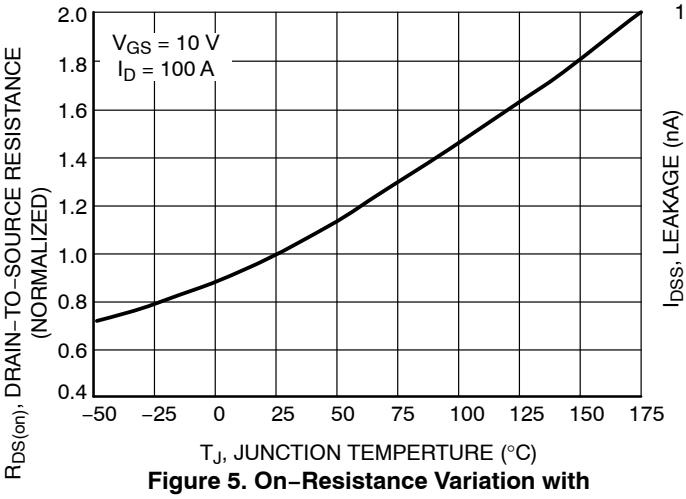


Figure 5. On−Resistance Variation with Temperature

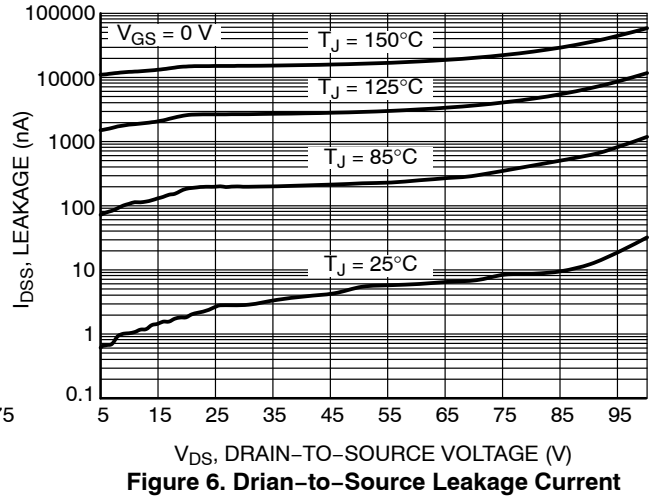


Figure 6. Drian−to−Source Leakage Current versus Voltage

TYPICAL CHARACTERISTICS

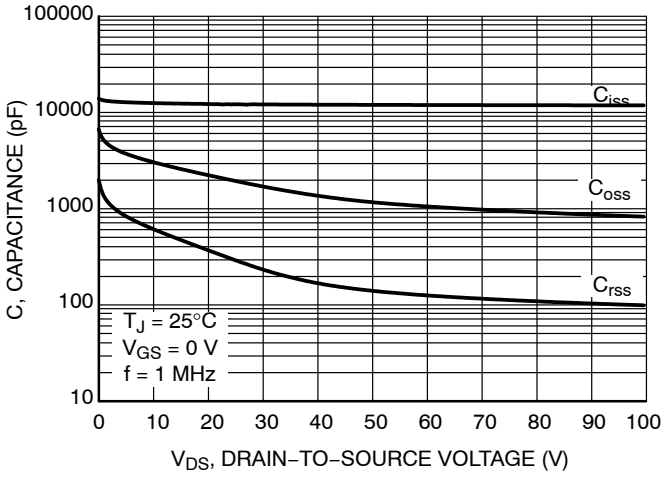


Figure 7. Capacitance Variation

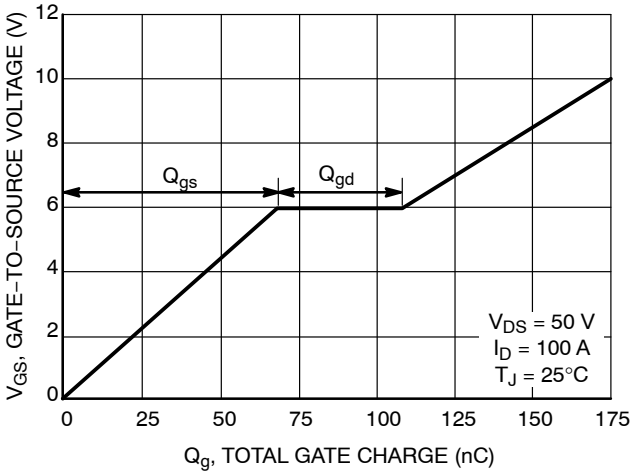


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

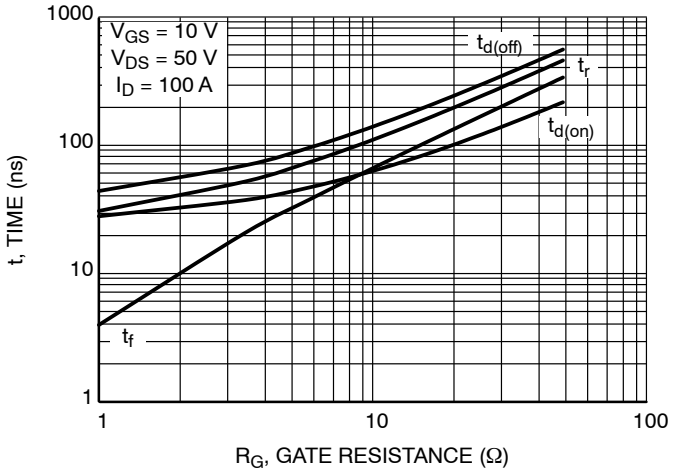


Figure 9. Resistive Switching Time Variation versus Gate Resistance

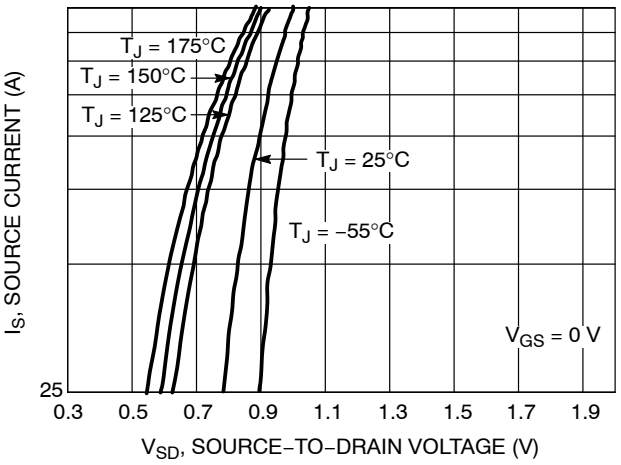


Figure 10. Diode Forward Voltage versus Current

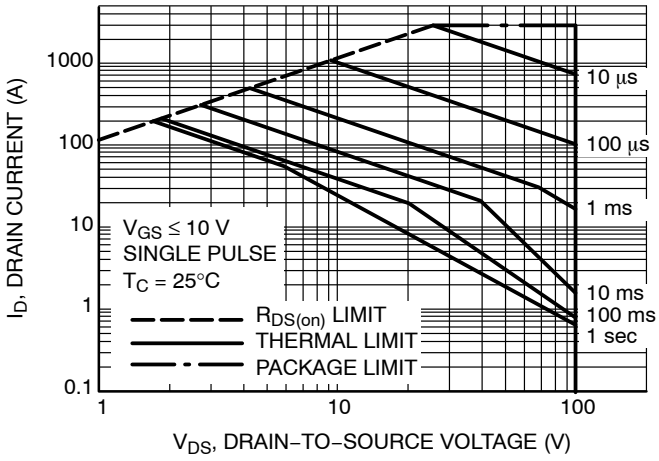


Figure 11. Maximum Rated Forward Biased Safe Opeating Area

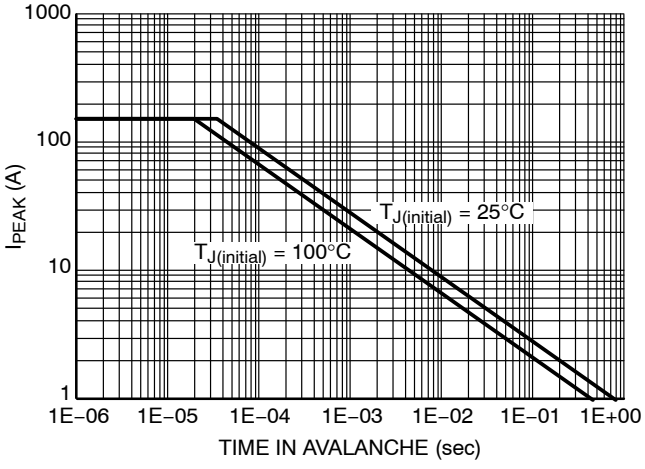


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS

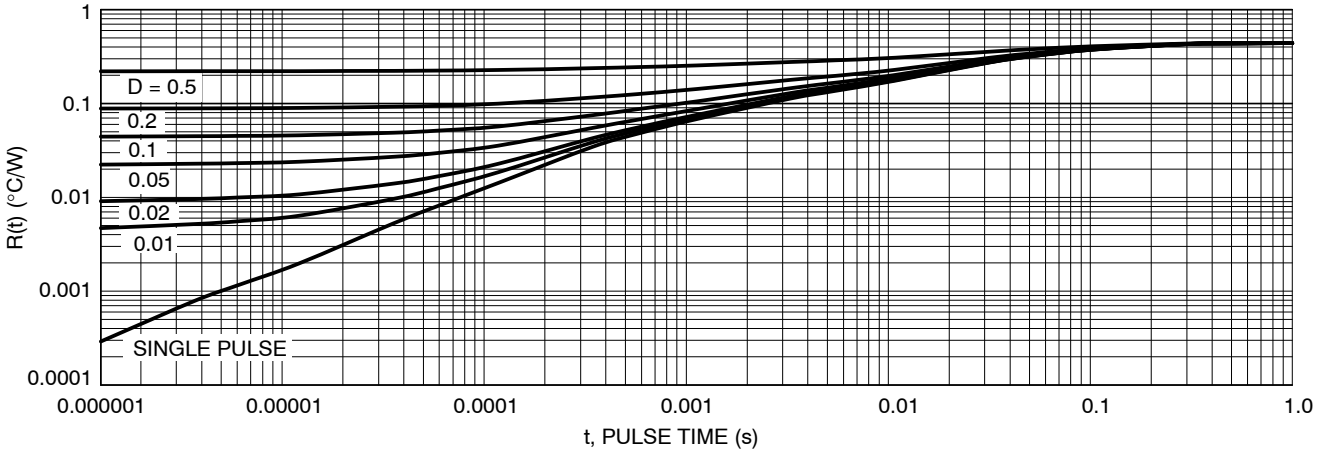


Figure 13. Thermal Response

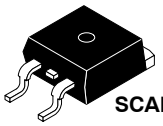
ORDERING INFORMATION

Device	Package	Shipping†
NTB004N10G	D²PAK (Pb−Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

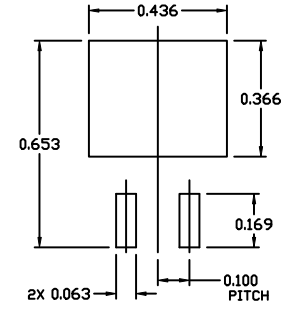
ON Semiconductor®



SCALE 1:1

D²PAK–3 (TO–263, 3–LEAD)
CASE 418AJ
ISSUE F

DATE 11 MAR 2021



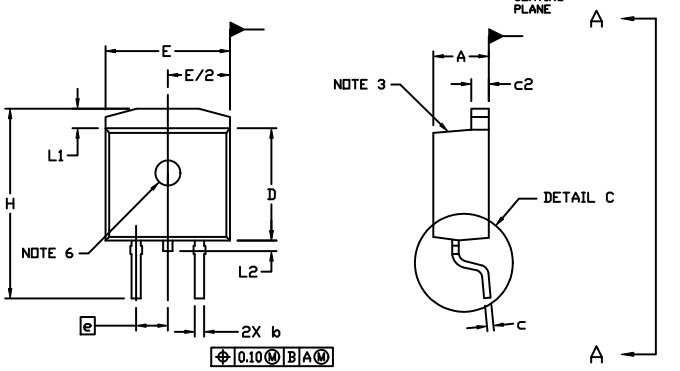
RECOMMENDED
MOUNTING FOOTPRINT

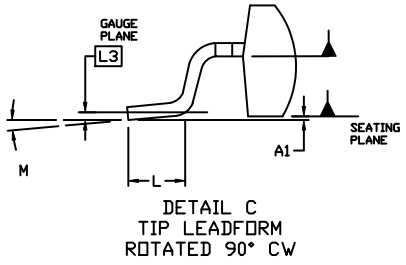
* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

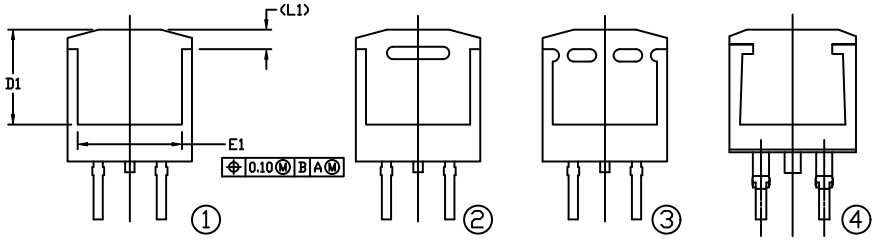
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100 BSC		2.54 BSC	
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010 BSC		0.25 BSC	
M	0°	8°	0°	8°





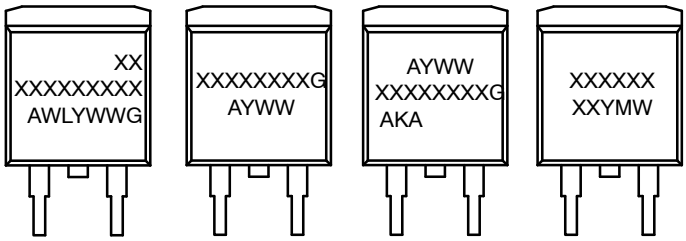
DETAIL C
TIP LEADFORM
ROTATED 90° CW



VIEW A–A

VIEW A–A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



IC | Standard | Rectifier | SSG

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb–Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**D²PAK–3 (TO–263, 3–LEAD)**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales