

## N-Channel Enhancement Mode Power MOSFET

## Description

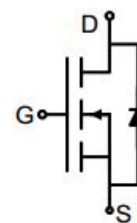
The GT080N10T uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge. It can be used in a wide variety of applications.

## General Features

- $V_{DS}$  100V
- $I_D$  (at  $V_{GS} = 10V$ ) 65A
- $R_{DS(ON)}$  (at  $V_{GS} = 10V$ ) < 8m $\Omega$
- $R_{DS(ON)}$  (at  $V_{GS} = 4.5V$ ) < 9.5m $\Omega$
- 100% Avalanche Tested
- RoHS Compliant

## Application

- Power switch
- DC/DC converters



Schematic diagram



TO-220

## Ordering Information

Device	Package	Marking	Packaging
GT080N10T	TO-220	GT080N10	50pcs/Tube

Absolute Maximum Ratings  $T_C = 25^\circ\text{C}$ , unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Continuous Drain Current	$I_D$	65	A
Pulsed Drain Current (note1)	$I_{DM}$	260	A
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Power Dissipation	$P_D$	100	W
Single pulse avalanche energy (note2)	$E_{AS}$	144	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 To 150	$^\circ\text{C}$

## Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	$R_{thJA}$	50	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{thJC}$	1.25	$^\circ\text{C/W}$

Specifications T <sub>J</sub> = 25°C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	100	--	--	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V	--	--	1	μA
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1.0	1.7	2.5	V
Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A	--	6.4	8.0	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 20A	--	8.0	9.5	
Forward Transconductance	g <sub>FS</sub>	V <sub>GS</sub> = 5V, I <sub>D</sub> = 20A	--	47	--	S
Dynamic Parameters						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 50V, f = 1.0MHz	--	2530	--	pF
Output Capacitance	C <sub>oss</sub>		--	395	--	
Reverse Transfer Capacitance	C <sub>rss</sub>		--	13	--	
Total Gate Charge	Q <sub>g</sub>	V <sub>DD</sub> = 50V, I <sub>D</sub> = 20A, V <sub>GS</sub> = 10V	--	43	--	nC
Gate-Source Charge	Q <sub>gs</sub>		--	7	--	
Gate-Drain Charge	Q <sub>gd</sub>		--	9	--	
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 50V, I <sub>D</sub> = 20A, R <sub>G</sub> = 1.6Ω	--	10	--	ns
Turn-on Rise Time	t <sub>r</sub>		--	8	--	
Turn-off Delay Time	t <sub>d(off)</sub>		--	23	--	
Turn-off Fall Time	t <sub>f</sub>		--	6	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25°C	--	--	65	A
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25°C, I <sub>SD</sub> = 20A, V <sub>GS</sub> = 0V	--	--	1.2	V
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = 20A, V <sub>GS</sub> = 0V di/dt=100A/us	--	75	--	nC
Reverse Recovery Time	T <sub>rr</sub>		--	42	--	ns

## Notes

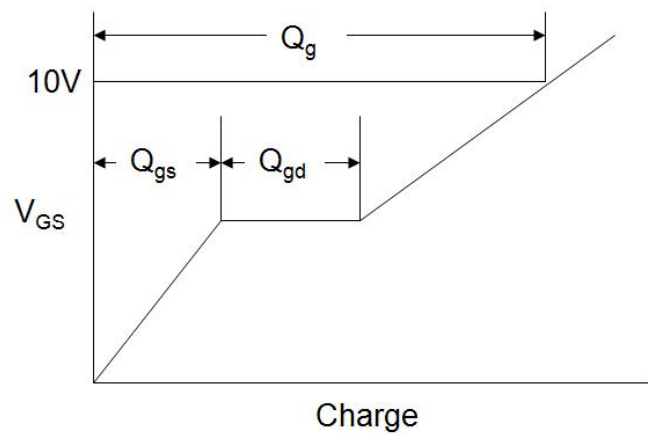
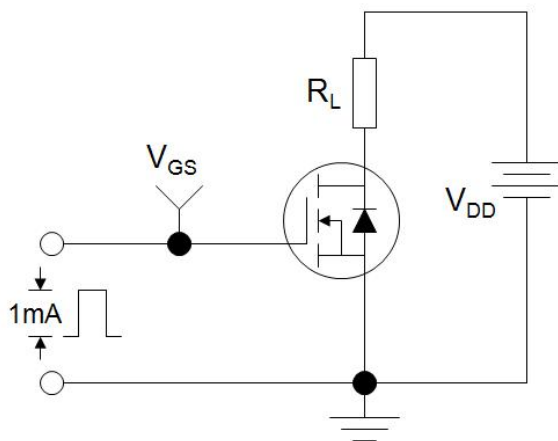
1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. EAS condition :  $T_J = 25^\circ\text{C}, V_{DD} = 50V, V_{GS} = 10V, L = 0.5mH, R_G = 25\Omega$

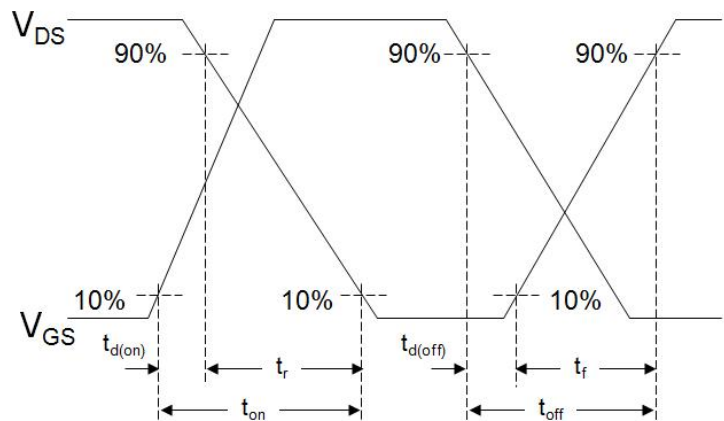
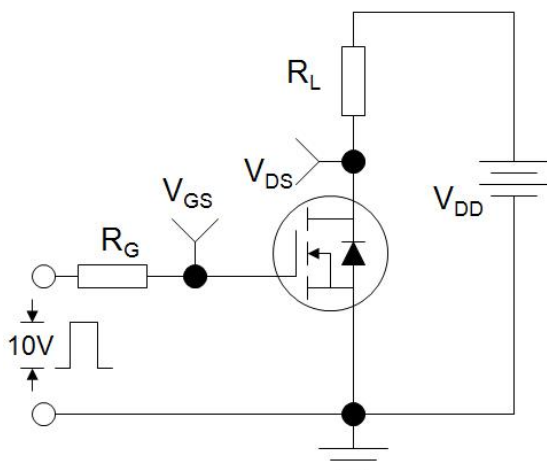
The table shows the minimum avalanche energy, which is 400mJ when the device is tested until failure

3. Identical low side and high side switch with identical  $R_G$

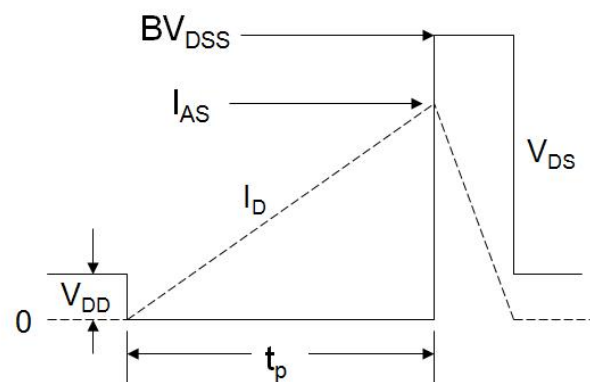
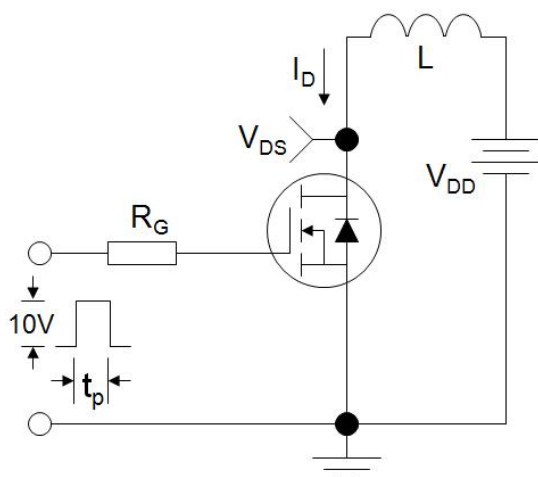
### Gate Charge Test Circuit



### Switch Time Test Circuit

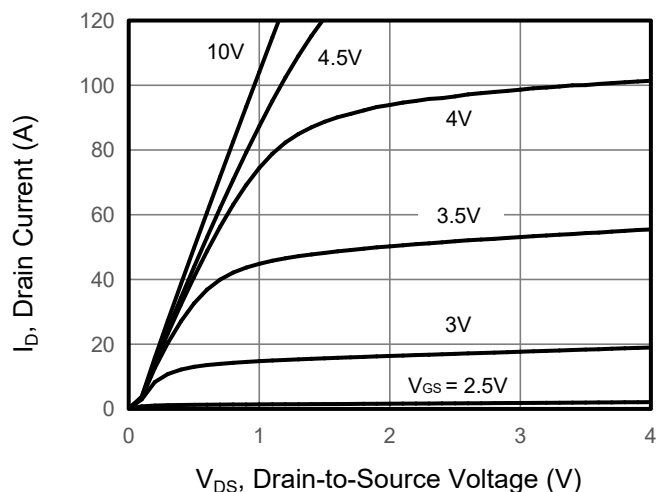


### EAS Test Circuit

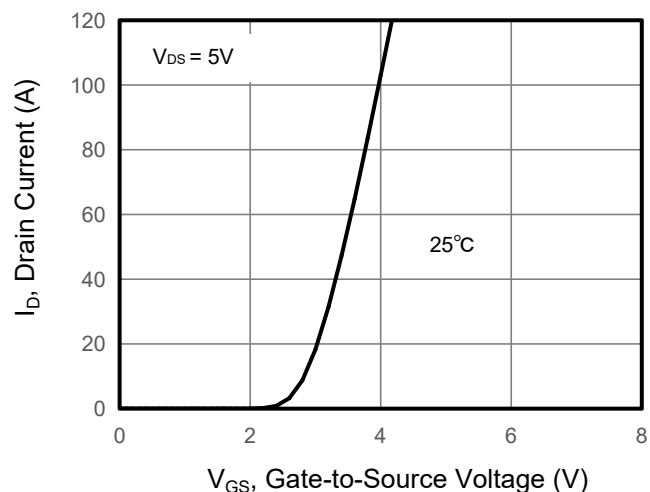


**Typical Characteristics**  $T_J = 25^\circ\text{C}$ , unless otherwise noted

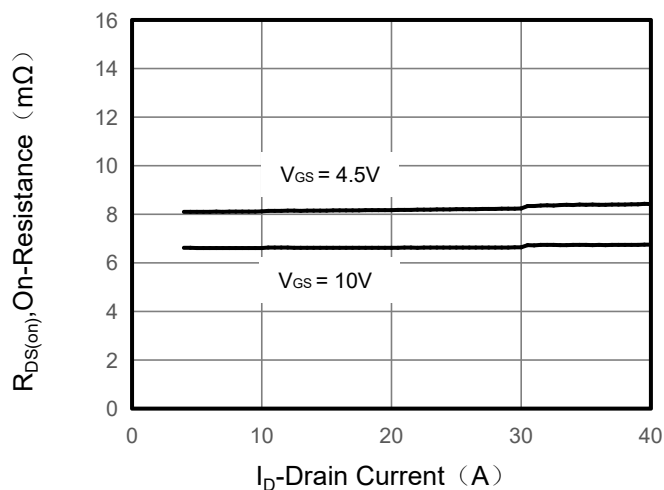
**Figure 1. Output Characteristics**



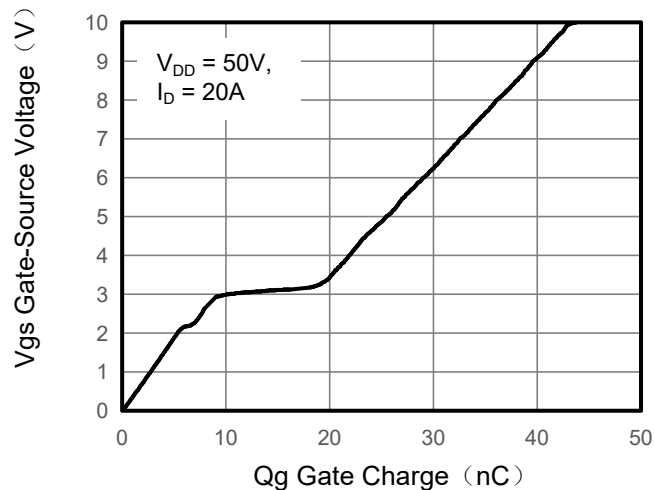
**Figure 2. Transfer Characteristics**



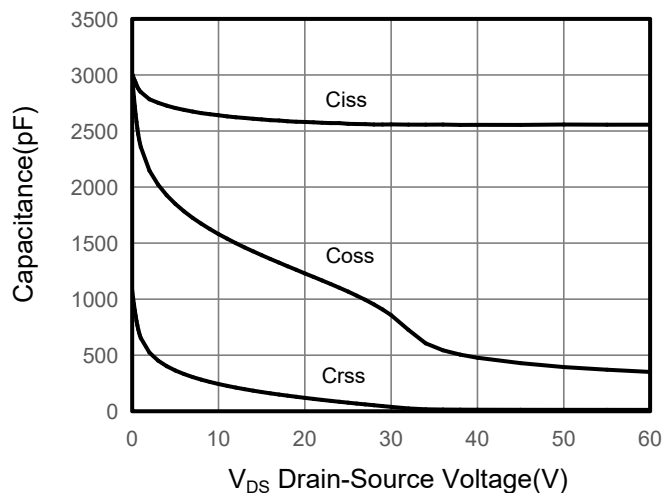
**Figure 3. Drain Source On Resistance**



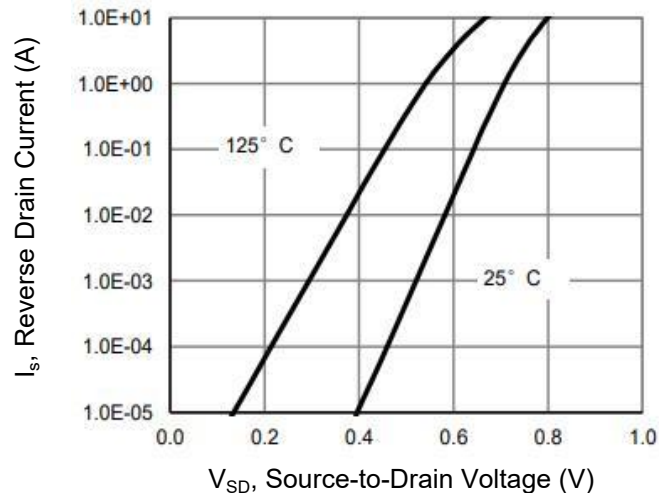
**Figure 4. Gate Charge**



**Figure 5. Capacitance**

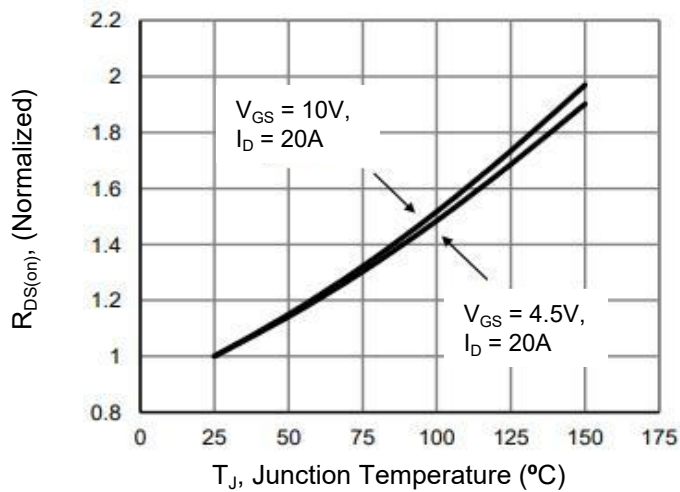


**Figure 6. Source-Drain Diode Forward**

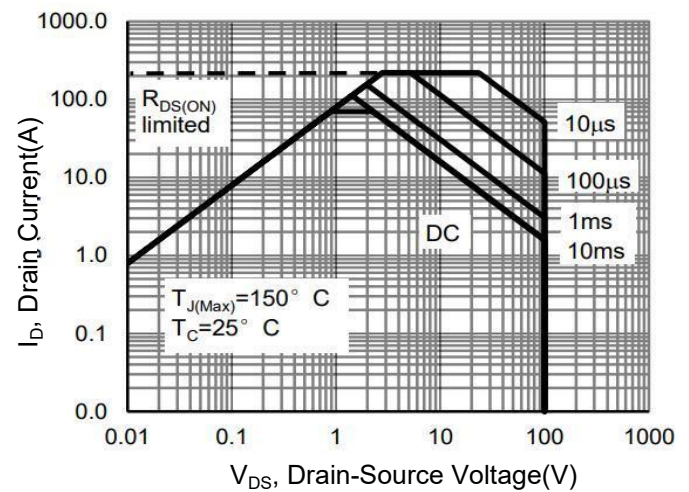


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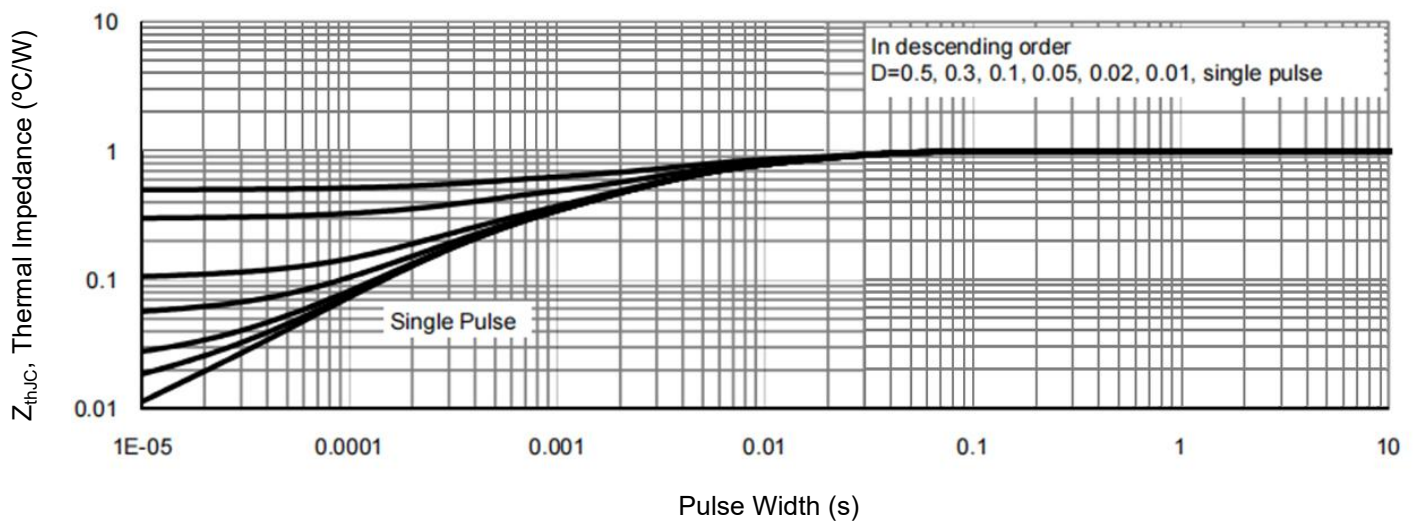
**Figure 7. Drain-Source On-Resistance**



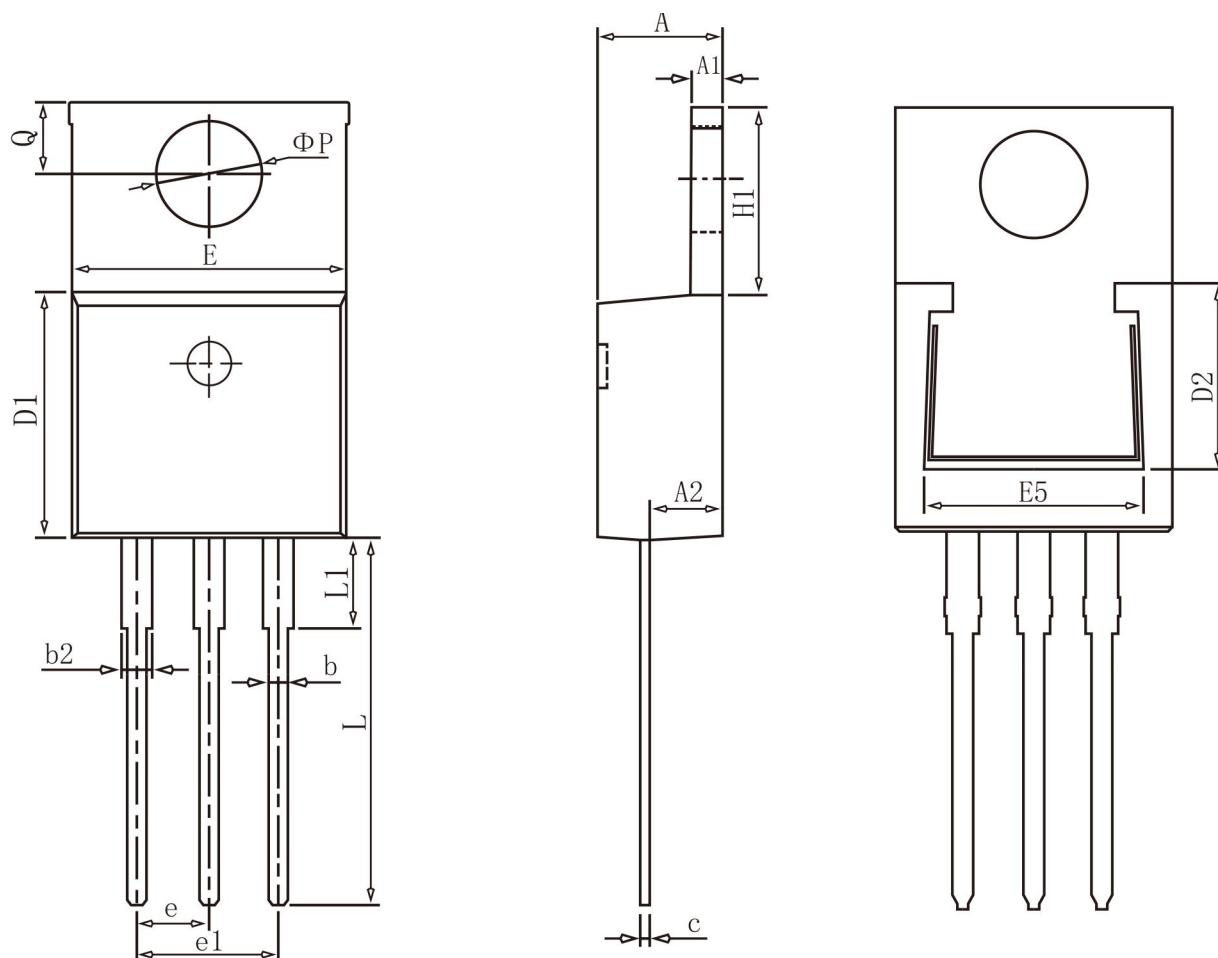
**Figure 8. Safe Operation Area**



**Figure 9. Normalized Maximum Transient Thermal Impedance**



## TO-220 Package Information



### COMMON DIMENSIONS

SYMBOL	mm		
	MIN	NOM	MAX
A	4.37	4.57	4.77
A1	1.22	1.27	1.42
A2	2.49	2.69	2.89
b	0.75	0.81	0.96
b2	1.22	1.27	1.47
c	0.30	0.38	0.48
D1	8.50	8.70	8.90
D2	5.20	—	—
E	9.86	10.16	10.36
E5	7.06	—	—
e	2.54BSC		
e1	5.08BSC		
H1	6.10	6.30	6.50
L	13.10	13.40	13.70
L1	—	3.75	4.10
$\Phi P$	3.70	3.84	3.99
Q	2.54	2.74	2.94