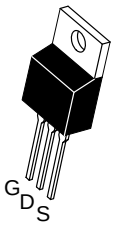
MOSFET – N-Channel, POWERTRENCH®

80 V, 171 A, 3.9 mΩ

FDP039N08B-F102

V_{DSS}	$R_{DS(on)}$ TYP	I_D MAX
80 V	3.16 mΩ @ 10 V	171 A*

*Package limitation current is 120 A.



TO−220
CASE 221A

Description

This N−Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been tailored to minimize the on−state resistance while maintaining superior switching performance.

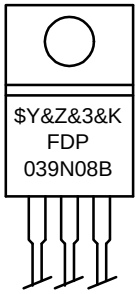
Features

- $R_{DS(on)}$ = 3.16 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 100 A
- Low FOM $R_{DS(on)} * Q_G$
- Low Reverse−Recovery Charge, Q_{rr} = 87.9 nC
- Soft Reverse−Recovery Body Diode
- Enables High Efficiency in Synchronous Rectification
- Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

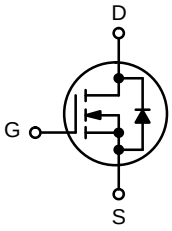
Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies

MARKING DIAGRAM



$Y	= Logo
&Z	= Assembly Plant Code
&3	= 3−Digit Date Code Format
&K	= 2−Digits Lot Run Traceability Code
FDP039N08B	= Device Code



N−Channel MOSFET

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

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ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		FDP039N08B−F102	Unit
V_{DSS}	Drain to Source Voltage		80	V
V_{GSS}	Gate to Source Voltage		±20	V
I_D	Drain Current	− Continuous (T_C = 25°C, Silicon Limited)	171*	A
		− Continuous (T_C = 100°C, Silicon Limited)	121*	
		− Continuous (T_C = 25°C, Package Limited)	120	
I_{DM}	Drain Current	− Pulsed (Note 1)	684	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		547	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		6.0	V/ns
P_D	Power Dissipation	(T_C = 25°C)	214	W
		− Derate Above 25°C	1.43	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +175	°C
T_L	Maximum Lead Temperature for Soldering, 1/8” from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Package limitation current is 120 A.
1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. L = 3 mH, I_{AS} = 19.1 A, starting T_J = 25°C.
3. $I_{SD} \le$ 100 A, di/dt ≤ 200 A/ms, $V_{DD} \le BV_{DSS}$, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDP039N08B−F102	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.7	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	80	−	−	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	−	0.089	−	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 64 V, V_{GS} = 0 V	−	−	1	μA
		V_{DS} = 64 V, T_C = 150°C	−	−	500	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	−	−	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.5	−	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 100 A	−	3.16	3.9	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 100 A	−	180	−	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz	−	7105	9450	pF
C_{oss}	Output Capacitance		−	1110	1475	pF
C_{rss}	Reverse Transfer Capacitance		−	30	−	pF
$C_{oss(er)}$	Energy Related Output Capacitance	V_{DS} = 40 V, V_{GS} = 0 V	−	1656	−	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 40 V, I_D = 100 A, V_{GS} = 10 V (Note 4)	−	102	133	nC
Q_{gs}	Gate to Source Gate Charge		−	39.9	−	nC
Q_{gd}	Gate to Drain “Miller” Charge		−	22	−	nC
$V_{plateau}$	Gate Plateau Voltage		−	5.6	−	V
Q_{sync}	Total Gate Charge Sync.	V_{DS} = 0 V, I_D = 50 A	−	87.4	−	nC
Q_{oss}	Output Charge	V_{DS} = 40 V, V_{GS} = 0 V	−	99.2	−	nC
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 40 V, I_D = 100 A, V_{GS} = 10 V, R_G = 4.7 Ω (Note 4)	−	36	82	ns
t_r	Turn−On Rise Time		−	49	108	ns
$t_{d(off)}$	Turn−Off Delay Time		−	71	152	ns
t_f	Turn−Off Fall Time		−	29	68	ns
ESR	Equivalent Series Resistance (G−S)	f = 1 MHz	−	2.2	−	Ω
DRAIN−SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain to Source Diode Forward Current		−	−	171*	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		−	−	684	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 100 A	−	−	1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, V_{DD} = 40 V, I_{SD} = 100 A, dI_F/dt = 100 A/μs	−	70.1	−	ns
Q_{rr}	Reverse Recovery Charge		−	87.9	−	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*Package limitation current is 120 A.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

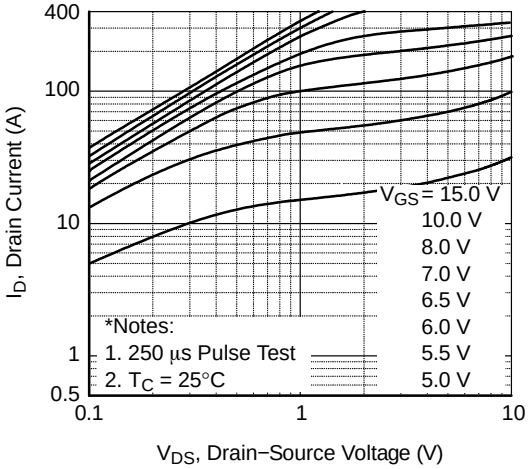

Figure 1. On−Region Characteristics

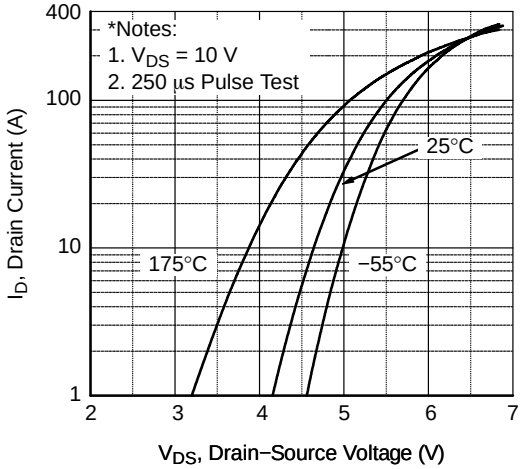

Figure 2. Transfer Characteristics

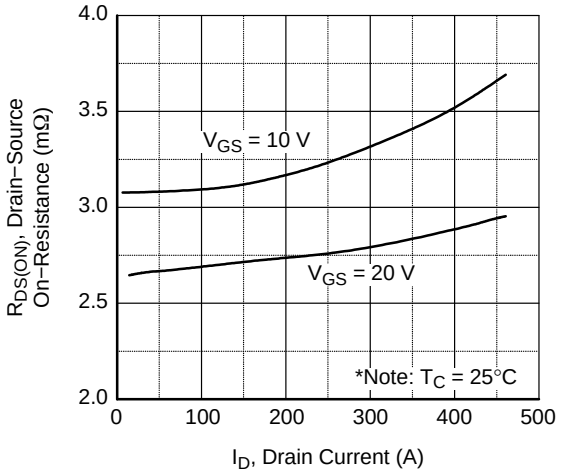

Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

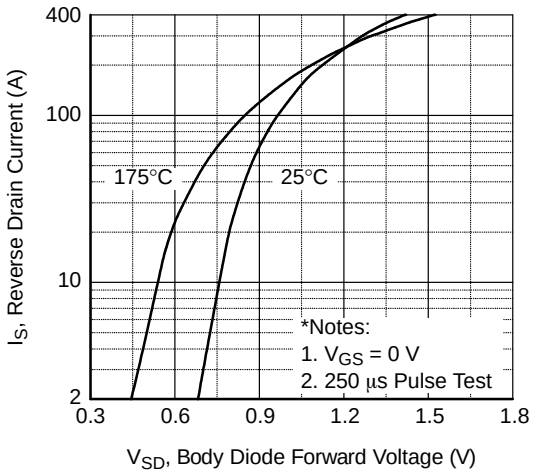

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

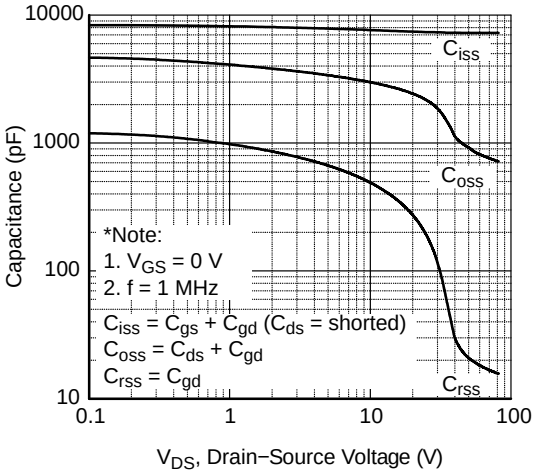

Figure 5. Capacitance Characteristics

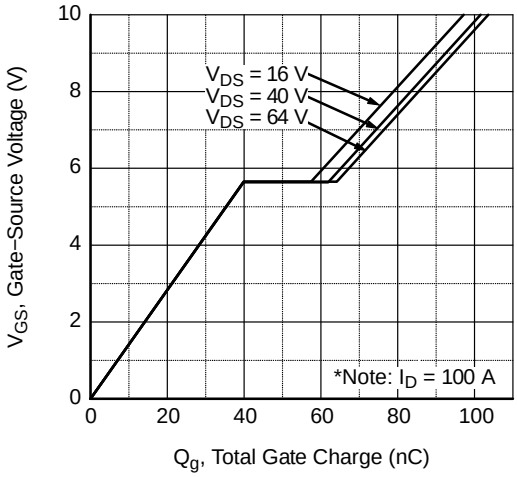

Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

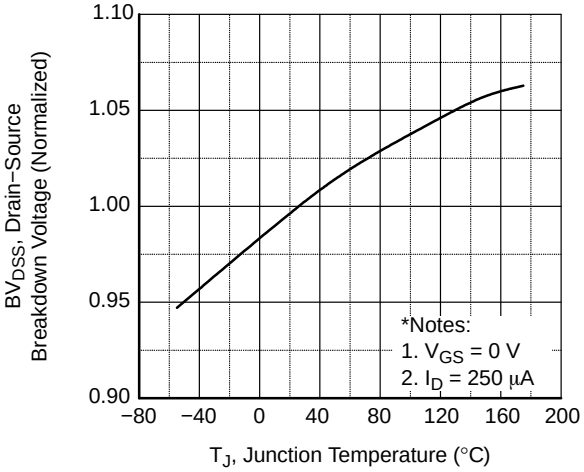

Figure 7. Breakdown Voltage Variation vs. Temperature

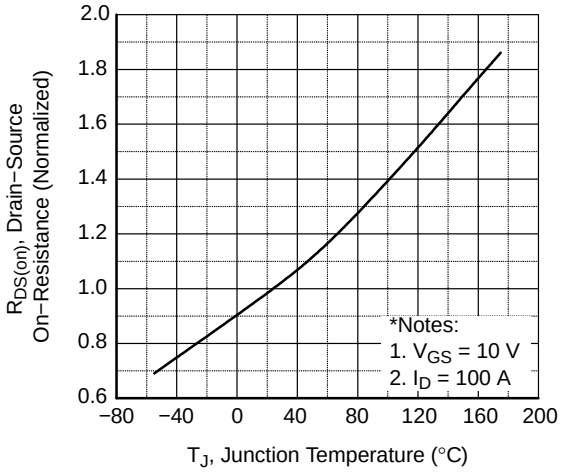

Figure 8. On−Resistance Variation vs. Temperature

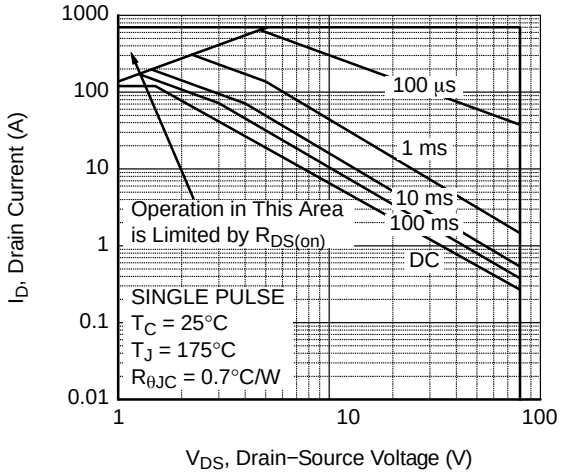

Figure 9. Maximum Safe Operating Area

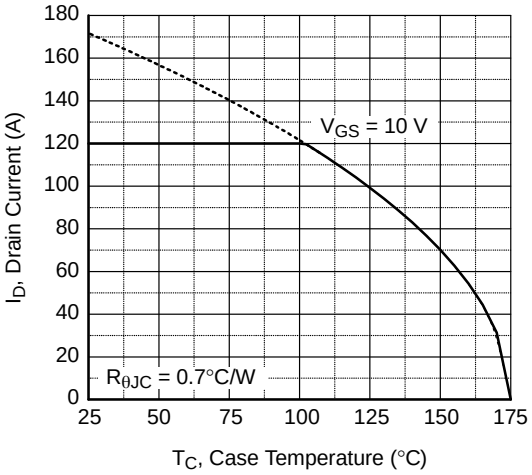

Figure 10. Maximum Drain Current vs. Case Temperature

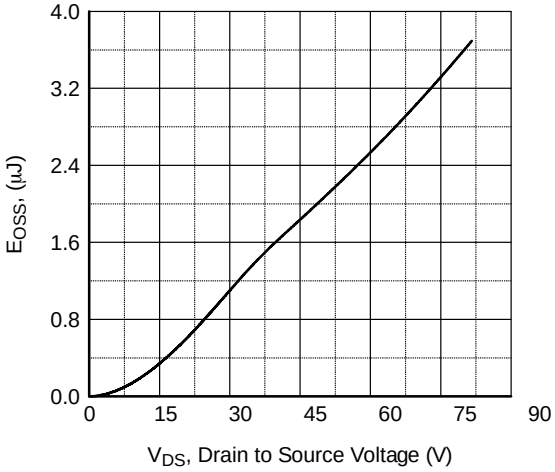

Figure 11. Eoss vs. Drain to Source Voltage

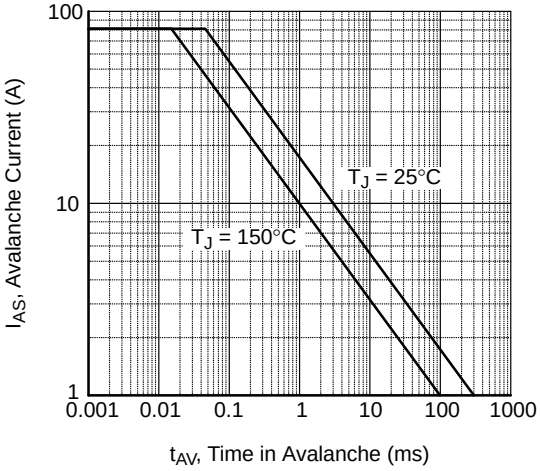

Figure 12. Unclamped Inductive Switching Capability

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

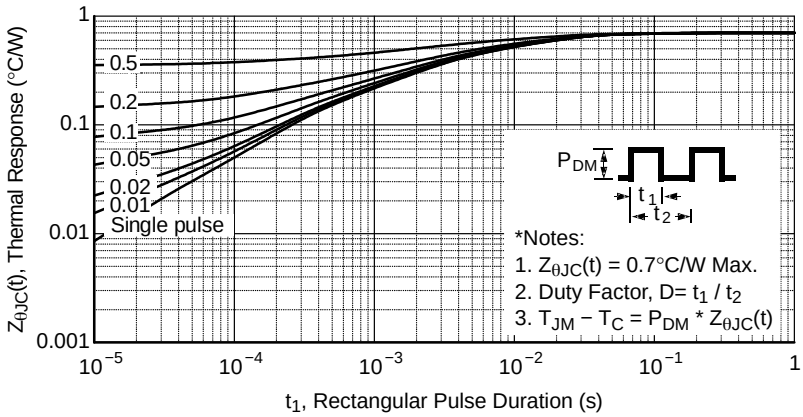

Figure 13. Transient Thermal Response Curve

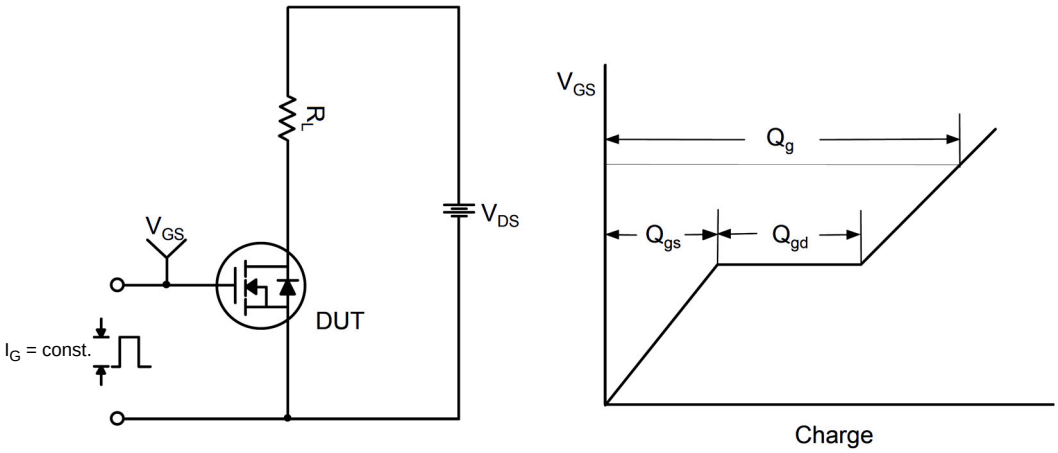

Figure 14. Gate Charge Test Circuit & Waveform

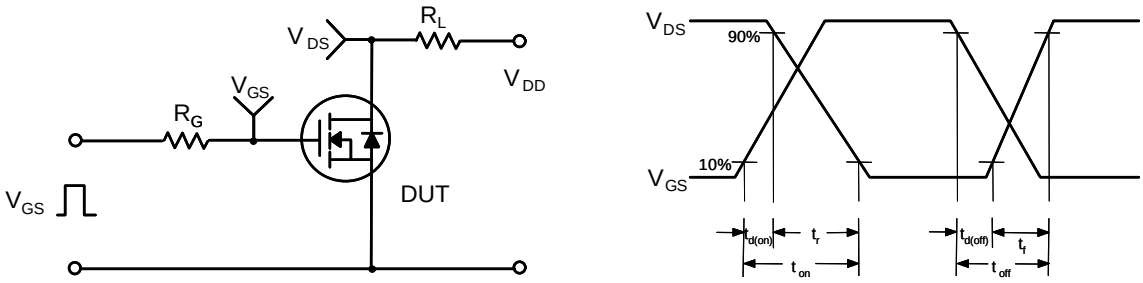

Figure 15. Resistive Switching Test Circuit & Waveforms

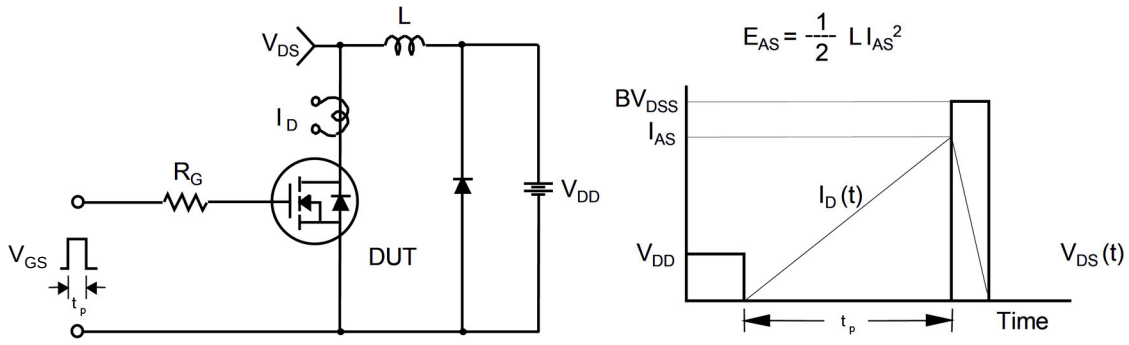

Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

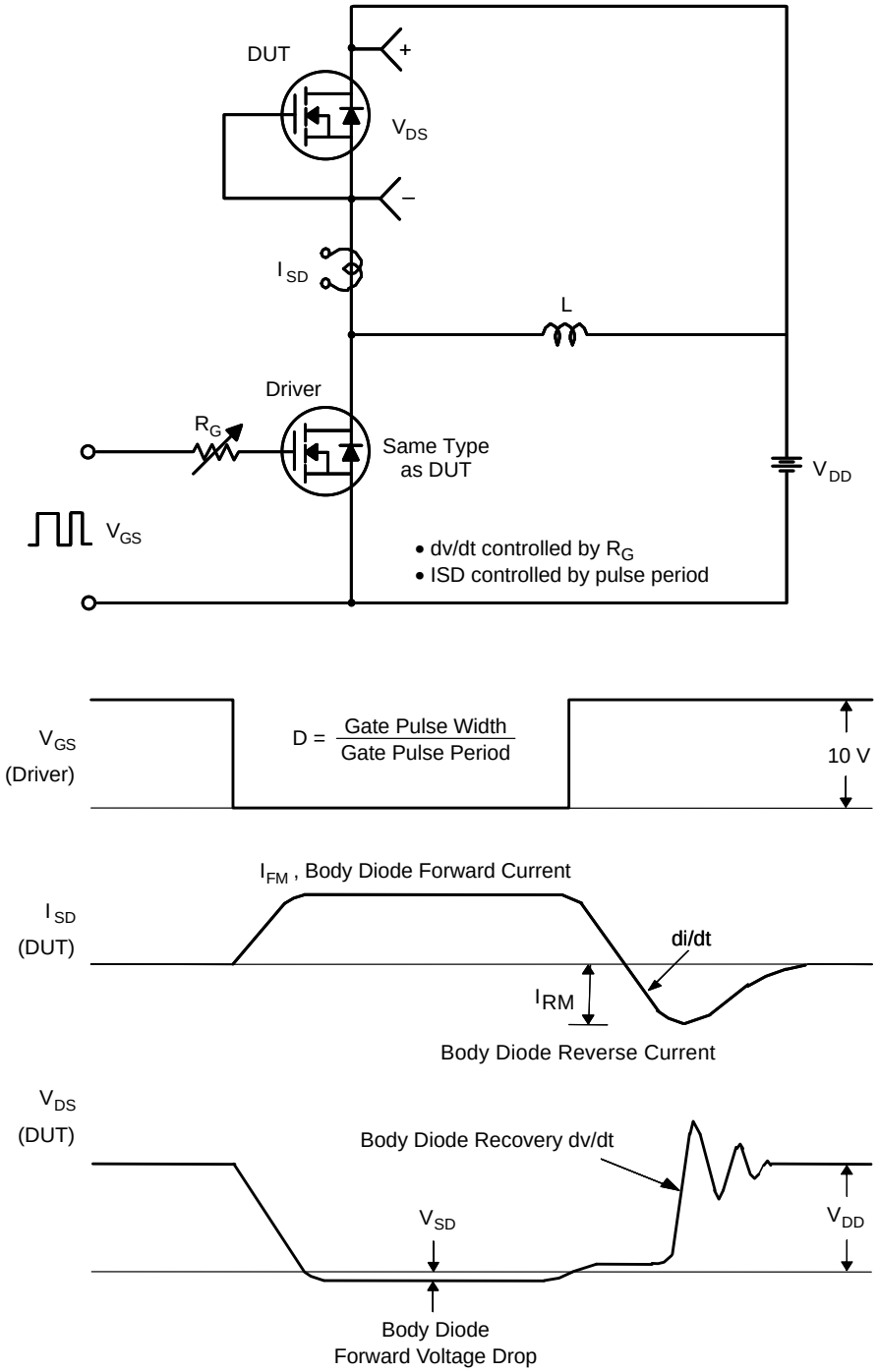

Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

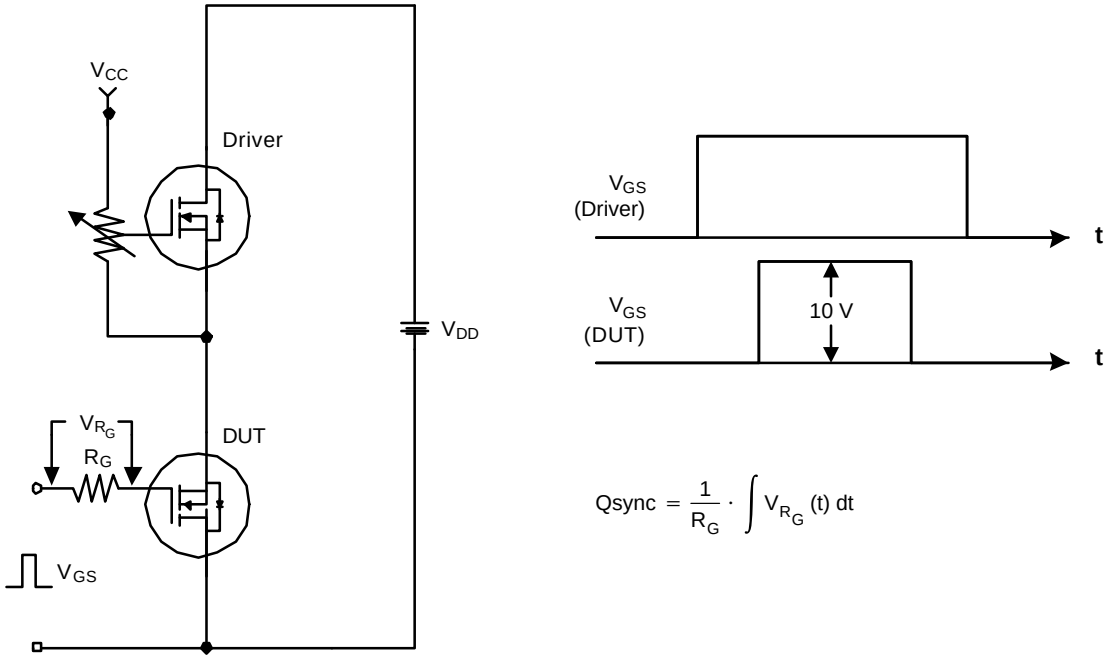

Figure 18. Total Gate Charge Qsync. Test Circuit & Waveforms

ORDERING INFORMATION

Part Number	Device Marking	Package	Shipping
FDP039N08B−F102	FDP039N08B	TO−220	50 Units / Tube

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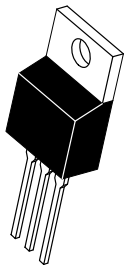
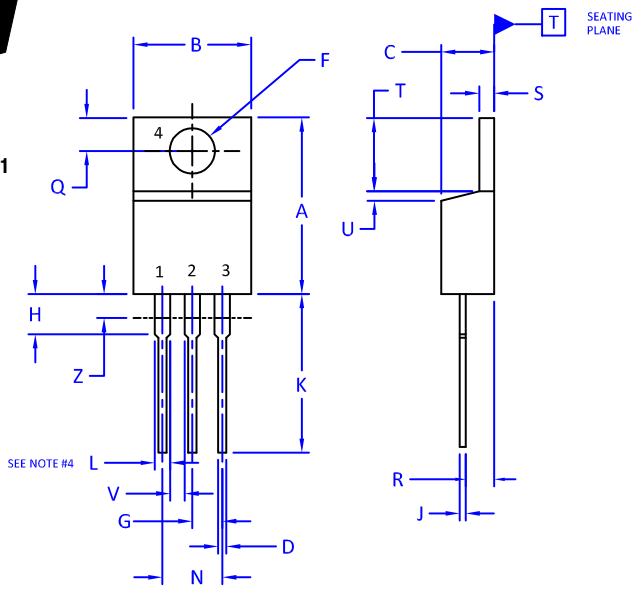
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TO−220
CASE 221A
ISSUE AK

DATE 13 JAN 2022



SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	----	1.15	---
Z	----	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

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