Vishay Siliconix

Automotive N-Channel 80 V (D-S) 175 °C MOSFET



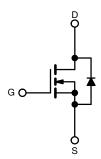
Marking code: Q049

PRODUCT SUMMARY				
V _{DS} (V)	80			
$R_{DS(on)}$ (Ω) at $V_{GS} = 10 \text{ V}$	0.00867			
I _D (A) ^e	72			
Configuration	Single			

FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % Rq and UIS tested
- · Wettable flank terminals
- Low thermal resistance with 0.75 mm profile
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912





N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK® 1212-8SLW
Lead (Pb)-free and halogen-free	SQS180ENW (for detailed order number please see www.vishay.com/doc?79771)

ABSOLUTE MAXIMUM RATING	(1) = 20 0, unloss			
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	80	V
Gate-source voltage		V_{GS}	± 20	V
Continuous drain current ^e	T _C = 25 °C	- I _D	72	
	T _C = 125 °C		41	
Continuous source current (diode conduction) e		I _S	108	А
Pulsed drain current ^{a, e}		I _{DM}	205	
Single pulse avalanche current	L = 0.1 mH	I _{AS}	29	
Single pulse avalanche energy	L = U.1 MH	E _{AS}	42	mJ
Maximum power dissipation ^a	T _C = 25 °C	P_{D}	119	W
	T _C = 125 °C		39	
Operating junction and storage temperature range Soldering recommendations (peak temperature) c		T _J , T _{stg}	-55 to +175	
		<u> </u>	260	°C

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-ambient	PCB mount ^b	R_{thJA}	54	°C/W	
Junction-to-case (drain) ^e		R_{thJC}	1.26		

Notes

- a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 % b. When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- d. As per on JESD51-14
- e. Values based on R_{thJC} and T_C of 25 °C. Actual values achievable will be dependent on the thermal characteristics of the complete system



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static			<u> </u>					
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0$, $I_D = 250 \mu A$		80	-	-	V	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.2	2.7	3.5	V	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA	
		$V_{GS} = 0 V$	V _{DS} = 80 V	-	-	1		
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 80 V, T _J = 125 °C	-	-	50	μΑ	
		V _{GS} = 0 V	V _{DS} = 80 V, T _J = 175 °C	-	-	150		
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	15	-	-	Α	
		V _{GS} = 10 V	I _D = 10 A	-	0.00723	0.00867		
Drain-source on-state resistance a	R _{DS(on)}	V _{GS} = 10 V	I _D = 10 A, T _J = 125 °C	-	-	0.0175	Ω	
		V _{GS} = 10 V	I _D = 10 A, T _J = 175 °C	-	-	0.0227		
Forward transconductance b	9 _{fs}	V _{DS} = 15 V, I _D = 6.5 A		-	45	-	S	
Dynamic ^b					•			
Input capacitance	C _{iss}			-	2208	3092	pF	
Output capacitance	C _{oss}	$V_{GS} = 0 V$	V _{DS} = 25 V, f = 1 MHz	-	372	521		
Reverse transfer capacitance	C _{rss}			-	26	37		
Total gate charge ^c	Qg		$V_{GS} = 10 \text{ V}$ $V_{DS} = 40 \text{ V}, I_D = 4 \text{ A}$	-	37	56	nC	
Gate-source charge c	Q _{gs}	V _{GS} = 10 V		-	9	-		
Gate-drain charge ^c	Q _{gd}			-	8	-		
Gate resistance	R _g	f = 1 MHz		0.4	0.9	1.4	Ω	
Turn-on delay time ^c	t _{d(on)}	$V_{DD} = 40 \text{ V}, \text{ R}_L = 16 \Omega$ $I_D \cong 2.5 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_g = 1 \Omega$		-	15	23		
Rise time ^c	t _r			-	5	9		
Turn-off delay time ^c	t _{d(off)}			-	32	48	ns -	
Fall time ^c	t _f			-	15	23		
Source-Drain Diode Ratings and Charac	teristic ^b		<u> </u>					
Pulsed current ^a	I _{SM}			-	-	350	Α	
Forward voltage	V _{SD}	I _F = 10 A, V _{GS} = 0 V		-	0.82	1.1	V	
Body diode reverse recovery time	t _{rr}	V_{DD} = 64 V, I _F = 3.5 A, di/dt = 100 A/μs, R = 10 Ω, L = 0.3 mH, pulse width = 2 μs		-	35	70	ns	
Body diode reverse recovery charge	Q_{rr}			-	52	104	nC	
Reverse recovery fall time	ta			-	28	-		
Reverse recovery rise time	t _b			-	7	-	ns	
Body diode peak reverse recovery current	I _{RM(REC)}			-	-2.4	-	Α	

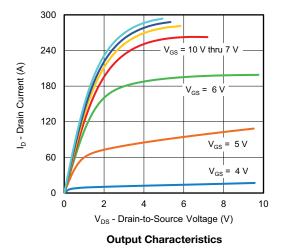
Notes

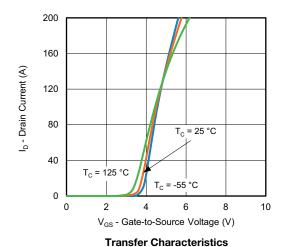
- a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

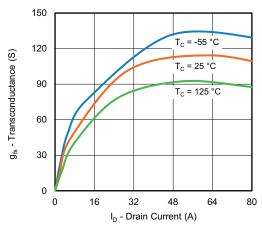
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

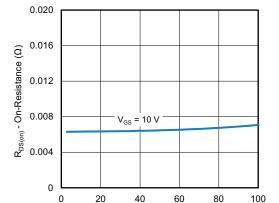


TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

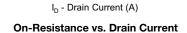


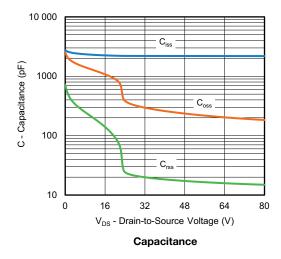


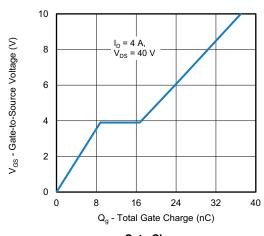




Transconductance

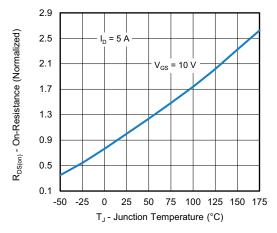




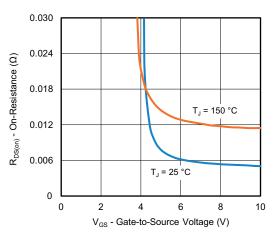




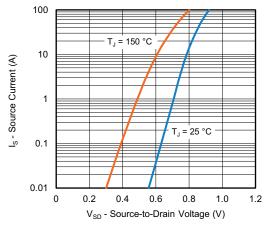
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



On-Resistance vs. Junction Temperature



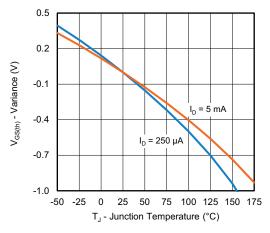
On-Resistance vs. Gate-to-Source Voltage



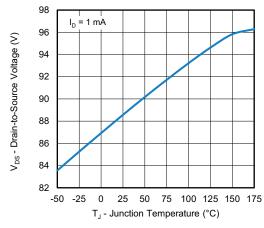
Source Drain Diode Forward Voltage

Note

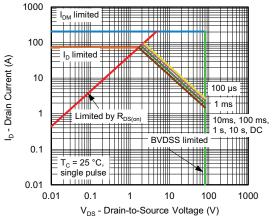
a. V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified



Threshold Voltage



Drain Source Breakdown vs. Junction Temperature

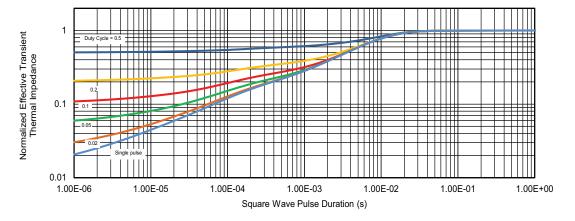


Safe Operating Area

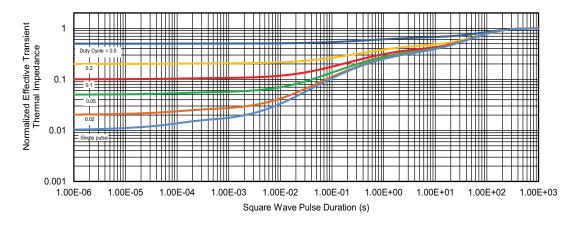
For technical questions, contact: automostechsu



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63169.



RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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