



STL75N8LF6

N-channel 80 V, 5.6 mΩ, 18 A, PowerFLAT™ 5x6
STripFET™ VI DeepGATE™ Power MOSFET

Features

Order code	V _{DSS}	R _{DS(on)} max	I _D
STL75N8LF6	80 V	< 7.4 mΩ	18 A ⁽¹⁾

1. The value is rated according R_{thj-pcb}

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- High avalanche ruggedness
- Low gate drive power losses

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R_{DS(on)} in all packages.

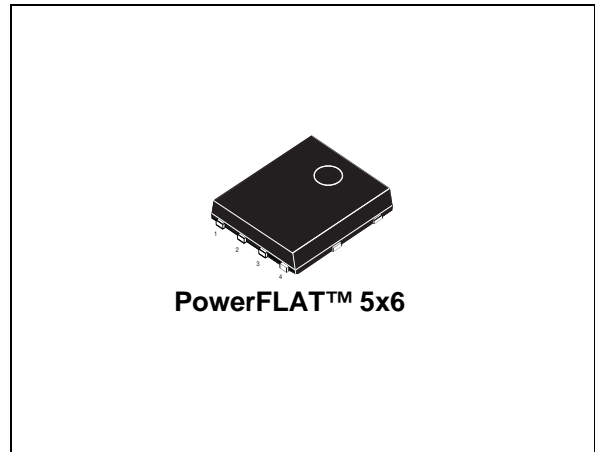


Figure 1. Internal schematic diagram

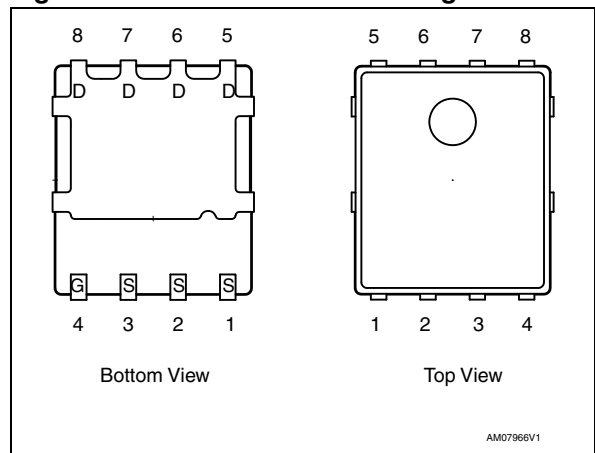


Table 1. Device summary

Order code	Marking	Package	Packaging
STL75N8LF6	75N8LF6	PowerFLAT™ 5x6	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	+20 / -16	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}$	75	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ °C}$	50	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ °C}$	18	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb}=100\text{ °C}$	11	A
$I_{DM}^{(3)}$	Drain current (pulsed)	72	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ °C}$	80	W
$P_{TOT}^{(3)}$	Total dissipation at $T_{pcb} = 25\text{ °C}$	4	W
	Derating factor	0.03	W/°C
T_J	Operating junction temperature	-55 to 175	°C
T_{stg}	Storage temperature		

1. The value is rated according to $R_{thj-case}$
2. The value is rated according to $R_{thj-pcb}$
3. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (drain, steady state)	1.56	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-ambient	31.3	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{ sec}$

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current, (pulse width limited by $T_J\text{ Max}$)	18	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = I_{AV}$, $V_{DD} = 50\text{ V}$)	670	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 250\text{ }\mu\text{A}$	80			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 80\text{ V}$, $V_{DS} = 80\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = +20 / -16\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 9\text{ A}$ $V_{GS} = 5\text{ V}$, $I_D = 9\text{ A}$		5.6 6	7.4 8.2	$\text{m}\Omega$ $\text{m}\Omega$

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	6895	-	pF
C_{oss}	Output capacitance			516		pF
C_{rss}	Reverse transfer capacitance			207		pF
Q_g	Total gate charge	$V_{DD} = 40\text{ V}$, $I_D = 18\text{ A}$	-	51	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 4.5\text{ V}$		14		nC
Q_{gd}	Gate-drain charge	(see Figure 14)		17		nC
R_G	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 Test signal level = 20 mV open drain	-	1.52	-	Ω

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 40\text{ V}$, $I_D = 9\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13)	-	17	-	ns
t_r	Rise time			14		ns
$t_{d(off)}$	Turn-off delay time			112		ns
t_f	Fall time			26		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		18	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				72	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 18\text{ A}$, $V_{GS} = 0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 18\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 63\text{ V}$	-	37		ns
Q_{rr}	Reverse recovery charge			49		nC
I_{RRM}	Reverse recovery current			2.7		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

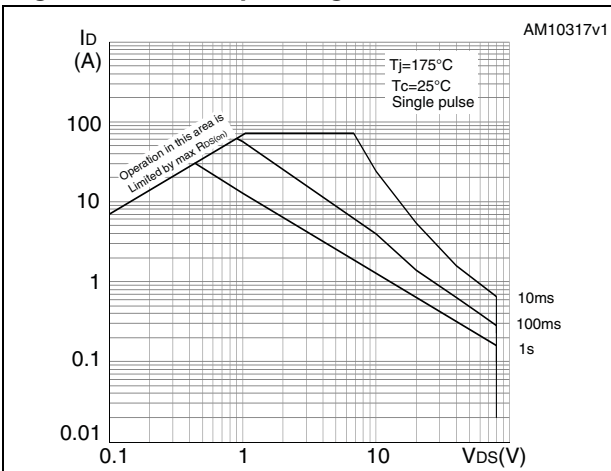


Figure 3. Thermal impedance

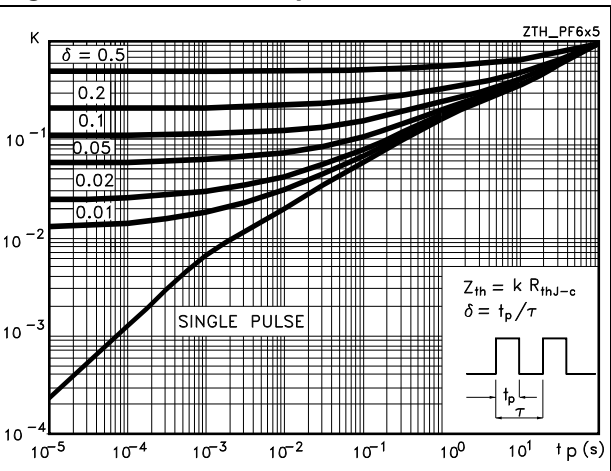


Figure 4. Output characteristics

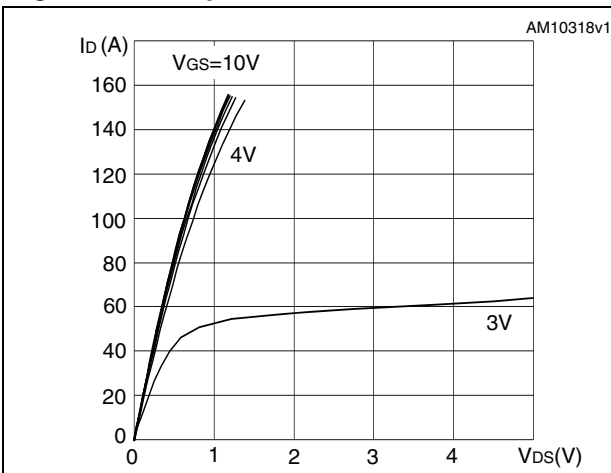


Figure 5. Transfer characteristics

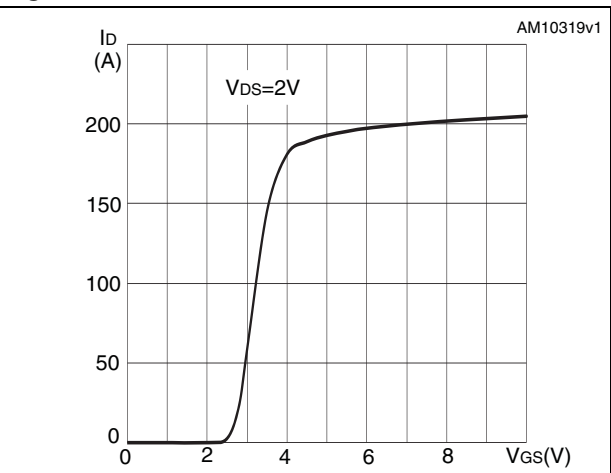


Figure 6. Normalized $B_{V_{DS}}$ vs temperature

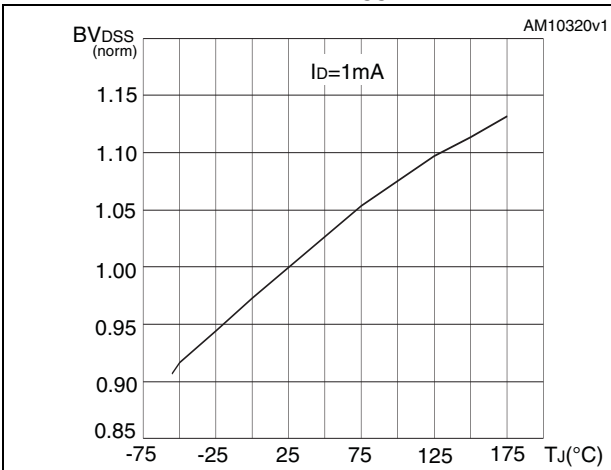


Figure 7. Static drain-source on resistance

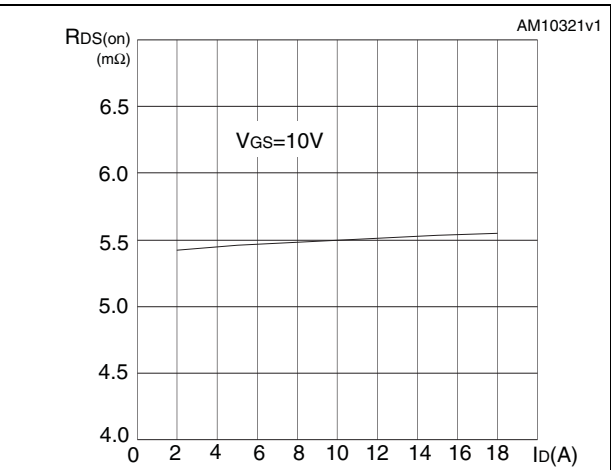


Figure 8. Gate charge vs gate-source voltage

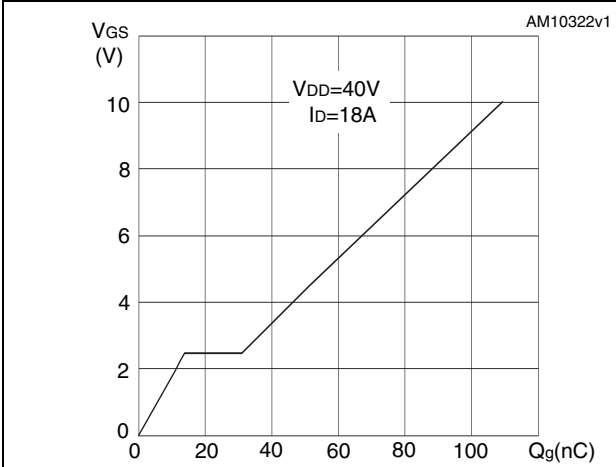


Figure 9. Capacitance variations

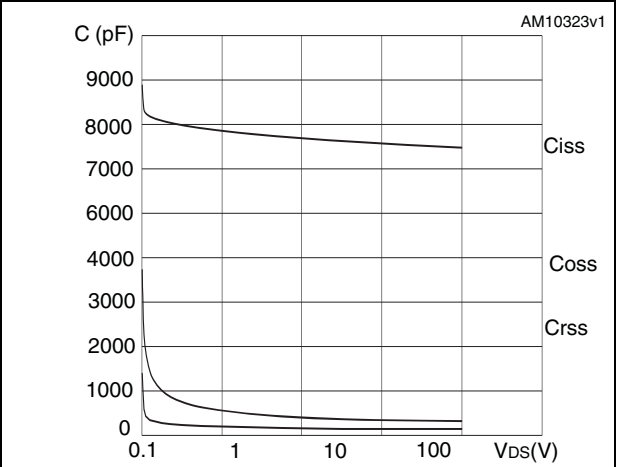


Figure 10. Normalized gate threshold voltage vs temperature

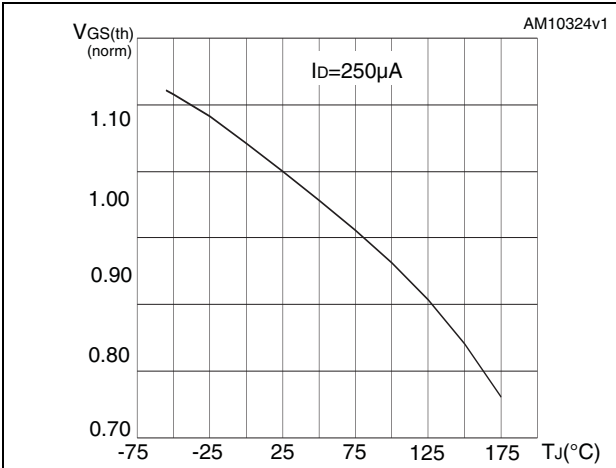


Figure 11. Normalized on resistance vs temperature

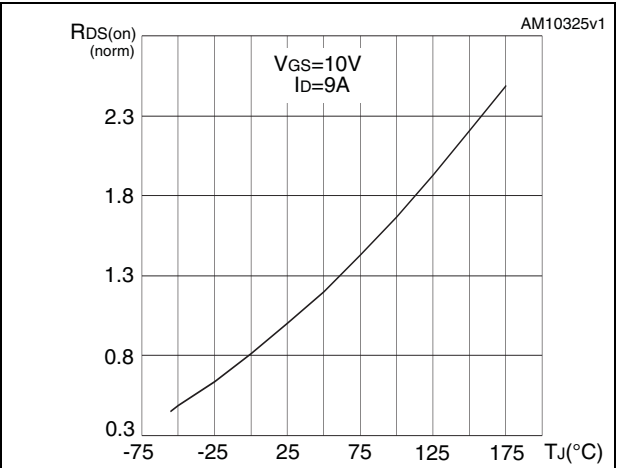
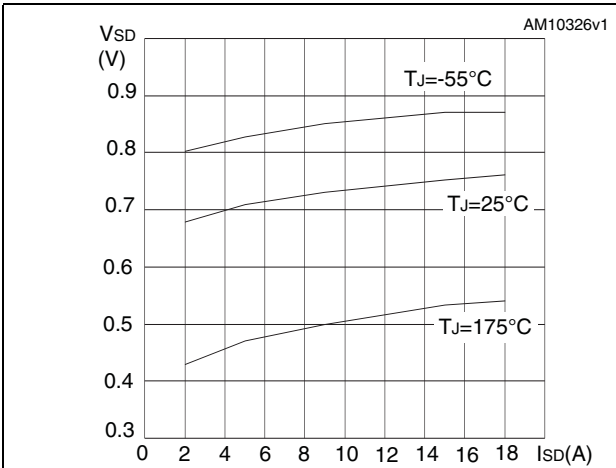


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

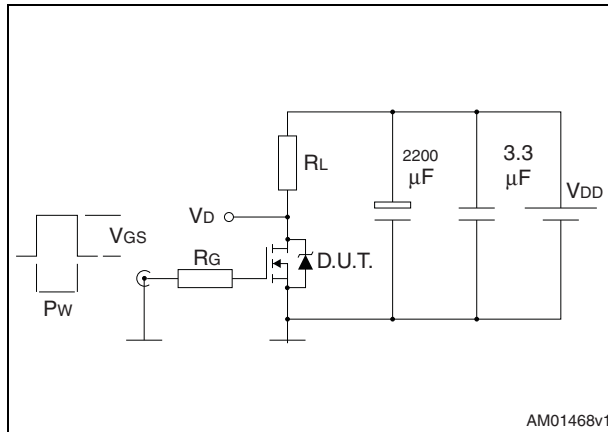


Figure 14. Gate charge test circuit

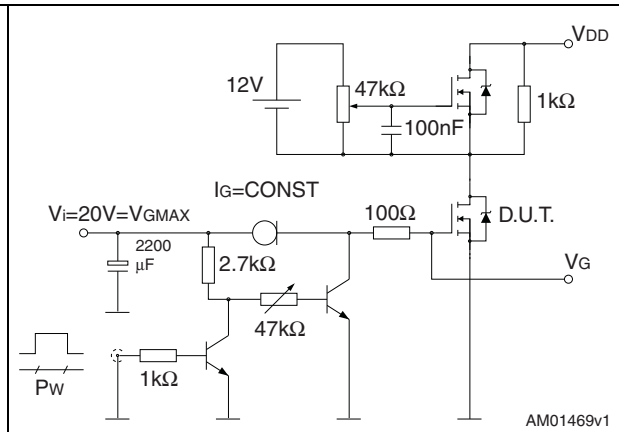


Figure 15. Test circuit for inductive load switching and diode recovery times

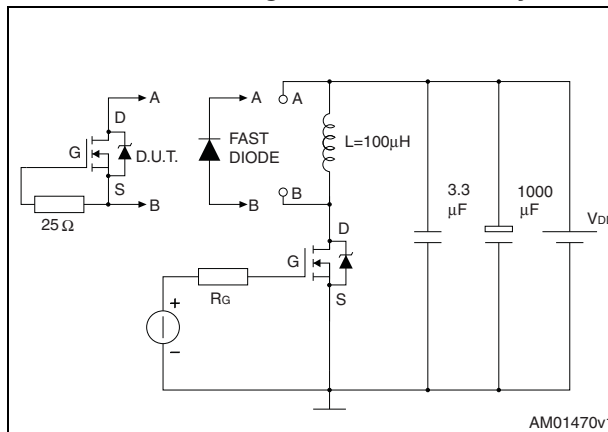


Figure 16. Unclamped inductive load test circuit

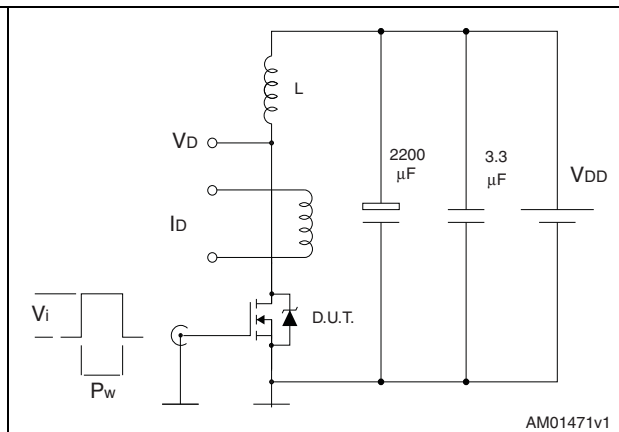


Figure 17. Unclamped inductive waveform

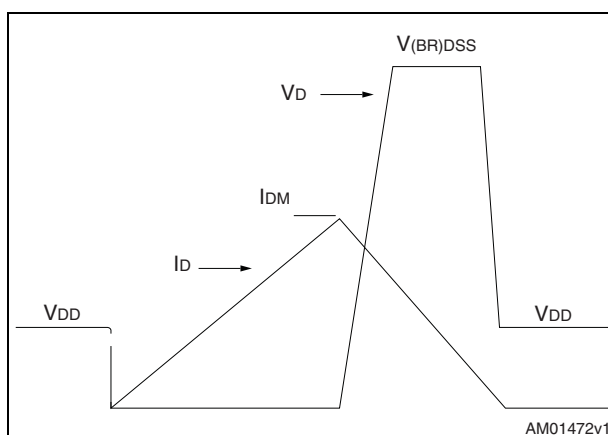
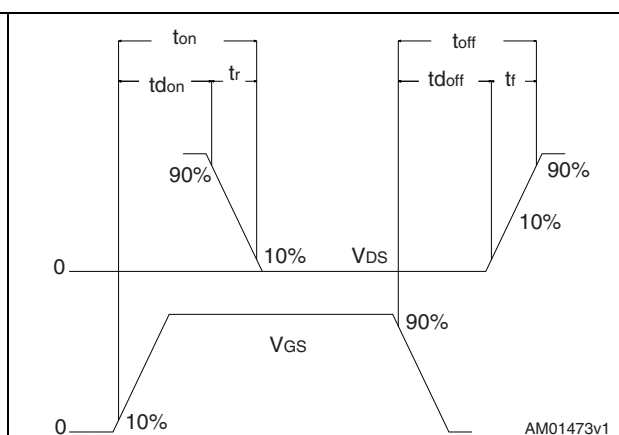


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. PowerFLAT™ 5x6 type C-B mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.83	0.93
A1	0	0.02	0.05
A3		0.20	
b	0.35	0.40	0.47
D		5.00	
D1		4.75	
D2	4.15	4.20	4.25
E		6.00	
E1		5.75	
E2	3.43	3.48	3.53
E4	2.58	2.63	2.68
e		1.27	
L	0.70	0.80	0.90

Figure 19. PowerFLAT™ 5x6 type C-B drawing

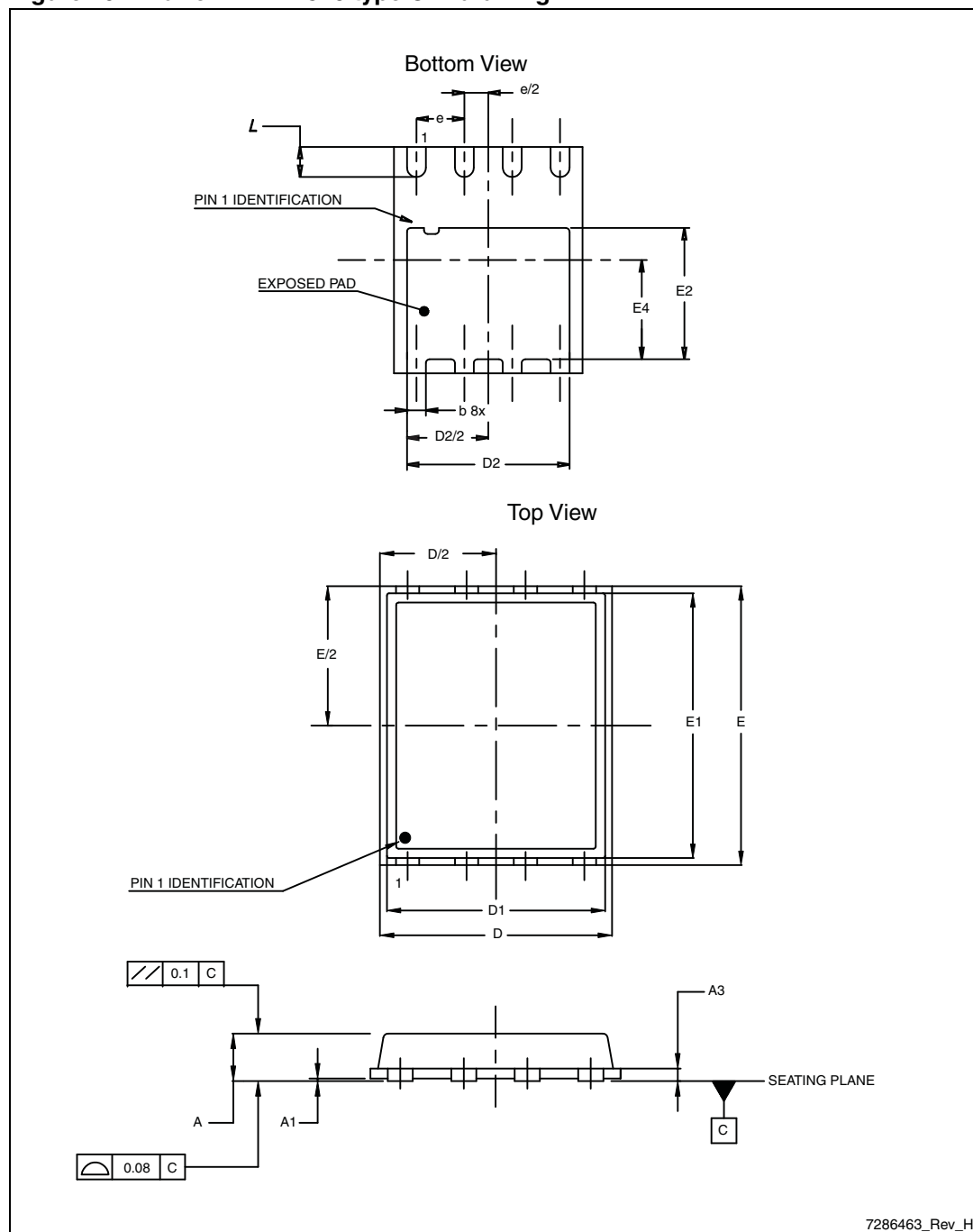


Table 10. PowerFLAT™ 5x6 type S-C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
e1		0.65	
L	0.715		1.015
K	1.05		1.35

Figure 20. PowerFLAT™ 5x6 type S-C mechanical data

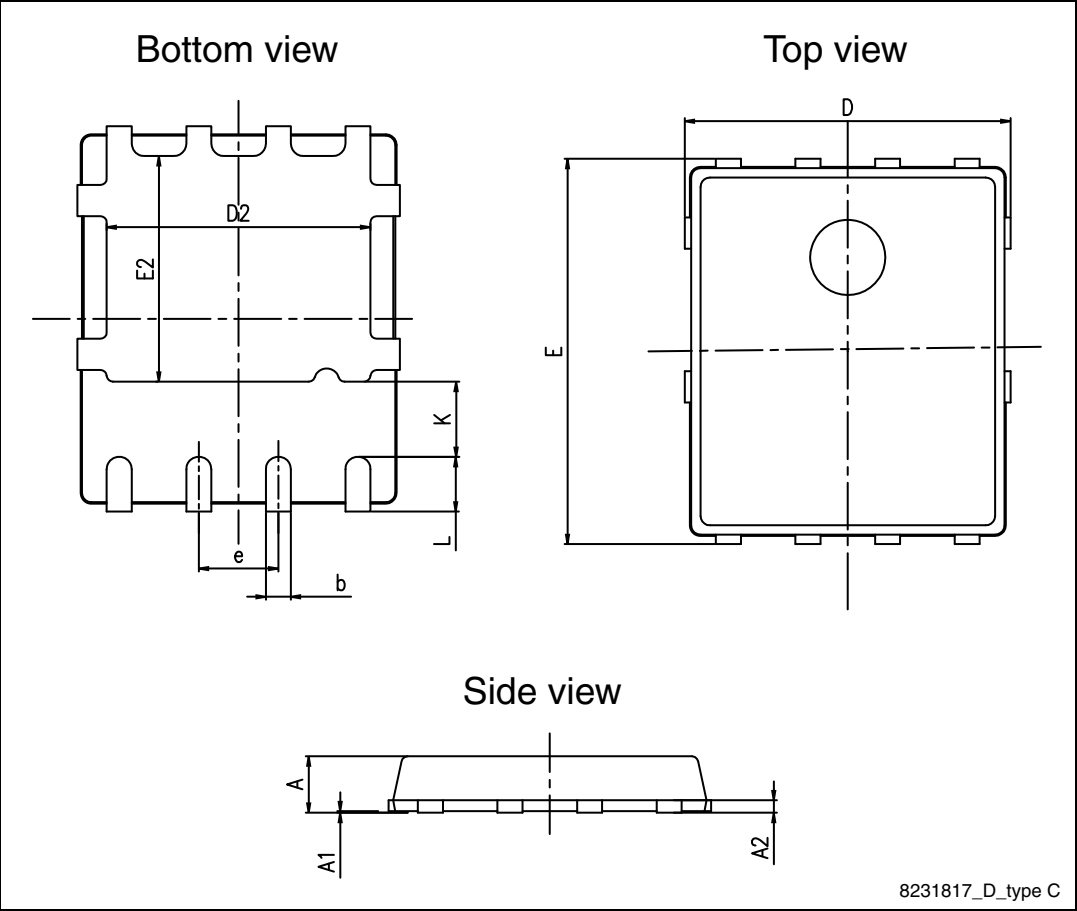
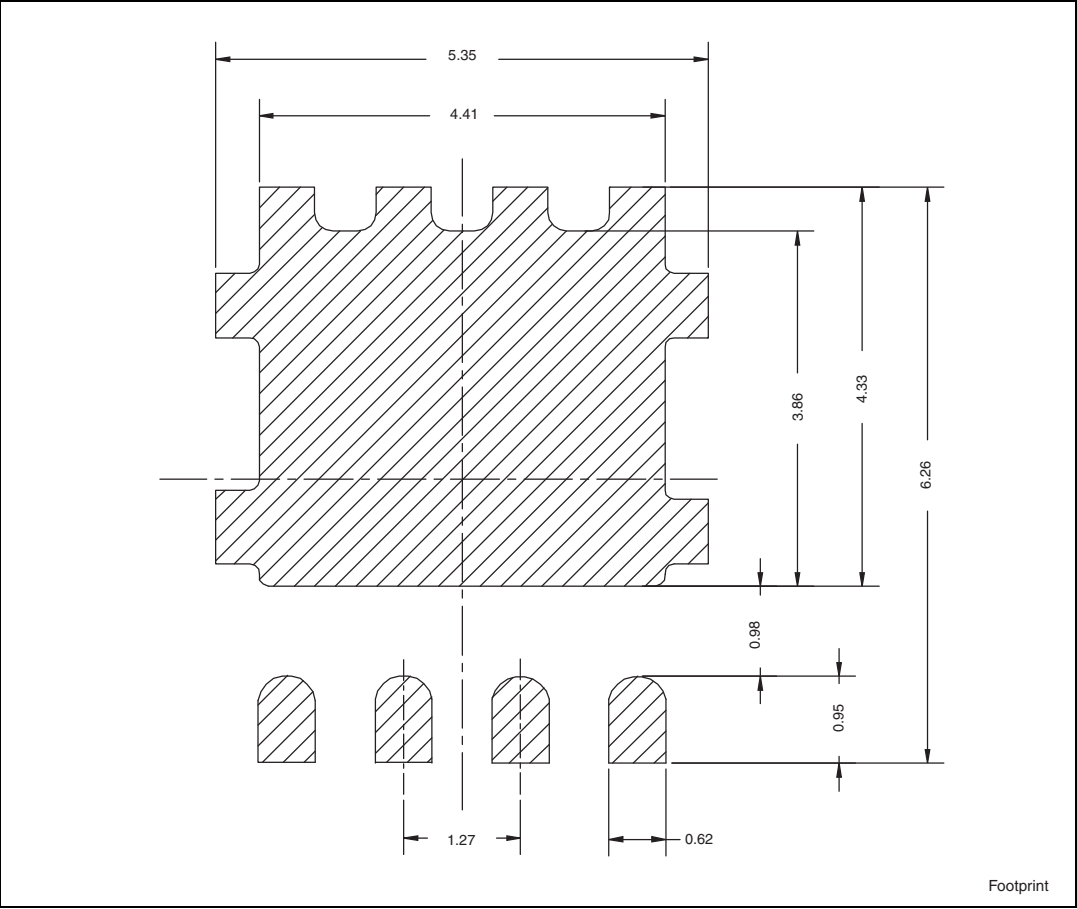


Figure 21. PowerFLAT™ 5x6 recommended footprint (dimensions in mm)



5 Revision history

Table 11. Document revision history

Date	Revision	Changes
11-May-2011	1	First release.
08-Jul-2011	2	Document status promoted from preliminary data to datasheet.
10-Nov-2011	3	Section 4: Package mechanical data has been updated.

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