

#### **N-Ch 80V Fast Switching MOSFETs**

#### **Description**

The HSBL020N08 is the high cell density SGT N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous rectification applications.

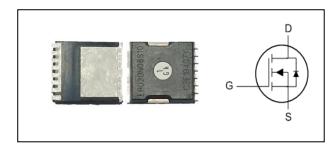
The HSBL020N08 meet the RoHS and Halogen-Free compliant product requirement, 100% EAS guaranteed with full function reliability approved.

- 100% EAS Guaranteed
- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

#### **Product Summary**

V <sub>DS</sub>	80	V
RDS(ON),typ	1.4	mΩ
lo	240	Α

#### **TOLL Pin Configuration**



#### **Absolute Maximum Ratings**

Symbol	Parameter Rating		Units
V <sub>DS</sub>	Drain-Source Voltage	80	V
$V_{GS}$	Gate-Source Voltage	±20	V
I <sub>D</sub> @T <sub>C</sub> =25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1,6</sup>	240	А
I <sub>D</sub> @T <sub>C</sub> =100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1,6</sup>	100	А
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	730	А
EAS	Single Pulse Avalanche Energy <sup>3</sup>	2500	mJ
P <sub>D</sub> @T <sub>C</sub> =25°C	5°C Total Power Dissipation <sup>4</sup> 225		W
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C
TJ	Operating Junction Temperature Range	-55 to 150	°C

#### **Thermal Data**

Symbol	Parameter	Тур.	Max.	Unit
RθJA	Thermal Resistance Junction-Ambient <sup>1</sup>		60	°C/W
Rejc	Thermal Resistance Junction-Case <sup>1</sup>		0.54	°C/W



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### Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS}$ =0 $V$ , $I_D$ =250 $u$ A	80			V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V , I <sub>D</sub> =50A		1.4	2.0	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$ , $I_{D}=250uA$	2	3	4	V
less	Drain Source Leakage Current	$V_{DS}$ =80V , $V_{GS}$ =0V , $T_J$ =25 $^{\circ}$ C			1	uA
I <sub>DSS</sub>	Drain-Source Leakage Current	$V_{DS}$ =80V , $V_{GS}$ =0V , $T_{J}$ =125 $^{\circ}$ C			5	uA
I <sub>GSS</sub>	Gate-Source Leakage Current	$V_{GS}=\pm 20V$ , $V_{DS}=0V$			±100	nA
$R_g$	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz		2	-	Ω
Qg	Total Gate Charge (10V)			204		
Qgs	Gate-Source Charge	VDS=40V, VGS=10V, ID=50A		54	-	nC
Qgd	Gate-Drain Charge			47		
Td(on)	Turn-On Delay Time			39		
Tr	Rise Time	$VDD=40V$ , $VGS=10V$ , $RL=3\Omega$ ,		136	-	ne
Td(off)	Turn-Off Delay Time	ID=20A		121		ns
Tf	Fall Time			156		
Ciss	Input Capacitance			13650		
Coss	Output Capacitance	VDS=45V , VGS=0V , f=1MHz		20100		pF
Crss	Reverse Transfer Capacitance			580		

#### **Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
$V_{\text{SD}}$	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =50A , T <sub>J</sub> =25°C		0.85	1.2	<b>V</b>
Trr	Body Diode Reverse Recovery Time	If=30A, DI/dt=500A/us		112		ns
Qrr	Body Diode Reverse Recovery charge	If=30A, DI/dt=500A/us		313		nC

#### Note

- 1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\,\leq\,$  300us , duty cycle  $\,\leq\,$  2%
- 3. The power dissipation is limited by 150°C junction temperature
- 4. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.
- 5. The maximum current rating is package limited.



#### **Typical Characteristics**

Figure 1. Typ. Output Characteristics (Tj=25°C)

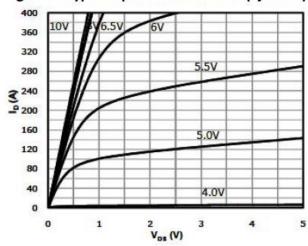


Figure 3. On-Resistance vs. DrainCurrent Junction and Gate Voltage Figure

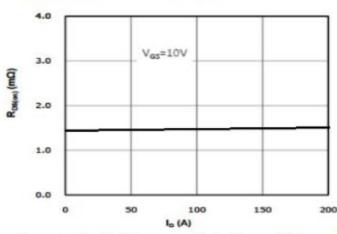
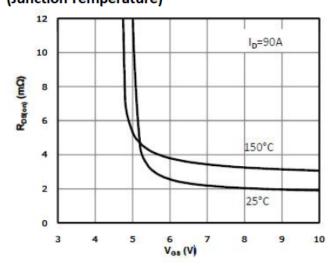


Figure 5. On-Resistance vs. Gate-Source Voltage (Junction Temperature)

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Figure 2. Transfer Characteristics (Junction Temperature)

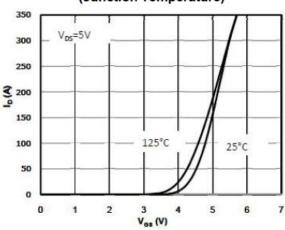


Figure 4. On-Resistance vs.

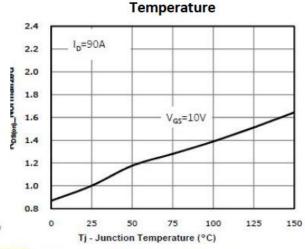
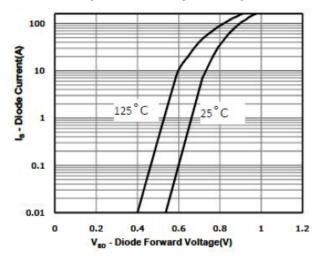


Figure 6. Body-Diode Characteristics (Junction Temperature)

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Figure 7. Gate-Charge Characteristics

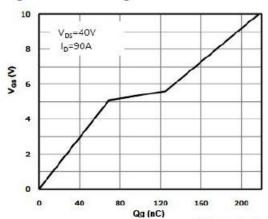


Figure 8. Drain Current Derating

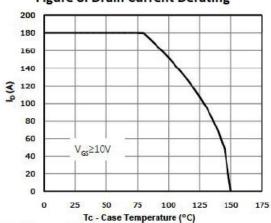


Figure 9. Capacitance Characteristics

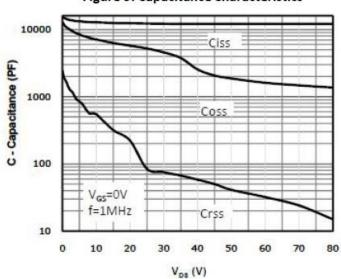
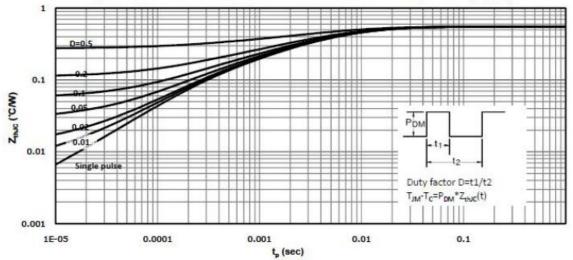


Figure 10. Normalized Maximum Transient Thermal Impedance (RthJC)



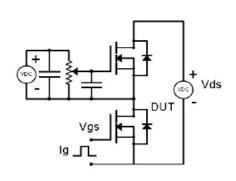


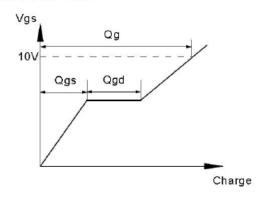


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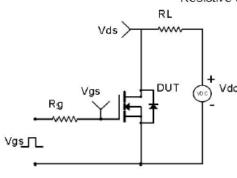
#### **Test Circuit & Waveform**

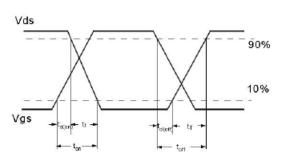
#### Gate Charge Test Circuit & Waveform



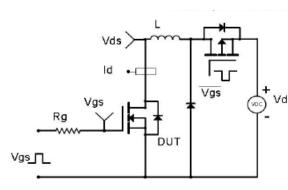


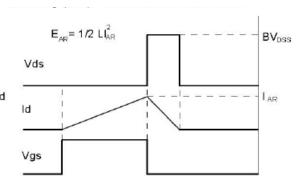
#### Resistive Switching Test Circuit & Waveforms



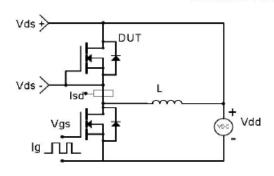


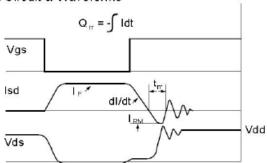
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms







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### Package Outline: TOLL

