

# PSMN3R5-80PS

# N-channel 80 V, 3.5 m $\Omega$ standard level MOSFET in TO-220 Rev. 03 — 19 April 2011 Product data s

Product data sheet

#### **Product profile** 1.

### 1.1 General description

Standard level N-channel MOSFET in TO-220 package qualified to 175C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive

### 1.3 Applications

- DC-to-DC converters
- Load switch

- Motor control
- Server power supplies

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}$		-	-	80	V
I <sub>D</sub>	drain current	$T_{mb}$ = 25 °C; $V_{GS}$ = 10 V; see <u>Figure 1</u>	[1]	-	-	120	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>		-	-	338	W
Tj	junction temperature			-55	-	175	°C
Static ch	aracteristics						
DOUL	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ $T_j = 100 ^{\circ}\text{C}; \text{ see } \frac{\text{Figure } 12}{}$		-	5	5.8	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure } 13}{}$	[2]	-	3	3.5	mΩ
Dynamic	characteristics						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10 \text{ V}; I_D = 75 \text{ A};$		-	27	-	nC
$Q_{G(tot)}$	total gate charge	$V_{DS} = 40 \text{ V}$ ; see Figure 14; see Figure 15		-	139	-	nC
Avalanch	ne ruggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$\begin{split} &V_{GS} = 10 \text{ V; } T_{j(\text{init})} = 25 \text{ °C;} \\ &I_D = 120 \text{ A; } V_{sup} \leq 80 \text{ V;} \\ &R_{GS} = 50 \text{ \Omega; unclamped} \end{split}$		-	-	676	mJ



- [1] Continuous current is limited by package.
- [2] Measured 3 mm from package.

### 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		_
2	D	drain	mb	D
3	S	source		G (EA)
mb	D	drain		mbb076 S
			SOT78 (TO-220AB)	

### 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN3R5-80PS	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

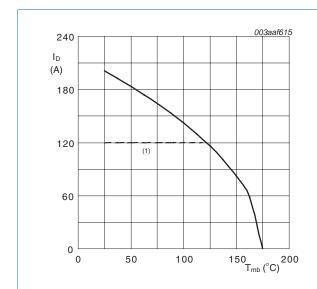
### 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

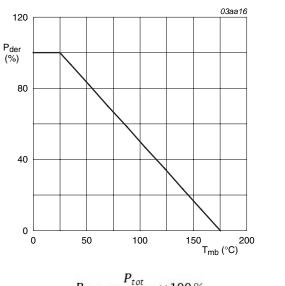
		9 , (				
Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C		-	80	V
$V_{DGR}$	drain-gate voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}; R_{GS} = 20 \text{ k}\Omega$		-	80	V
$V_{GS}$	gate-source voltage			-20	20	V
I <sub>D</sub>	drain current	$V_{GS} = 10 \text{ V; } T_{mb} = 100 \text{ °C; see } \frac{\text{Figure 1}}{}$	<u>[1]</u>	-	120	Α
		$V_{GS} = 10 \text{ V; } T_{mb} = 25 \text{ °C; see } \frac{\text{Figure 1}}{\text{Mode of }}$	[1]	-	120	Α
I <sub>DM</sub>	peak drain current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 \text{ °C}$ ; see Figure 3		-	803	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>		-	338	W
T <sub>stg</sub>	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
T <sub>sld(M)</sub>	peak soldering temperature			-	260	°C
Source-drai	n diode					
Is	source current	T <sub>mb</sub> = 25 °C	<u>[1]</u>	-	120	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^{\circ}C$		-	803	Α
Avalanche r	ruggedness					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $I_D$ = 120 A; $V_{sup} \le$ 80 V; $R_{GS}$ = 50 $\Omega$ ; unclamped		-	676	mJ

### [1] Continuous current is limited by package.



 $V_{\it GS} \geq$  10 V; (1) capped at 120 A due to package.

Fig 1. Continuous drain current as a function of mounting base temperature



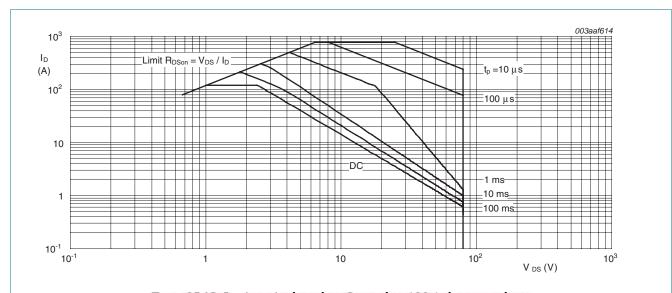
 $P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$ 

Fig 2. Normalized total power dissipation as a function of mounting base temperature

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 $T_{mb}$  = 25 °C;  $I_{DM}$  is a single pulse; Capped at 120 A due to package

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

### 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.22	0.44	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	Vertical in free air	-	60	-	K/W

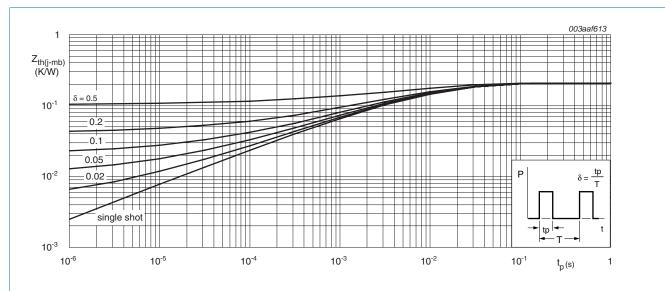


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

### 6. Characteristics

Table 6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	aracteristics					
V <sub>(BR)DSS</sub>	drain-source breakdown	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	73	-	-	V
	voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	80	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$ ; $T_j = 175$ °C; see <u>Figure 10</u>	1	-	-	V
		$I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$ ; $T_j$ = -55 °C; see <u>Figure 10</u>	-	-	4.6	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$ ; $T_j = 25$ °C; see <u>Figure 10</u> ; see <u>Figure 11</u>	2	3	4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.02	10	μΑ
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ °C}$	-	-	500	μΑ
I <sub>GSS</sub> g	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nΑ
		$V_{GS}$ = 20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C	-	-	100	nΑ
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 ^{\circ}\text{C};$ see Figure 12	-	7.2	8.4	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 ^{\circ}\text{C};$ see Figure 12	-	5	5.8	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see Figure 13	[1] -	3	3.5	mΩ
R <sub>G</sub>	internal gate resistance (AC)	f = 1 MHz	-	0.9	-	Ω
Dynamic	characteristics					
Q <sub>G(tot)</sub>	total gate charge	$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	135	-	nC
		$I_D = 75 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V};$	-	139	-	nC
Q <sub>GS</sub>	gate-source charge	see Figure 14; see Figure 15	-	51	-	nC
Q <sub>GS(th)</sub>	pre-threshold gate-source charge		-	30	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate-source charge		-	21	-	nC
$Q_{GD}$	gate-drain charge		-	27	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}$ ; $V_{DS} = 40 \text{ V}$ ; see <u>Figure 14</u> ; see <u>Figure 15</u>	-	5.8	-	V
C <sub>iss</sub>	input capacitance	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	9961	-	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; see <u>Figure 16</u>	-	847	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	401	-	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 40 \text{ V}; R_L = 0.53 \Omega; V_{GS} = 10 \text{ V};$	-	41	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 10 \Omega; I_D = 75 A$	-	43	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	109	-	ns
	fall time					

Table 6. Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Source-dra	in diode					
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ °C}$ ; see Figure 17	-	8.0	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S = 25 \text{ A}$ ; $dI_S/dt = 100 \text{ A/}\mu\text{s}$ ;	-	63	-	ns
Q <sub>r</sub>	recovered charge	$V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V}$	-	121	-	nC

#### [1] Measured 3 mm from package.

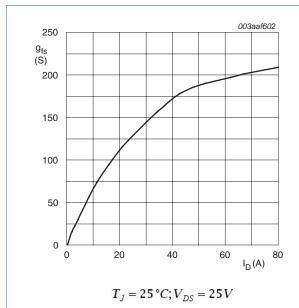


Fig 5. Forward transconductance as a function of drain current; typical values

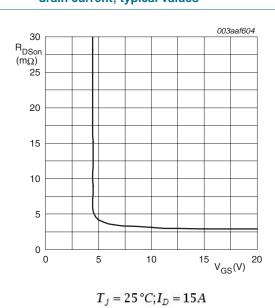
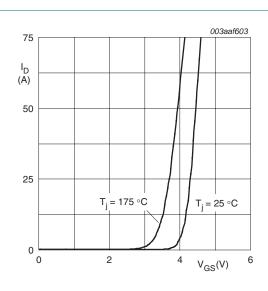
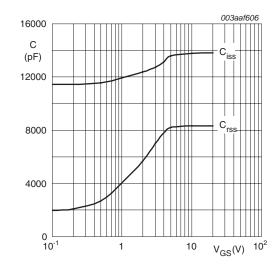


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



 $V_{DS} > I_D \times R_{DSon}$ 

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



 $V_{DS} = 0V; f = 1MHz$ 

Fig 8. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

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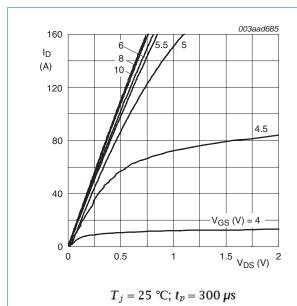


Fig 9. Output characteristics: drain current as a function of drain-source voltage; typical values

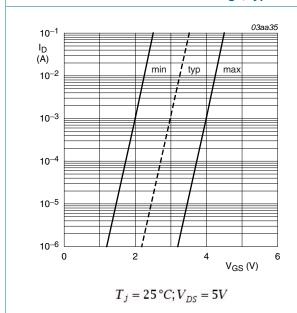


Fig 11. Sub-threshold drain current as a function of gate-source voltage

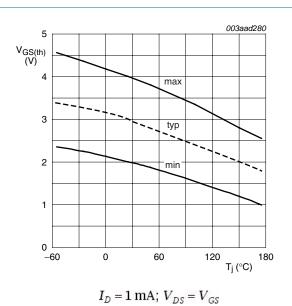


Fig 10. Gate-source threshold voltage as a function of junction temperature

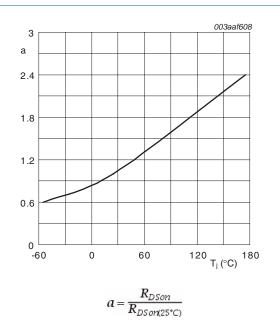
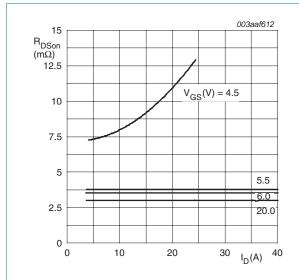


Fig 12. Normailzed drain-source on-state resistance factor as a function of junction temperature



V<sub>DS</sub>

V<sub>GS(pl)</sub>

V<sub>GS(th)</sub>

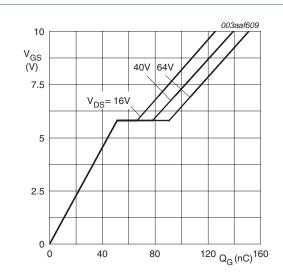
V<sub>GS</sub>

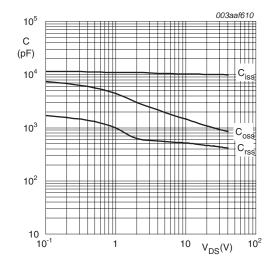
Q<sub>GS1</sub>
Q<sub>GS2</sub>
Q<sub>G</sub>(tot)

003aaa508

Fig 13. Drain-source on-state resistance as a function of drain current; typical values

Fig 14. Gate charge waveform definitions



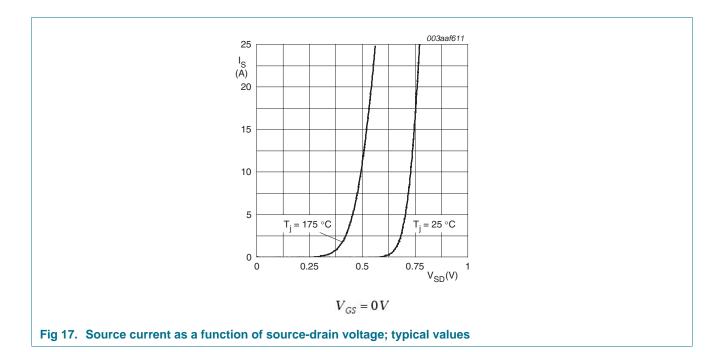


 $T_j = 25$  °C;  $I_D = 75$  A

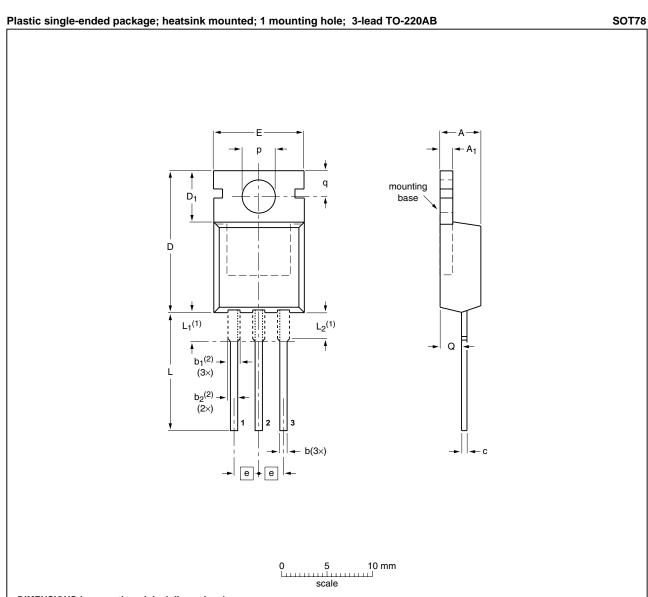
 $V_{GS} = 0V; f = 1MHz$ 

Fig 15. Gate-source voltage as a function of gate charge; typical values

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



### 7. Package outline



### DIMENSIONS (mm are the original dimensions)

UNIT	А	A <sub>1</sub>	b	b <sub>1</sub> (2)	b <sub>2</sub> (2)	С	D	D <sub>1</sub>	E	е	L	L <sub>1</sub> (1)	L <sub>2</sub> <sup>(1)</sup> max.	р	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

#### Notes

- 1. Lead shoulder designs may vary.
- 2. Dimension includes excess dambar.

OUTLINE		REFER	ENCES	CES EUROPEAN		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT78		3-lead TO-220AB	SC-46			<del>08-04-23</del> 08-06-13

Fig 18. Package outline SOT78 (TO-220AB)

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### 8. Revision history

### Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
PSMN3R5-80PS v.3	20110419	Product data sheet	-	PSMN3R5-80PS v.2		
Modifications:  • Status changed from objective to product.						
	<ul> <li>Various changes</li> </ul>	s to content.				
PSMN3R5-80PS v.2	20110304	Objective data sheet	-	PSMN3R5-80PS v.1		

### 9. Legal information

#### 9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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# **PSMN3R5-80PS**

### **Nexperia**

N-channel 80 V, 3.5 m $\Omega$  standard level MOSFET in TO-220

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