

# Automotive N-Channel 80 V (D-S) 175 °C MOSFET

## PRODUCT SUMMARY

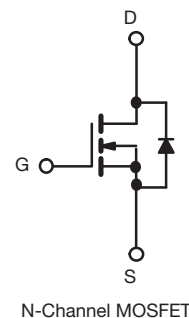
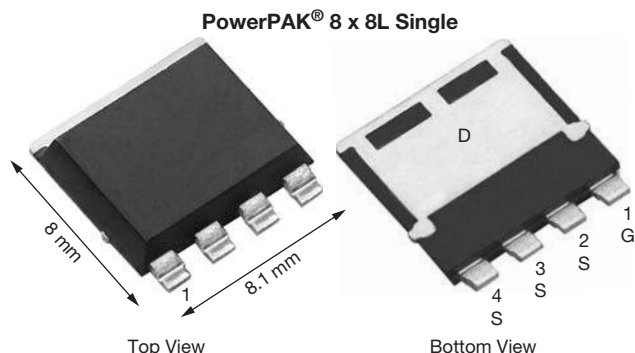
$V_{DS}$ (V)	80
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 10$ V	0.003
$I_D$ (A)	150
Configuration	Single
Package	PowerPAK 8 x 8L

## FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 %  $R_g$  and UIS tested
- Fully lead (Pb)-free device
- Thin 1.9 mm height
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	80	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current	$T_C = 25$ °C $T_C = 125$ °C	150	A
		87	
Continuous Source Current (Diode conduction)	$I_S$	124	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	210	
Single Pulse Avalanche Current	$I_{AS}$	53	
Single Pulse Avalanche Energy	$E_{AS}$	140	mJ
Maximum Power Dissipation	$T_C = 25$ °C $T_C = 125$ °C	136	W
		45	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	°C
Soldering Recommendations (Peak temperature) <sup>c, d</sup>		260	

## THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	$R_{thJA}$	50	°C/W
Junction-to-Case (Drain)	$R_{thJC}$	1.1	

### Notes

- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %.
- When mounted on 1" square PCB (FR4 material).
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 8 x 8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

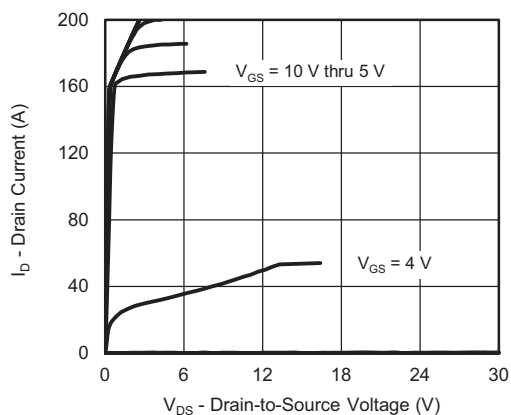
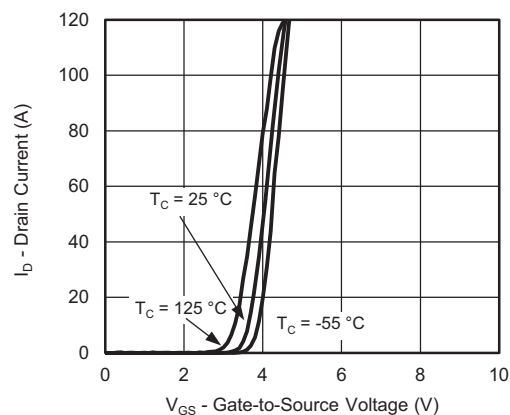
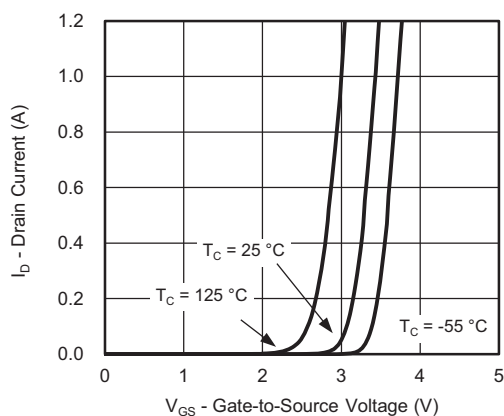
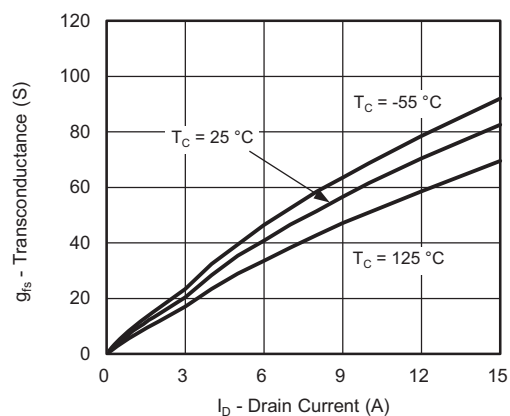
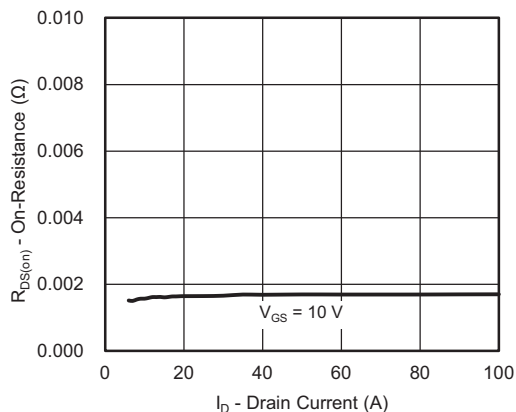
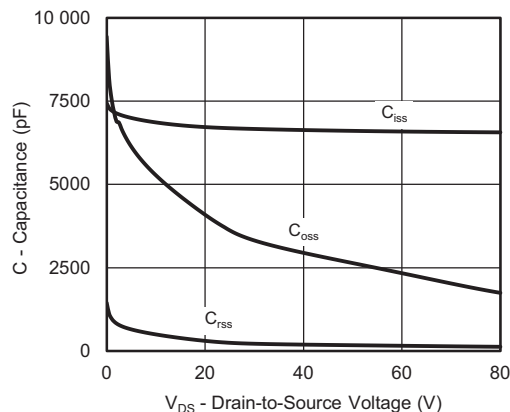


SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA		80	-	-	V
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.5	3	3.5	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 80 V	-	-	1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 80 V, T <sub>J</sub> = 125 °C	-	-	50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 80 V, T <sub>J</sub> = 175 °C	-	-	500	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> ≥ 5 V	50	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A	-	0.0024	0.0030	Ω
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C	-	-	0.0048	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C	-	-	0.0060	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A		-	82	-	S
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 25 V, f = 1 MHz	-	6900	8625	pF
Output Capacitance	C <sub>oss</sub>			-	3655	4570	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	250	311	
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 10 A	-	82	144	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			-	11	-	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	21	-	
Gate Resistance	R <sub>g</sub>	f = 1 MHz		0.4	0.8	1.2	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 40 V, R <sub>L</sub> = 4 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		-	19	30	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			-	7.3	11	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	40	60	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	15	23	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	210	A
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = 40 A, V <sub>GS</sub> = 0 V		-	0.7	1.2	V

**Notes**

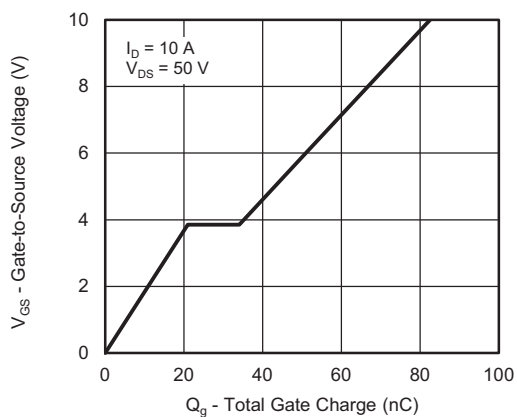
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.  
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

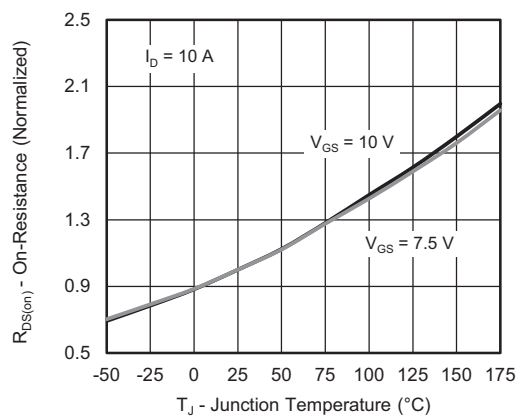
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**Transfer Characteristics**

**Transconductance**

**On-Resistance vs. Drain Current**

**Capacitance**



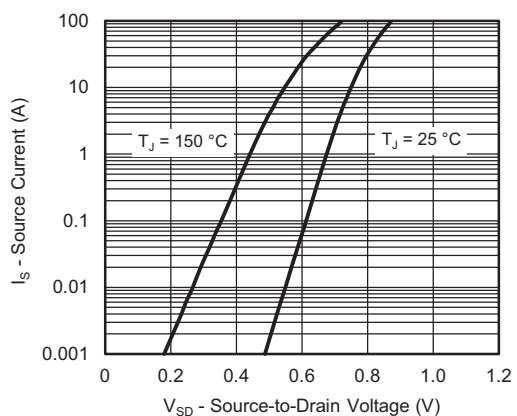
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



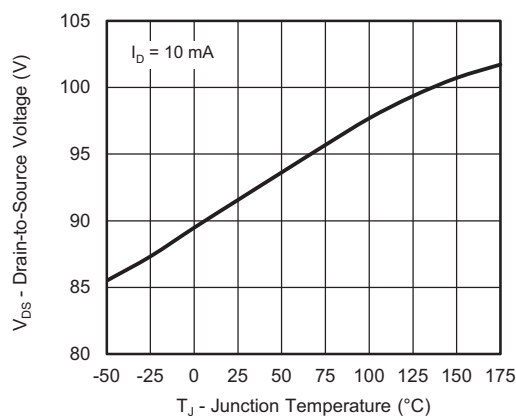
**Gate Charge**



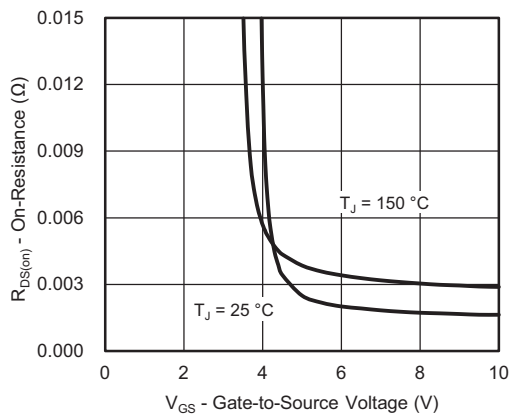
**On-Resistance vs. Junction Temperature**



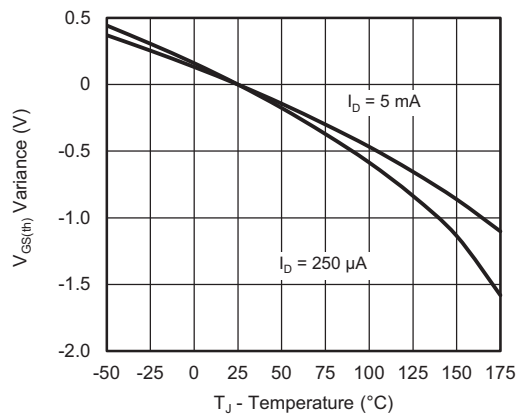
**Source Drain Diode Forward Voltage**



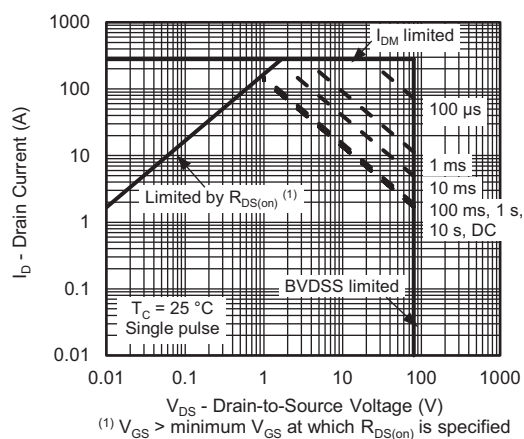
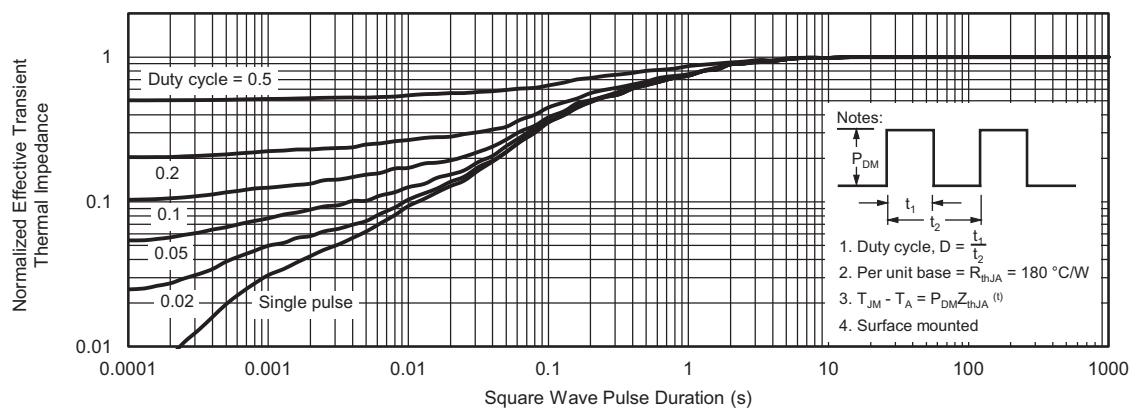
**Drain Source Breakdown vs. Junction Temperature**



**On-Resistance vs. Gate-to-Source Voltage**

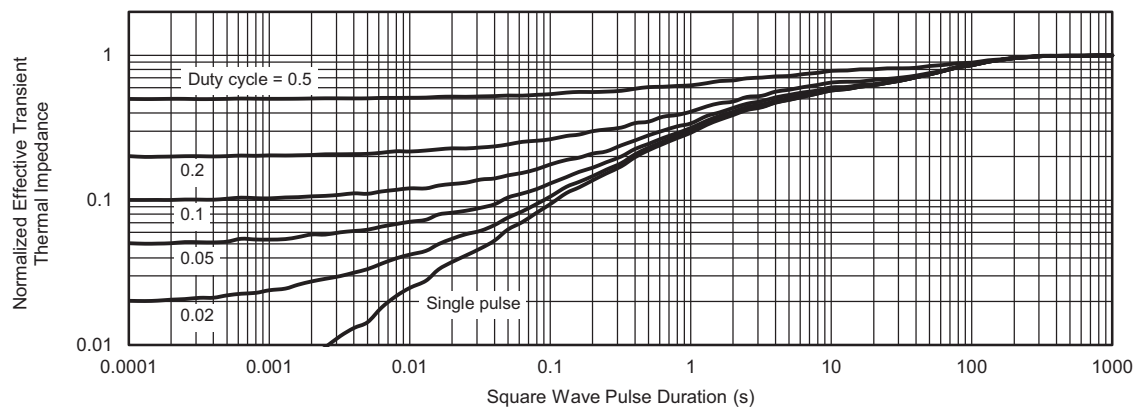


**Threshold Voltage**

**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Safe Operating Area**
**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Normalized Thermal Transient Impedance, Junction-to-Ambient**



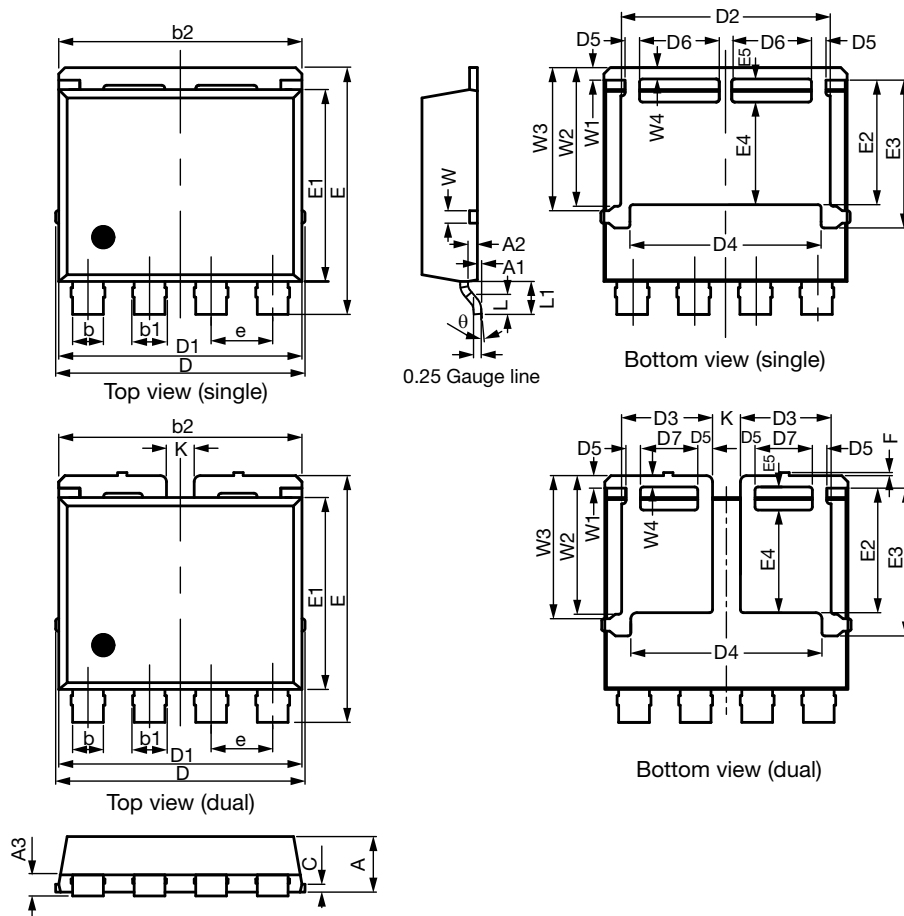
**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?76718](http://www.vishay.com/ppg?76718).

## PowerPAK® 8 x 8L Case Outline



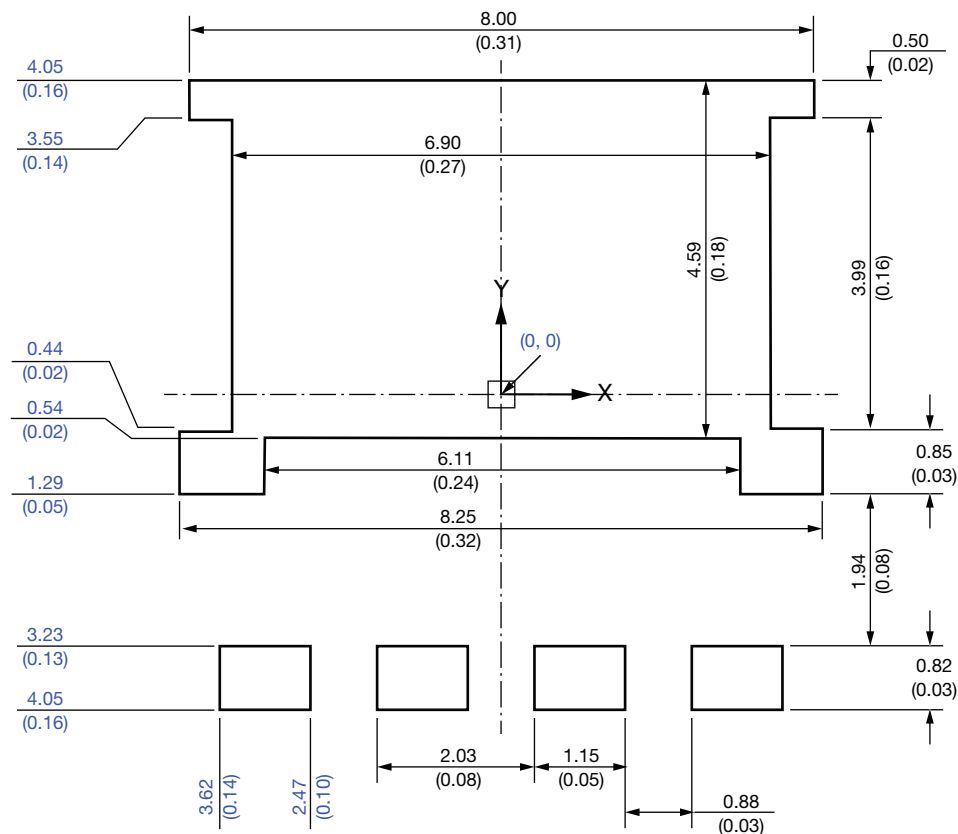
DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.70	1.80	1.90	0.067	0.071	0.075
A1	0.00	0.08	0.13	0.000	0.003	0.005
A2	0.25	0.30	0.35	0.010	0.012	0.014
A3	0.55	0.62	0.70	0.022	0.024	0.028
b	0.92	1.00	1.08	0.036	0.039	0.043
b1	1.02	1.10	1.18	0.040	0.043	0.046
b2	7.80	7.90	8.00	0.307	0.311	0.315
c	0.20	0.25	0.30	0.008	0.010	0.012
D	8.00	8.10	8.25	0.315	0.319	0.325
D1	7.80	7.90	8.00	0.307	0.311	0.315
D2	6.70	6.80	6.90	0.264	0.268	0.272
D3	2.85	2.95	3.05	0.112	0.116	0.120
D4	6.11	6.21	6.31	0.241	0.244	0.248
D5	0.37	0.47	0.57	0.015	0.019	0.022
D6	2.49	2.59	2.69	0.098	0.102	0.106
D7	1.76	1.86	1.96	0.069	0.073	0.077



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
e	1.95	2.00	2.05	0.077	0.079	0.081
E	7.90	8.00	8.10	0.311	0.315	0.319
E1	6.12	6.22	6.32	0.241	0.245	0.249
E2	3.94	4.04	4.14	0.140	0.159	0.163
E3	4.69	4.79	4.89	0.185	0.189	0.193
E4	3.23	3.33	3.43	0.127	0.131	0.135
E5	0.65	0.75	0.85	0.026	0.030	0.033
F	0.00	0.10	0.15	0.000	0.004	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.80	0.90	1.00	0.031	0.035	0.039
W	0.30	0.40	0.50	0.012	0.016	0.020
W1	0.30	0.40	0.50	0.012	0.016	0.020
W2	4.39	4.49	4.59	0.173	0.177	0.181
W3	4.54	4.64	4.74	0.179	0.183	0.187
W4	0.32	0.37	0.42	0.013	0.015	0.017
θ	6°	10°	14°	6°	10°	14°
C17-1388-Rev. B, 16-Oct-17 DWG: 6026						



### Recommended Minimum PADs for PowerPAK® 8 x 8L Single



Dimensions in millimeters (inches)

### Note

- Linear dimensions are in black, the same information is provided in ordinate dimensions which are in blue.



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