

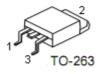
1. General Features

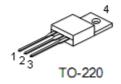
- n Proprietary New Trench Technology
- n $R_{DS(ON),typ.}=4.0m\Omega@V_{GS}=10V$
- n Low Gate Charge Minimize Switching Loss
- n Fast Recovery Body Diode

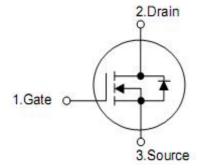
2. Applications

- n High efficiency DC/DC converters
- n Synchronous Rectification
- n UPS Inverter

3. Pin configuration







Pin	Function	
1	Gate	
2	Drain	
3	Source	
4	Drain	



4. Ordering Information

Part Number	Package	Brand
KNP2708A	TO-220	KIA
KNB2708A	TO-263	KIA

5. Absolute maximum ratings

(Tc= 25 °C, unless otherwise specified)

Symbol	Parameter	Rating	Unit	
V _{DSS}	Drain-to-Source Voltage ^[1]	80	V	
V _{GSS}	Gate-to-Source Voltage	±20		
I _D	Continuous Drain Current ^[2]	160		
	Continuous Drain Current [3]	80		
I _D @ T _C =100°C	Continuous Drain Current@T _C =100 °C [2]	116	A	
I _{DM}	Pulsed Drain Current at V _{GS} =10V ^[2,4]	640		
E _{AS}	Single Pulse Avalanche Energy	1100	mJ	
dv /dt	Peak Diode Recovery dv/dt[3]	5.0	V/ns	
P _D	Power Dissipation	313	W	
	Derating Factor above 25 °C	2.08	W/°C	
T _L T _{PAK}	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260	°C	
T _J &T _{STG}	Operating and Storage Temperature Range	-55 to 175		

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

6. Thermal characteristics

Symb	ol Parameter	Rating	Unit
Rejc	Thermal Resistance, Junction-to	o-Case 0.48	°C /W
R _{θJA}	Thermal Resistance, Junction-to-	Ambient 62	- C /VV



7. Electrical characteristics

	racteristics	(TJ=25°C,unless oth		·		
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
BV _{DSS}	Drain-to-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	80			V
I_{DSS}	Drain-to-Source Leakage Current	V _{DS} =80V, V _{GS} =0V V _{DS} =64V,V _{GS} =0V, T _J =125°C			100	uA
I _{GSS}	Gate-to-Source Leakage Current	V _{GS} =+20V,V _{DS} =0V			+100	nA
1655	IGSS Gate-to-Source Leakage Current	V_{GS} =-20V, V_{DS} =0V			-100	
ON Char	acteristics	(TJ=25°C,unless oth	erwise	specifie	d)	
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
$R_{\text{DS}(\text{ON})}$	Static Drain-to-Source On-Resistance	V _{GS} =10V, I _D =24A ^[5]		4.0	4.8	mΩ
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =250uA	2.0		4.0	V
gfs	Forward Transconductance	$V_{DS}=10V, I_{D}=80A^{[5]}$	-	130	-	S
Dynamic	Characteristics	Essentially independ	lent of c	perating	temper	ature
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input Capacitance	V _{GS} =0V,		9300		pF
Coss	Output Capacitance	V _{DS} =25V,		650		
Crss	Reverse Transfer Capacitance	f=1.0MHZ		260		
Rg	Gate Series Resistance	f=1.0MHZ		2.7		Ω
Q_g	Total Gate Charge	V _{DD} =40V,		115		nC
Q _{gs}	Gate-to-Source Charge	I _D =80A,		40		
Q_{gd}	Gate-to-Drain (Miller) Charge	V _{GS} =0 to 10V		30		
Resistive	Switching Characteristics	Essentially independ	dent of o	operatin	g tempe	rature
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(ON)}	Turn-on Delay Time	\/ 40\/		50		nS
t _{rise}	Rise Time	$V_{DD}=40V$, $I_{D}=40A$,		135		
t _{d(OFF)}	Turn-Off Delay Time	V _{GS} = 10V		112		
t _{fall}	Fall Time	$R_{G}=10\Omega$		75		
Source-D	Prain Body Diode Characteristics	(T _J =25°C,unless other	erwise s	specified	l)	
Symbol	Parameter	Test Conditions	Min	Тур.	Max.	Unit
I _{SD}	Continuous Source Current ^[2]	Integral PN-diode in MOSFET			160	A
I _{SM}	Pulsed Source Current ^[2]				640	
V _{SD}	Diode Forward Voltage	I _S =80A, V _{GS} =0V			1.2	V
t _{rr}	Reverse recovery time	V _{GS} =0V ,I _F =80A, diF/dt=100A/μs		85		ns
Qrr	Reverse recovery charge			205		nC
N1-4[41 T	F . OF OC 45 . 47F OC	-1				

Note:[1] T $_{\rm J}$ =+25 °C to +175 °C.

^[2] Silicon limited current only.

^[3] Package limited current .

^[4] Repetitive rating; pulse width limited by maximum junction temperature.

^[5] Pulse width≤380µs; duty cycle≤2%.



8. Test circuits and waveforms

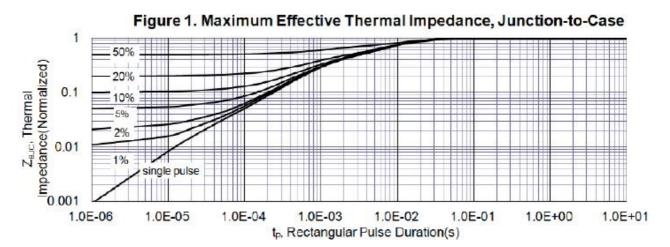


Figure 2. Maximum Power Dissipation vs. Case Temperature 350 300 Power Dissipation (M) 250 200 150 100 50 25 50 100 75 125 150 T_c, Case Temperature (*C)

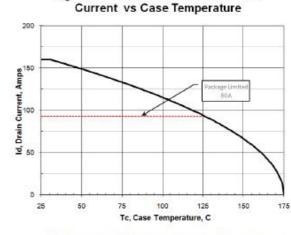
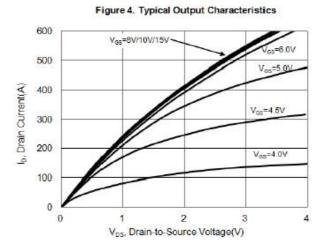
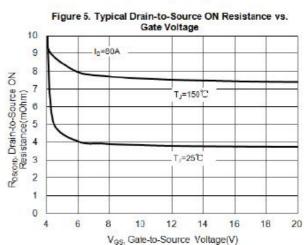
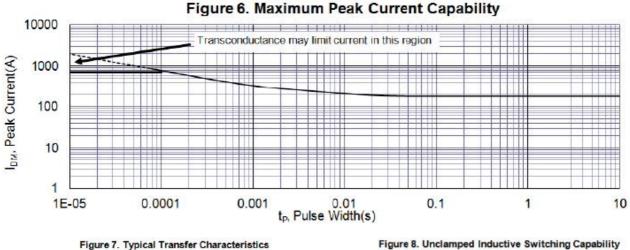


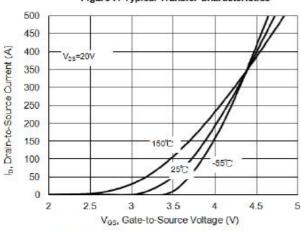
Figure 3 .Maximum Continuous Drain

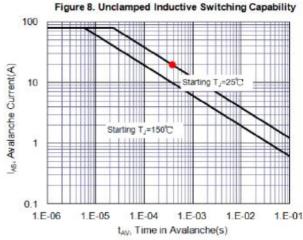


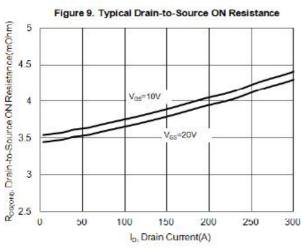


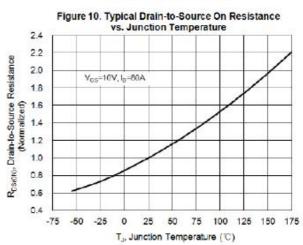














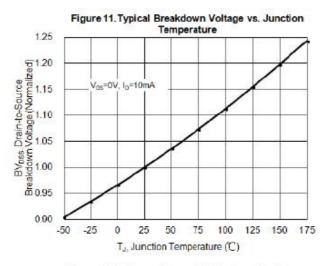


Figure 13. Maximum Forward Safe Operation Area

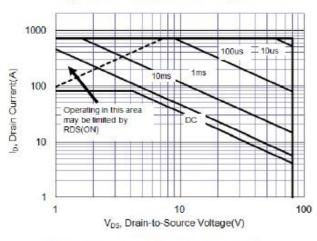


Figure 15. Typical Gate Charge vs. Gate-to-Source

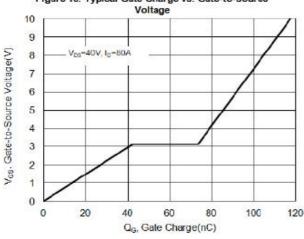


Figure 12. Typical Threshold Voltage vs. Junction Temperature

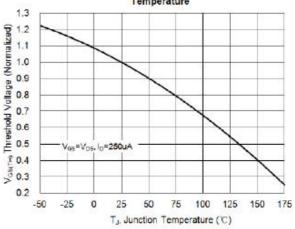
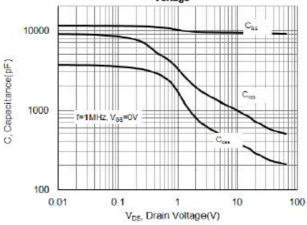
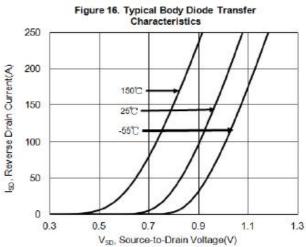


Figure 14. Typical Capacitance vs. Drain-to-Source Voltage





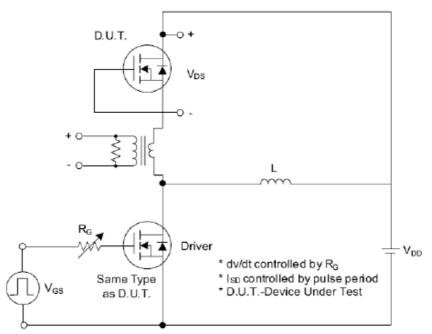


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

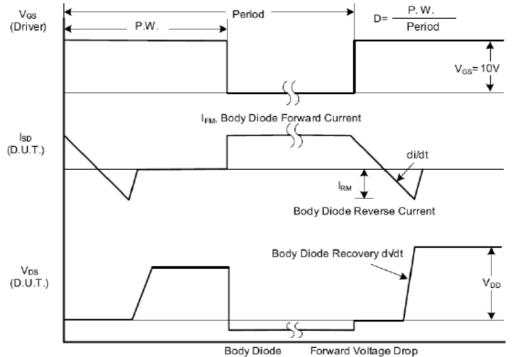


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

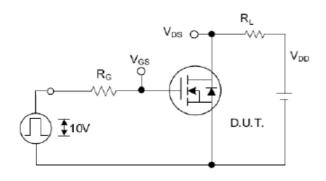


Fig. 2.1 Switching Test Circuit

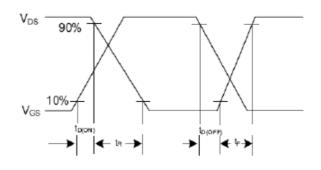


Fig. 2.2 Switching Waveforms

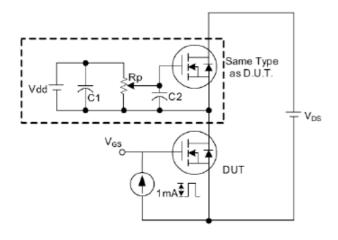


Fig. 3 . 1 Gate Charge Test Circuit

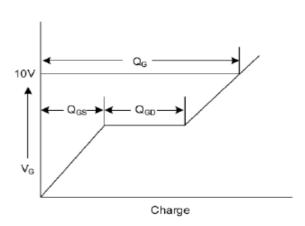


Fig. 3.2 Gate Charge Waveform

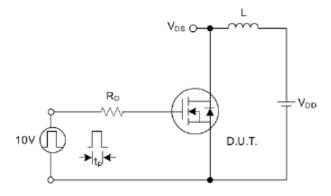


Fig. 4.1 Unclamped Inductive Switching Test Circuit

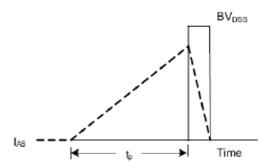


Fig. 4.2 Unclamped Inductive Switching Waveforms