

FDP045N10A / FDI045N10A

MOSFET – N-Channel, POWERTRENCH®

100 V, 164 A, 4.5 mΩ

Description

This N-Channel MOSFET is produced using ON Semiconductor's advance POWERTRENCH process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Features

- $R_{DS(on)} = 3.8 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 100 \text{ A}$
- Fast Switching Speed
- Low Gate Charge, $Q_G = 54 \text{ nC}$ (Typ.)
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- This Device is Pb-Free and is RoHS Compliant

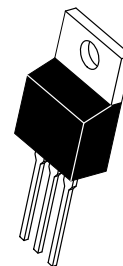
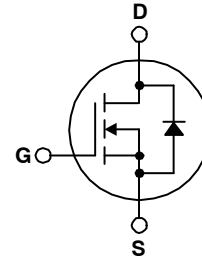
Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

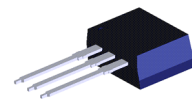


ON Semiconductor®

www.onsemi.com

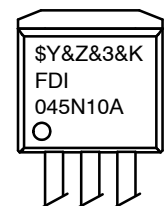
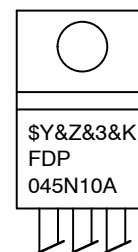


TO-220
CASE 221A-09



I²PAK
CASE 418AV

MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDP/FDI045N10A	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDP045N10A / FDI045N10A

MOSFET MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

Symbol	Parameter		FDP045N10A_F102 FDI045N10A_F102	Unit
V _{DSS}	Drain to Source Voltage		100	V
V _{GSS}	Gate to Source Voltage		±20	V
I _D	Drain Current	– Continuous (T _C = 25°C, Silicon Limited)	164*	A
		– Continuous (T _C = 100°C, Silicon Limited)	116	
		– Continuous (T _C = 25°C, Package Limited)	120	
I _{DM}	Drain Current	– Pulsed (Note 1)	656	A
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		637	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		6.0	V/ns
P _D	Power Dissipation	(T _C = 25°C)	263	W
		– Derate Above 25°C	1.75	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		–55 to +175	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120 A.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDP045N10A_F102 FDI045N10A_F102	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	0.57	°C
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	62.5	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP045N10A_F102	FDP045N10A	TO-220	Tube	N/A	N/A	50 Units
FDI045N10A_F102	FDI045N10A	I ² -PAK	Tube	N/A	N/A	50 Units

ELECTRICAL CHARACTERISTICS (T_C = 25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
--------	-----------	-----------------	------	------	------	------

OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 mA, V _{GS} = 0 V	100	–	–	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 mA, Referenced to 25°C	–	0.07	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 80 V, V _{GS} = 0 V	–	–	1	μA
		V _{DS} = 80 V, T _C = 150°C	–	–	500	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 mA	2.0	–	4.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 100 A	–	3.8	4.5	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 100 A	–	132	–	S

FDP045N10A / FDI045N10A

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ Unless Otherwise Noted) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
--------	-----------	-----------------	------	------	------	------

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$	–	3960	5270	pF
C_{oss}	Output Capacitance		–	925	1230	pF
C_{rss}	Reverse Transfer Capacitance		–	34	–	pF
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$	–	1520	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V},$ $I_D = 100\text{ A}$ (Note 4)	–	54	74	nC
Q_{gs}	Gate to Source Gate Charge		–	17	–	nC
Q_{gs2}	Gate Charge Threshold to Plateau		–	8	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	13	–	nC
ESR	Equivalent Series Resistance (G–S)	$f = 1\text{ MHz}$	–	1.9	–	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}, I_D = 100\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 4.7\text{ }\Omega$ (Note 4)	–	23	56	ns
t_r	Turn-On Rise Time		–	26	62	ns
$t_{d(off)}$	Turn-Off Delay Time		–	50	110	ns
t_f	Turn-Off Fall Time		–	15	40	ns

DRAIN–SOURCE DIODE CHARACTERISTICS

I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	164*	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	656	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 100\text{ A}$	–	–	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, V_{DD} = 50\text{ V},$ $I_{SD} = 100\text{ A},$ $di_F/dt = 100\text{ A/ms}$	–	75	–	ns
Q_{rr}	Reverse Recovery Charge		–	120	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Repetitive rating; pulse-width limited by maximum junction temperature.
2. $L = 3\text{ mH}, I_{AS} = 20.6\text{ A}, R_G = 25\text{ }\Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 100\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

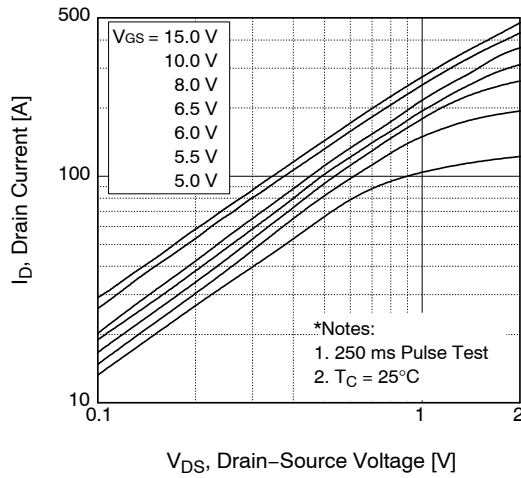


Figure 1. On-Region Characteristics

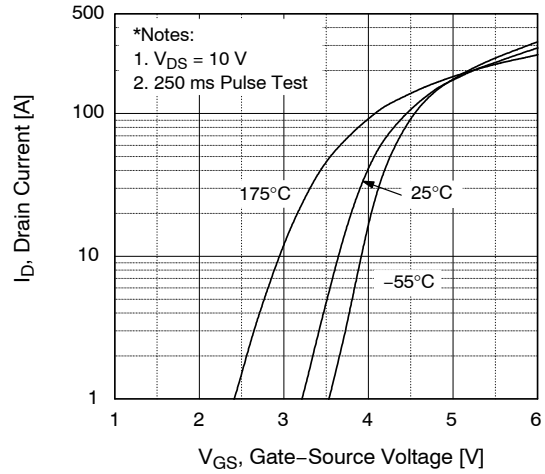


Figure 2. Transfer Characteristics

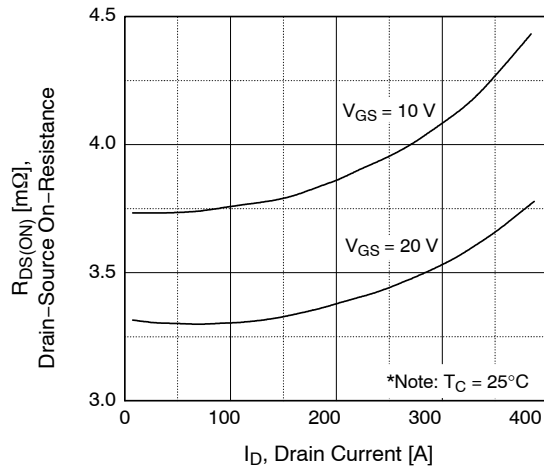


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

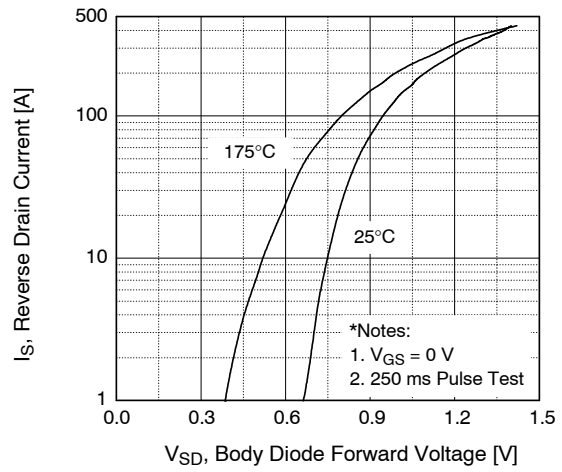


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

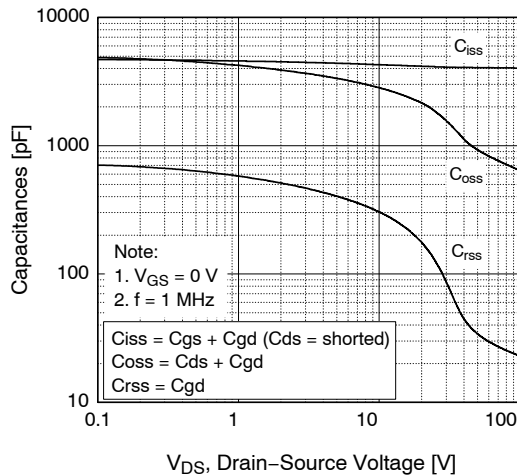


Figure 5. Capacitance Characteristics

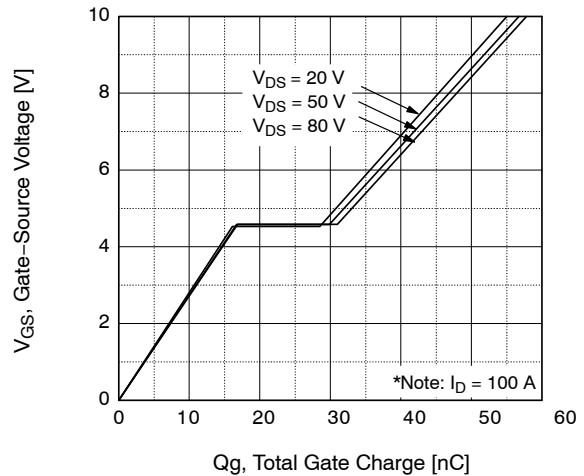


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

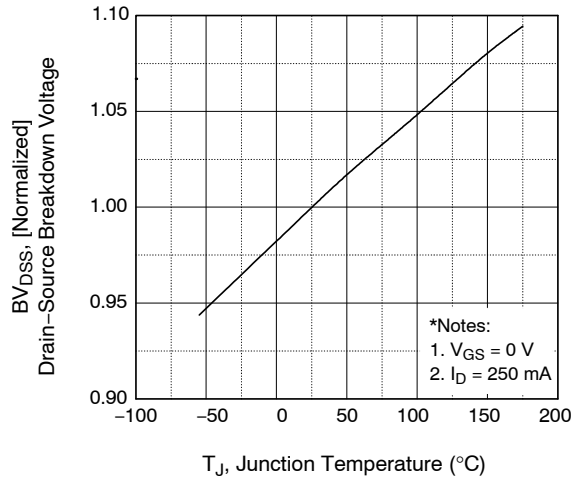


Figure 7. Maximum Safe Operating Area

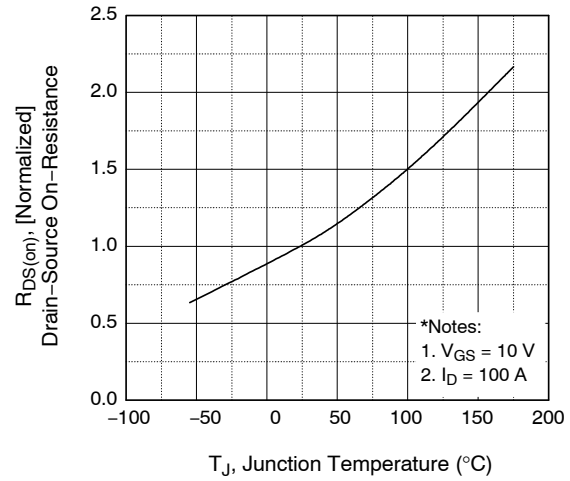


Figure 8. On-Resistance Variation vs. Temperature

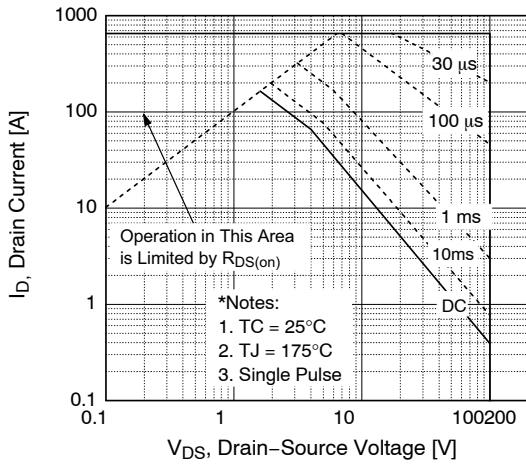


Figure 9. Maximum Safe Operating Area

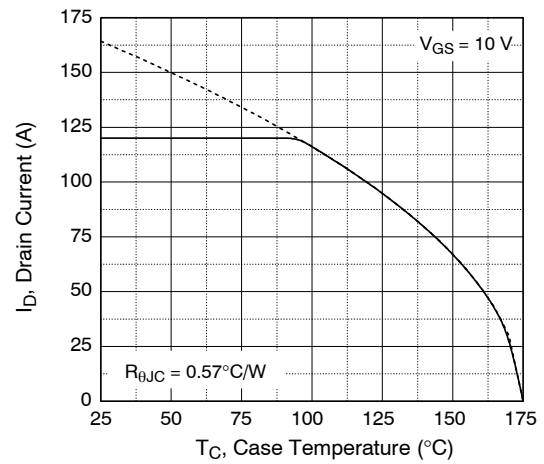


Figure 10. Maximum Drain Current vs. Case Temperature

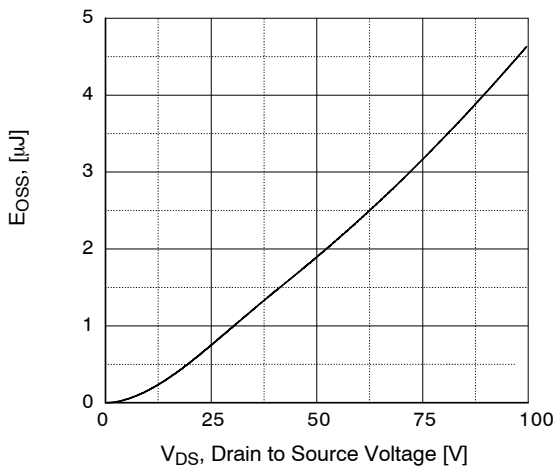


Figure 11. E_{oss} vs. Drain to Source Voltage

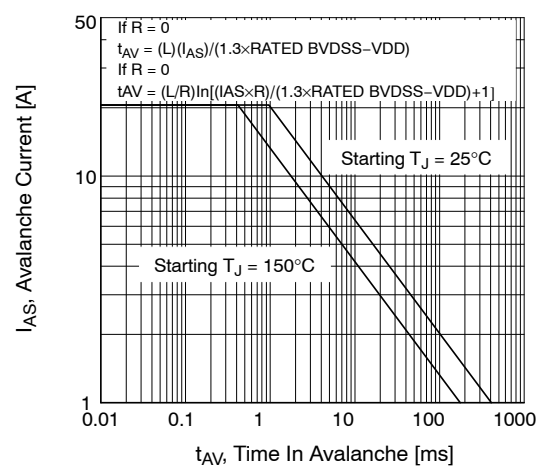


Figure 12. Unclamped Inductive Switching Capability

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

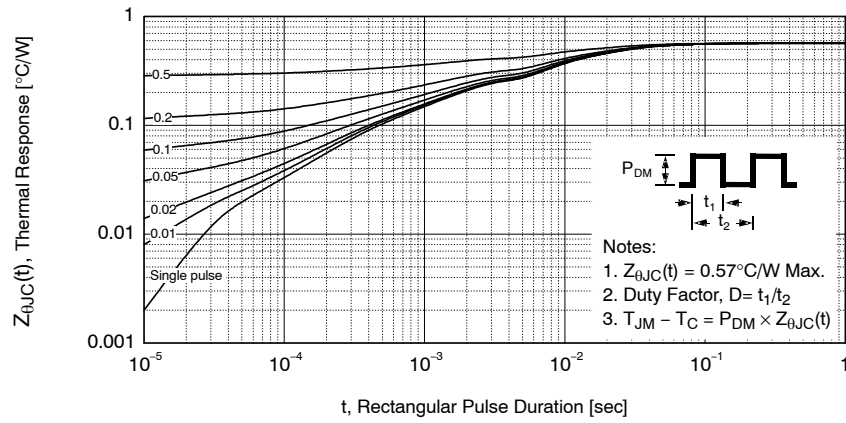


Figure 13. Transient Thermal Response Curve

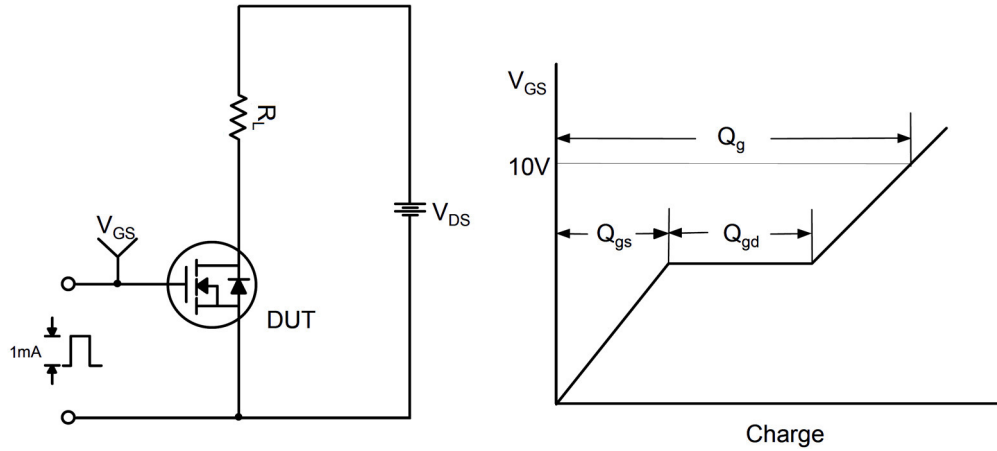


Figure 14. Gate Charge Test Circuit & Waveform

FDP045N10A / FDI045N10A

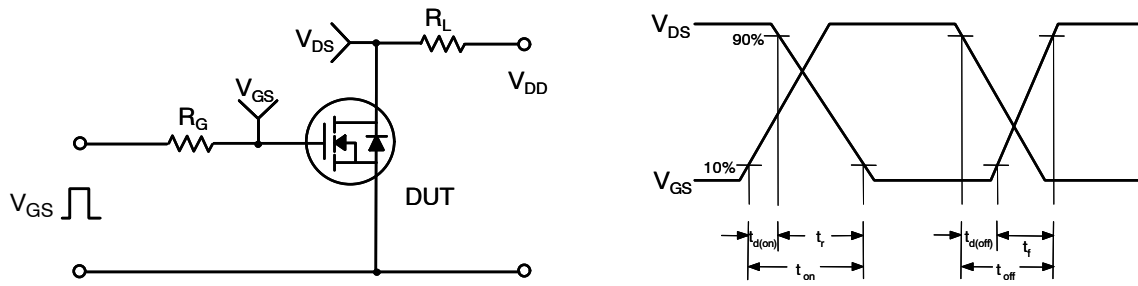


Figure 15. Resistive Switching Test Circuit & Waveforms

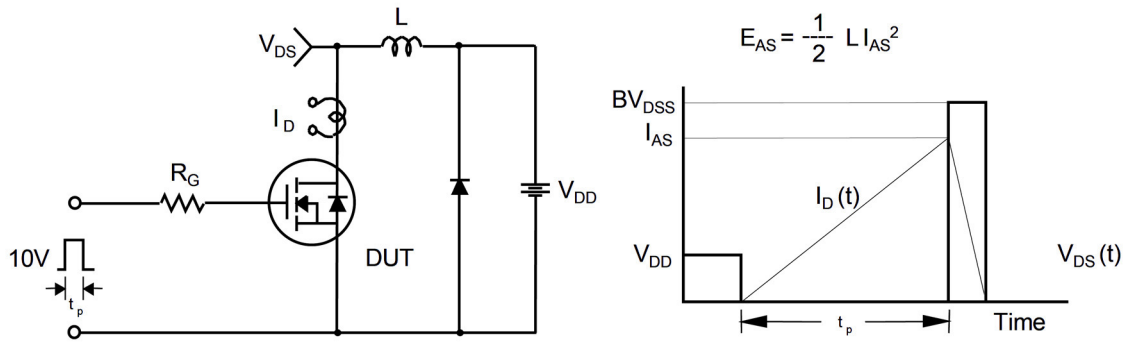


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

FDP045N10A / FDI045N10A

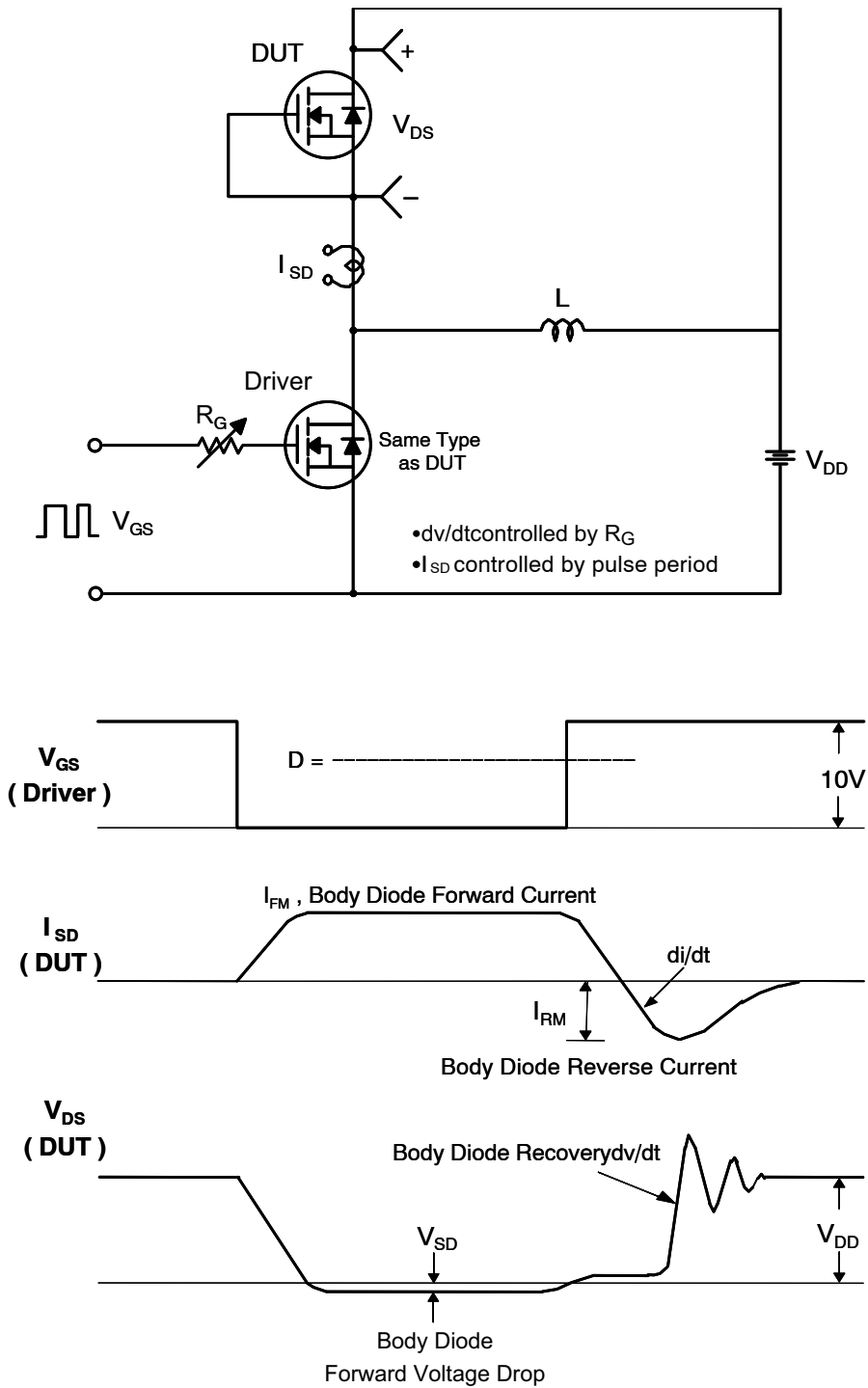
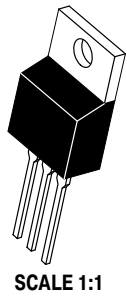


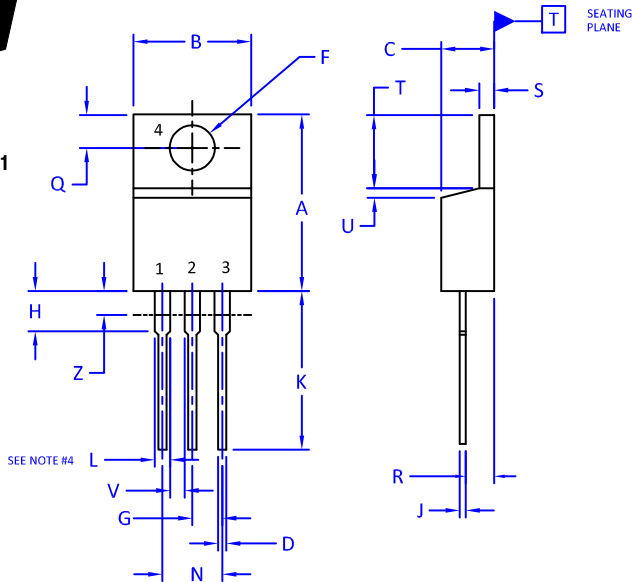
Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TO-220 CASE 221A ISSUE AK

DATE 13 JAN 2022



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	----	1.15	---
Z	----	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

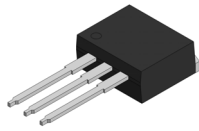
STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

DOCUMENT NUMBER:	98ASB42148B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TO-220	PAGE 1 OF 1

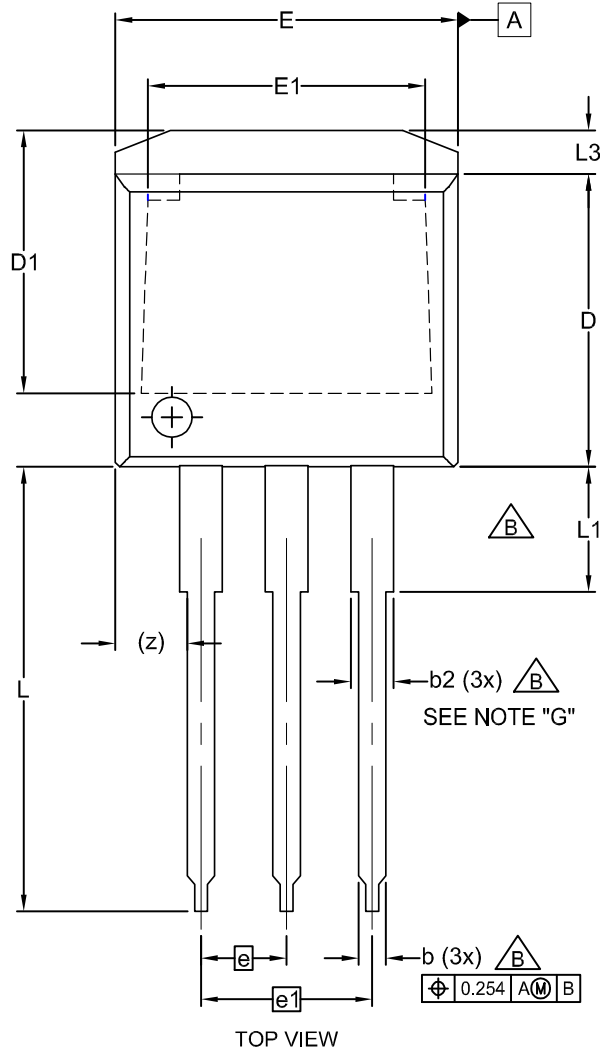
onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

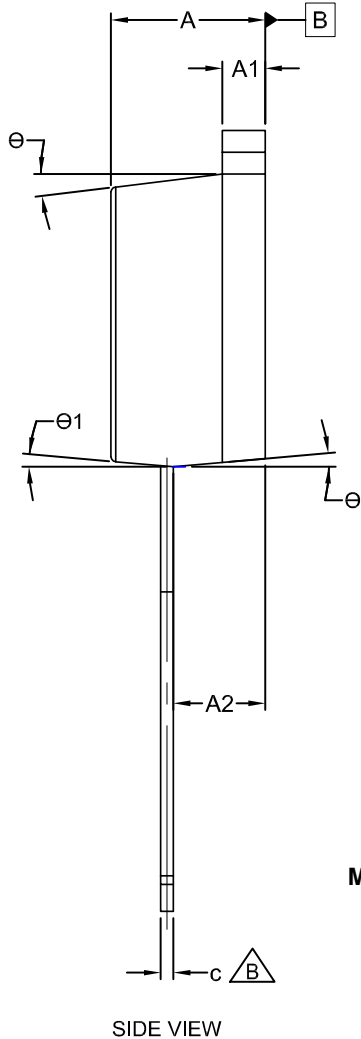


I2PAK (TO-262 3 LD)
CASE 418AV
ISSUE A

DATE 30 AUG 2022



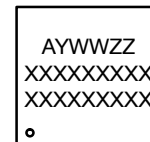
TOP VIEW



SIDE VIEW

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.06	4.45	4.83
A1	1.14	1.27	1.40
A2	2.03	2.41	2.79
b	0.64	0.77	0.90
b2	1.14	1.46	1.78
c	0.33	0.49	0.64
D	8.64	9.15	9.65
D1	6.86	7.37	7.88
E	9.65	9.97	10.29
E1	6.22	7.28	8.33
e	2.54 BSC		
e1	5.08 BSC		
L	12.70	13.72	14.73
L1	2.80	3.38	3.96
L3	1.00	1.20	1.40
z	2.13 REF		
θ	0°	--	7°
θ1	0°	--	5°

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code

A = Assembly Location

Y = Year

WW = Work Week

ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

- EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.
- DOES NOT COMPLY JEDEC STD. VALUE.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
- LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)
- MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.

DOCUMENT NUMBER:	98AON13814G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	I2PAK (TO-262 3 LD)	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales