N-Channel Enhancement Mode Power MOSFET

Description

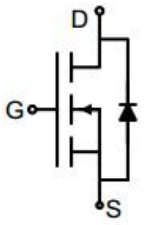
The GT080N10K uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

General Features

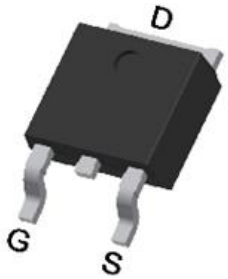
- V_{DS} 100V
- I_D (at V_{GS} = 10V) 65A
- $R_{DS(ON)}$ (at V_{GS} = 10V) < 8mΩ
- $R_{DS(ON)}$ (at V_{GS} = 4.5V) < 9.5mΩ
- 100% Avalanche Tested
- RoHS Compliant

Application

- Power switch
- DC/DC converters



Schematic diagram



TO-252

Ordering Information

Device	Package	Marking	Packaging
GT080N10K	TO-252	GT080N10	2500pcs/Reel

Absolute Maximum Ratings T_C = 25ºC, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Continuous Drain Current	I_D	65	A
Pulsed Drain Current (note1)	I_{DM}	260	A
Gate-Source Voltage	V_{GS}	±20	V
Power Dissipation	P_D	100	W
Single pulse avalanche energy （note2）	E_{AS}	144	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	ºC

Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	50	ºC/W
Maximum Junction-to-Case	R_{thJC}	1.25	ºC/W

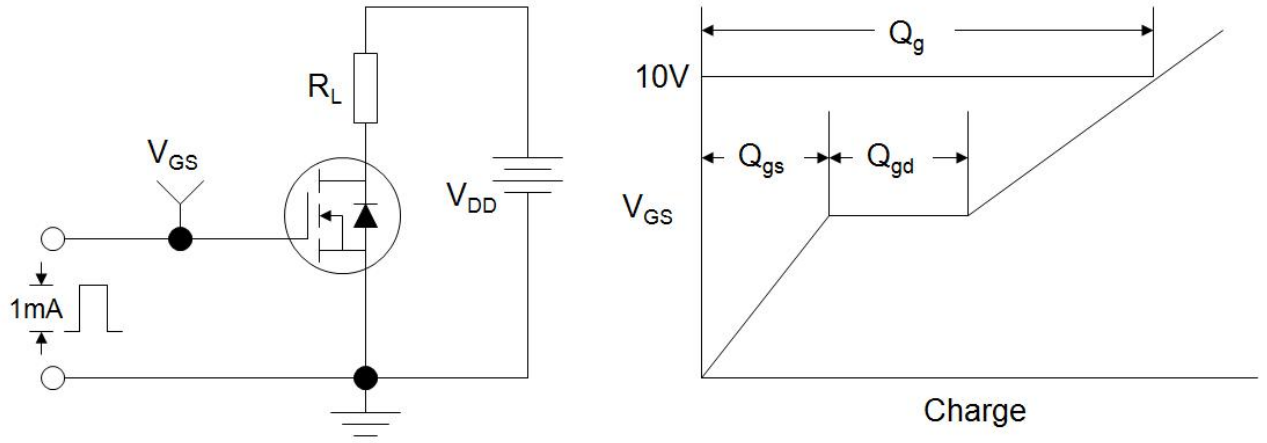
Specifications T_J = 25ºC, unless otherwise noted

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	100	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V, V_{GS} = 0V	--	--	1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.0	1.7	2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 20A	--	6.2	8.0	mΩ
		V_{GS} = 4.5V, I_D = 20A	--	7.8	9.5	
Forward Transconductance	g_{FS}	V_{GS} = 5V, I_D = 20A	--	48	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 50V, f = 1.0MHz	--	2530	--	pF
Output Capacitance	C_{oss}		--	395	--	
Reverse Transfer Capacitance	C_{rss}		--	13	--	
Total Gate Charge	Q_g	V_{DD} = 50V, I_D = 20A, V_{GS} = 10V	--	43	--	nC
Gate-Source Charge	Q_{gs}		--	7	--	
Gate-Drain Charge	Q_{gd}		--	9	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 50V, I_D = 20A, R_G = 1.6Ω	--	10	--	ns
Turn-on Rise Time	t_r		--	8	--	
Turn-off Delay Time	$t_{d(off)}$		--	23	--	
Turn-off Fall Time	t_f		--	6	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	65	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} = 20A, V_{GS} = 0V	--	--	1.2	V
Reverse Recovery Charge	Qrr	I_F = 20A, V_{GS} = 0V di/dt=100A/us	--	75	--	nC
Reverse Recovery Time	Trr		--	42	--	ns

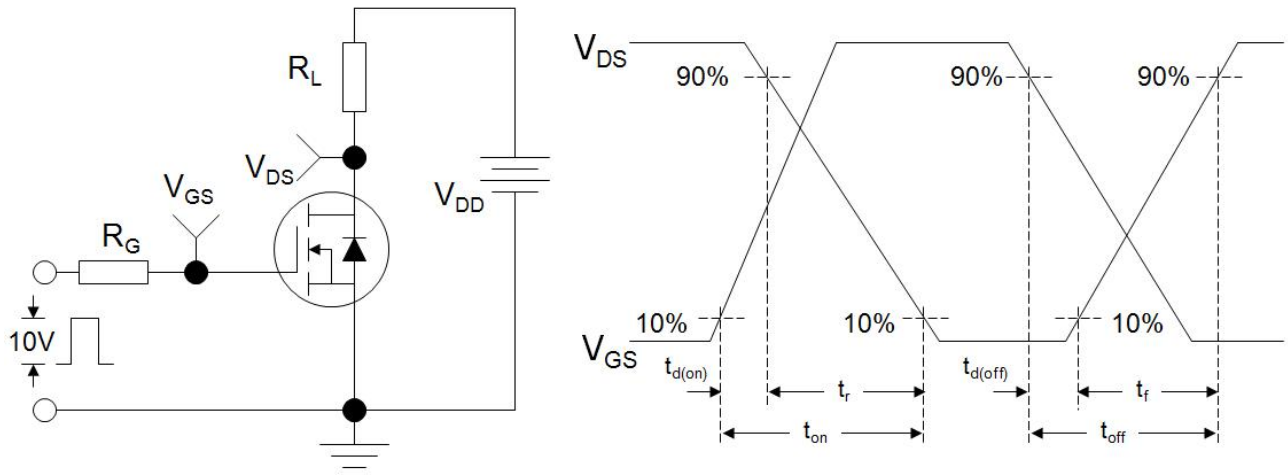
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : Tj=25℃ ,VDD=50V,VGS=10V,L=0.5mH,Rg=25Ω
   The table shows the minimum avalanche energy, which is 400mJ when the device is tested until failure
3. Identical low side and high side switch with identical R_G

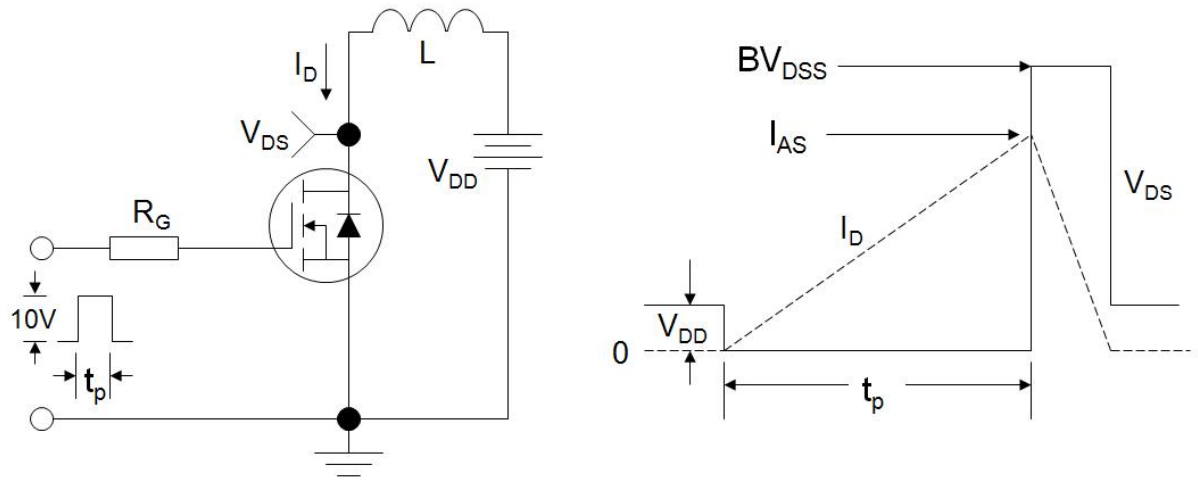
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

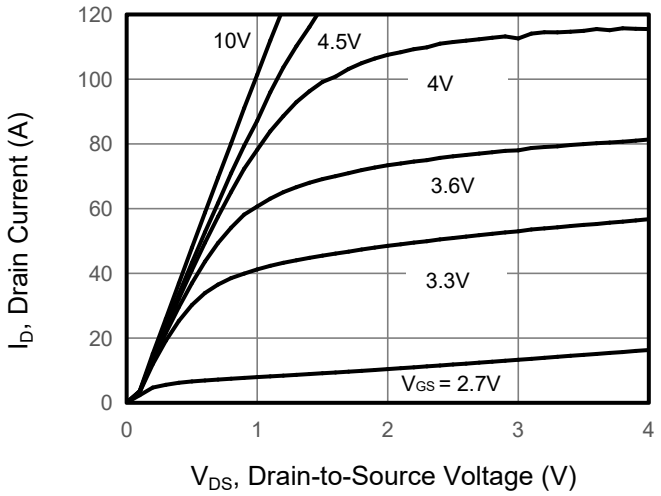


Figure 2. Transfer Characteristics

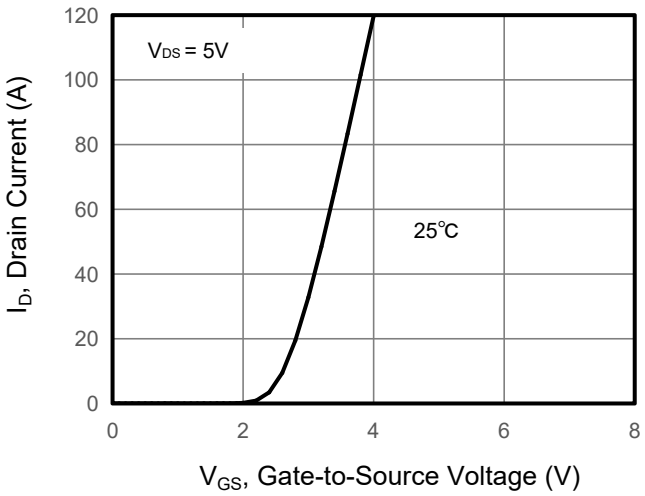


Figure 3. Drain Source On Resistance

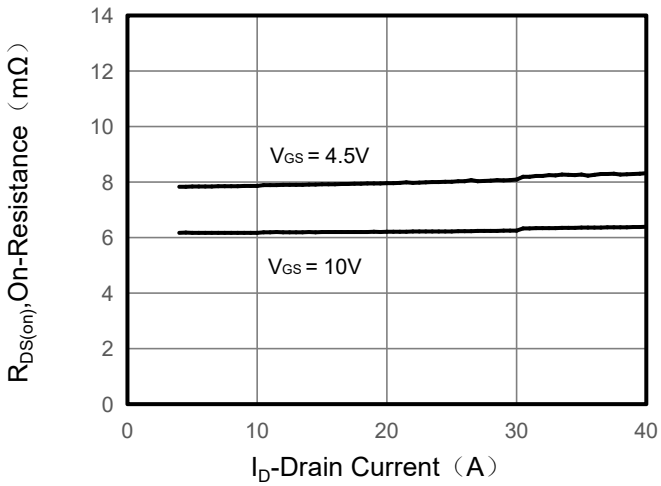


Figure 4. Gate Charge

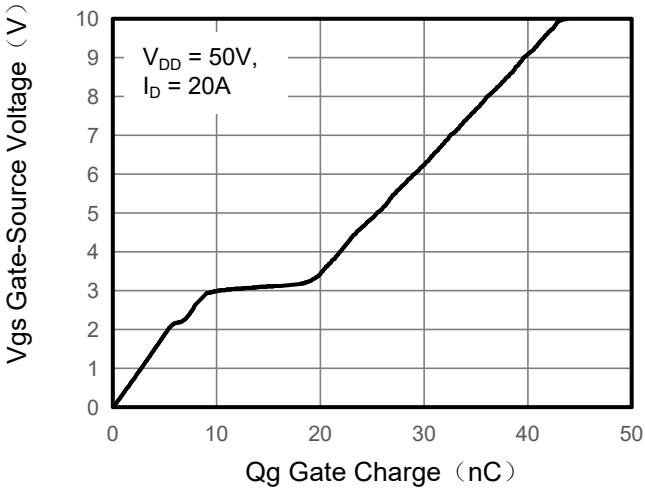


Figure 5. Capacitance

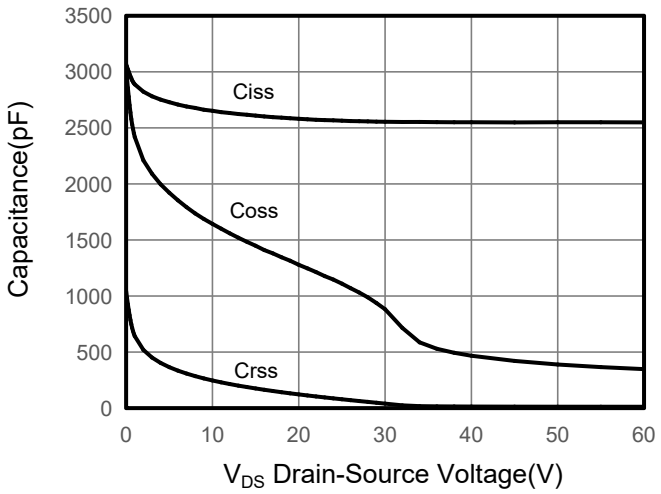
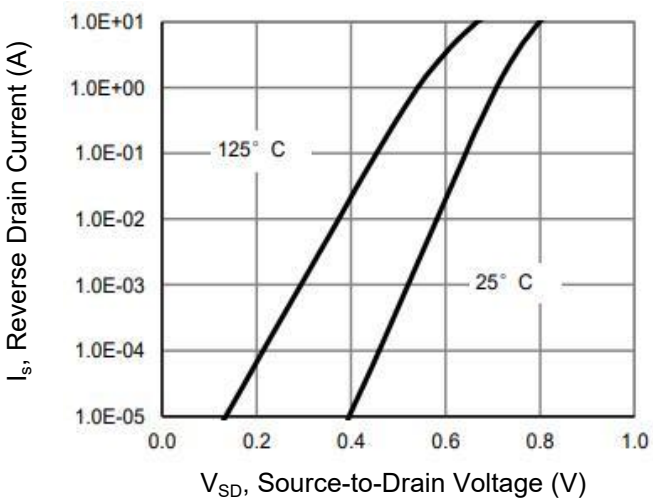


Figure 6. Source-Drain Diode Forward



Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 7. Drain-Source On-Resistance

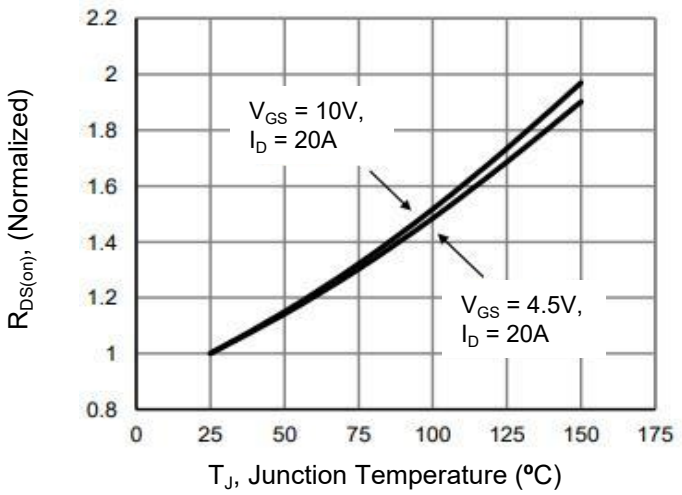


Figure 8. Safe Operation Area

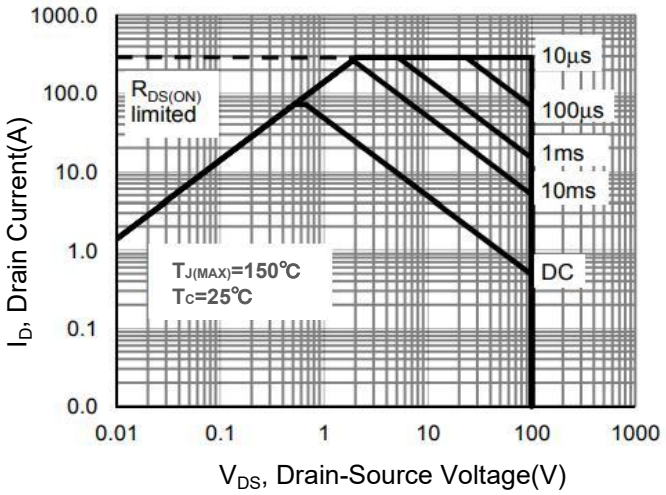
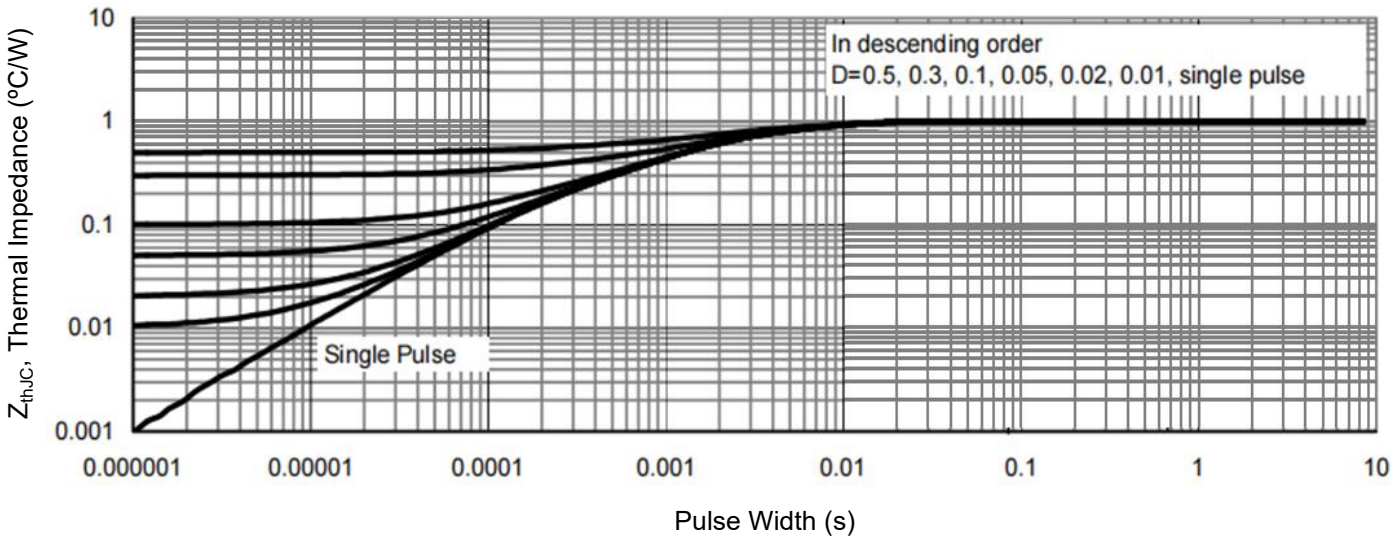
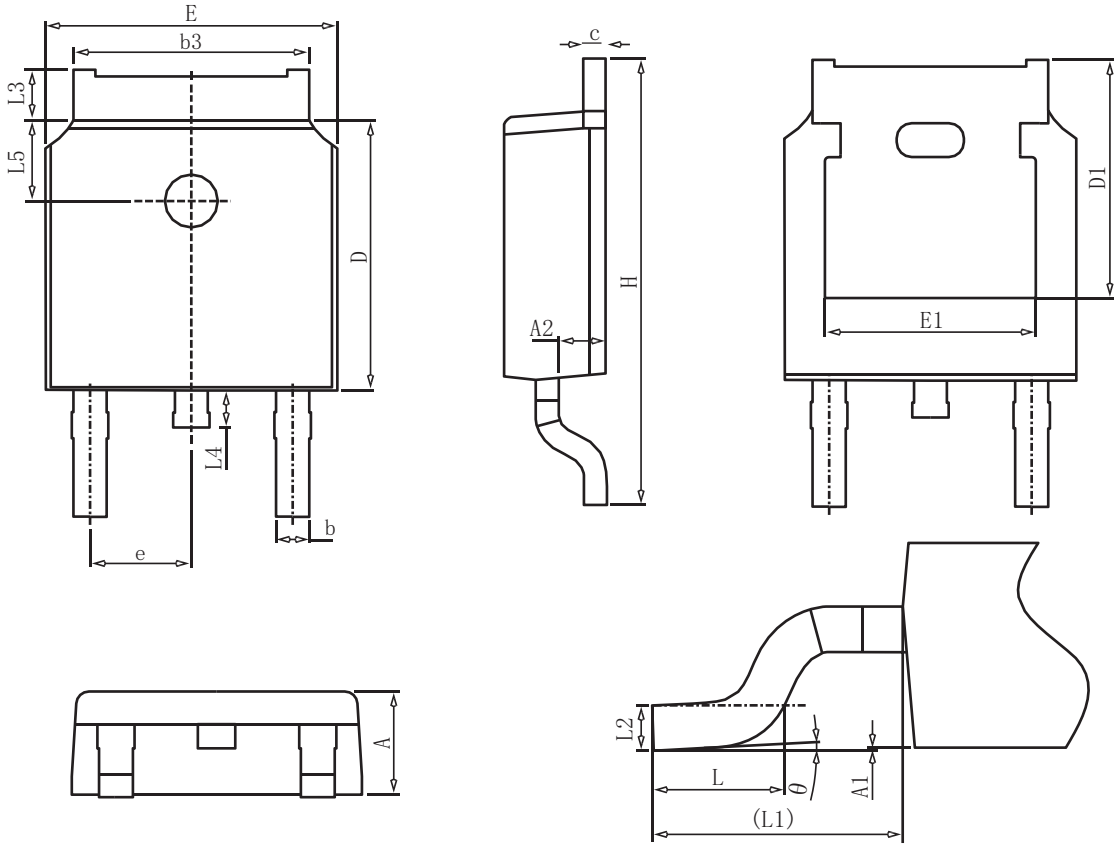


Figure 9. Normalized Maximum Transient Thermal Impedance



TO-252 Package Information



COMMON DIMENSIONS

SYMBOL	mm		
	MIN	NOM	MAX
A	2.20	2.30	2.40
A1	0.00	-	0.20
A2	0.97	1.07	1.17
b	0.68	0.78	0.90
b3	5.20	5.33	5.50
c	0.43	0.53	0.63
D	5.98	6.10	6.22
D1		5.30REF	
E	6.40	6.60	6.80
E1	4.63	-	-
e		2.286BSC	
H	9.40	10.10	10.50
L	1.38	1.50	1.75
L1		2.90REF	
L2		0.51BSC	
L3	0.88	-	1.28
L4	0.50	-	1.00
L5	1.65	1.80	1.95
θ	0°	-	8°