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January 2015

FDMS86350ET80

N-Channel PowerTrench[®] MOSFET 80 V, 198 A, 2.4 m Ω

Features

- Extended T_J rating to 175°C
- Max $r_{DS(on)}$ = 2.4 m Ω at V_{GS} = 10 V, I_D = 25 A
- Max $r_{DS(on)} = 3.2 \text{ m}\Omega$ at $V_{GS} = 8 \text{ V}$, $I_D = 22 \text{ A}$
- Advanced Package and Silicon combination for low r_{DS(on)} and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

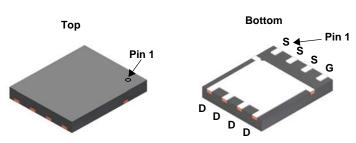


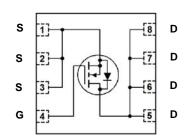
General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Applications

- Primary MOSFET
- Synchronous Rectifier
- Load Switch
- Motor Control Switch





Power 56

MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parame	eter		Ratings	Units
V _{DS}	Drain to Source Voltage			80	V
V_{GS}	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T _C = 25 °C	(Note 5)	198	
	-Continuous	T _C = 100 °C	(Note 5)	140	_
ID	-Continuous	T _A = 25 °C	(Note 1a)	25	Α
	-Pulsed		(Note 4)	693	
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	864	mJ
Б	Power Dissipation	T _C = 25 °C		187	W
P_{D}	Power Dissipation	T _A = 25 °C	(Note 1a)	3.3	VV
T _J , T _{STG}	Operating and Storage Junction Tempera	Operating and Storage Junction Temperature Range			°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	45	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86350ET	FDMS86350ET80	Power 56	13 "	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		45		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 64 V, V _{GS} = 0 V			1	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	2.5	3.8	4.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		-12		mV/°C
		V _{GS} = 10 V, I _D = 25 A		2.0	2.4	
r _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 8 \text{ V}, I_D = 22 \text{ A}$		2.5	3.2	mΩ
, ,		$V_{GS} = 10 \text{ V}, I_D = 25 \text{ A}, T_J = 125 \text{ °C}$		3.1	3.8	
9 _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 25 A		70		S

Dynamic Characteristics

C _{iss}	Input Capacitance	10 1/ 1/ 0 1/		8030		pF
C _{oss}	Output Capacitance	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz		1370		pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1011 12		31		pF
R_g	Gate Resistance		0.1	1.1	3	Ω

Switching Characteristics

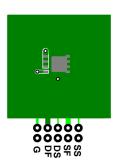
t _{d(on)}	Turn-On Delay Time		50	80	ns
t _r	Rise Time	V _{DD} = 40 V, I _D = 25 A,	34	55	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	40	65	ns
t _f	Fall Time		11	20	ns
Q_g	Total Gate Charge	V _{GS} = 0 V to 10 V	110	155	nC
Qg	Total Gate Charge	$V_{GS} = 0 \text{ V to 8 V}$ $V_{DD} = 40 \text{ V},$	90	127	nC
Q _{gs}	Gate to Source Charge	I _D = 25 A	46		nC
Q_{gd}	Gate to Drain "Miller" Charge		23		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.1 A (Note 2)	0.71	1.2	V
	Source to Drain blode Forward voltage	$V_{GS} = 0 \text{ V}, I_S = 25 \text{ A}$ (Note 2)	0.79	1.3	
t _{rr}	Reverse Recovery Time	1 25 A di/dt 100 A/va	63	101	ns
Q _{rr}	Reverse Recovery Charge	$I_F = 25 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s}$	62	100	nC

Notes:

1. R_{0JA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0CA} is determined by the user's board design.



a. 45 °C/W when mounted on a 1 in² pad of 2 oz copper.



b. 115 °C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test: Pulse Width < 300 $\mu\text{s},$ Duty cycle < 2.0%.
- 3. E_{AS} of 864 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 24 A, V_{DD} = 80 V, V_{GS} = 10 V, 100% test at L = 0.1 mH, I_{AS} = 74 A.
- 4. Pulse Id please refer to Fig.11 SOA curve for more details.
- 5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics $T_J = 25$ °C unless otherwise noted

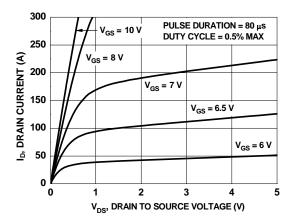


Figure 1. On-Region Characteristics

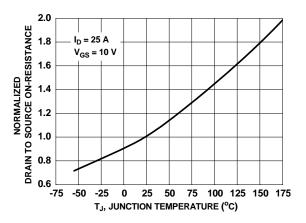


Figure 3. Normalized On-Resistance vs Junction Temperature

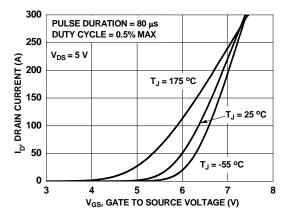


Figure 5. Transfer Characteristics

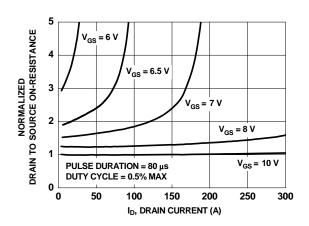


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

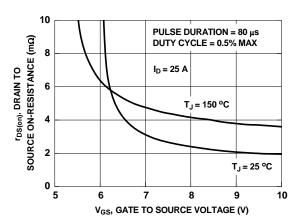


Figure 4. On-Resistance vs Gate to Source Voltage

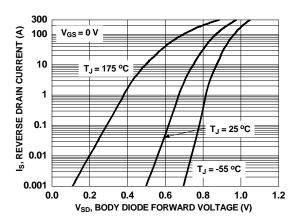


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

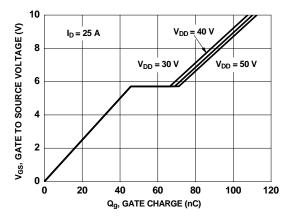


Figure 7. Gate Charge Characteristics

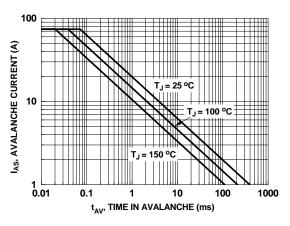


Figure 9. Unclamped Inductive Switching Capability

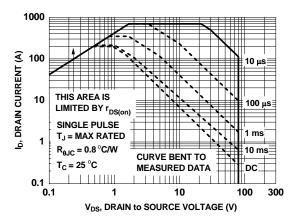


Figure 11. Forward Bias Safe Operating Area

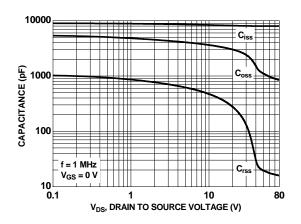


Figure 8. Capacitance vs Drain to Source Voltage

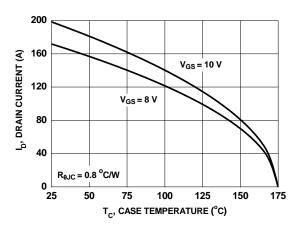


Figure 10. Maximum Continuous Drain Current vs Case Temperature

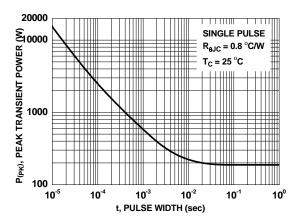


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

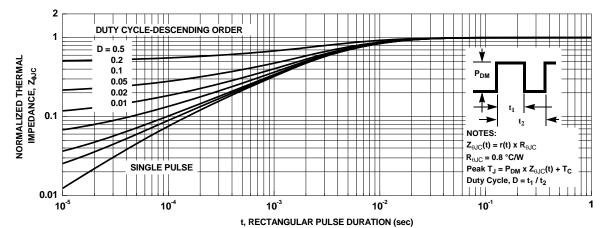
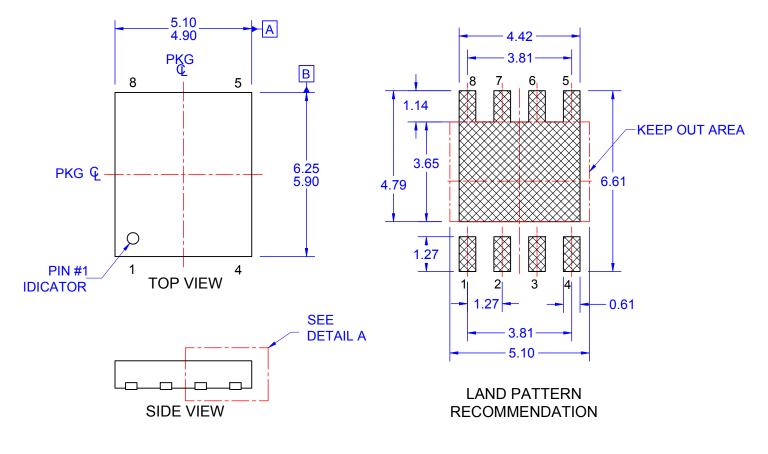
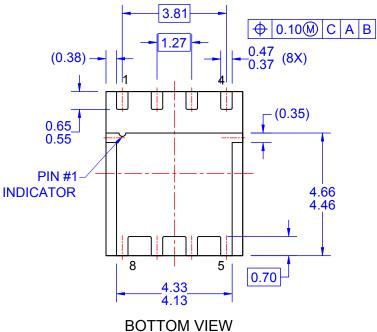
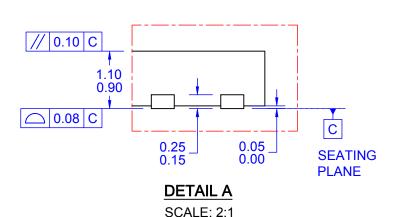


Figure 13. Junction-to-Case Transient Thermal Response Curve







NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
- F) DRAWING FILE NAME: PQFN08JREV3.



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