### XP10NA8R4IT

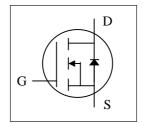
### **Halogen-Free Product**



# N-CHANNEL ENHANCEMENT MODE

#### POWER MOSFET

- ▼ 100% R<sub>q</sub> & UIS Test
- **▼** Simple Drive Requirement
- **▼** Fast Switching Characteristic
- **▼** RoHS Compliant & Halogen-Free

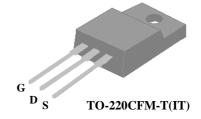


$BV_{DSS}$	100V
R <sub>DS(ON)</sub>	$\mathbf{8.4m}\Omega$
$I_D$	44A

### **Description**

XP10NA8R4 series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-220CFM package is widely preferred for all commercial-industrial through hole applications. The mold compound provides a high isolation voltage capability and low thermal resistance between the tab and the external heat-sink.



### Absolute Maximum Ratings@T<sub>i</sub>=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	100	V
$V_{GS}$	Gate-Source Voltage	<u>+</u> 20	V
I <sub>D</sub> @T <sub>C</sub> =25°C	Drain Current, V <sub>GS</sub> @ 10V	44	А
I <sub>D</sub> @T <sub>C</sub> =100°C	Drain Current, V <sub>GS</sub> @ 10V	28	Α
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	180	А
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation	32	W
P <sub>D</sub> @T <sub>A</sub> =25°C	Total Power Dissipation	1.92	W
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>3</sup>	125	mJ
$T_{STG}$	Storage Temperature Range	-55 to 150	$^{\circ}\!\mathbb{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^{\circ}\!\mathbb{C}$

#### **Thermal Data**

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	3.9	°C/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient	65	°C/W



## Electrical Characteristics@T<sub>j</sub>=25°C(unless otherwise specified)

Parameter	Test Conditions	Min.	Тур.	Max.	Units
Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	100	-	-	V
Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =24A	-	-	8.4	mΩ
Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_{D}=250uA$	2	ı	4	V
Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =24A	-	47	-	S
Drain-Source Leakage Current	V <sub>DS</sub> =80V, V <sub>GS</sub> =0V	-	-	25	uA
Gate-Source Leakage	V <sub>GS</sub> = <u>+</u> 20V, V <sub>DS</sub> =0V	-	-	<u>+</u> 0.1	uA
Total Gate Charge <sup>4</sup>	I <sub>D</sub> =24A	-	42	67.2	nC
Gate-Source Charge <sup>4</sup>	V <sub>DS</sub> =50V	-	11	-	nC
Gate-Drain ("Miller") Charge <sup>4</sup>	V <sub>GS</sub> =10V	-	16	-	nC
Turn-on Delay Time <sup>4</sup>	V <sub>DS</sub> =50V	-	14	-	ns
Rise Time <sup>4</sup>	I <sub>D</sub> =24A	-	60	-	ns
Turn-off Delay Time⁴	$R_G=7.5\Omega$	-	35	-	ns
Fall Time <sup>4</sup>	V <sub>GS</sub> =10V	-	70	-	ns
Input Capacitance <sup>4</sup>	V <sub>GS</sub> =0V	-	2030	3248	pF
Output Capacitance <sup>4</sup>	V <sub>DS</sub> =80V	-	300	-	pF
Reverse Transfer Capacitance <sup>4</sup>	f=1.0MHz	-	20	-	pF
Gate Resistance	f=1.0MHz	-	0.7	1.4	Ω
	Drain-Source Breakdown Voltage  Static Drain-Source On-Resistance <sup>2</sup> Gate Threshold Voltage  Forward Transconductance  Drain-Source Leakage Current  Gate-Source Leakage  Total Gate Charge <sup>4</sup> Gate-Source Charge <sup>4</sup> Gate-Drain ("Miller") Charge <sup>4</sup> Turn-on Delay Time <sup>4</sup> Rise Time <sup>4</sup> Turn-off Delay Time <sup>4</sup> Fall Time <sup>4</sup> Input Capacitance <sup>4</sup> Output Capacitance <sup>4</sup> Reverse Transfer Capacitance <sup>4</sup>	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Drain-Source Breakdown Voltage $V_{GS}$ =0V, $I_D$ =250uA 100 - Static Drain-Source On-Resistance $V_{GS}$ =10V, $I_D$ =24A Gate Threshold Voltage $V_{DS}$ = $V_{GS}$ , $I_D$ =250uA 2 - Forward Transconductance $V_{DS}$ =5V, $I_D$ =24A - 47 Drain-Source Leakage Current $V_{DS}$ =80V, $V_{GS}$ =0V Gate-Source Leakage $V_{GS}$ = $\frac{1}{2}$ 20V, $V_{DS}$ =0V Total Gate Charge $V_{DS}$ =50V - 11 Gate-Drain ("Miller") Charge $V_{DS}$ =50V - 16 Turn-on Delay Time $V_{DS}$ =50V - 14 Rise Time $V_{DS}$ =50V - 35 Fall Time $V_{DS}$ =10V - 70 Input Capacitance $V_{DS}$ =80V - 300 Reverse Transfer Capacitance $V_{DS}$ =80V - 300 Reverse Transfer Capacitance $V_{DS}$ =80V - 2030	Drain-Source Breakdown Voltage $V_{GS}$ =0V, $I_D$ =250uA         100         -         -           Static Drain-Source On-Resistance² $V_{GS}$ =10V, $I_D$ =24A         -         -         8.4           Gate Threshold Voltage $V_{DS}$ = $V_{GS}$ , $I_D$ =250uA         2         -         4           Forward Transconductance $V_{DS}$ =5V, $I_D$ =24A         -         47         -           Drain-Source Leakage Current $V_{DS}$ =80V, $V_{GS}$ =0V         -         -         25           Gate-Source Leakage $V_{GS}$ =±20V, $V_{DS}$ =0V         -         -         ±0.1           Total Gate Charge⁴ $I_D$ =24A         -         42         67.2           Gate-Source Charge⁴ $V_{DS}$ =50V         -         11         -           Gate-Drain ("Miller") Charge⁴ $V_{DS}$ =50V         -         16         -           Turn-on Delay Time⁴ $V_{DS}$ =50V         -         14         -           Rise Time⁴ $I_D$ =24A         -         60         -           Turn-off Delay Time⁴ $V_{CS}$ =10V         -         35         -           Fall Time⁴ $V_{CS}$ =10V         -         70         -           Input Capacitance⁴

#### **Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
$V_{SD}$	Forward On Voltage <sup>2</sup>	I <sub>S</sub> =24A, V <sub>GS</sub> =0V	-	-	1.3	V
t <sub>rr</sub>	Reverse Recovery Time <sup>4</sup>	I <sub>S</sub> =24A, V <sub>GS</sub> =0V	-	50	1	ns
Q <sub>rr</sub>	Reverse Recovery Charge <sup>4</sup>	dl/dt=100A/µs	-	70	-	nC

#### Notes:

- 1. Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Starting  $T_i$ =25°C ,  $V_{DD}$ =50V , L=0.1mH ,  $R_G$ =25 $\Omega$  ,  $V_{GS}$ =10V
- 4. Guaranteed by design.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT, AUTOMOTIVE OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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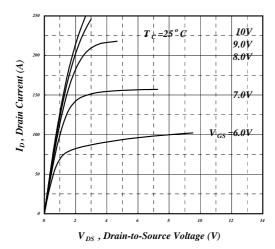


Fig 1. Typical Output Characteristics

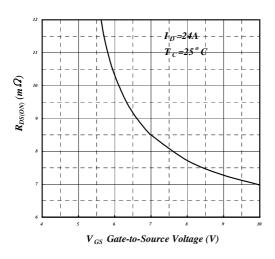


Fig 3. On-Resistance v.s. Gate Voltage

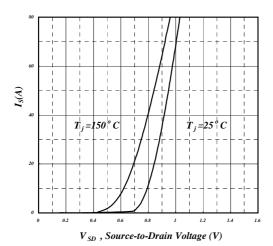


Fig 5. Forward Characteristic of Reverse Diode

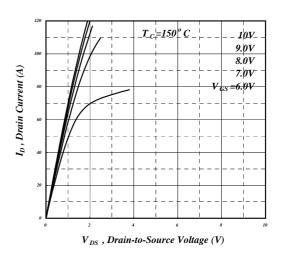


Fig 2. Typical Output Characteristics

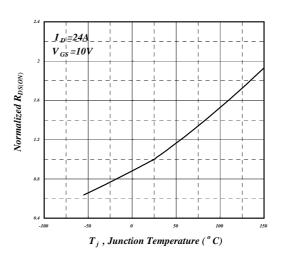


Fig 4. Normalized On-Resistance v.s. Junction Temperature

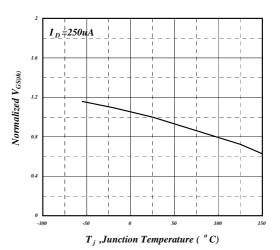


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

f=1.0MHz



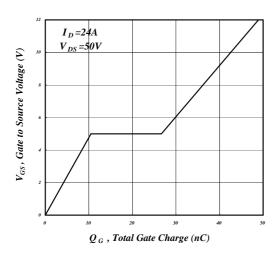


Fig 7. Gate Charge Characteristics

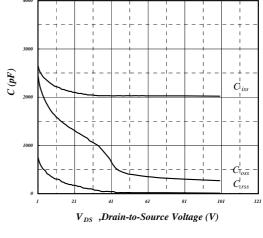


Fig 8. Typical Capacitance Characteristics

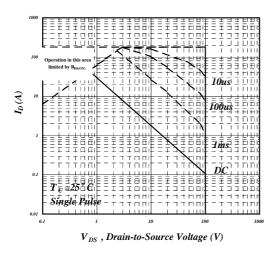


Fig 9. Maximum Safe Operating Area

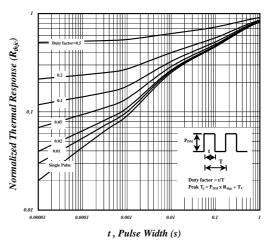


Fig 10. Effective Transient Thermal Impedance

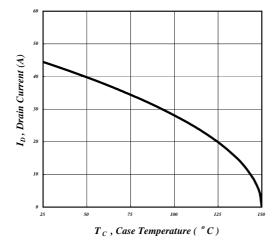


Fig 11. Drain Current v.s. Case Temperature

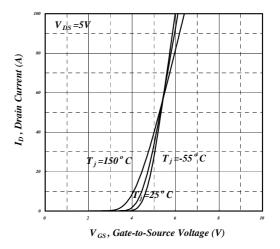


Fig 12. Transfer Characteristics



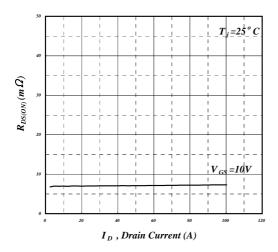
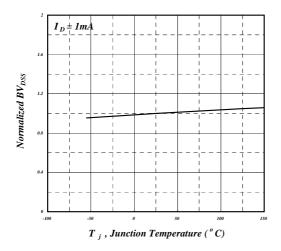


Fig 13. Typ. Drain-Source on State Resistance



 $\label{eq:bydef} \textbf{Fig 15. Normalized BV}_{DSS} \ \ \textbf{v.s. Junction} \\ \textbf{Temperature}$ 

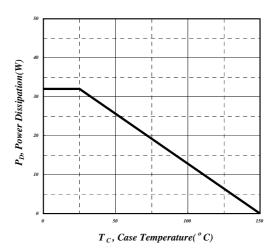
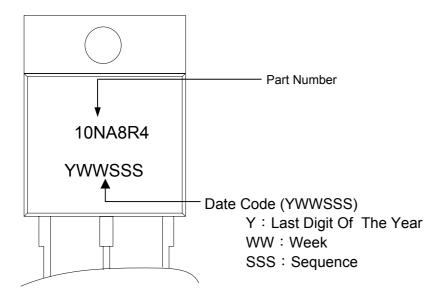


Fig 14. Total Power Dissipation

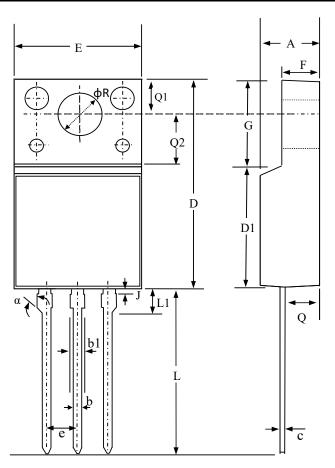


### **MARKING INFORMATION**





# Package Outline: TO-220CFM-T



SYMBOLS	Millimeters			
	MIN	NOM	MAX	
A	4.30	4.50	4.70	
b	0.54	0.69	0.84	
b1	0.99	1.14	1.29	
c	0.45	0.62	0.79	
D	14.70	15.30		
D1	8.5 Ref.			
e	2.54 Ref.			
E	9.70	10.00	10.30	
F	2.50	2.70	2.90	
G	6.30	6.70	7.10	
L	12.50	13.00	13.50	
L1	1.80	2.30	2.80	
J	0.10	0.20		
Q	2.50	2.60	2.90	
Q1	2.90	3.10	3.30	
Q2	3.5 Ref.			
φR	3.00	3.20	3.40	
α	45° Ref.			

- 1.All dimension are in millimeters.
- 2.Dimension does not include burrs and mold flash/protrusions.
- 3.The outline schematic is not to scale and slightly different from the actual product appearance.





### **TO-220CFM-T FOOTPRINT:**

