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Vishay Siliconix

Automotive N-Channel 80 V (D-S) 175 °C MOSFET

PowerPAK® SO-8L

Bottom View

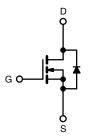
PRODUCT SUMMARY				
V _{DS} (V)	80			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0075			
I _D (A)	118			
Configuration	Single			
Package	PowerPAK SO-8L			

Top View

FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % Rq and UIS tested
- Material categorization: for definitions of compliance please see www.vishav.com/doc?99912





N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25 ^{\circ}C$, unles	s otherwise noted)	
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V _{DS}	80	V
Gate-source voltage		V_{GS}	± 20	V
Continuous drain current	T _C = 25 °C	,	118	
Continuous drain current	T _C = 125 °C	I _D	68	
Continuous source current (diode conduction)		Is	210	Α
Pulsed drain current		I _{DM}	240	
Single pulse avalanche current	L = 0.1 mH	I _{AS}	32	
Single pulse avalanche energy	L=0.11III	E _{AS}	51	mJ
Maying an away dispination	T _C = 25 °C	D	234	W
Maximum power dissipation	T _C = 125 °C	P_{D}	78	VV
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) b			260	C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount a	R_{thJA}	42	°C/W
Junction-to-case (drain)		R_{thJC}	0.64	G/ VV

Notes

- a. When mounted on 1" square PCB (FR4 material)
- b. See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection



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PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static	•	•					
Drain-source breakdown voltage	V _{DS}	V _{GS}	= 0, I _D = 250 μA	80	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	· V _{GS} , I _D = 250 μA	2.2	2.7	3.5	V
Gate-source leakage	I _{GSS}	V _{DS} =	$0 \text{ V}, \text{ V}_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA
		$V_{GS} = 0 V$	V _{DS} = 80 V	-	-	1	
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 80 V, T _J = 125 °C	-	-	50	μΑ
		$V_{GS} = 0 V$	V _{DS} = 80 V, T _J = 175 °C	-	-	250	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	30	-	-	Α
		V _{GS} = 10 V	I _D = 15 A	-	0.0060	0.0075	
Drain-source on-state resistance a	R _{DS(on)}	V _{GS} = 10 V	I _D = 15 A, T _J = 125 °C	-	-	0.0124	Ω
		V _{GS} = 10 V	I _D = 15 A, T _J = 175 °C	-	-	0.0156	
Forward transconductance b	9 _{fs}	V_{DS}	= 15 V, I _D = 10 A	-	67	-	S
Dynamic ^b							
Input capacitance	C _{iss}			-	2484	3478	
Output capacitance	C _{oss}	$V_{GS} = 0 V$	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$	-	1029	1441	рF
Reverse transfer capacitance	C _{rss}			-	76	107	
Total gate charge ^c	Qg			-	46	69	
Gate-source charge ^c	Q_{gs}	$V_{GS} = 10 \text{ V}$	$V_{DS} = 40 \text{ V}, I_{D} = 30 \text{ A}$	-	12	-	nC
Gate-drain charge c	Q_{gd}			-	13	-	
Gate resistance	Rg		f = 1 MHz	0.6	1.2	1.8	Ω
Turn-on delay time ^c	t _{d(on)}			-	12	18	
Rise time ^c	t _r	$V_{DD} =$	40 V, $R_L = 1.33 \Omega$,	-	4	6	
Turn-off delay time ^c	t _{d(off)}	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		35	ns 5		
Fall time ^c	t _f			-	5	8	1
Source-Drain Diode Ratings and Chara	acteristics ^b						•
Pulsed current ^a	I _{SM}			-	-	240	Α
Forward voltage	V _{SD}	I _F =	15 A, V _{GS} = 0 V	-	-	1.1	V
Body diode reverse recovery time	t _{rr}			-	37	74	ns
Body diode reverse recovery charge	Q _{rr}	1 10 4 11/11 100 4/		-	38	76	nC
Reverse recovery fall time	ta] I _F = 10	A, di/dt = 100 A/μs	-	21	-	
Reverse recovery rise time	t _b	7		-	15	-	ns
Body diode peak reverse recovery current	I _{RM(REC)}			-	-2.0	-	Α

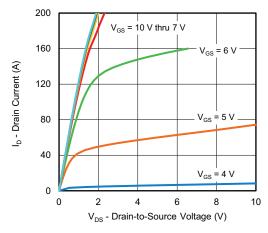
Notes

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

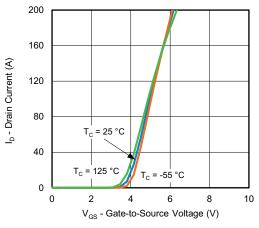
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



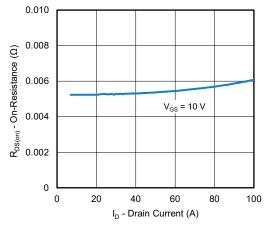
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



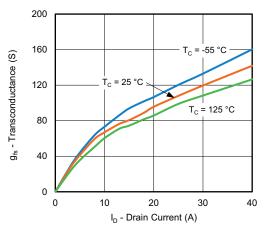
Output Characteristics



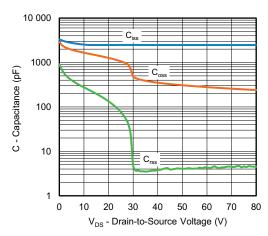
Transfer Characteristics



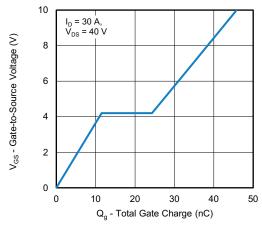
On-Resistance vs. Drain Current



Transconductance



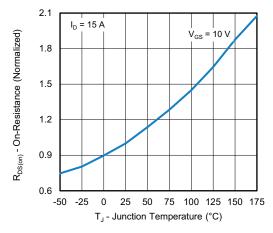
Capacitance



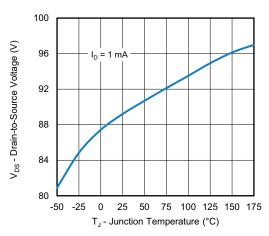
Gate Charge



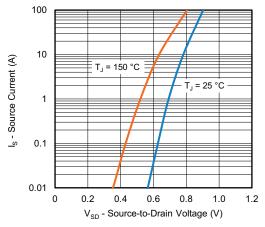
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



On-Resistance vs. Junction Temperature



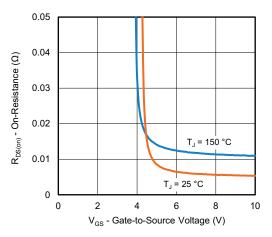
Drain Source Breakdown vs. Junction Temperature



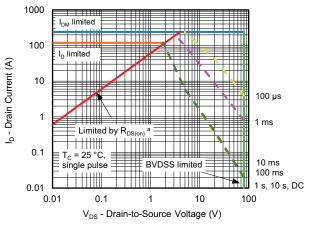
Source Drain Diode Forward Voltage

Note

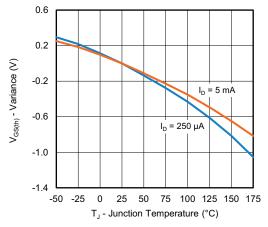
a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified



On-Resistance vs. Gate-to Source Voltage



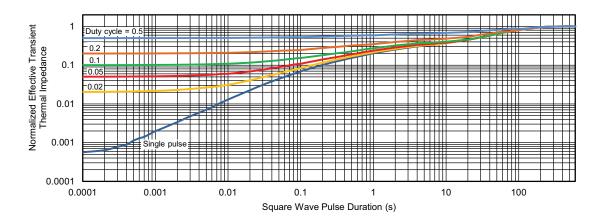
Safe Operating Area



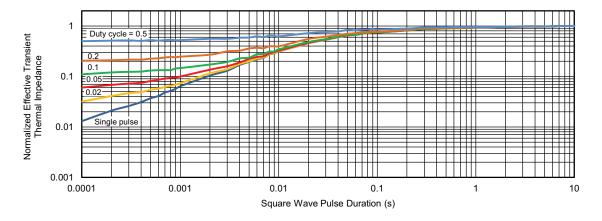
Threshold Voltage



TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg262032.



PowerPAK® SO-8L (PPKSO8LWLA) Case Outline 3



DIM.		MILLIMETERS			INCHES			
DIIVI.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
Α	1.00	1.05	1.10	0.039	0.041	0.043		
A1	0.00		0.127	0.000		0.005		
b	0.33	0.41	0.49	0.013	0.016	0.019		
b1	0.43	0.51	0.59	0.017	0.020	0.023		
b2	4.00	4.10	4.20	0.157	0.161	0.165		
С	0.15	0.20	0.25	0.006	0.008	0.010		
D1	4.80	4.90	5.00	0.189	0.193	0.197		
D2	3.86	3.96	4.06	0.152	0.156	0.160		
D5	0.51	0.61	0.71	0.020	0.024	0.028		
D6	2.64	2.74	2.84	0.104	0.108	0.112		
е		1.27 BSC		0.050 BSC				
E	6.05	6.15	6.25	0.238	0.242	0.246		
E1	4.27	4.37	4.47	0.168	0.172	0.176		
E2	3.18	3.28	3.38	0.125	0.129	0.133		
E3	3.48	3.58	3.68	0.137	0.141	0.145		
E4	2.72	2.82	2.92	0.107	0.111	0.115		
E5	0.71	0.81	0.91	0.028	0.032	0.036		
L	0.62	0.72	0.82	0.024	0.028	0.032		
L1	0.92	1.07	1.22	0.036	0.042	0.048		
W1	0.31	0.41	0.51	0.012	0.016	0.020		
W4	0.31	0.36	0.41	0.012	0.014	0.016		
z1	0.37	0.47	0.57	0.015	0.019	0.022		
z2	0.99	1.09	1.19	0.039	0.043	0.047		
θ	0°		5°	0°		5°		

Note

• Millimeter will govern

Revison: 18-Sep-2023 1 Document Number: 76666



Recommended Land Pattern PowerPAK® SO-8L Single Short Ear



Dimensions in Millimeters (Inches)

Revision: 24-Aug-2021 1 Document Number: 78020



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