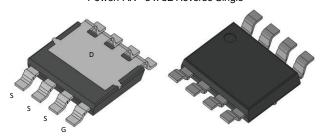


www.vishay.com

Vishay Siliconix

Automotive N-Channel 80 V (D-S) 175 °C MOSFET

PowerPAK® 8 x 8L Reverse Single



Top	View
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Bottom View

- 45

- TrenchFET® power MOSFET
- AEC-Q101 qualified

FEATURES

- 100 % Rq and UIS tested
- Thin 1.9 mm height
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



FREE

PRODUCT SUMMARY				
V _{DS} (V)	80			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0014			
I _D (A)	430			
Configuration	Single			
Package	PowerPAK 8 x 8L Reverse			

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G O	
N-Channel MOSFET (5

ABSOLUTE MAXIMUM RATINGS	(T _C = 25 °C, unless	s otherwise noted)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V_{DS}	80	V	
Gate-source voltage	V_{GS}	± 20			
Continuous drain current	T _C = 25 °C	- I _D	430		
	T _C = 125 °C		250		
Continuous source current (diode conduction)		I _S	450	Α	
Pulsed drain current ^a		I _{DM}	1200		
Single pulse avalanche current	L = 0.1 mH	I _{AS}	65		
Single pulse avalanche energy	L = 0.1 IIII	E _{AS}	211	mJ	
Maximum power dissipation	T _C = 25 °C	D	600	W	
	T _C = 125 °C	P _D	200		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175		
Soldering recommendations (peak temperature) c			260	°C	

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	LIMIT	UNIT		
Junction-to-ambient	PCB mount b	R_{thJA}	40	°C/W		
Junction-to-case (drain)		R _{thJC}	0.25	G/ VV		

Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. When mounted on 1" square PCB (FR4 material)
- c. See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection



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PARAMETER	SYMBOL	TES	TEST CONDITIONS		TYP.	MAX.	UNIT
Static				I.	l	<u>'</u>	
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0$, $I_D = 250 \mu A$		80	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	· V _{GS} , I _D = 250 μA	2	3	3.5	V
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
		$V_{GS} = 0 V$	V _{DS} = 80 V	-	-	1	
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 80 V, T _J = 125 °C	-	-	50	μΑ
-		V _{GS} = 0 V	V _{DS} = 80 V, T _J = 175 °C	-	-	500	
On-state drain current a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	50	-	-	Α
Drain-source on-state resistance ^a		V _{GS} = 10 V	I _D = 20 A	-	0.0012	0.0014	Ω
	R _{DS(on)}	V _{GS} = 10 V	I _D = 20 A, T _J = 125 °C	-	-	0.00281	
		V _{GS} = 10 V	I _D = 20 A, T _J = 175 °C	-	-	0.0037	
Forward transconductance b	9 _{fs}	V _{DS} = 15 V, I _D = 15 A		-	82	-	S
Dynamic ^b							
Input capacitance	C _{iss}			-	11 435	16 009	
Output capacitance	Coss	$V_{GS} = 0 V$	$V_{GS} = 0 \text{ V}$ $V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$	-	1896	2655	pF
Reverse transfer capacitance	C _{rss}			-	92	129	
Total gate charge c	Qg			-	183	240	
Gate-source charge ^c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 40 \text{ V}, I_{D} = 10 \text{ A}$	-	47	-	nC
Gate-drain charge ^c	Q _{gd}			-	85	-	1
Gate resistance	R_g	f = 1 MHz		0.7	1.3	2	Ω
Turn-on delay time ^c	t _{d(on)}				21	28	ns
Rise time ^c	t _r	$V_{DD} = 40 \text{ V}, \text{ R}_L = 0.8 \Omega$ $I_D \cong 50 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_g = 1 \Omega$		-	80	105	
Turn-off delay time ^c	t _{d(off)}			-	65	85	
Fall time ^c	t _f			-	20	28	
Source-Drain Diode Ratings and Cha	aracteristics ^b						
Pulsed current a	I _{SM}			-	-	1100	Α
Forward voltage	V _{SD}	$I_{F} = 40 \text{ A}, V_{GS} = 0 \text{ V}$		_	0.7	1.2	V

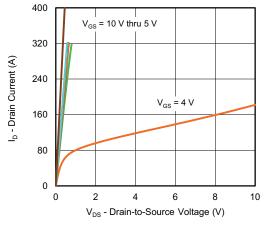
Notes

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

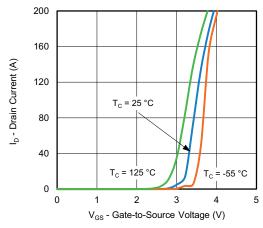
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



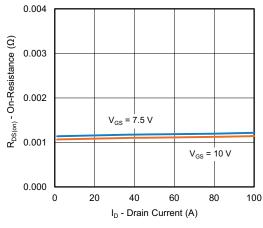
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



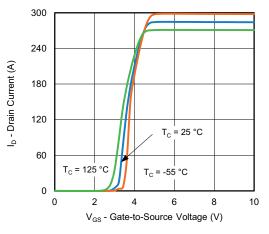




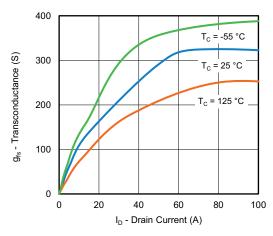
Transfer Characteristics



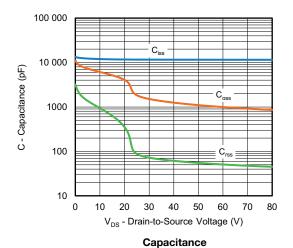
On-Resistance vs. Drain Current



Transfer Characteristics

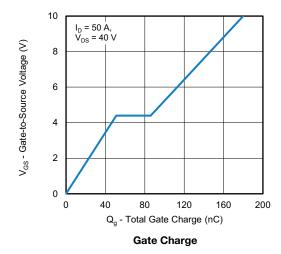


Transconductance





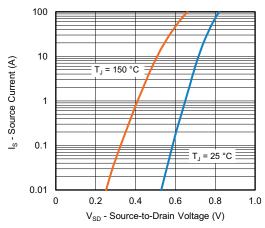
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

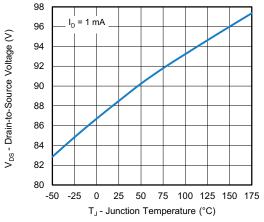


I_D = 30 A R_{DS(on)} - On-Resistance (Normalized) 2.0 V_{GS} = 10 V 1.6 $V_{GS} = 7.5 \text{ V}$ 1.2 0.8 0.4 -50 -25 0 25 50 75 100 125 150 175 T_{.1} - Junction Temperature (°C)

2.4

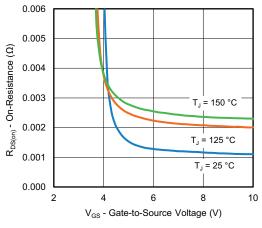
On-Resistance vs. Junction Temperature

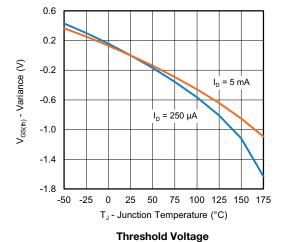




Source Drain Diode Forward Voltage

Drain Source Breakdown vs. Junction Temperature

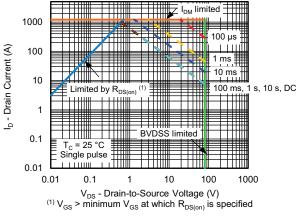




On-Resistance vs. Gate-to-Source Voltage

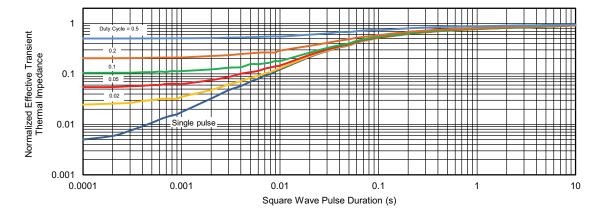


TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



Safe Operating Area

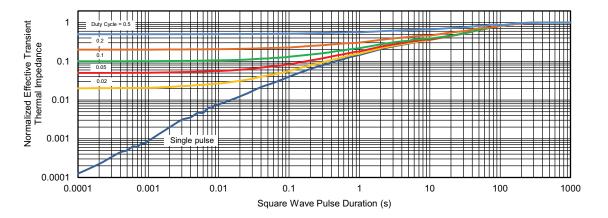
THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)

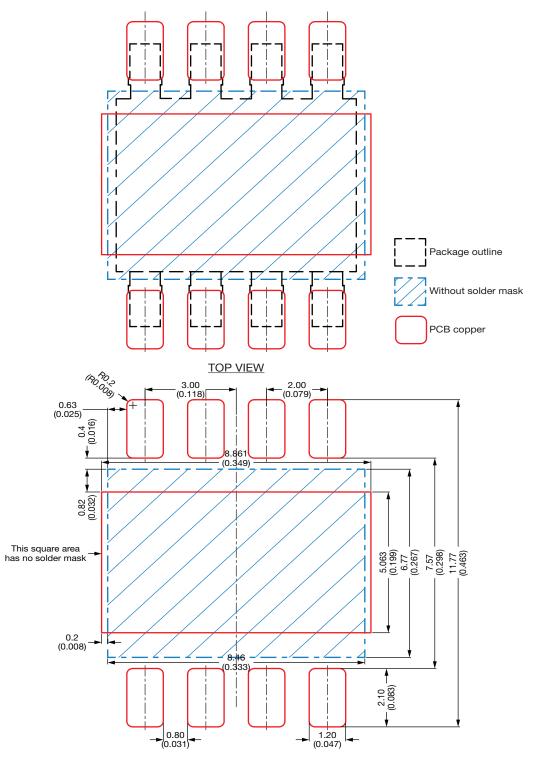


Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71298.



Recommended Land Pattern PowerPAK® 8 x 8LR



Notes

- This land pattern is for reference
- Proposed stencil thickness 200 µm All dimensions are in millimeter (inches)

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DWG: 3002

Revision: 17-Apr-2023

Document Number: 63166



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