

# NTAT6H406N

## MOSFET – N-Channel

**80 V, 2.9 mΩ, 175 A**

### Features

- Low On-Resistance
- High Current Capability
- 100% Avalanche Tested
- ATPAK Package is Pin-compatible with DPAK (TO-252)
- Pb-Free, Halogen Free and RoHS Compliance

### Typical Applications

- Multi Lib Protection
- Motor Control

### Specifications

**Table 1. ABSOLUTE MAXIMUM RATING** at  $T_A = 25^\circ\text{C}$

Parameter	Symbol	Value	Unit
Drain to Source Voltage	$V_{DS}$	80	V
Gate to Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current (DC)	$I_D$	175	A
Drain Current (Pulse) $PW \leq 10$ ms, Duty Cycle $\leq 1\%$	$I_{DP}$	600	A
Power Dissipation $T_C = 25^\circ\text{C}$	$P_D$	90	W
Operating Junction and Storage Temperature	$T_J, T_{STG}$	$-55$ to $+150$	$^\circ\text{C}$
Single Pulse Drain to Source Avalanche Energy ( $L = 0.1$ mH, $I_{L(pk)} = 55$ A)	$E_{AS}$	151	mJ
Lead Temperature for Soldering Purposes, 3 mm from Case for 10 seconds	$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 2. THERMAL RESISTANCE RATINGS**

Parameter	Symbol	Value	Unit
Junction to Case Steady State ( $T_C = 25^\circ\text{C}$ )	$R_{\theta JC}$	1.38	$^\circ\text{C/W}$
Junction to Ambient (Note 1)	$R_{\theta JA}$	77.2	$^\circ\text{C/W}$

1. Surface mounted on FR4 board using a 130 mm<sup>2</sup>, 1 oz. Cu pad.

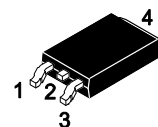
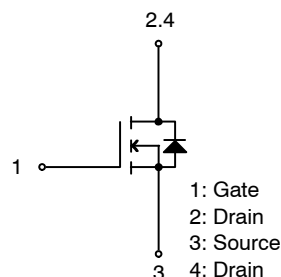


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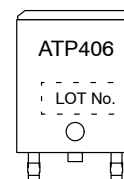
$V_{DS}$	$R_{DS(on)}$ Max	$I_D$ Max
80 V	2.9 mΩ @ 10V	175 A

### ELECTRICAL CONNECTION N-Channel



**DPAK / ATPAK  
CASE 369AM**

### MARKING DIAGRAM



### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# NTAT6H406N

**Table 3. ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = 1\text{ mA}, V_{GS} = 0\text{ V}$	80			V
Zero-Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$			10	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	2.0		4.0	V
Forward Transconductance	$g_{FS}$	$V_{DS} = 10\text{ V}, I_D = 50\text{ A}$		185		S
Static Drain to Source On-State Resistance	$R_{DS(on)}$	$I_D = 50\text{ A}, V_{GS} = 10\text{ V}$		2.2	2.9	$\text{m}\Omega$
Input Capacitance	$C_{ISS}$	$V_{DS} = 40\text{ V}, f = 1\text{ MHz}$		8040		pF
Output Capacitance	$C_{OSS}$			1120		pF
Reverse Transfer Capacitance	$C_{RSS}$			40		pF
Turn-ON Delay Time	$t_d(on)$	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V},$ $I_D = 50\text{ A}, R_G = 50\text{ }\Omega,$		77		ns
Rise Time	$t_r$			420		ns
Turn-OFF Delay Time	$t_d(off)$			310		ns
Fall Time	$t_f$			155		ns
Total Gate Charge	$Q_G$	$V_{DS} = 48\text{ V}, V_{GS} = 10\text{ V},$ $I_D = 50\text{ A}$		110		nC
Gate to Source Charge	$Q_{GS}$			32.4		nC
Gate to Drain "Miller" Charge	$Q_{GD}$			31.8		nC
Forward Diode Voltage	$V_{SD}$	$I_S = 100\text{ A}, V_{GS} = 0\text{ V}$		0.9	1.5	V
Reverse Recovery Time	$t_{RR}$	$I_S = 50\text{ A}, V_{GS} = 0\text{ V},$ $dI/dt = 100\text{ A}/\mu\text{s}$		90		ns
Reverse Recovery Charge	$Q_{RR}$			126		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# TYPICAL CHARACTERISTICS

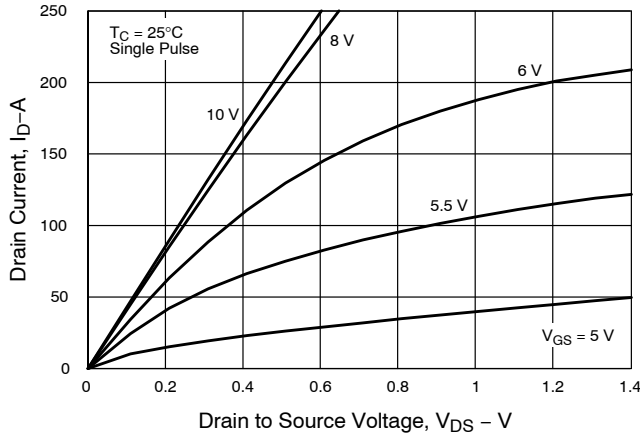


Figure 1. On-Region Characteristics

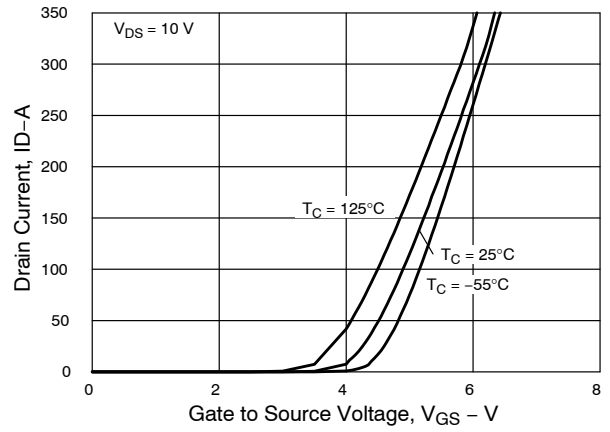


Figure 2. Transfer Characteristics

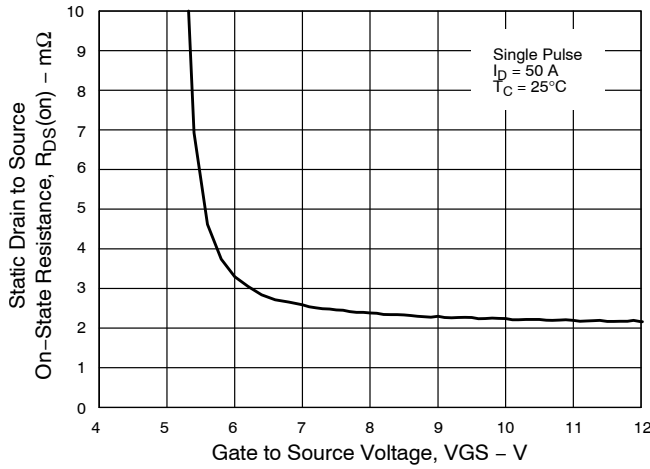


Figure 3. On-Resistance vs. Gate to Source Voltage

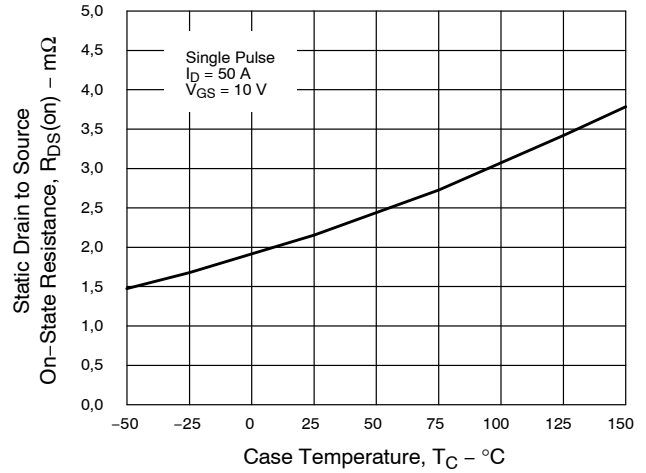


Figure 4. On-Resistance vs. Case Temperature

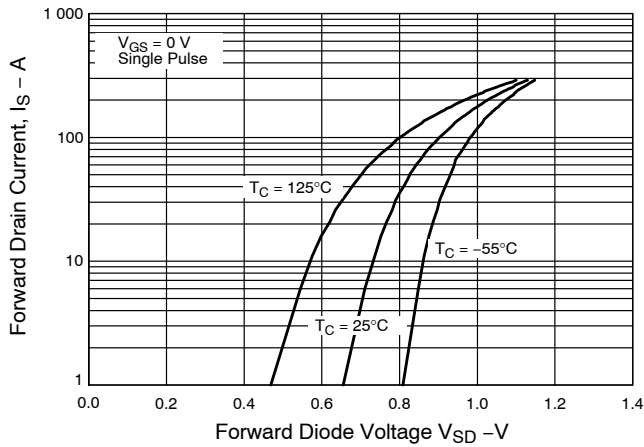


Figure 5. Diode Forward Voltage vs. Current

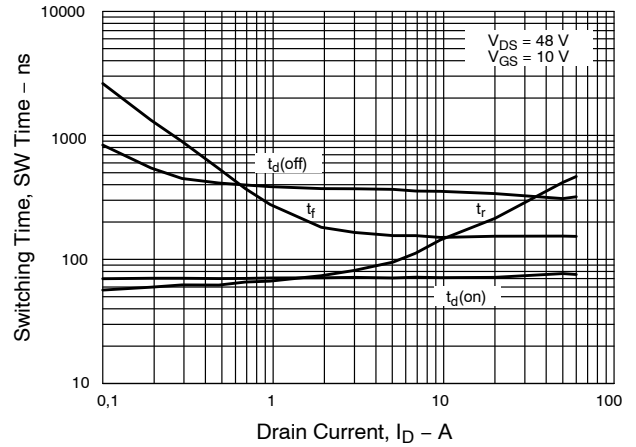


Figure 6. Switching Time vs. Drain Current

TYPICAL CHARACTERISTICS (continued)

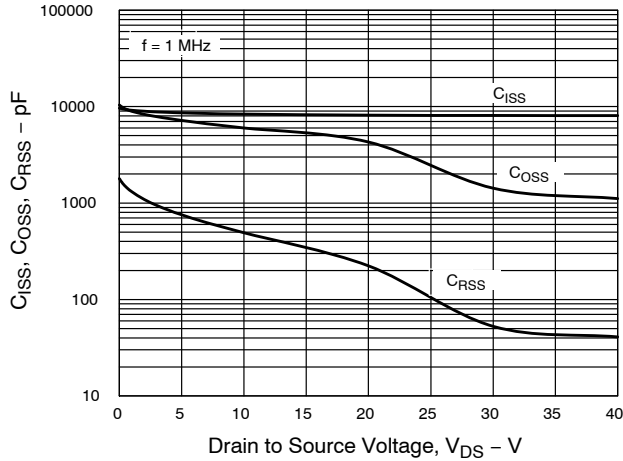


Figure 7. Capacitance Variation

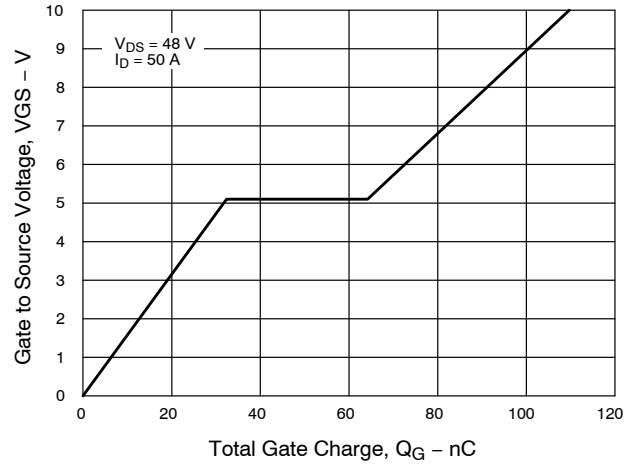


Figure 8. Gate to Source Voltage vs. Total Charge

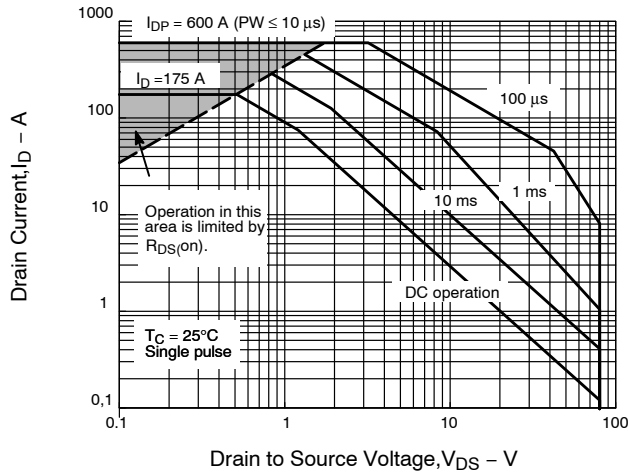


Figure 9. Safe Operating Area

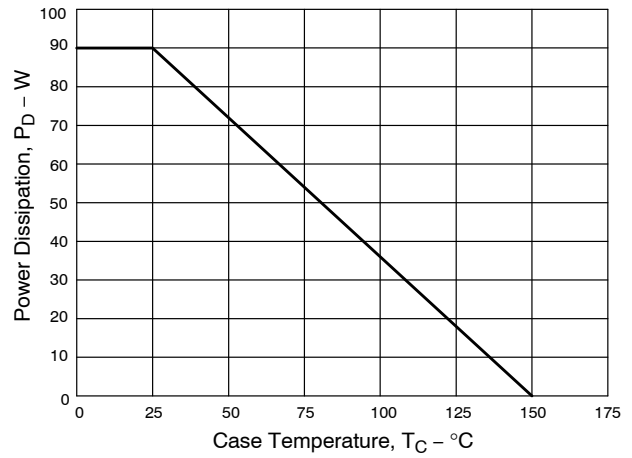


Figure 10. Power Dissipation vs. Case Temperature

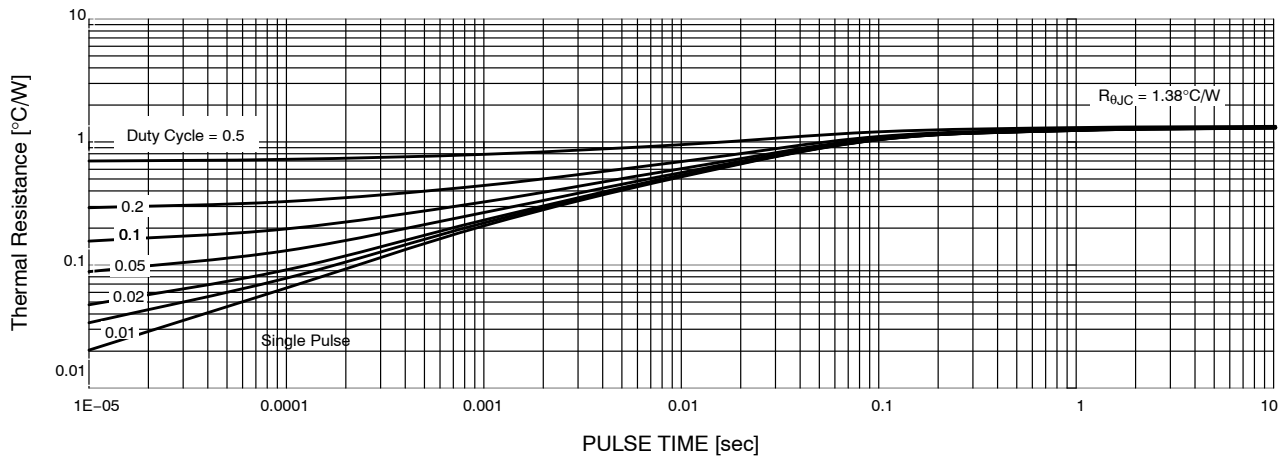


Figure 11. Thermal Response

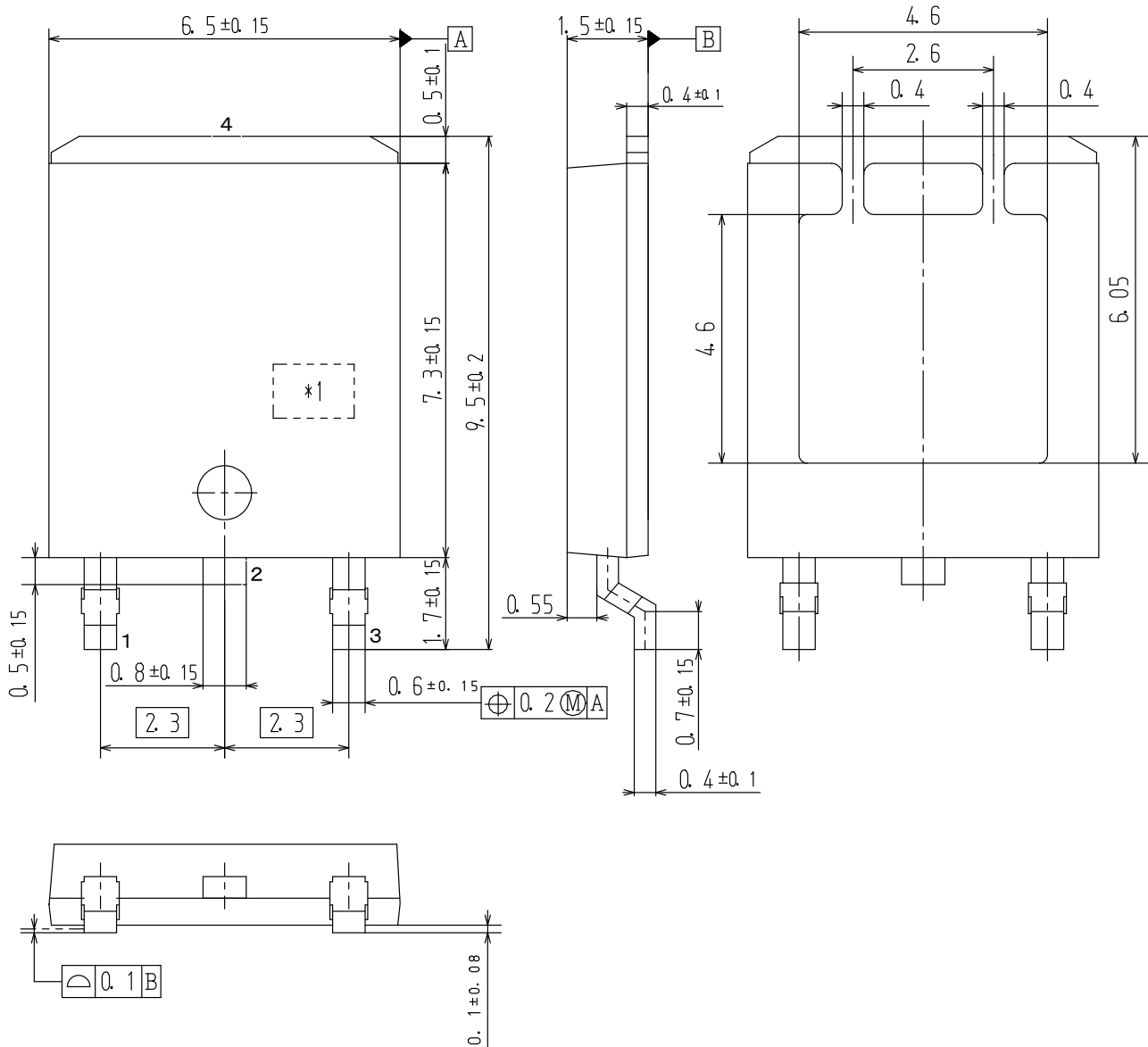
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



## DPAK (Single Gauge) / ATPAK CASE 369AM ISSUE O

DATE 29 FEB 2012



Pin2 is idle pin with electrical  
designation only carried

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