Low-Cost Impedance Tuner Utilizing Quadrature Coupled-Line Coupler for Load and Source Pull Transistor Measurement Applications

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***Abstract* — A low-cost impedance tuner, well suitable for load and source pull transistor measurements is presented. The proposed circuit consists of 3-dB quadrature coupled-line directional coupler with tuning components realized as shorted microstrip line sections with appropriate sliding shorting elements, which allow to provide any desired impedance. The theoretical analysis of the proposed circuit has been performed and the principle of circuit's behavior has been explained. An exemplary impedance tuner has been designed, manufactured and measured. The obtained measurement results prove the usefulness and demonstrate the advantages of the presented approach.**

***Index Terms* — Quadrature directional coupler, impedance tuner, source and load pull transistor measurement.**

I. Introduction

Power amplifiers are widely used devices in many industrial applications requiring high output quality, appropriate dynamic performance etc. [1]-[4]. The commonly used technique for the purpose of designing a power amplifier is source and load pull technique in which a high-power transistor's input and output are simultaneously matched in an iterative process, whereas, the gain and output power are controlled aiming to their maximization. The variation of the impedances at the input and output ports can be performed with the use of manual or automated tuning systems using passive or active impedance synthesis [5]-[6]. The passive impedance synthesis is low-cost, however the synthesized reflection coefficient is limited due to the losses. The active impedance synthesis is capable to transform the impedance to very low values, however requires additional hardware and calibration procedure, which increase cost of the entire system. Simplicity and low cost of the tools are important aspects for e.g. R&D centers for which power amplifier design is rather seldom than "regular" basis activity.

The idea of low-cost and simple manual impedance tuner has been presented in [7], where 3 dB/180° rat-race directional couplers together with two shorted transmission lines have been used as a source and load pull tuners. It has been shown that such circuits can be successfully utilized for power transistor measurement and allow for efficient power amplifiers design.

In this paper, we present novel low-cost impedance tuner featuring reduced losses in comparison to [7]. The proposed structure is composed of 3-dB quadrature coupled-line directional coupler with two shorted transmission lines. The presented impedance tuner has been theoretically and experimentally investigated and the obtained measurement results proved the usefulness of the proposed device.

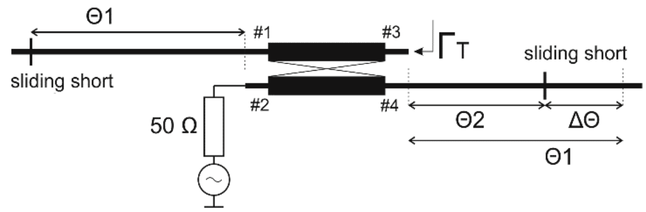


Fig. 1. Proposed low-cost impedance tuner realized using 3-dB quadrature coupled-line directional coupler with two shorted transmission lines.

II. Quadrature Coupler Impedance Tuner

The proposed impedance tuner is composed of 3-dB quadrature coupled-line directional coupler and two shorted transmission line sections as shown in Fig. 1. The length of shorted transmission line sections can be adjusted which results in impedance change at the matching network input Γ_T. The behavior of such a matching network can be described using analysis of signal flow graph (see Fig. 2) of the circuit, assuming S parameters of an ideal 3-dB coupled-line directional coupler and ideal shorted transmission lines (both taken for the center frequency).

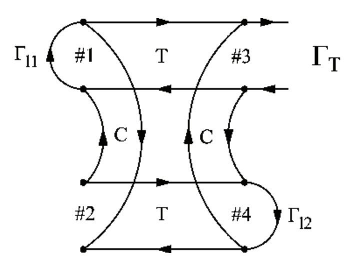


Fig. 2. Flow graph of the proposed impedance tuner.

It can be seen that reflection coefficient Γ_T is a result of parallel connection of two signal loops and can be expressed as:

$$\Gamma_T = \frac{1}{2} T \Gamma_{l1} T + \frac{1}{2} C \Gamma_{l2} C \tag{1}$$

where Γ_{l1} and Γ_{l2} are reflection coefficients of shorted sections of 50 Ω transmission lines while T and C are directional coupler`s transmission and coupling S-parameters [8]:

$$\Gamma_{l1,2} = -e^{-j2\theta_{1,2}} \tag{2}$$

$$T = S_{13} = S_{31} = -j\frac{1}{\sqrt{2}} \qquad C = S_{43} = S_{34} = \frac{1}{\sqrt{2}} \tag{3}$$

$$\Delta\theta = \theta_1 - \theta_2 \tag{4}$$

By inserting (2) - (4) into (1), one can see that the reflection coefficient Γ_T of a matching network is only a function of electrical lengths of the shorted sections:

$$\Gamma_T = \frac{1}{2}\left(e^{-j2\theta_1} - e^{-j2\theta_2}\right) = \frac{1}{2}e^{-j2\theta_1}\left(1 - e^{j2\Delta\theta}\right) \tag{5}$$

By analyzing (4) one can prove that any reflection coefficient, and thus impedance of a passive network can be realized for $\theta_{1,2} \in \langle 0;\pi\rangle$. The resulting change of reflection coefficient Γ_T in a function of transmission line lengths θ_1 and $\Delta\theta$ has been presented using Smith chart in Fig. 3. One can see, that value of Γ_T along the circle O_1 can be changed by changing $\Delta\theta$, whereas θ_1 allows to shift the center of the O_1 circle. Within the range of 0 to π the reflection coefficient travels full circle for one of the variables ($\Delta\theta$) and the circle center performs full turn around the Smith chart for the other (θ_1), allowing to realize any desired reflection coefficient.

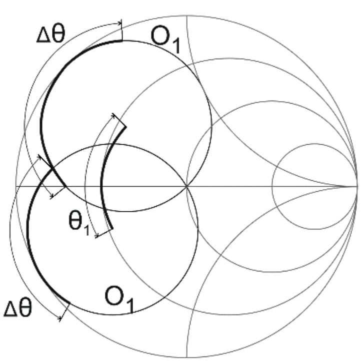


Fig. 3. Reflection coefficient of a coupled-line directional coupler matching network with reflection coefficient displacement as a function of shorted line lengths θ_1 and $\Delta\theta$.

Additionally, the proposed circuit features for $\theta_1 = \theta_2 = 0$ ideal match ($\Gamma_T = 0$) while circuit presented in [7] provide ideal open circuit ($\Gamma_T = 1$). Such property is very useful for transistor matching application when low impedances are to be realized. The reason is that to realize ideal short the proposed circuit requires θ_1 = 90º, θ_2 = 0º while one described in [7] $\theta_1 = \theta_2$ = 90º. It is an advantages, since in real circuit, transmission line losses modify reflection coefficient of shorted lines limiting minimal realizable impedance, and hence loss reduction is desired.

III. Experimental Results

In order to experimentally verify the presented approach and to examine the maximum obtainable VSWR, a coupled-line coupler matching network operating at center frequency f_0 = 1.05 GHz has been designed, manufactured in microstrip technique and measured. First, a 3-dB coupled-line directional coupler has been developed with the use of multilayer microstrip technique, since it is hardly possible to realize such tight coupling in single-layer microstrip. Therefore, to overcome this problem an additional thin layer of Arlon 25N laminate (h_2 = 0.152 mm, ε_{r2} = 3.38) has been bonded with prepreg to a thick Arlon 25N laminate (h_1 = 0.762 mm, ε_{r1} = 3.38) as shown in Fig. 4. This allowed to realize coupled strips of the coupler on metal layers *m1* and *m2*. Performance of the designed directional coupler has been improved using compensation technique presented in [9] since in microstrip structure conditions of ideal coupler realization are in most cases not fulfilled (inductive and capacitive coupling coefficients are unequal) what has deteriorative influence on the circuit. Additionally, for practical reasons, the designed coupler has been provided with the crossing in the middle allowing for ports #1 and #4 to be on the same site, thus both tuning transmission line sections can be on the same side of the tuner. All other elements of the tuner have been realized on a thick substrate only.

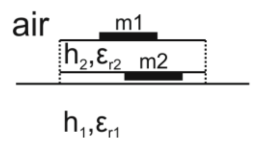
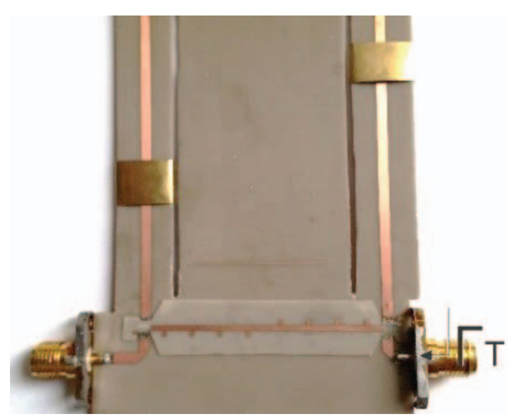
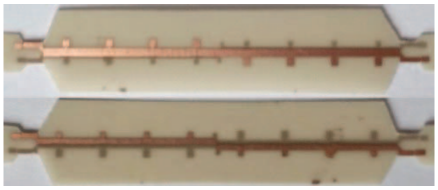


Fig. 4. Cross-sectional view of the utilized dielectric structure. Entire circuit has been realized in single-layer microstrip structure except directional coupler which required additional thin laminate to provide tight coupling.



(a)



(b)

Fig. 5. Photograph of the manufactured coupled-line directional coupler matching network where two sliding shorts and directional coupler are clearly visible (a) and close-up of both sides (top and bottom respectively) of thin 6mil laminate with etched coupled strips (b). SMA connector on the left is used to connect 50 Ω load, e.g. signal generator or power detector. Right SMA connector is matching network port.

Moreover, transmission line sections have been realized as finite ground microstrip lines allowing for applying sliding elements shorting the transmission line strips to the ground.

The manufactured impedance tuner has been shown in Fig. 5a while close-up of coupled-line directional coupler is shown in Fig. 5b. It is worth noting that the physically realized tuner requires additional, short sections of 50 Ω transmission lines (see Fig. 5a) to provide input/output for the circuit. Finite length transmission lines transform reflection coefficient Γ_T and to obtain desired impedance, electrical lengths θ_1 and θ_2 must be slightly adjusted.

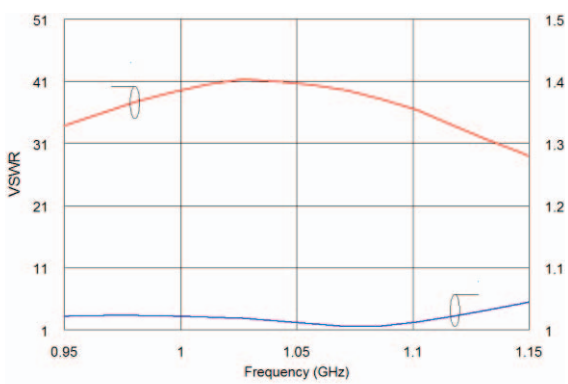


Fig. 6. Measured min. (blue line) and max. (red line) VSWR of the manufactured impedance matching network.

Measured minimum and maximum obtainable VSWR value of the manufactured network is shown in Fig. 6. As it is seen, on one hand very good VSWR < 1.01 with transmission losses around 0.2 dB can be achieved and on the other hand VSWR > 41 can be obtained. m The VSWR ratio for the manufactured network equals 41:1 and allows for achieving impedance on the level of $Z_T = 1.26$ Ω which is more than a two times lower value compared to circuit shown in [7]. It is worth mentioning that achievable impedance is more than sufficient to match majority of power transistors.

VII. Conclusion

A low-cost impedance tuner composed of quadrature 3-dB coupled-line directional coupler with tuning components realized as shorted microstrip line sections with appropriate sliding shorting elements has been proposed. The principle of behavior of the proposed matching networks as well as the possibility of realization of any desired impedance have been outlined. Measurement results prove the usefulness and features of the proposed impedance tuner. Impedance as low as 1.26 Ω can be realized which is more than sufficient for majority of power transistors and makes the proposed circuit well suitable for load and source pull transistor measurement applications.

Acknowledgement

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