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PHD THESIS

**STATIC AND DYNAMIC CHARACTERIZATION OF MAGNETIC
TUNNEL JUNCTIONS WITH PERPENDICULAR ANISOTROPY.**

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1. Definitions and abbreviated terms

1.1. Definitions

- **Storage element** – a single magnetic tunnel junction or other magnetoresistive device capable of being stable in two or more resistance states.
- **Storage cell** – a single storage element or a group of storage elements driven by a single read-write circuit.
- **Multi-bit (storage) cell** – a storage cell capable of being stable in more than two states, resulting in the ability to store more than one bit of data.
- **Magnetoresistance ratio** – a measure of the amplitude of magnetoresistive effects, defined as $(R_{max} - R_{min})/R_{min}$.
- **Critical current** – current that induces switching of the storage element.

1.2. Abbreviations

- **AF** – Antiferromagnet
- **AP** – Antiparallel
- **CIMS** – Current Induced Magnetisation Switching
- **DI** – Deionized
- **FL** – Free Layer
- **FM** – Ferromagnet
- **GPIB** – General Purpose Interface Bus (IEEE-488)
- **IEC** – Interlayer Exchange Coupling

- **IP** – In Plane
- **MR** – Magnetoresistance Ratio
- **MRAM** – Magnetic Random Access Memory
- **MTJ** – Magnetic Tunnel Junction
- **NM** – Non-magnetic
- **P** – Parallel
- **PC** – Personal Computer
- **PL** – Pinned Layer
- **PMA** – Perpendicular Magnetic Anisotropy
- **PSV** – Pseudo Spin Valve
- **RAM** – Random Access Memory
- **RKKY** – Ruderman–Kittel–Kasuya–Yosida (coupling)
- **RL** – Reference Layer
- **RT** – Room Temperature
- **SAF** – Synthetic Anti-ferromagnet
- **SEM** – Scanning Electron Microscopy
- **STT** – Spin Transfer Torque
- **TMR** – Tunnel Magnetoresistance
- **USB** – Universal Serial Bus

2. Introduction

Computer memories can be primarily classified into two groups: volatile and non-volatile memories. Non-volatile memories are able to store data without power applied for a long period of time, but usually are relatively slow in terms of writing speed and data access time. Such memories are for example Hard Drive Disks (HDD) or Flash memories. They exhibit large data density, what makes them perfect for storage of data without a need of fast access.

Volatile memories, in contrast, need constant power supply to preserve data, but offer very fast read and write operations. The data density is smaller than for non-volatile memories.

In the past few years some new types of memories have been presented [1, 2], which connect advantages of standard volatile and non-volatile memories. They offer read-write speeds comparable to fast volatile memories, while still being able to preserve data without power. These types include:

- FRAM – Ferroelectric Random Access Memory (RAM), which is similar to the classic Dynamic RAM (DRAM) memory, but replaces the dielectric with a ferroelectric material
- PCRAM – Phase Change RAM, which bases on materials, that can change the phase from amorphous to crystal, what is reflected in the change of resistance of the storage element
- ReRAM – Redox RAM, which bases on redox reactions in the storage element, what is reflected in the change of resistance of the storage element
- MRAM – Magnetoresistive RAM, which bases on effects such as Tunnel Magnetoresistance, Spin Transfer Torque and other relate to spin electronics

However, considering current state of the art, all these memories have some disadvantages. FRAM memories have very low data density, PCRAM and ReRAM exhibit very limited endurance and the capability of MRAM chips is limited due to the size of the cell driving circuit [3], which is considerably bigger than a storage element.

MRAM memories, which are subject of interest of this work, have the following advantages: their endurance is theoretically unlimited [2], their write and read speeds can be compared to DRAM memory (especially the writing speed is much shorter than for FLASH). In addition they are ionizing-cosmic-radiation resistant, which makes them perfect for use in avionics and space electronics.

There are several types of MRAM memories, taking into account the method of data writing, for example: field-driven (toggle), spin transfer torque (STT-MRAM), domain-wall motion (DW motion) and voltage-controlled spintronics memories (VoCSM) [4]. The field-driven MRAMs as well as STT-MRAMs are commercially available nowadays, while other types are still the subject of research. Additionally, field-driven memories turn out to be less power efficient and have lower densities than STT-memories.

The limitation of data density, mentioned above, is the result of the current needed to switch the STT-MRAM storage element compared to current density allowed in state-of-the-art transistors. Therefore, the ability to drive multiple storage elements using one transistor, resulting in having a multi-bit memory cell, can lead to considerable improvement in terms of MRAMs capability and, as a result, extend the area of their application.

To date, very few practical implementations of multi-bit MRAM cells have been presented. This is mainly due to the fact, that efforts were made to produce a single storage element capable of being stable in more than two states, or to produce multiple storage elements on the top of each other. Both of these approaches are very challenging for the process of manufacture.

In this thesis a new approach is presented. The analysis of serial and parallel connections of multiple standard STT-MRAM elements was performed, as well as experiments were conducted. The final result of this work includes practical realisation of three-bit storage cell based on STT-MRAM elements.

In Sec. 3 the physical phenomenon, MRAMs are based on, is introduced to the reader and the approach presented in the thesis justified. Then, in Sec. 4, a complete fabrication process of MRAM cell is described. Later, in Sec. 5, an experiment is described, and results discussed. As a conclusion, future challenges of the presented solutions are briefly described in Sec. 6. The work is summarized in Sec. 7.

3. Principles of operation

This chapter describes fundamental physical phenomena: magnetic tunnel junctions (MTJs), tunnel magnetoresistance (TMR), spin transfer torque (STT), current induced magnetisation switching (CIMS) and presents design of an MRAM storage element. Also a design model of construction of a multi-bit storage cell is presented.

3.1. Magnetic tunnel junction

A basic magnetic tunnel junction consists of two ferromagnetic (FM) layers separated by a thin insulator layer, called a tunnel barrier (Fig. 3.1 a). The MTJ is usually fabricated as a circular (in case of perpendicular magnetic anisotropy - PMA) or elliptical (in case of in plane - IP - anisotropy) pillar, and finally provided with electrodes. MTJs exhibit magnetoresistive effect (called TMR) due to tunnelling between FM layers through the insulator barrier [5, 6].

The resistance of MTJ depends on the relation between magnetisations of both FM layers. If magnetisation directions of both layers are the same (parallel - P) the resistance is the lowest (R_P), and if the directions are opposite (anti-parallel - AP) the resistance of the junction is the highest (R_{AP}).

The phenomenon of tunnelling between ferromagnetic films was first observed and described by Julliere in 1975 at low temperatures [7]. The first low-temperature MTJs were made by Nowak and Raułuskiewicz in 1992 and by Moodera et al. in 1994 [8, 9]. After that, Miyazaki and Tezuka made MTJs with aluminium oxide barrier, which resulted in achieving the magnetoresistance ratio (MR) of 18% at room temperature (RT) [10]. Recently, by using *CoFeB* FM layers and crystalline *MgO* barrier, MR of 600% at RT and above 1000% at temperature of 5 K was observed [11]. The use of crystalline *MgO* barrier allowed much better preservation of spin-polarisation during the tunnelling process, compared with *Al₂O₃* barrier, which is amorphous [12].

The orientation of the magnetization of the ferromagnetic material is determined by the minimal energy of the system. In the discussed thin film structures, the energy is the sum of: Zeeman, anisotropy and demagnetization energy. The magnetic anisotropy of FM layers, which is here defining the direction of magnetisation in stable state (Fig. 3.1), can be both parallel to the plane of the substrate (in plane - IP)

[5] or perpendicular to the plane (out of plane, perpendicular magnetic anisotropy - PMA) [13]. Effective magnetic anisotropy energy K_{eff} can be calculated using the simplified formula [14, 15, 16]:

$$K_{eff} = K_b - \frac{1}{2}\mu_0 M_s^2 + \frac{K_i}{t}, \quad (3.1)$$

where K_b is the bulk crystalline anisotropy, μ_0 - magnetic permeability of the free space, M_s - magnetization saturation, K_i - interfacial anisotropy energy and t - layer thickness. For negative K_{eff} anisotropy is IP, and for positive - PMA is observed. Usually K_i is positive, and $K_b \ll \mu_0 M_s^2$. Therefore, achieving PMA can be obtained by using a sufficiently thin FM layer. Nowadays, the PMA is used for MRAM storage elements construction, as higher thermal stability and lower switching energies, compared to the IP ones, are obtained [17].

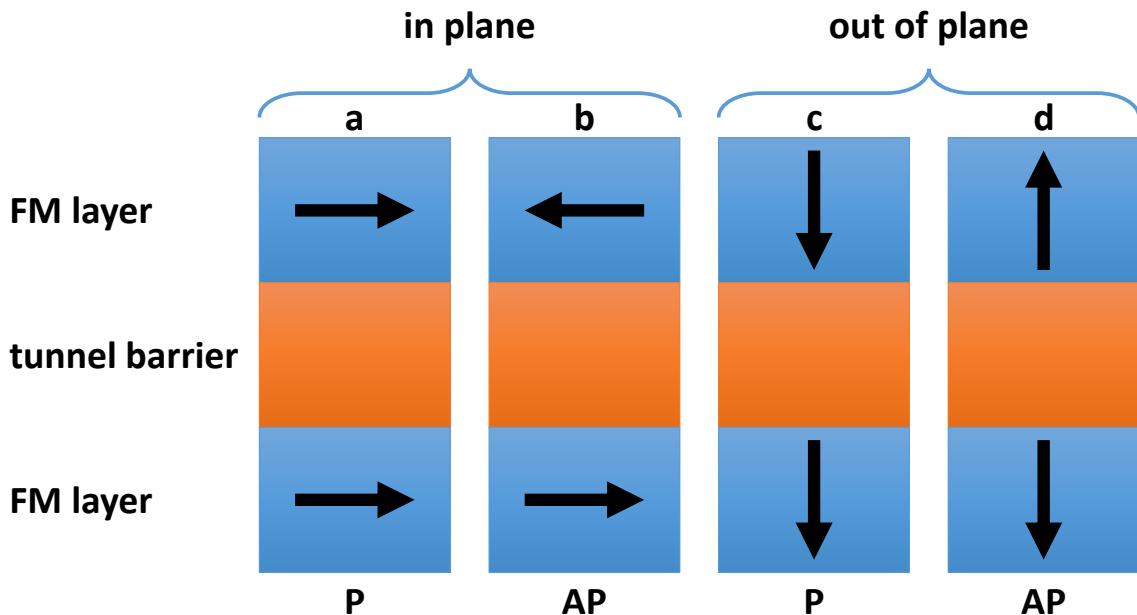


Figure 3.1: Schematic of MTJ with IP anisotropy in P (a) and AP (b) state, and with PMA P (c) and AP (d) state. Arrows denote magnetisation vector of FM layers.

3.2. Tunnel magnetoresistance effect

The TMR effect is observed when FM layers separated by tunnel barrier exhibit different density of states D in the $3d$ band (which also takes part in the tunneling process) at Fermi energy E_F for electrons with spin oriented up (D_{\uparrow}) and down (D_{\downarrow}) (Fig. 3.2). Such materials are for example Fe , Ni , Co or some alloys, like $CoFeB$ [6].

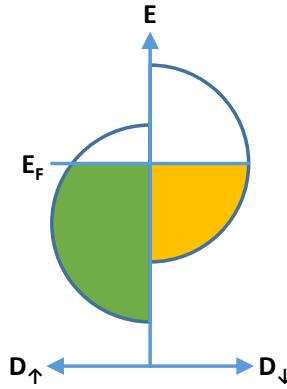


Figure 3.2: Schematic diagram of density of states in 3d band in *Fe*. Fermi energy is denoted.

Assuming that electrons are not changing their spin direction during tunnelling through barrier (which may be true only for sufficiently thin barriers; also electron flow is not fully spin-polarised) and must tunnel to sub-band with matching spin, the TMR effect can be explained in a simplified way presented below.

In the P state (Fig. 3.3 a) there is relatively large amount of electrons with spin ↓ at E_F available in the FM1 layer, and also in the FM2 layer there is plenty of space for the electrons at E_F with spin ↓ - that results in a significant current flow of electrons with that spin. For electrons with spin ↑ - the amount in the FM1 layer at E_F is small, and also available space in the FM2 layer is small, so the current of electrons with spin ↑ is small. Overall current is significant due to tunnelling of electrons with spin ↓, resulting in low resistance (R_P).

In the AP state (Fig. 3.3 b), as previously, the amount of electrons with spin ↓ available in the FM1 layer is high, but, due to opposite magnetisation of the FM2 layer, available space in the FM2 layer for those electrons is small, resulting in small current. Considering electrons with spin ↑ - there is plenty of space in the FM2 layer, but only limited amount in the FM1 layer - also resulting in small current flow. The overall current is small, so the resistance is large (R_{AP}) [5].

The *TMR* effect can be quantified as follows:

$$TMR = \frac{R_{AP} - R_P}{R_P} \quad (3.2)$$

According to the simple Julliere's model [7] *TMR* can also be expressed as a function of spin-polarisation of FM layers (P_{FMx}), which is the fraction of electrons that are becoming spin-polarized in each FM layer:

$$TMR = \frac{2 \cdot P_{FM1} \cdot P_{FM2}}{1 - P_{FM1} \cdot P_{FM2}}, \quad (3.3)$$

however the nature of the phenomena is in reality much more complicated, and other factors are influencing the actual *TMR*, like for example spin filter effect in a tunnel barrier, the quality of FM / tunnel barrier interface or trapping states in tunnel barrier [18].

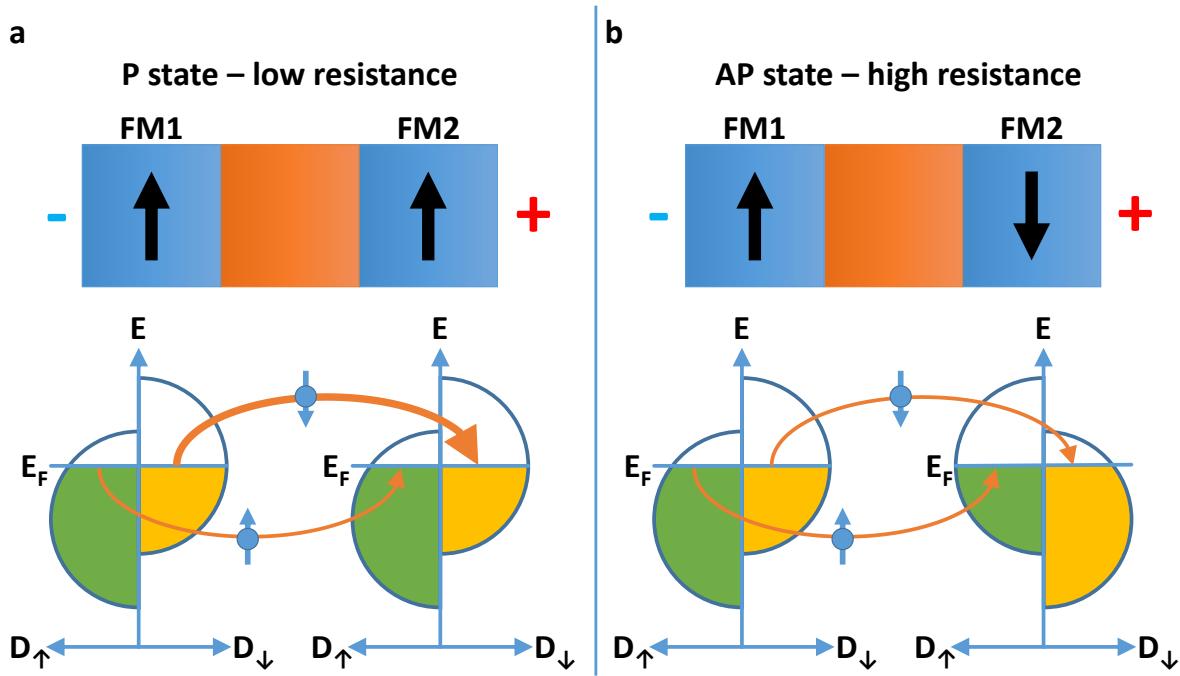


Figure 3.3: Schematic explanation of origin of TMR effect in MTJs. The thickness of orange arrows are proportional to current densities.

Also when considering layers having magnetization vectors at any relative angle θ (not only 0° for P and 180° for AP states), phenomenologically, the resistance of the MTJ can be expressed as the following function [19]:

$$R(\theta) = R_P + \frac{R_{AP} - R_P}{2}(1 - \cos\theta). \quad (3.4)$$

3.3. Defining reference layer by pinning

To produce a working MRAM storage element it is important to define one FM layer as a storage layer (of which magnetisation direction is to be changed while writing, so called free layer - FL) and the second as a fixed layer (or reference layer - RL), of which magnetisation direction should be hard to change. Without that one can observe pseudo spin valve (PSV) behaviour presented in Fig. 3.4. As the bottom FM layer (FM2) is nearly as easy to magnetize, as the top one (FM1), hysteresis loops are very narrow. This justifies the need of pinning one of the layers and defining the RL.

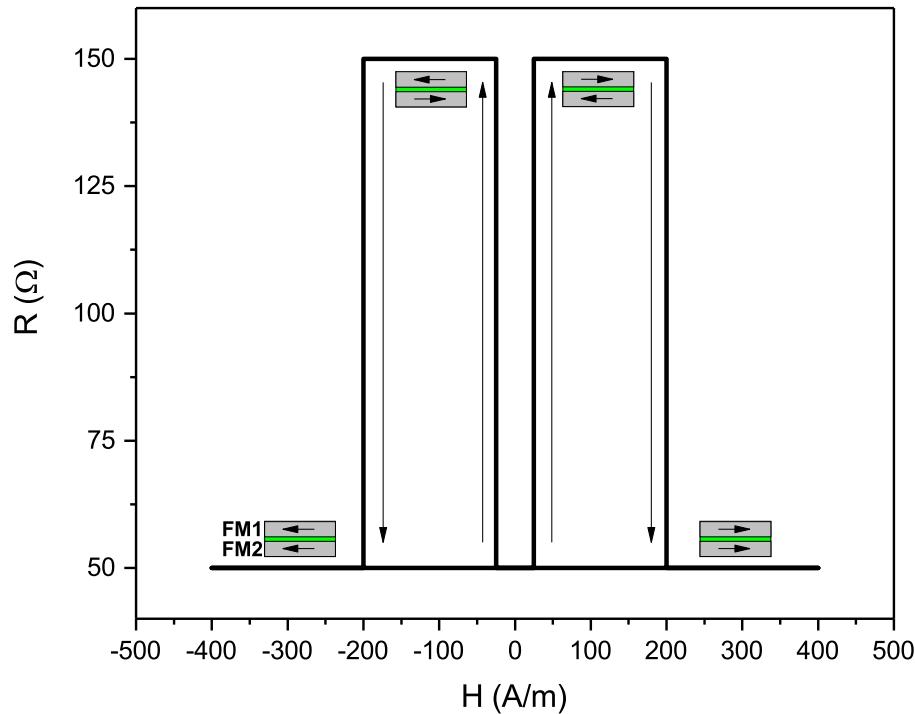


Figure 3.4: PSV behaviour in external magnetic field H . Magnetization directions of both FM layers presented in stable states.

Different coupling mechanisms between thin FM layers were discovered, depending on the type of the spacer. The Ruderman–Kittel–Kasuya–Yosida (RKKY) [20] coupling is measured between FM layers separated by a non-magnetic (NM) metallic layer (Fig. 3.5 a). Depending on NM layer thickness, the coupling can be both ferromagnetic and anti-ferromagnetic, resulting in magnetisation vectors with the same, and opposite direction, respectively [6].

By intentionally coupling two FM layers a synthetic anti-ferromagnet is created. One of the FM layers can be used as RL in MTJ (Fig. 3.5 b) [21, 22], as well as additional layers may be coupled to the SAF for the purpose [23].

When anisotropy is not defined mainly by dimensions (size and thickness), a natural AF (e.g. $IrMn$) is used to induce unidirectional anisotropy in one of the SAF layers (Fig. 3.5 c).

The second type of coupling, namely an interlayer exchange coupling (IEC) exists between FM layers separated by an insulator layer (e.g. MgO tunnel barrier) [24, 25]. This coupling causes the shift of the hysteresis loop (Sec. 3.4, Eq. 3.5). In practice, it is vital to reduce the influence, because the lower the shift, the more symmetrical the switching currents. Reduction of the IEC can be done by using careful design of SAF and SAF-like structures for the top FM layer.

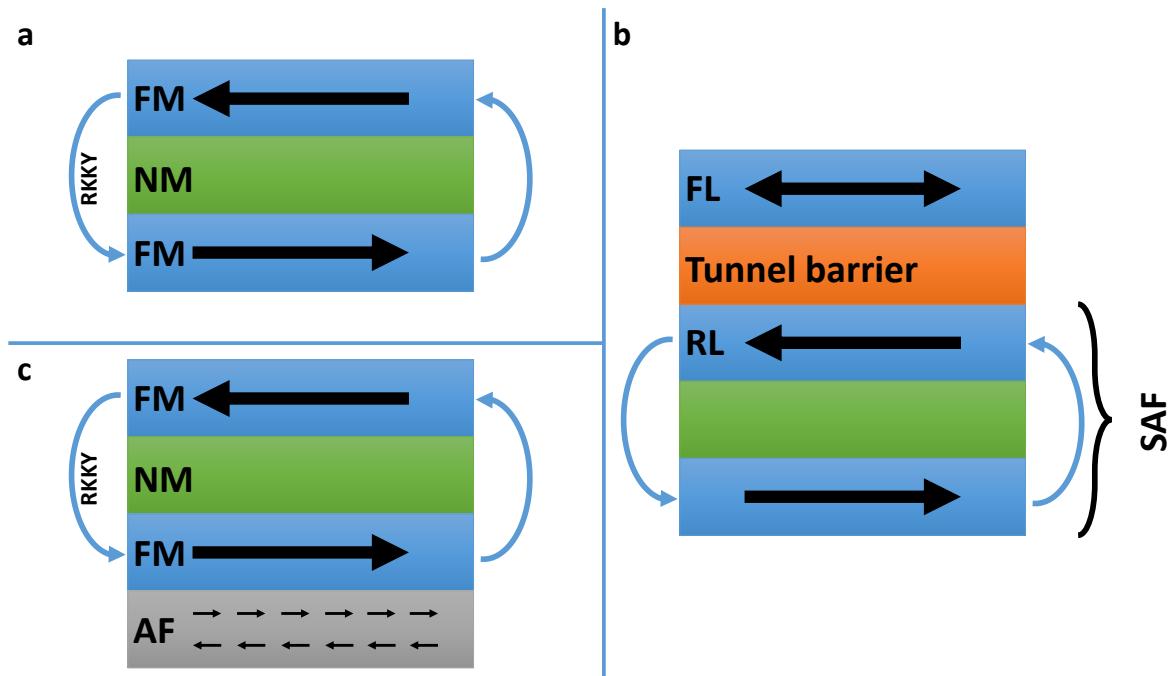


Figure 3.5: a) RKKY anti-ferromagnetic coupling between two FM layers separated by NM metallic spacer. b) Schematic of MTJ junction with RL pinned using SAF structure. c) Additional AF used to induce anisotropy in the bottom FM layer.

3.4. Behaviour of the MTJ with pinned layer

The storage element can be primarily characterised using $R(H)$ measurement, i.e. resistance (R) versus external magnetic field (H) applied parallel to the anisotropy of the sample. This measurement allows to determine TMR of the examined MTJ, and therefore it is called a TMR measurement. Theoretical characteristics are presented in Fig. 3.6 together with illustrated orientation of RL and FL in characteristic regions.

When applying low magnetic field only FL is changing its magnetisation and, depending on the orientation of RL, two different minor hysteresis loops (symmetrical to each other) can be observed (Fig. 3.6 a, b). Usually each minor loop tends not to be symmetrical around zero field, due to coupling between FL and RL. Applying sufficiently strong fields results in switching of RL, and a major hysteresis loop is observed (Fig. 3.6 c), in contrast to PSV, when smaller magnetic field caused such behaviour (Fig. 3.4).

By repeating $R(H)$ measurements (Fig. 3.6 a or b) multiple times in the same conditions, and by changing the magnetic field slow enough, a distribution of magnetic field for switching from P to AP and vice versa can be obtained. Using the formula (Eq. 3.5) presented by Sato et al. to fit the experimental data, a thermal stability (Δ) can be obtained as well as other important parameters [26]. The formula was corrected from the originally presented version, by inserting absolute value.

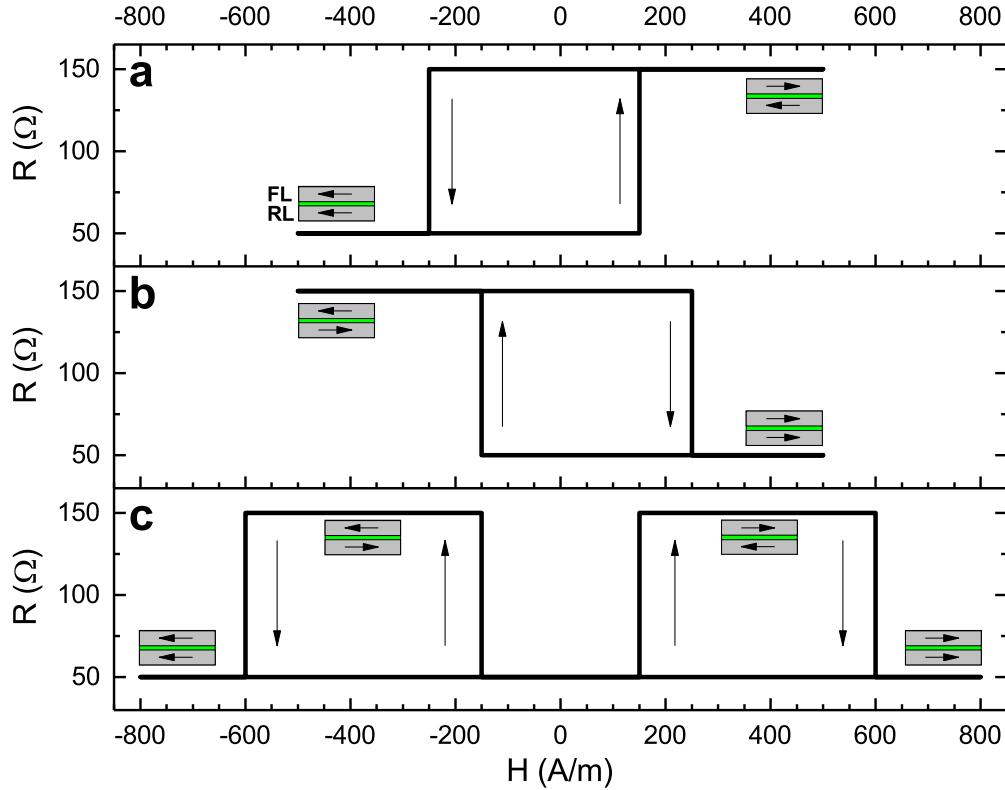


Figure 3.6: Theoretically predicted characteristics of MTJ resistance versus external magnetic field applied in a direction parallel to the anisotropy of the MTJ (with orientation of FL (upper) and RL (lower) in characteristic regions) when: a) and b) only FL is switching in lower fields, c) RL is switching in higher fields.

$$P(\tau) = 1 - \exp \left[-\frac{\tau}{\tau_0} \exp \left\{ -\Delta \left(1 - \frac{|H - H_s|}{H_k^{eff}} \right) \right\} \right] \quad (3.5)$$

In Eq. 3.5 τ denotes the magnetic field step duration (in the study 1 s), τ_0 the inverse of attempt frequency (in the thesis assumed to be 1 ns), Δ the thermal stability, H the external magnetic field, H_s shift field of the TMR loops (i.e. the field between zero and the center of $R(H)$ hysteresis loop) and H_k^{eff} denotes the effective magnetic anisotropy field. The thermal stability is expressed as:

$$\Delta = \frac{E}{k_b T}, \quad (3.6)$$

where E denotes the energy barrier between P and AP states, k_b the Boltzmann constant and T denotes the absolute temperature (in the experiment 300 K). For practical applications thermal stability should be $\Delta \geq 60$ [27].

3.5. Spin transfer torque (STT) and current induced magnetisation switching (CIMS) effects

In order to switch the magnetisation of the storage layer (FL) one can apply external magnetic field or use the spin transfer torque phenomenon [28]. When using external magnetic field to switch the storage element, additional current lines need to be present, to generate Oersted field. This require additional area inside the memory chip and is not energy-efficient [2, 1]. On the other hand, using the STT effect does not require current lines for write operation, and uses less energy. To understand the STT phenomenon, two cases need to be analysed: switching from AP to P state, and vice versa. The explanation presented below uses a simplified model, as the nature of the phenomenon is very complex.

When the MTJ is initially in the AP state (Fig. 3.7 a), in order to switch the magnetization of the FL electrons must flow upwards (from RL to FL). Electrons are spin-polarised by RL and a considerable amount of them does not change its spin during tunnelling. As they enter FL, magnetization of which is oriented in the opposite way, they need to change their spin, and, therefore, angular momentum. This momentum change induces torque (called spin transfer torque), that rotates magnetization of the FL. If the amount of electrons is big enough, the STT can cause the magnetization to flip to the opposite stable position (P) - the process is called current induced magnetisation switching (CIMS). A current which induces CIMS is called the critical current.

When the MTJ is in P state (Fig. 3.7 b) to switch the magnetization of the FL, electrons must flow from FL to RL (downwards). Electrons are spin-polarised by FL and some of them reverse their spin during tunnelling. As RL is pinned, it is more energy-efficient to return to the FL, rather than tunnelling to RL. These electrons now have spin opposite to the magnetisation of FL, so they are generating STT. With sufficient amount of these electrons CIMS effect takes place to change the MTJ state to AP.

A CIMS, as discussed above, can be induced by applying a voltage across the MTJ. When the voltage induces sufficient current the CIMS occurs, what is presented in Fig. 3.8. Such measurement, conducted in constant external magnetic field H , is called a CIMS measurement. It is important to notice, that when the resistance changes with constant voltage applied, the current also increases or decreases abruptly (Fig. 3.8 b). Additionally, by performing series of such measurements in different external magnetic fields and marking voltages of CIMS and the field, a stability diagram can be obtained [29]. The diagram (Fig. 3.9 shows regions (in voltage-field coordinates) where only P, AP, or both of the states are possible.

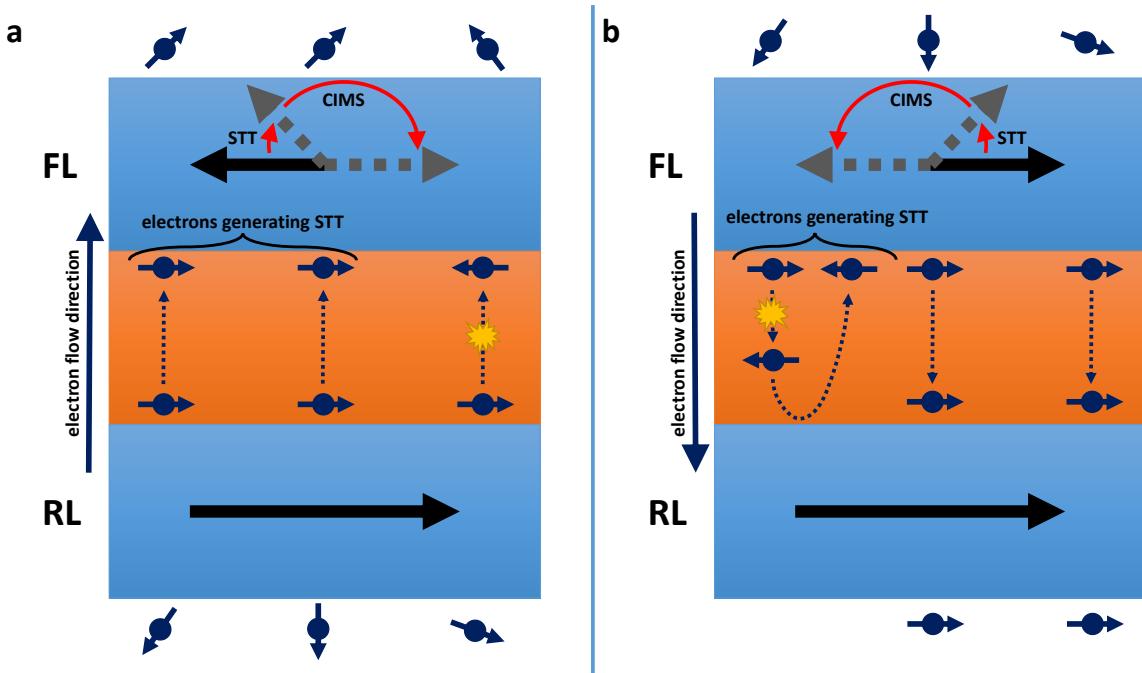


Figure 3.7: Schematic explanation of CIMS process for switching from AP to P (a) and from P to AP (b). For better illustration, IP anisotropy was presented.

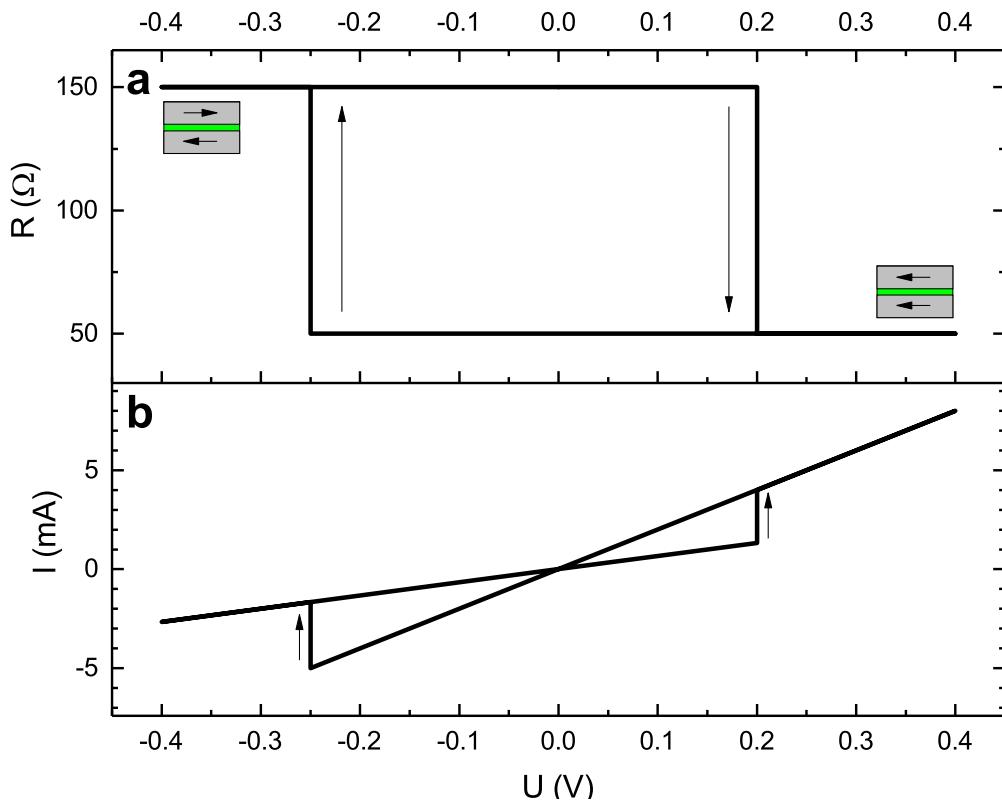


Figure 3.8: Theoretically predicted a) resistance and b) current versus voltage applied to an MTJ. A CIMS may be observed.

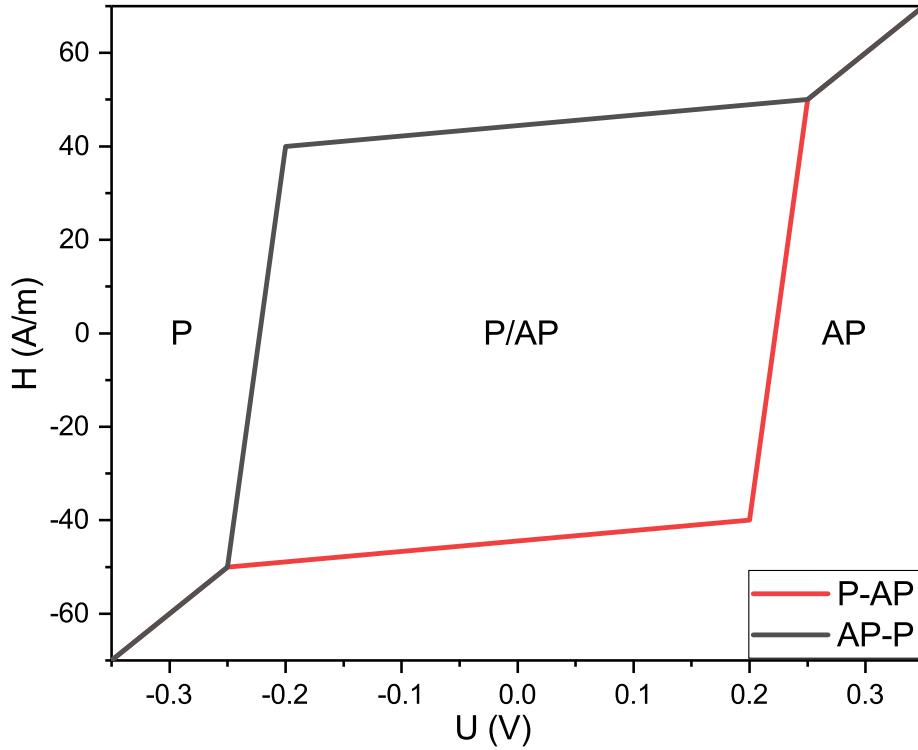


Figure 3.9: Theoretically predicted stability diagram. Lines indicate switching from P to AP or vice versa. Regions are marked with possible states of an MTJ (P, P/AP, AP).

3.6. Perpendicular magnetic anisotropy

To understand the need of using PMA in MRAM storage elements, critical currents (I_C) need to be taken into account. With the use of the model presented by Mangin et al., critical currents for IP anisotropy and PMA can be approximated as follows [17]:

$$I_C^{IP} \approx \frac{A\alpha M_S V}{g(\theta)p} (H + H_{dip} \stackrel{+}{\pm} H_{K\parallel} \stackrel{+}{\pm} \frac{M_S}{2}) \mu_0 \quad (3.7)$$

$$I_C^{PMA} \approx \frac{A\alpha M_S V}{g(\theta)p} (-H - H_{dip} \stackrel{+}{\pm} H_{K\perp} \stackrel{-}{\pm} M_S) \mu_0 \quad (3.8)$$

In the above equations 3.7 (for IP anisotropy) and 3.8 (for PMA) M_S , V and α are the saturation magnetization, volume and Gilbert damping constant for FL, respectively, θ is the relative angle between magnetizations of FL and RL, and the g factor depends on this angle, p is the magnitude of the angular dependence, A is a phenomenological factor dependent on transport model used, and it's unit is Wb⁻¹.

H is the external magnetic field applied parallel to the easy axis of magnetization, H_{dip} is the dipole field from the RL acting on the FL. $H_{K\parallel}$ and $H_{K\perp}$ are the uniaxial IP anisotropy or PMA fields, respectively. $\theta = 180^\circ$ and operators in brackets are true for AP to P switching, and $\theta = 0^\circ$ and operators without brackets are true for switching from P to AP.

A potential advantage of PMA is that the critical currents for switching the magnetization (for small H and H_{dip} , which are true for no external magnetic field and reduced IEC) are directly proportional to the anisotropy $H_{K\perp}$, and, hence, the stability of the bit. For the IP devices the current must overcome the additive factor $\frac{M_S}{2}$ that does not contribute to the stability of the bit against thermal fluctuations, but suppresses CIMS. Therefore, storage elements with PMA have lower write energies than the ones with IP anisotropy [30, 31]. The PMA can be obtained by using sufficiently thin layer of ferromagnetic material (Fig. 3.10 a) [32].

As the effect described above takes place for thickness about 1 nm, the volume of the layer after forming of the pillar is too small to observe an effect suitable for the application. In order to increase effective thickness, while maintaining out of plane anisotropy, a multilayer has to be deposited, with alternating FM and non-magnetic materials (such as *Pt* or *Pd*) (Fig. 3.10 b) [33, 34].

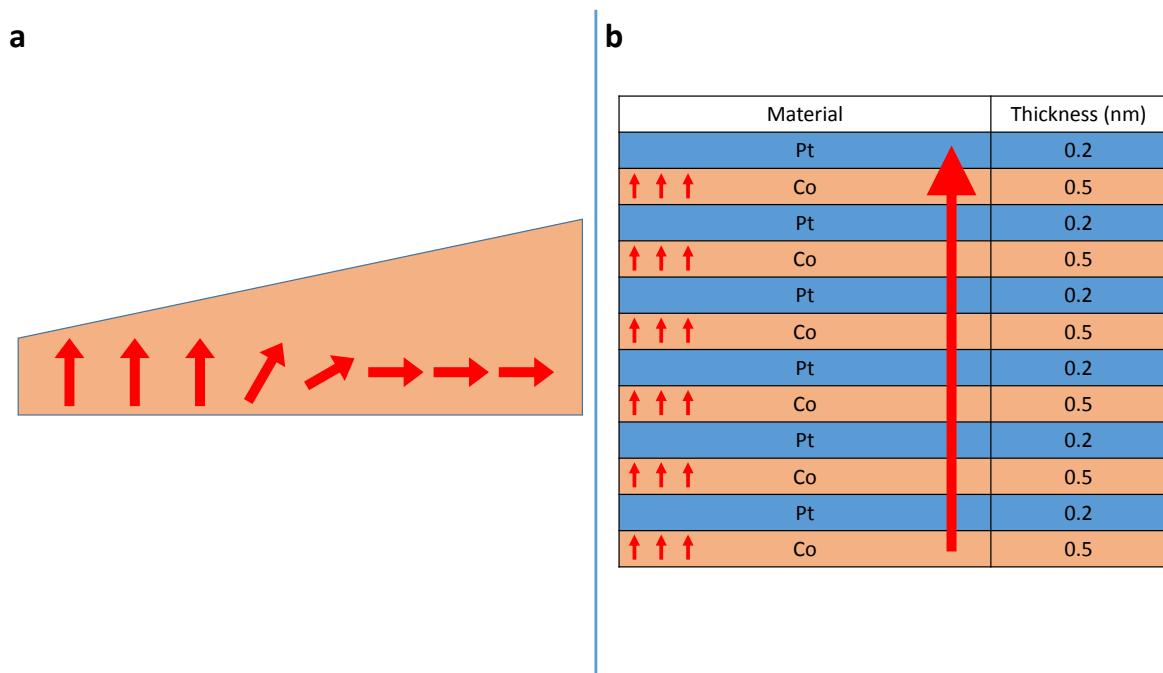


Figure 3.10: a) As the thickness of FM layer (light red) decreases, the magnetization (red arrows) tends to prefer perpendicular orientation (PMA), rather than IP anisotropy observed in thicker layers. b) Exemplary [Co/Pt] multilayer stack that exhibits PMA.

3.7. Storage element overview

Using all principles presented in Sections 3.1 through 3.6, a functional storage element can be built (Fig. 3.11). The prototype MRAM storage element, manufactured on *Si* substrate consists of:

- metallic bottom electrode
- synthetic anti-ferromagnet structure (SAF), that defines reference layer (RL) magnetisation
- thin tunnel barrier
- free layer (FL), that is used as a storage layer
- metallic top electrode

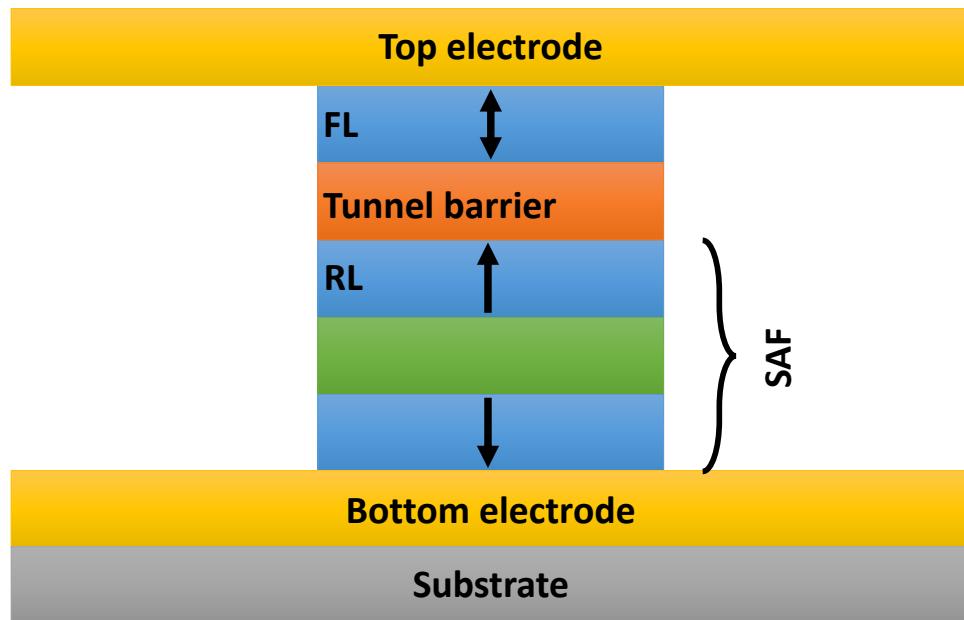


Figure 3.11: Schematic overview of functional MRAM storage element (MTJ).

The presented behaviour explains the usage of the MTJ as a storage element in MRAM memories - applying voltages lower than required to induce CIMS allows to measure the resistance (read the value), while applying sufficiently higher voltages results in writing the value.

3.8. Theoretical analysis of the serial connection of storage elements

One of the possible arrangements of MTJs in a storage cell is a serial connection, where bottom contact of the first element is connected to the top contact of the next element, as shown in Fig. 3.12.

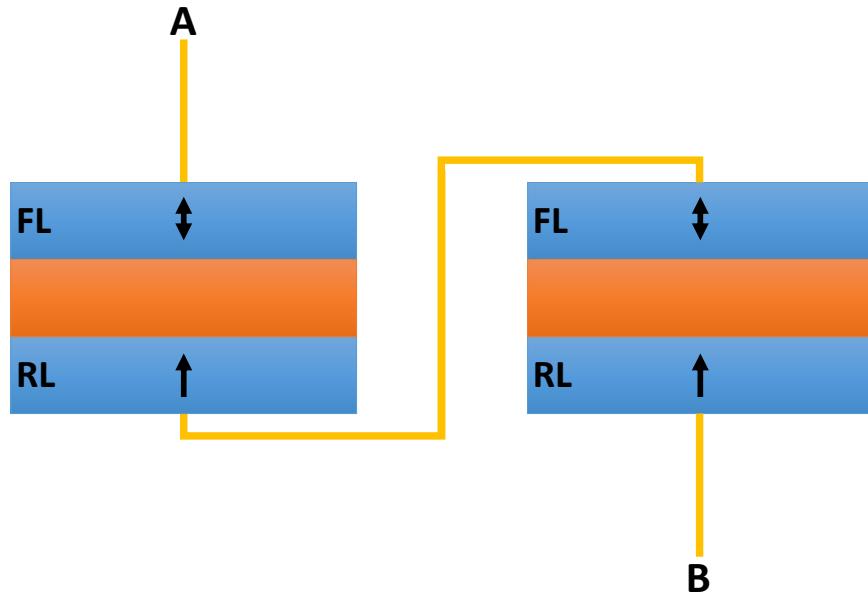


Figure 3.12: Schematic of serial connection of two MTJs. A and B denote two ports of the storage cell.

The behaviour of the presented arrangement of storage elements can be predicted by analysing characteristics of a single MTJ (Fig. 3.8). If both junctions are in P state lowest resistance is observed. When negative voltage is applied, the current increases, until it reaches critical value inducing CIMS. The CIMS occurs only in one element, as it is a stochastic process. As one of the elements switches to AP state, with constant voltage applied, the current decreases. This prevents the other element from switching, as the current drops below the critical value. By further increasing the voltage, the critical current is reached again, and the second MTJ switches to AP state.

By changing polarisation of the current, switching to the P state can be achieved. In the case, as soon as the critical current is reached, one of the elements switches to P state. With constant voltage applied, the current rises even higher above the critical value, causing the other element to switch to P state.

The complete characteristics, presenting this behaviour are presented in Fig. 3.13. The above mechanism is believed to work also for more than two elements, as similar reasoning can be carried out. For the series connection utilizing the presented mechanism, $N + 1$ stable resistance states would be observed for N elements connected. This is because there is no possibility to individually determine the states of all incorporated storage elements - only number of elements in P and AP state may be determined, based on the resistance measurement.

The storage cell capable of storing two bits of data would therefore consist of three serially connected storage elements. The predicted characteristics of such storage cell are presented in Fig. 3.14. Voltages for writing different states, as well as reading the cell can be defined. It is important to notice, that there is no possibility to reduce the resistance gradually.

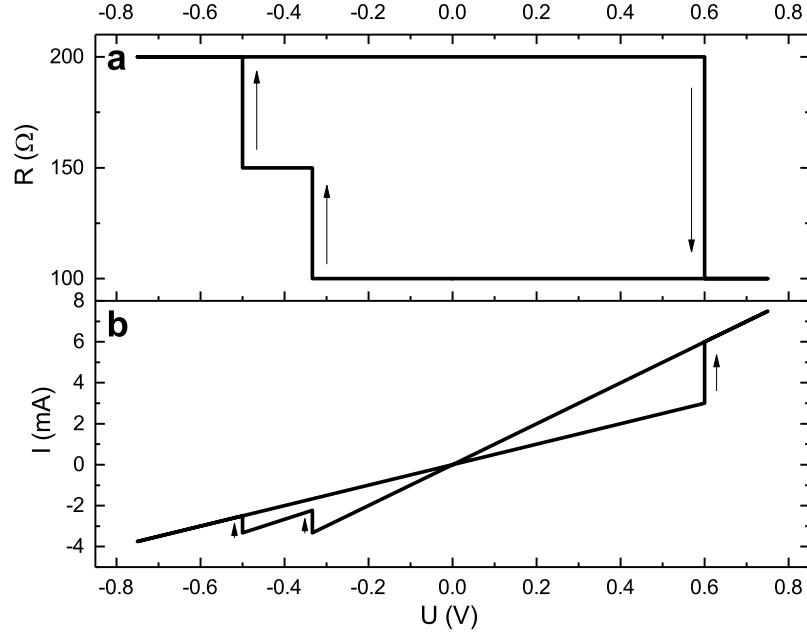


Figure 3.13: Theoretically predicted a) resistance and b) current versus voltage applied to a storage cell constructed by use of two serially connected MTJs.

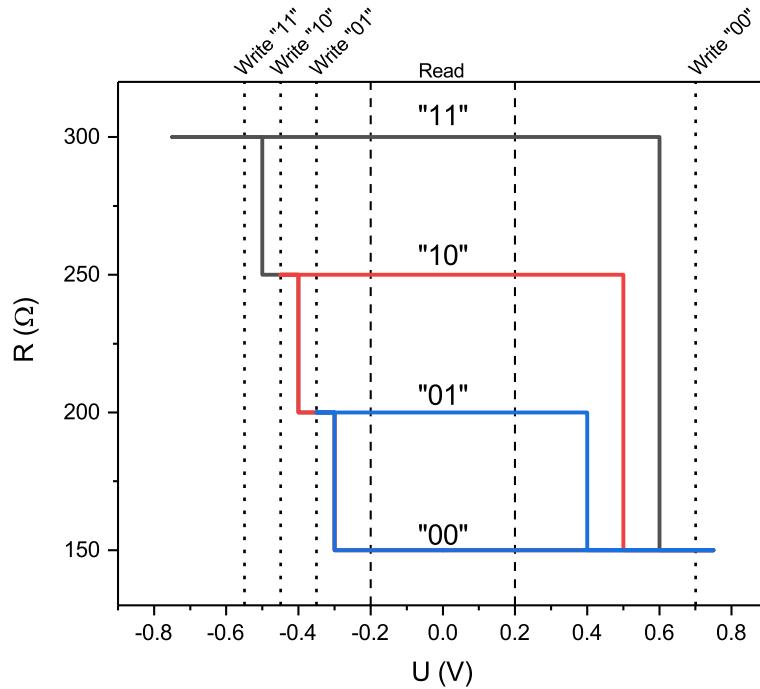


Figure 3.14: Theoretically predicted resistance versus voltage applied to a storage cell constructed by use of three serially connected MTJs. Possible mapping between resistance and binary value as well as proposed voltages to write and read the cell are marked on the plot. Different colours represent behaviour after writing different values.

3.9. Theoretical analysis of behaviour of the parallel connection of storage elements

Driving storage elements connected in parallel with constant voltage would cause all of them to switch in nearly the same moment, therefore no interesting behaviour would be observed. The parallel connection may exhibit interesting behaviour when driven with constant current, but in this case the highest current would always flow through the element with the lowest resistance (P state). Therefore, switching other storage elements would require to pass higher current through the element in P state, with an increasing possibility to permanently damage it. Also taking into consideration a need to incorporate a precise variable current source into the memory design, this arrangement will not be the subject of the experimental part of this work. However, parallel connections may be in the area of interest when considering spin torque oscillators or microwave spin detectors.

4. Fabrication techniques

This chapter presents MTJ stack used for the experiment and describes the complete fabrication process of the sample.

4.1. MTJ stack deposition

Based on previous experiments [29], an MTJ layer structure with PMA was proposed and deposited by Singulus AG using TIMARIS sputtering system in *Ar* atmosphere on an oxidised *Si* substrate. The substrate was etched before the deposition using ion etching, in order to clean the surface. The layer structure is presented in Tab. 4.1.

Layers 37-35 form a buffer, which reduces the surface roughness and induces proper crystal growth of other layers [35]. Layers 34-8 form a SAF, with a reference layer (10-8) on the top. *Co/Pt* layers 34-21 form a superlattice with strong PMA (Sec. 3.6) which is coupled antiferromagnetically to another *Co/Pt* superlattice (19-12) through a 0.8 nm *Ru* spacer (20). A composite reference layer (10-8) is also coupled through thin *W* layer (which, in addition, serves as a texture break), completing the SAF. A 0.89 nm thick *MgO* is used as a tunnel barrier (7), which results in the resistance area (RA) product of around $20 \Omega \times \mu\text{m}^2$. Above, a composite free layer is placed (6-4). An important part of the top capping (3-1) is another *MgO* layer (3), which increases PMA of the free layer.

After the deposition process the sample was annealed at 380 °C for 60 min. The process allowed to relax interface stresses of the layers.

Table 4.1: Layer structure of the sample used for experiment, from top to bottom.

No.	Material	Thickness (nm)	
1	<i>Ru</i>	5.00	Top capping
2	<i>Ta</i>	3.00	
3	<i>MgO</i>	1.00	
4	<i>CoFeB</i>	0.50	Free layer
5	<i>W</i>	0.30	
6	<i>CoFeB</i>	1.30	
7	<i>MgO</i>	0.89	Tunnel barrier
8	<i>CoFeB</i>	1.00	Reference layer
9	<i>W</i>	0.25	
10	<i>Co</i>	0.90	
11	<i>Ta</i>	0.15	
12	<i>Pt</i>	0.20	
13~18	$\left\{ \begin{array}{l} \text{Co} \\ \text{Pt} \end{array} \right.$	$\left\{ \begin{array}{l} 0.50 \\ 0.20 \end{array} \right.$	$\left. \times 3 \right\}$ SAF
19	<i>Co</i>	0.60	
20	<i>Ru</i>	0.80	
21	<i>Co</i>	0.60	
22~33	$\left\{ \begin{array}{l} \text{Pt} \\ \text{Co} \end{array} \right.$	$\left\{ \begin{array}{l} 0.20 \\ 0.50 \end{array} \right.$	$\left. \times 6 \right\}$
34	<i>Pt</i>	1.50	
35	<i>Ta</i>	0.70	Bottom buffer
36	<i>Ru</i>	7.00	
37	<i>Ta</i>	2.00	
	<i>SiO₂</i>		Oxidised substrate
	<i>Si</i>		

4.2. MTJ nanostructurization

To conduct the experiment, and check the behaviour of serially connected storage elements, nanostructurization was done, as effects presented in Sec. 3 take place only when the size of the junction is

small enough. During the process, MTJs, vias, electrical contacts and connections were fabricated, as described below in Sec. 4.3.

The mask used for the process is presented in Fig. 4.1.

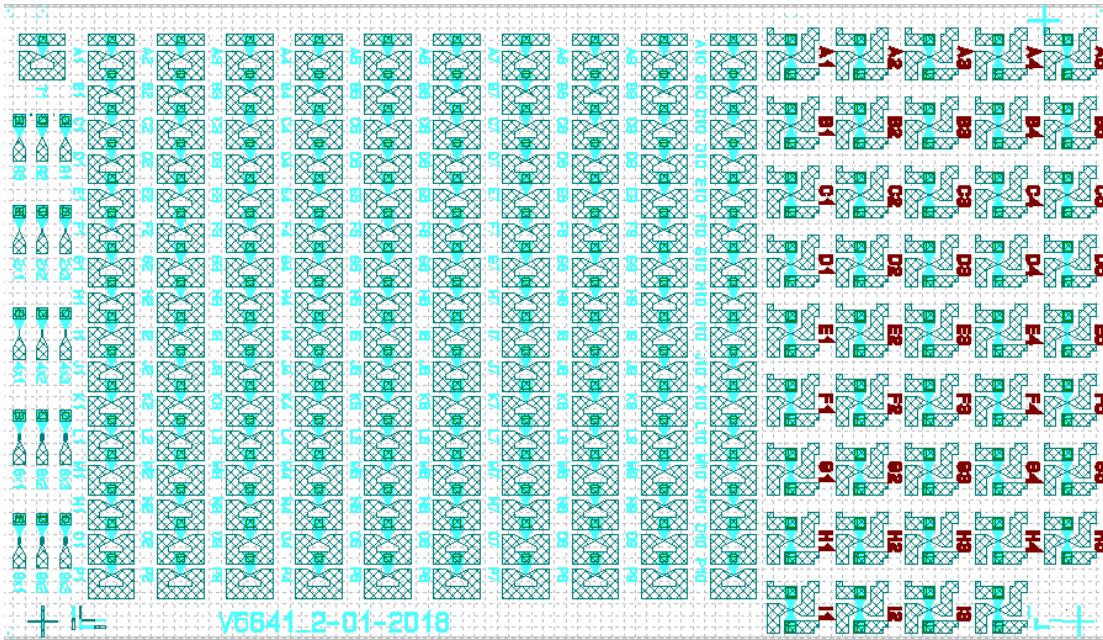


Figure 4.1: The overview of the mask used for nanostructurization process.

The mask is divided into four regions:

- Individual elements for separate storage elements characterization (top, Fig. 4.2a).
- Storage elements connected in series of 16 with separate access to each storage element, that allows testing different numbers of elements connected in series, and also gives the possibility to deal with malfunctioning elements (middle, Fig. 4.2b)
- Miniaturised series connections of 2, 4, 8 and 9 storage elements without separate access (bottom right, Fig. 4.2c)
- Structures prepared for testing resistance of vias and scanning electron microscopy (SEM) imaging during the fabrication process (bottom left, close-up not presented).

All the MTJ devices were fabricated as cylinders with nominal diameter of 100 nm. During the process, after forming of the pillar (Fig. 4.16), a SEM image was taken (Fig. 4.4) to verify the diameter of the pillar obtained - 130 nm. The difference from the intended size is normal for the process used, and originates from slight overexposure of the photo-resist. All elements were equipped with $100 \times 100 \mu\text{m}^2$ raster contact pads. Optical microscope images of the sample after complete nanostructurization are presented in Fig. 4.3. After the fabrication the sample was ready for the measurement process.

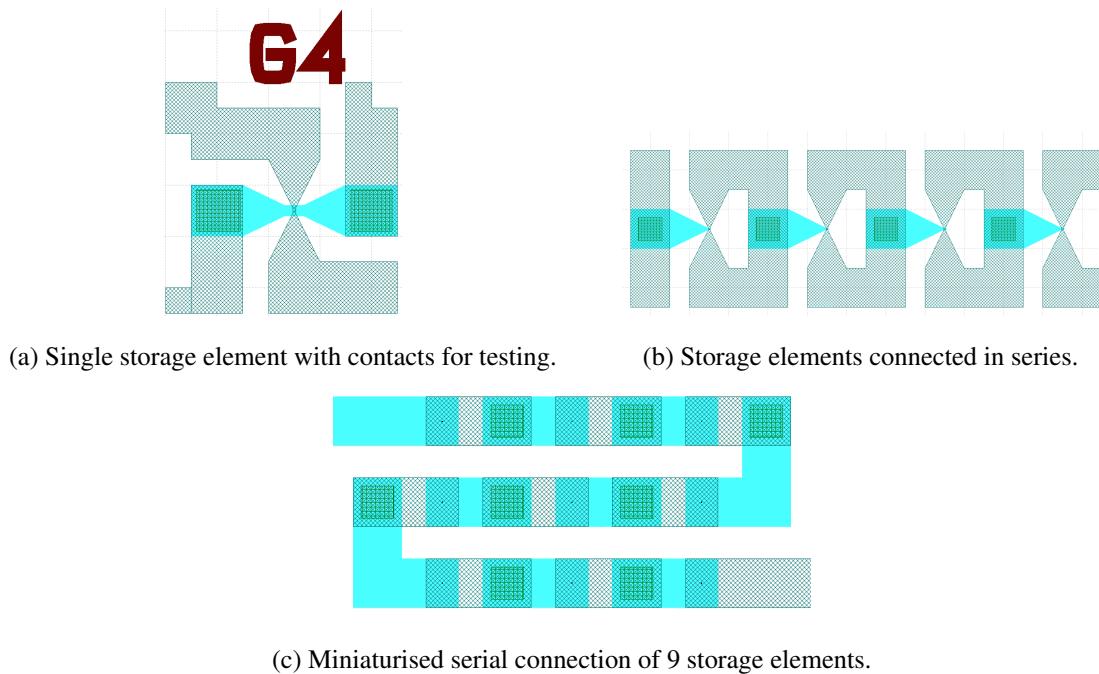


Figure 4.2: Close-ups of different parts of the mask. Scale is not the same for each element.

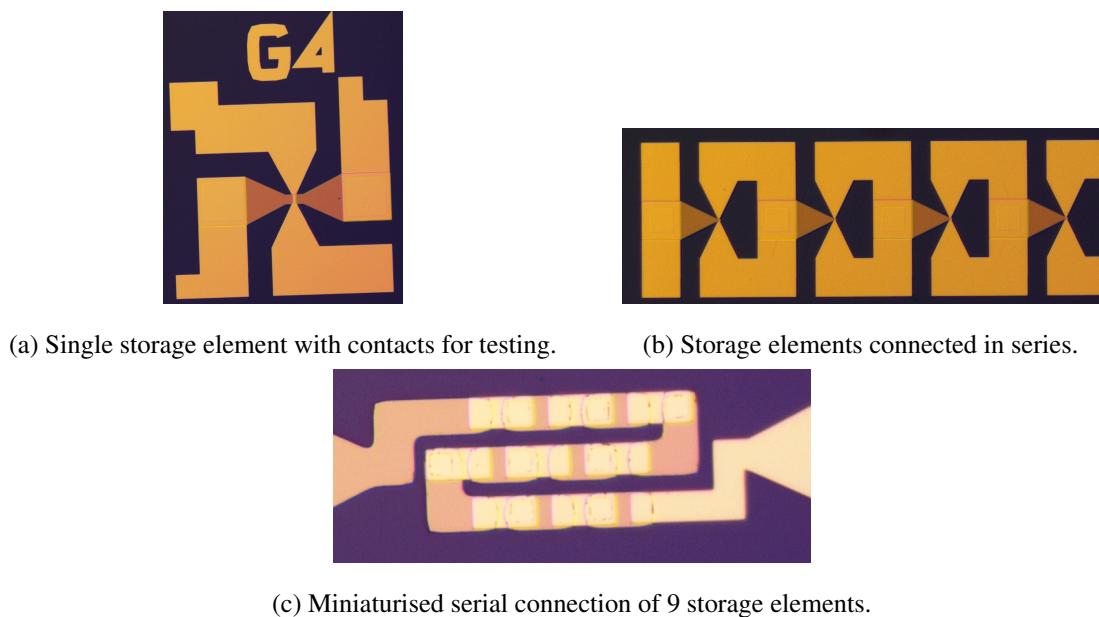


Figure 4.3: Close-ups of different parts of the sample. Scale is not the same for each element.



Figure 4.4: SEM image of the cylindrical storage element. The diameter was determined to be approximately 130 nm.

4.3. Fabrication

Layers forming MTJ, together with bottom buffer and top capping are deposited by Singulus AG on an oxidised silicon substrate (Figs. 4.5-4.7). These processing steps are performed by the company, because very precise control of deposition conditions are required to obtain correct crystalline structure, and finally a working MTJ. The deposition process is far beyond the scope of this thesis.

Further processing is performed in the Academic Center of Materials and Nanotechnology (ACMiN AGH). In subsequent steps:

- the bottom electrode is being formed (Figs. 4.8-4.11)
- the insulation is applied, to prevent forming unwanted connections during further processing (Figs. 4.12-4.13)
- pillars and vias are formed and the insulation oxide is applied (Figs. 4.14-4.18)
- top electrode is formed, including measurement contacts and connections between MTJ pillars (Figs. 4.19-4.24)



Figure 4.5: A polished and (if required) oxidised silicon wafer is prepared for processing. Size/thickness in this and the following figures are not to scale.

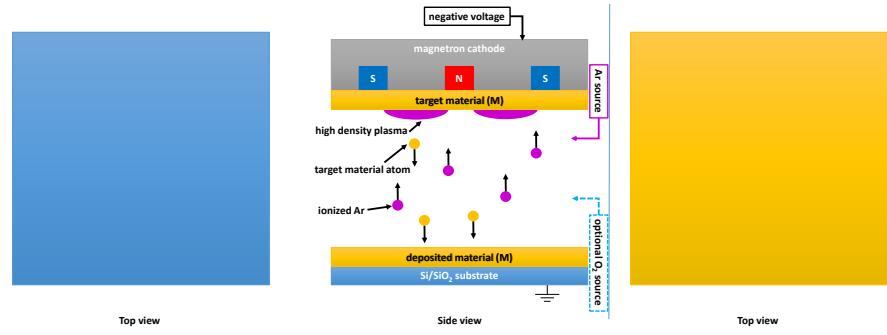


Figure 4.6: A thin film of target material is deposited by means of magnetron sputtering. Optionally, an oxygen flow may be provided in order to deposit target material oxide (e.g. MgO , Al_2O_3).

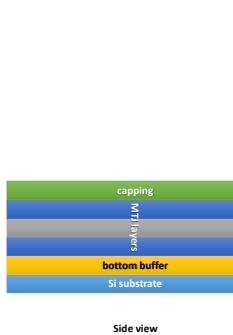


Figure 4.7: Requested layer stack with metallic bottom buffer and capping layer is deposited by means of magnetron sputtering. This process is conducted by Singulus AG, as conditions of deposition are crucial for correct crystallization, and therefore, operation of the MTJ. The sample is annealed to recrystallize all layers.

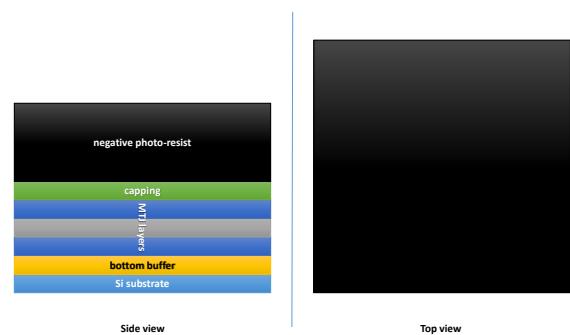


Figure 4.8: A negative photo-resist (AR-N 7720.30) is applied in spin-coater at 6000 rpm, resulting in thickness of approx. 1.24 μm . Then the sample is baked for 120 s at 85 °C.

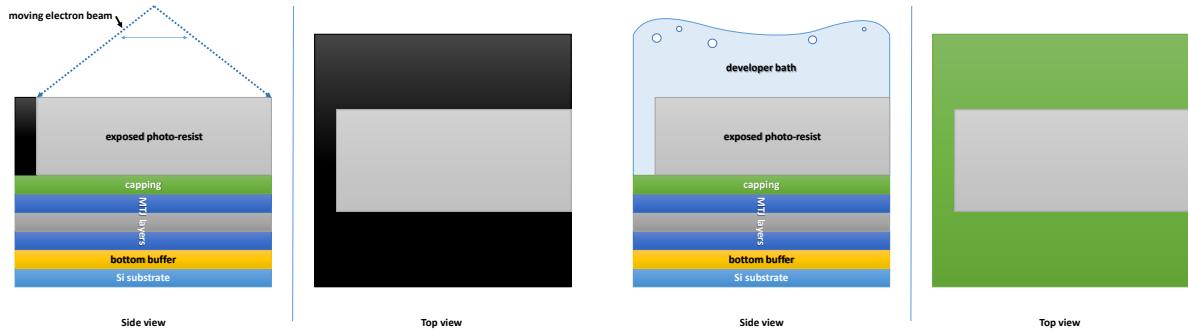


Figure 4.9: The photo-resist is exposed using electron beam to transfer bottom electrode shape. After the exposure the sample is baked for 60 s at 105 °C, and then for 20 min at 70 °C

Figure 4.10: The photo-resist is developed using AR 300-47 developer bath for 90 s and then rinsed in deionized water ($DI-H_2O$) for 30 s.

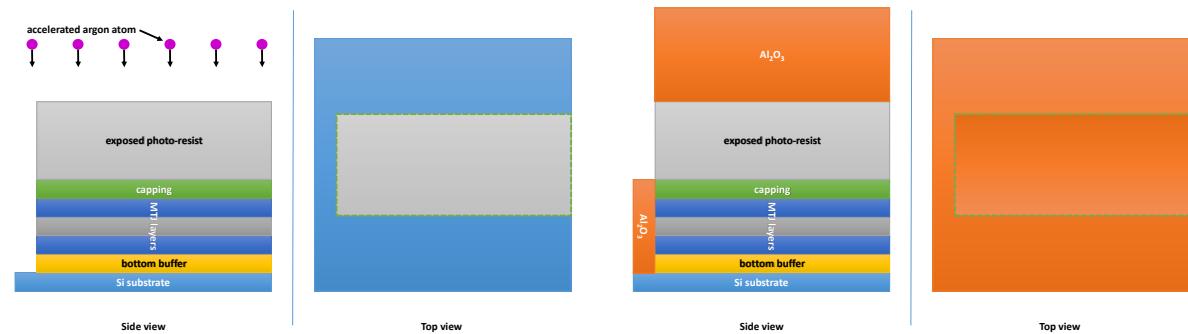


Figure 4.11: The sample is etched using ion etching to form a bottom electrode shape by reaching Si substrate. Mass spectrometer is used to determine layers that are being etched.

Figure 4.12: Al_2O_3 is deposited to match the etched height, using magnetron sputtering with Al target and O_2 injection near the sample.

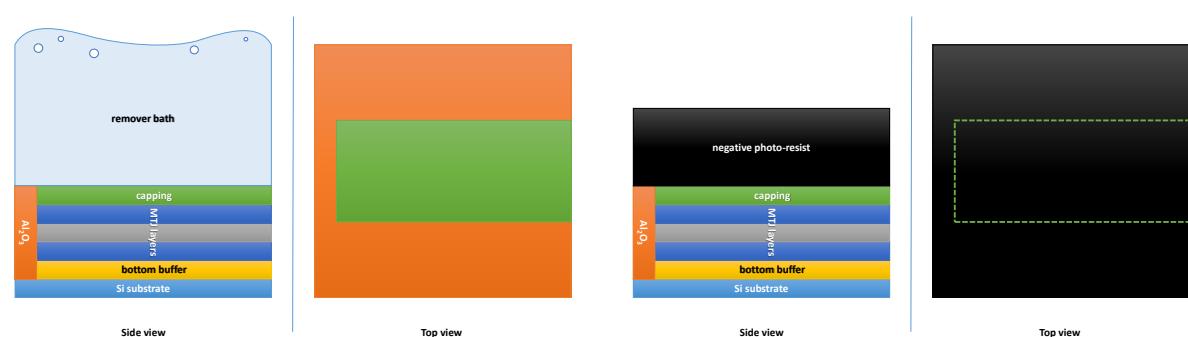


Figure 4.13: The photo-resist is removed with excess Al_2O_3 (the lift-off process) using 1-Methyl-2-pyrrolidinone by Sigma-Aldrich in ultrasonic washer for 15 min at 72 °C.

Figure 4.14: A negative photo-resist (AR-N 7520.17) is applied in spin-coater at 6000 rpm, resulting in thickness of approx. $0.3\ \mu m$. Then the sample is baked for 60 s at 85 °C.

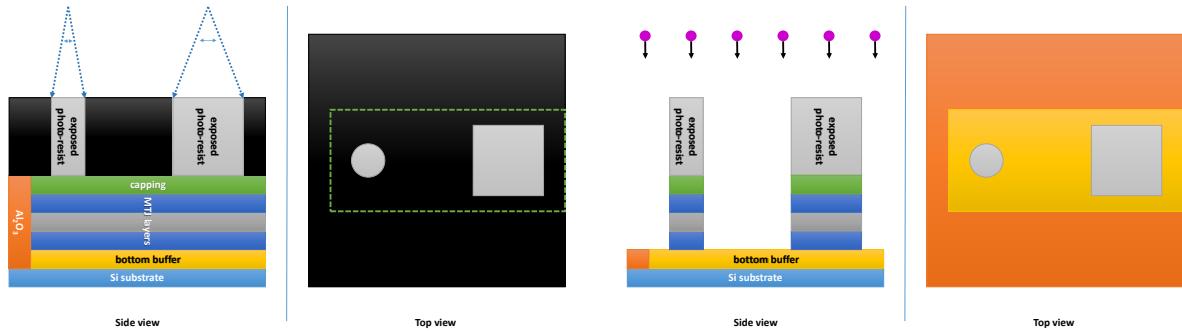


Figure 4.15: The photo-resist is exposed using electron beam to transfer pillar (circle) and via (square) shapes. (Dimensions in the figure are not to scale).

Figure 4.16: After developing the photo-resist (AR 300-46 for 90 s, $DI-H_2O$ for 30 s) etching is performed to reach bottom buffer. Etching time is strictly controlled based on the mass spectrometer signal, referenced to the data obtained during the first etching process (Fig. 4.11). The pillar and the via are formed.

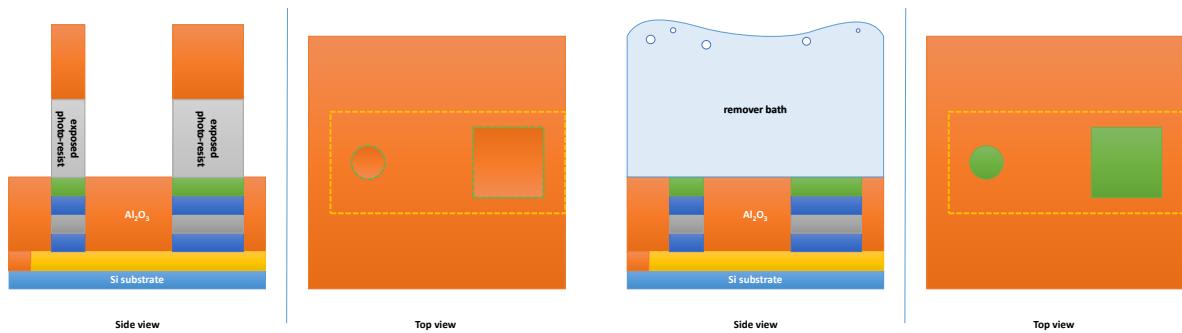


Figure 4.17: Al_2O_3 is deposited to match the etched height, using magnetron sputtering.

Figure 4.18: The photo-resist is removed with excess Al_2O_3 (the lift-off process) using 1-Methyl-2-pyrrolidinone by Sigma-Aldrich in ultrasonic washer for 15 min at 72 °C.

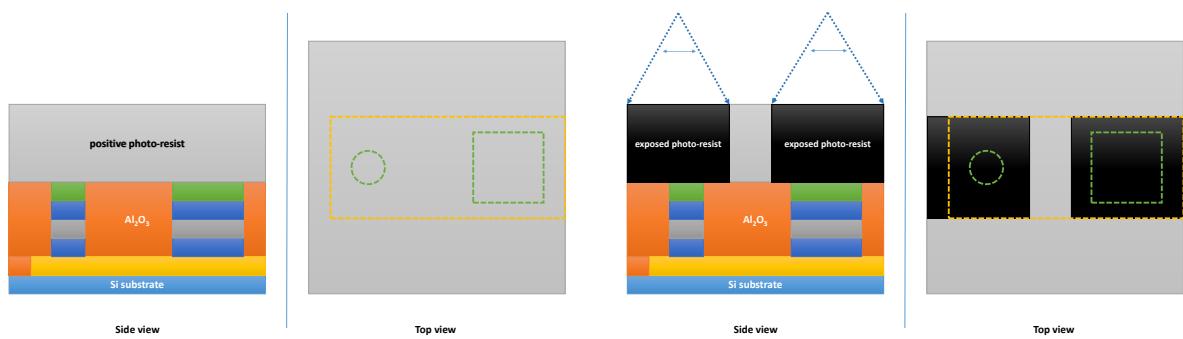


Figure 4.19: A positive photo-resist (AR-P 672.08) is applied in spin-coater at 6000 rpm, resulting in thickness of approx. 0.75 μm . Then the sample is baked for 180 s at 150 $^{\circ}\text{C}$.

Figure 4.20: The photo-resist is exposed using electron beam to transfer top electrode shape.

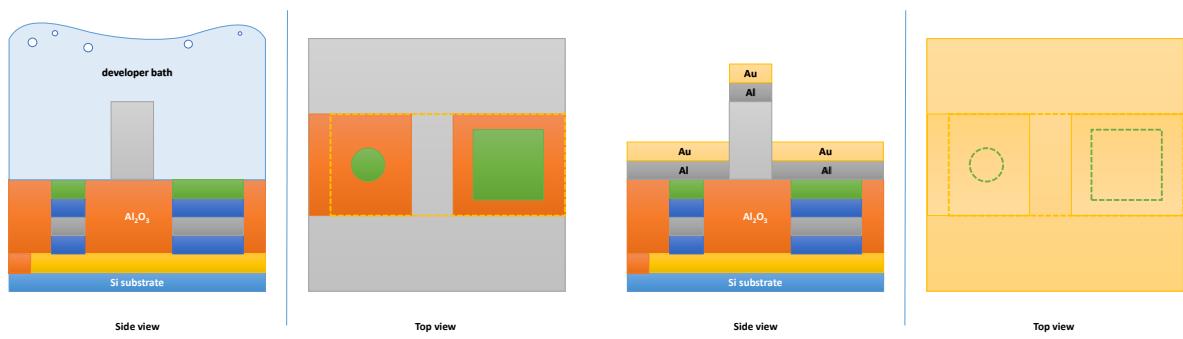


Figure 4.21: The photo-resist is developed using AR 600-55 developer bath for 60 s and then rinsed in *DI-H₂O* for 30 s.

Figure 4.22: *Al* (as buffer) and then *Au* (as top electrode) are deposited using magnetron sputtering.

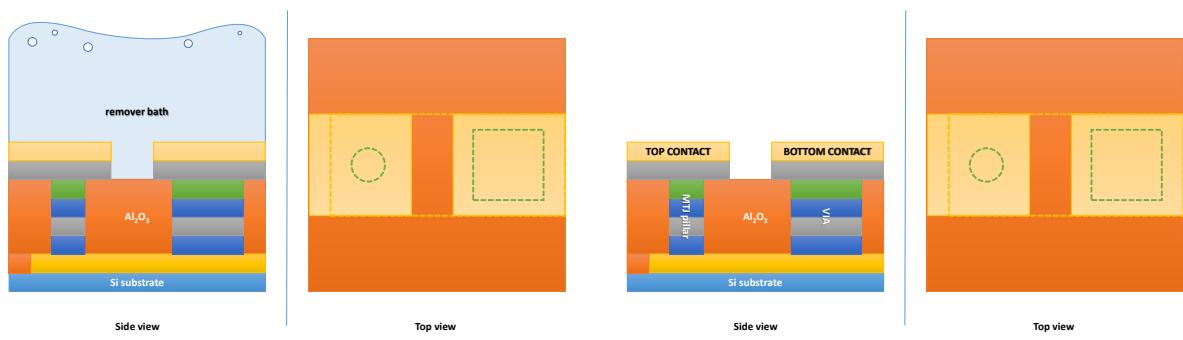


Figure 4.23: The photo-resist is removed with excess *Al* and *Au* (the lift-off process) using 1-Methyl-2-pyrrolidinone by Sigma-Aldrich in ultrasonic washer for 15 min at 72 $^{\circ}\text{C}$.

Figure 4.24: The process is completed. Contacts to access top and bottom side of the MTJ pillar are available.

5. Electrical measurements

This chapter describes the experimental setup, and presents the results of the measurements taken.

5.1. Measurement setup

In order to characterise a single storage element, as well as examine the behaviour of series connections, the experimental equipment should be able to:

- Apply and measure external magnetic field perpendicular to the sample plane.
- Measure the resistance of the sample
- Apply short (~ 1 ms) square voltage pulses and measure the resistance during each pulse.
- Provide precise and stable connection to the sample contact pads

All the requirements were met by using the setup presented in Figs. 5.1 and 5.2. The equipment used for the experiment consists of:

- GMW Dipole Electromagnet, model 3470, capable of generating magnetic field up to 790 kA/m
- Kepco BOP-series power supply (voltage controlled current source) with digital-to-analog USB adapter
- LakeShore 475 DSP Gaussmeter with Hall probe
- Keithley 2636A Sourcemeter
- Set of micropositioners equipped with tungsten or gold tips of ca. $20 - 50 \mu\text{m}$ in diameter
- PC with LabVIEW software for measurement automation
- microscope for positioning of the test tips

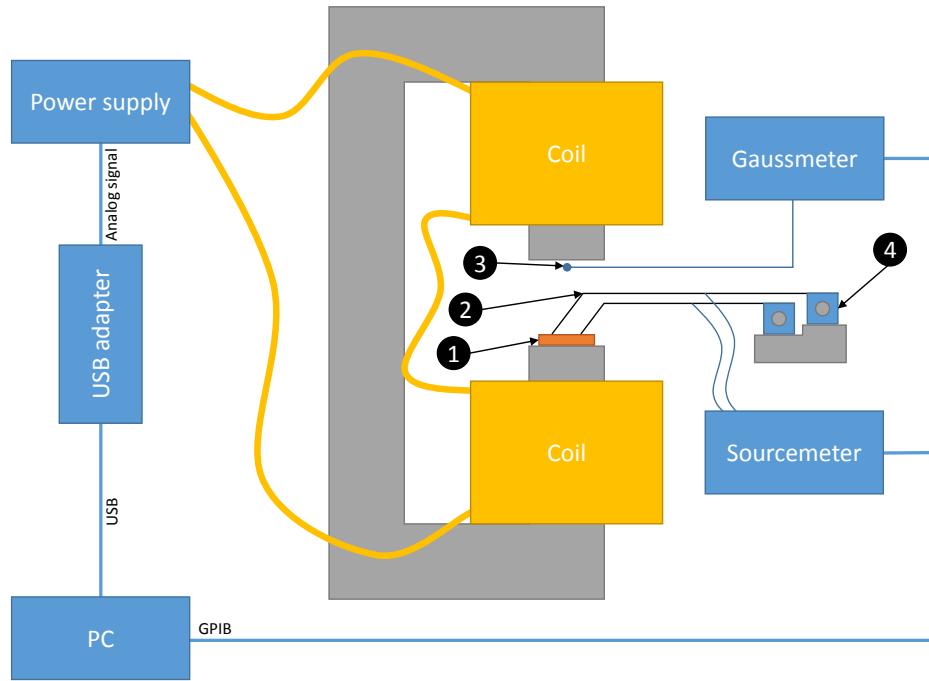
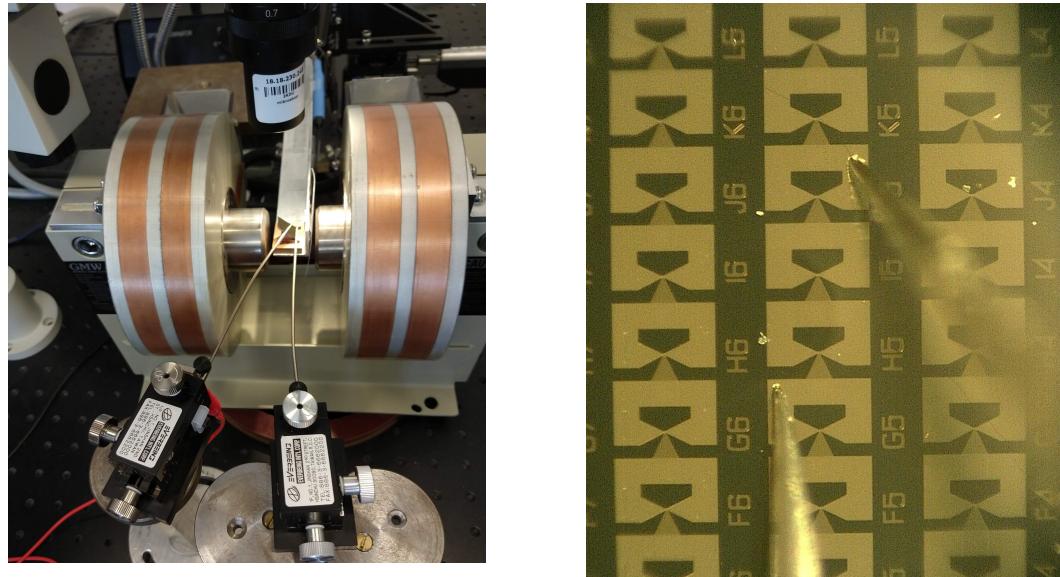


Figure 5.1: The schematic drawing of the measurement station. (1) denotes sample, (2) tungsten or gold tips, (3) Hall probe, (4) micropositioners.



(a) Photo of the main part of the measurement setup, including micropositioners, Hall probe and electromagnet. The mirror and the microscope is used to watch the sample while connecting the tips.

(b) Microscopic image of the sample under measurement with tungsten tips connected.

Figure 5.2: Photos of the measurement setup.

5.1.1. Measurement procedures

There are two types of measurement used in the characterisation of storage elements: measurement of resistance (with constant voltage applied across the element) as a function of external magnetic field (so called TMR measurement, see Sec. 3.4) and measurement of resistance as a function of amplitude of voltage pulse applied with constant external magnetic field (so called CIMS measurement, see Sec. 3.5). The exemplary waveform used for the second measurement is presented in Fig. 5.3. In the experiment the waveform with $t_p = 1 \text{ ms}$, $T = 10 \text{ ms}$ and $V_b = 50 \text{ mV}$ was used. The waveform is used instead of constant voltage in order to decrease the influence of thermal effects due to heating (by controlling energy applied to the element), and also to present impulse switching of the storage element. The CIMS measurement process incorporates four subsequent sweeps of V_p :

- from $-V_{min}$ to V_{neg}
- from V_{neg} to $-V_{min}$
- from V_{min} to V_{pos}
- from V_{pos} to V_{min}

V_{pos} and V_{neg} represent maximum positive and minimum negative impulse amplitude used in the experiment, respectively. V_{min} represents absolute minimum voltage, below which resistance/current measurement is unreliable when using selected measurement equipment.

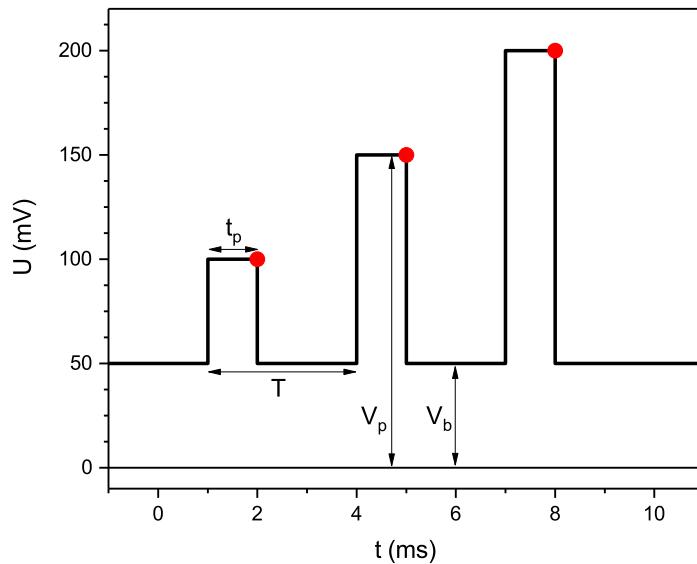


Figure 5.3: The exemplary waveform used for CIMS measurements. t_p denotes pulse duration, T - period, V_p - pulse amplitude and V_b - bias voltage. Red dots mark moments, when resistance measurement is taken.

5.2. Measurements

5.2.1. Separate storage element characterisation

In order to verify the operation of storage elements, TMR and CIMS measurements were performed on some of the separate elements. The results of TMR measurement (Fig. 5.4) in low magnetic field (see Fig. 3.6 b) show correct behaviour of the storage element.

Also, as described in Sec. 3.4, these TMR measurements were repeated about 50 times, with field step of 80 A/m in the area of interest, and time step of 1 s. The obtained data was analysed according to Eq. 3.5, and the results are presented in Fig. 5.5, together with derived parameters and representative TMR loops.

The CIMS measurement (Fig. 5.6) proved, that the produced storage element is able to be switched from P to AP and vice versa (compare with Fig. 3.8). Non-constant resistance versus V_p for the AP state is caused by the strong influence of the STT and is normally observed for such MTJ structures.

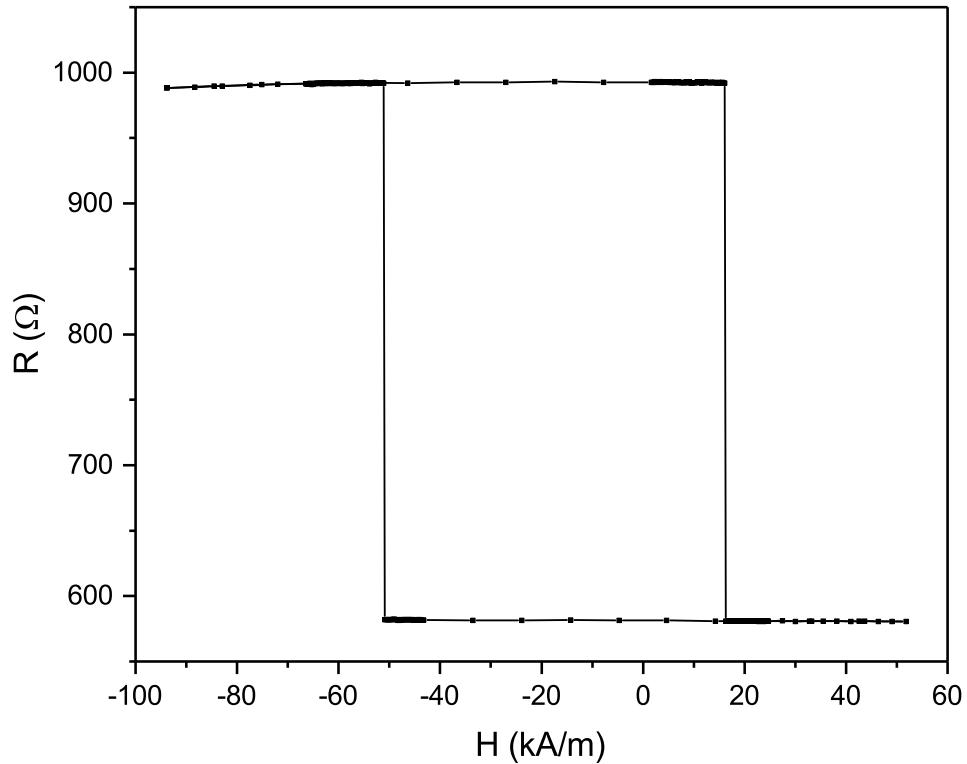


Figure 5.4: Hysteresis loop measured for a single storage element (MTJ). Two stable states are observed for $H = 0$ A/m. TMR is equal to 70.6 %

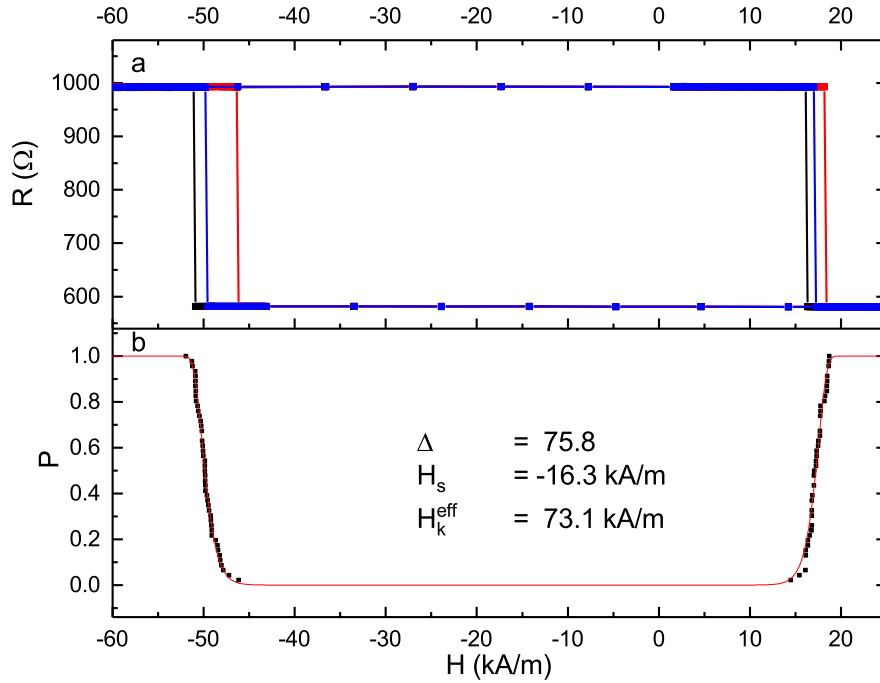


Figure 5.5: a) Representative TMR loops, with densified measurement points in regions where switching is expected to take place, b) calculated (based on measurements) switching probability (black points) and fitted theoretical curve. Derived Δ , H_s and H_k^{eff} are presented.

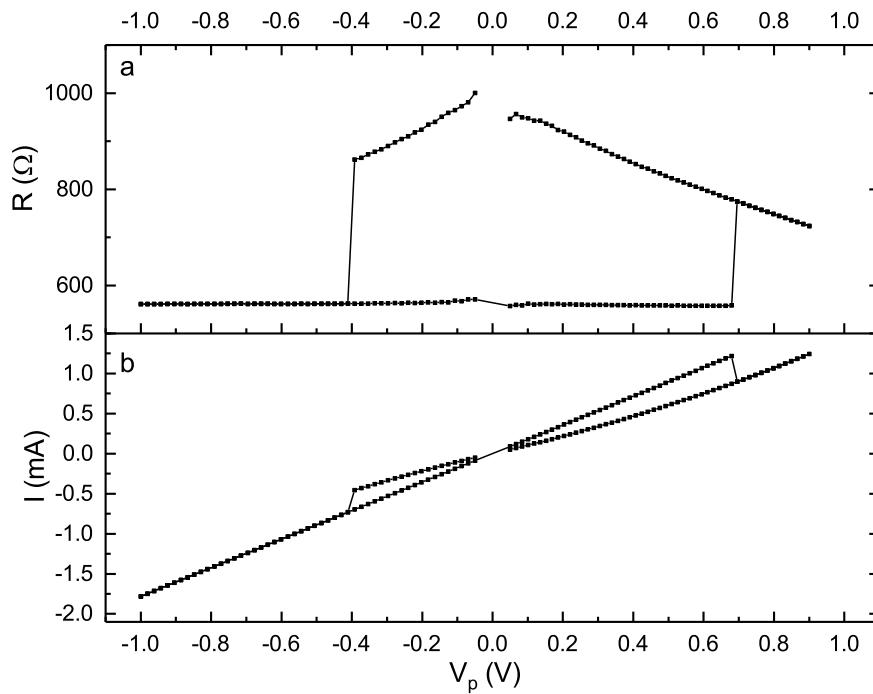


Figure 5.6: Resistance (a) and current (b) versus V_p at $H = 0$ A/m for a single storage element. CIMS effect is observed.

CIMS measurements (Fig. 5.7 a) were repeated with a range of external magnetic field H applied. For each external magnetic field, switching voltages from P to AP and vice versa were established, and plotted as voltage versus magnetic field (Fig. 5.7 b). These points created a stability diagram, which shows the region, where both P and AP states are stable, as well as only one of them above and below the region. Going outside P/AP stability region (by changing magnetic field, or amplitude of the voltage pulse) results in changing state to P or AP (writing data), while remaining inside the area allows measuring the resistance of the element (reading the data).

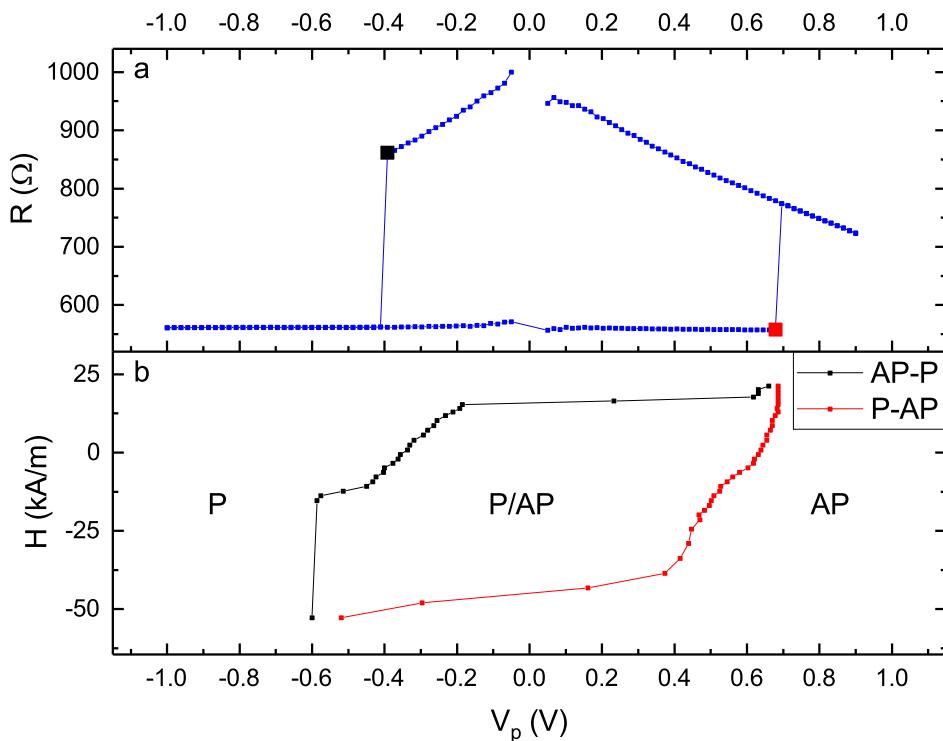


Figure 5.7: a) Representative CIMS measurement result at $H = 0$ A/m. Switching from AP to P, and from P to AP marked with black and red symbol, respectively, b) Stability diagram of the storage element. Lines indicate switching from P to AP or vice versa. Regions are marked with possible states of the storage MTJ (P, P/AP, AP).

It is vital to notice, that the element in zero field can be stable in both P and AP states and, therefore, it can be used as non-volatile storage without external magnetic field.

Some of the elements on the sample were found not working (no connection or short-circuit) due to non-ideal fabrication process.

5.2.2. Dual bit storage cell experiment

After the successful verification of operation of a single storage element, on a proper section of the sample three serially connected elements were selected and tested during CIMS measurements (Fig. 5.8). In subsequent measurements V_{pos} was increased. The predicted behaviour (Fig. 3.13) of serially connected storage elements was confirmed. In such storage cell, constructed of three individual storage elements, four stable states can be defined, and binary numbers can be assigned to them:

- all elements in AP state \Rightarrow "11"
- one element in P state and two elements in AP state \Rightarrow "10"
- two elements in P state and one element in AP state \Rightarrow "01"
- all elements in P state \Rightarrow "00"

Also, voltages to write particular states, as well as a region safe for reading the storage cell can be defined (Fig. 5.8 a).

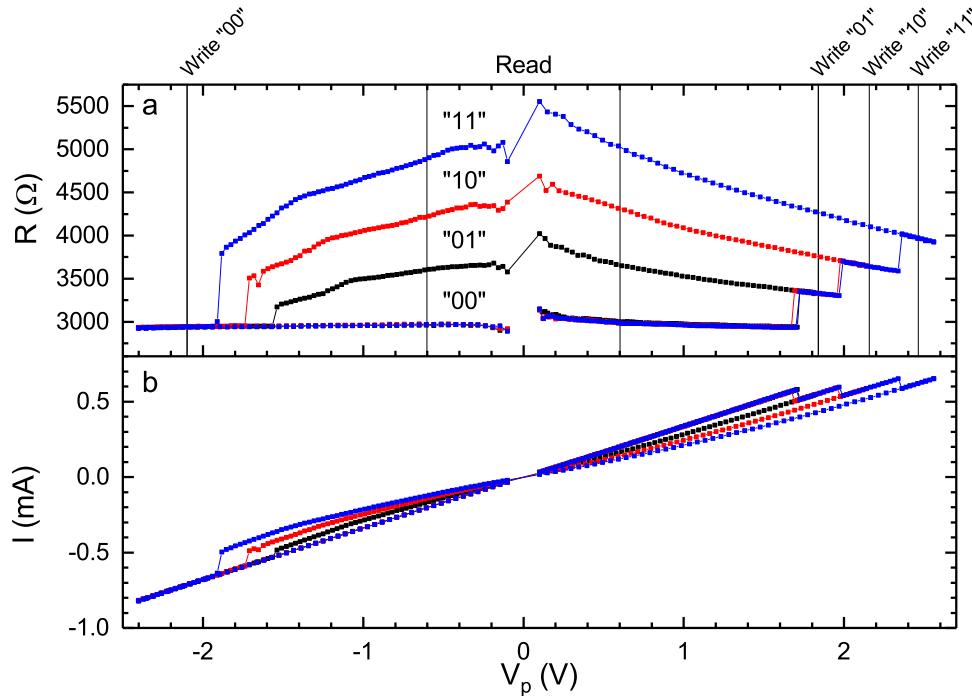


Figure 5.8: Results of CIMS measurement for storage cell constructed of three serially connected storage elements. Resistance changes for loops measured with different V_{pos} (different colours) prove the ability of the storage cell to act as a multi-bit cell. The proposed binary coding, voltages for writing, and safe readout are presented (a). Current changes during the process (b).

Also, the principle of operation, involving the current decreasing below the critical current after one element switching into AP state, was confirmed (Fig. 5.9). Due to non-ideal manufacturing process, critical currents of all incorporated elements are non-equal, but this has no adverse effect on the process.

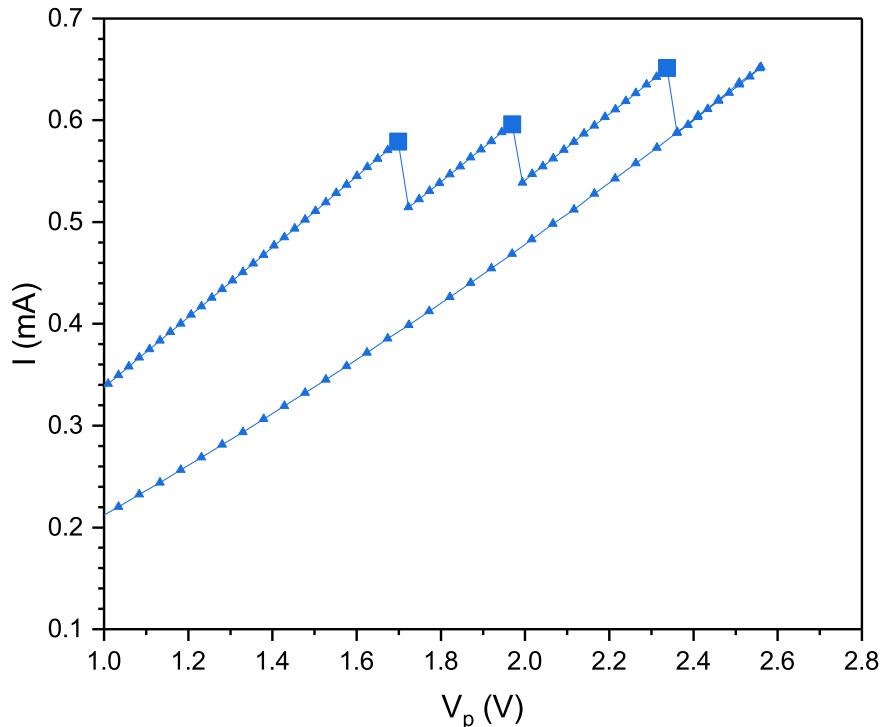


Figure 5.9: A close up of current in the CIMS measurement. Critical currents, causing subsequent elements to switch to the AP state are marked with squares.

5.2.3. Triple bit storage cell experiment

Utilising the mechanism a storage cell constructed of seven storage elements were subjected to CIMS measurement. As predicted, the cell exhibited eight stable states (Fig. 5.10). The issue was noticed, that regions for writing some of the states are very narrow, due to variation of the switching voltage (related with the switching current). It is believed, that the behaviour is due to very similar critical currents of all incorporated elements. Also switching to "000" state was not ideal in the case, and needs further investigation.

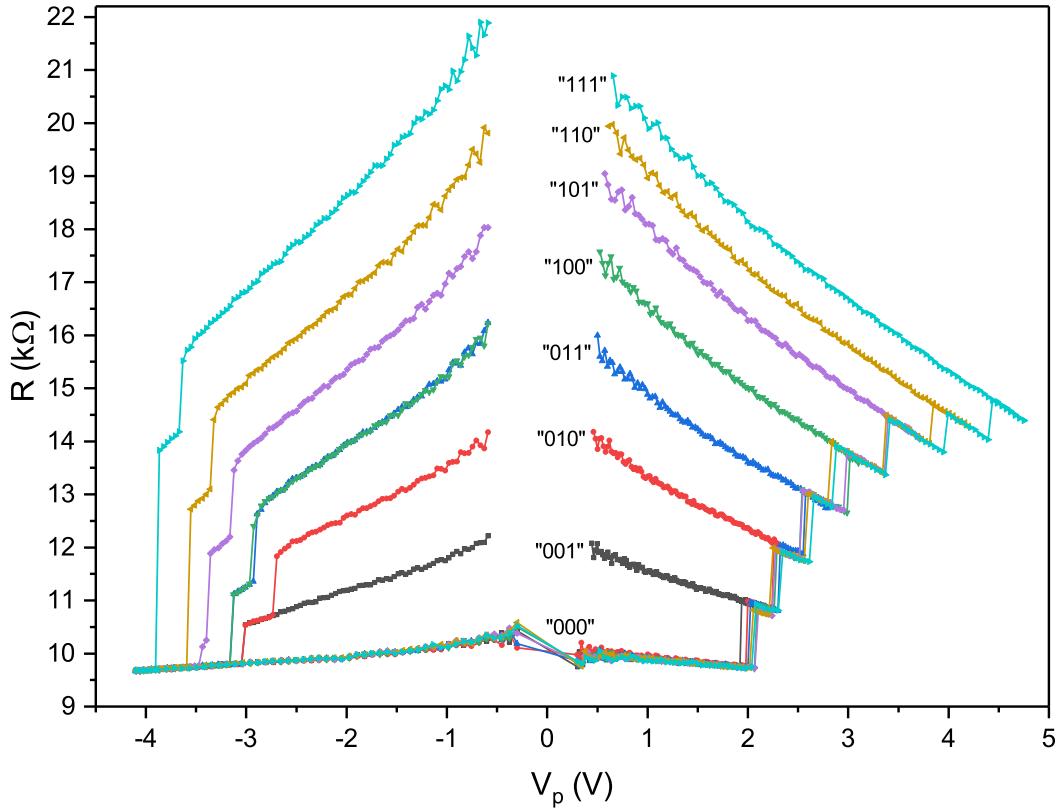


Figure 5.10: Results of CIMS measurement for storage cell constructed of seven serially connected storage elements. Resistance changes for loops measured with different V_{pos} are presented in different colours. The proposed binary coding is presented.

5.3. Experiment summary

The conducted experiments were successful and confirmed the predicted behaviour of single storage elements as well as multi-bit (two- and three-bit) storage cells. Larger cells were not tested, because it was not possible to find 15 subsequent serially connected working storage elements and also miniaturised storage cells were not operating due to fabrication issues.

6. Future work

The measurements' results revealed, that the biggest issue with such design of multi-bit storage cell is the narrow region for writing higher resistances, due to the stochastic nature of the switching process of the cells with very similar parameters. A solution to the problem may be to intentionally vary some of the parameters, by using serially connected elements of different sizes. By varying the size, the critical current and resistance of the element may be changed.

Another vital improvement is to optimise the nanostructurization process in order to minimize the number of non-working elements. This improvement would increase chances to test bigger storage cells as well as produce fully operational miniaturised serial connections.

With the increased number of storage elements in a storage cell, higher voltage is needed to switch the cell. Another field of improvement would be to decrease resistance of the element, maximize TMR as well as minimise the critical current. Such improvements would lead to the decrease of supply voltage of the memory, but they are most difficult to implement, due to the complex layer structure of the MTJ.

7. Summary

By analysing the theoretical behaviour of MTJa described in the literature, the performance of serially and parallelly connected elements was predicted. Serial connection was believed to act as a multi-bit storage cell, and was selected for experimental verification.

The experiment involved fabrication of multi-bit storage cells, utilizing the previously developed MTJ layer structure. Two- and three-bit storage cells were successfully tested, proving that the theoretical analysis was correct.

The developed method of manufacturing and driving multi-bit non-volatile storage elements is a significant improvement in MRAM technology, as it allows to store more data using the same area of the memory. This is achieved by driving a multi-bit storage cell using a single transistor rated for the same current, as a single storage element (the critical current remains the same for any number of serially connected elements). Also, the manufacturing process, utilizing vias fabricated in the same step as the MTJ pillar, does not require significant changes compared to single storage element fabrication.

For now, significant drawbacks of the storage cell are quite narrow regions for switching subsequent elements to the AP state and relatively high voltages involved. The first one may be overcome by using serially connected elements of slightly different sizes. The other drawback needs careful MTJ stack redesign.

In conclusion, the presented work is an important step to develop a functional STT-MRAM memory with increased data density, and proves, that multi-bit storage elements may be easily manufactured. Also, the presented solution is the subject of patent proceedings.

8. Acknowledgements

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