NAME

PAPI_presets - PAPI predefined named events

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SYNOPSIS

#include <papi.h>

DESCRIPTION

The PAPI library names a number of predefined events. This set is a collection of events typically found in many CPUs that provide performance counters. A PAPI preset event name is mapped onto one or more of the countable events on each hardware platform. On any particular platform, the preset can either be directly available as a single counter, derived using a combination of counters or unavailable.

The PAPI preset events can be broken loosely into several categories, as shown in the table below:

Conditional Branching:

Name	Description
Conditional Branching	
PAPI_BR_CN	Conditional branch instructions
PAPI_BR_INS	Branch instructions
PAPI_BR_MSP	Conditional branch instructions mispredicted
PAPI_BR_NTK	Conditional branch instructions not taken
PAPI_BR_PRC	Conditional branch instructions correctly predicted
PAPI_BR_TKN	Conditional branch instructions taken
PAPI_BR_UCN	Unconditional branch instructions
PAPI_BRU_IDL	Cycles branch units are idle
PAPI_BTAC_M	Branch target address cache misses
Cache Requests:	
PAPI_CA_CLN	Requests for exclusive access to clean cache line
PAPI_CA_INV	Requests for cache line invalidation
PAPI_CA_ITV	Requests for cache line intervention
PAPI_CA_SHR	Requests for exclusive access to shared cache line
PAPI_CA_SNP	Requests for a snoop
Conditional Store:	
PAPI_CSR_FAL	Failed store conditional instructions

PAPI_CSR_SUC	Successful store conditional instructions
PAPI_CSR_TOT	Total store conditional instructions
Floating Point Operations:	
PAPI_FAD_INS	Floating point add instructions
PAPI_FDV_INS	Floating point divide instructions
PAPI_FLOPS	Floating point instructions per second
PAPI_FMA_INS	FMA instructions completed
PAPI_FML_INS	Floating point multiply instructions
PAPI_FNV_INS	Floating point inverse instructions
PAPI_FP_INS	Floating point instructions
PAPI_FP_STAL	Cycles the FP unit
PAPI_FPU_IDL	Cycles floating point units are idle
PAPI_FSQ_INS	Floating point square root instructions
Instruction Counting:	
PAPI_FUL_CCY	Cycles with maximum instructions completed
PAPI_FUL_ICY	Cycles with maximum instruction issue
PAPI_FXU_IDL	Cycles integer units are idle
PAPI_HW_INT	Hardware interrupts
PAPI_INT_INS	Integer instructions
PAPI_IPS	Instructions per second
PAPI_TOT_CYC	Total cycles
PAPI_TOT_IIS	Instructions issued
PAPI_TOT_INS	Instructions completed
PAPI_VEC_INS	Vector/SIMD instructions
Cache Access:	
PAPI_L1_DCA	L1 data cache accesses
PAPI_L1_DCH	L1 data cache hits
PAPI_L1_DCM	Level 1 data cache misses
PAPI_L1_DCR	L1 data cache reads
PAPI_L1_DCW	L1 data cache writes
PAPI_L1_ICA	L1 instruction cache accesses
PAPI_L1_ICH	L1 instruction cache hits
PAPI_L1_ICM	Level 1 instruction cache misses
PAPI_L1_ICR	L1 instruction cache reads
PAPI_L1_ICW	L1 instruction cache writes
PAPI_L1_LDM	Level 1 load misses
PAPI_L1_STM	Level 1 store misses
PAPI_L1_TCA	L1 total cache accesses
PAPI_L1_TCH	L1 total cache hits
PAPI_L1_TCM	Level 1 cache misses
PAPI_L1_TCR	L1 total cache reads
PAPI_L1_TCW	L1 total cache writes
PAPI_L2_DCA	L2 data cache accesses
PAPI_L2_DCH	L2 data cache hits

PAPI_L2_DCM	Level 2 data cache misses
PAPI_L2_DCR	L2 data cache reads
PAPI_L2_DCW	L2 data cache writes
PAPI_L2_ICA	L2 instruction cache accesses
PAPI_L2_ICH	L2 instruction cache hits
PAPI_L2_ICM	Level 2 instruction cache misses
PAPI_L2_ICR	L2 instruction cache reads
PAPI_L2_ICW	L2 instruction cache writes
PAPI_L2_LDM	Level 2 load misses
PAPI_L2_STM	Level 2 store misses
PAPI_L2_TCA	L2 total cache accesses
PAPI_L2_TCH	L2 total cache hits
PAPI_L2_TCM	Level 2 cache misses
PAPI_L2_TCR	L2 total cache reads
PAPI_L2_TCW	L2 total cache writes
PAPI_L3_DCA	L3 data cache accesses
PAPI_L3_DCH	Level 3 Data Cache Hits
PAPI_L3_DCM	Level 3 data cache misses
PAPI_L3_DCR	L3 data cache reads
PAPI_L3_DCW	L3 data cache writes
PAPI_L3_ICA	L3 instruction cache accesses
PAPI_L3_ICH	L3 instruction cache hits
PAPI_L3_ICM	Level 3 instruction cache misses
PAPI_L3_ICR	L3 instruction cache reads
PAPI_L3_ICW	L3 instruction cache writes
PAPI_L3_LDM	Level 3 load misses
PAPI_L3_STM	Level 3 store misses
PAPI_L3_TCA	L3 total cache accesses
PAPI_L3_TCH	L3 total cache hits
PAPI_L3_TCM	Level 3 cache misses
PAPI_L3_TCR	L3 total cache reads
PAPI_L3_TCW	L3 total cache writes
Data Access:	
PAPI_LD_INS	Load instructions
PAPI_LST_INS	Load/store instructions completed
PAPI_LSU_IDL	Cycles load/store units are idle
PAPI_MEM_RCY	Cycles Stalled Waiting for memory Reads
PAPI_MEM_SCY	Cycles Stalled Waiting for memory accesses
PAPI_MEM_WCY	Cycles Stalled Waiting for memory writes
PAPI_PRF_DM	Data prefetch cache misses
PAPI_RES_STL	Cycles stalled on any resource
PAPI_SR_INS	Store instructions
PAPI_STL_CCY	Cycles with no instructions completed

PAPI_STL_ICY	Cycles with no instruction issue
PAPI_SYC_INS	Synchronization instructions completed
TLB Operations:	
PAPI_TLB_DM	Data translation lookaside buffer misses
PAPI_TLB_IM	Instruction translation lookaside buffer misses
PAPI_TLB_SD	Translation lookaside buffer shootdowns
PAPI_TLB_TL	Total translation lookaside buffer misses

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BUGS

The exact semantics of an event counter are platform dependent. PAPI preset names are mapped onto available events in a way so as to count as similar types of events as possible on different platforms. Due to hardware implementation differences it is not necessarily possible to directly compare the counts of a particular PAPI event obtained on different hardware platforms.

SEE ALSO

PAPI (3), PAPI_query_event (3) The PAPI Web Site: http://icl.cs.utk.edu/projects/papi