Low-Noise, Very Low Drift, Precision VOLTAGE REFERENCE

Check for Samples: REF5010, REF5020, REF5025, REF5030, REF5040, REF5045, REF5050

FEATURES

- LOW TEMPERATURE DRIFT:
  - High-Grade: 3ppm/°C (max)
  - Standard-Grade: 8ppm/°C (max)
- HIGH ACCURACY:
  - High-Grade: 0.05% (max)
  - Standard-Grade: 0.1% (max)
- LOW NOISE: 3μV_{PP}/V
- EXCELLENT LONG-TERM STABILITY:
  - 5ppm/1000hr (typ) after 1000 hours
- HIGH OUTPUT CURRENT: ±10mA
- TEMPERATURE RANGE: –40°C to +125°C

APPLICATIONS

- 16-BIT DATA ACQUISITION SYSTEMS
- ATE EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- MEDICAL INSTRUMENTATION
- OPTICAL CONTROL SYSTEMS
- PRECISION INSTRUMENTATION

DESCRIPTION

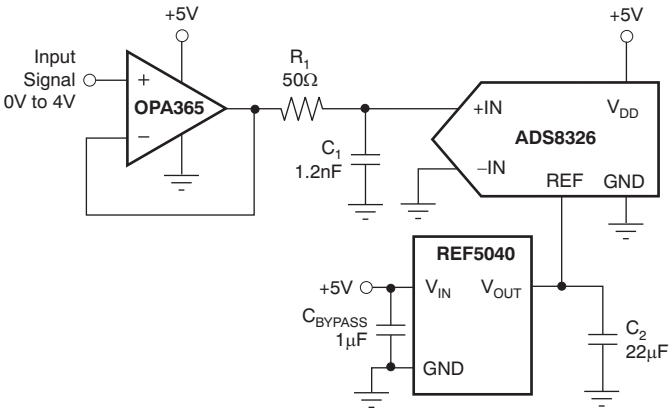
The REF50xx is a family of low-noise, low-drift, very high precision voltage references. These references are capable of both sinking and sourcing, and are very robust with regard to line and load changes.

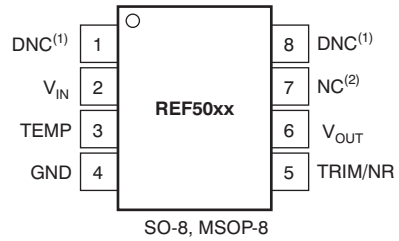
Excellent temperature drift (3ppm/°C) and high accuracy (0.05%) are achieved using proprietary design techniques. These features, combined with very low noise, make the REF50xx family ideal for use in high-precision data acquisition systems.

Each reference voltage is available in both standard- and high-grade versions. They are offered in MSOP-8 and SO-8 packages, and are specified from –40°C to +125°C.

REF50xx Family

MODEL	OUTPUT VOLTAGE
REF5020	2.048V
REF5025	2.5V
REF5030	3.0V
REF5040	4.096V
REF5045	4.5V
REF5050	5.0V
REF5010	10.0V





NOTES: (1) DNC = Do not connect.
(2) NC = No internal connection.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	OUTPUT VOLTAGE	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
STANDARD GRADE (8ppm, 0.1%)				
REF5020A	2.048V	SO-8	D	REF5020
		MSOP-8	DGK	R50A
REF5025A	2.5V	SO-8	D	REF5025
		MSOP-8	DGK	R50B
REF5030A	3.0V	SO-8	D	REF5030
		MSOP-8	DGK	R50C
REF5040A	4.096V	SO-8	D	REF5040
		MSOP-8	DGK	R50D
REF5045A	4.5V	SO-8	D	REF5045
		MSOP-8	DGK	R50E
REF5050A	5.0V	SO-8	D	REF5050
		MSOP-8	DGK	R50F
REF5010A	10.0V	SO-8	D	REF5010
		MSOP-8	DGK	R50G
HIGH GRADE (3ppm, 0.05%)				
REF5020I	2.048V	SO-8	D	REF5020
		MSOP-8	DGK	R50A
REF5025I	2.5V	SO-8	D	REF5025
		MSOP-8	DGK	R50B
REF5030I	3.0V	SO-8	D	REF5030
		MSOP-8	DGK	R50C
REF5040I	4.096V	SO-8	D	REF5040
		MSOP-8	DGK	R50D
REF5045I	4.5V	SO-8	D	REF5045
		MSOP-8	DGK	R50E
REF5050I	5.0V	SO-8	D	REF5050
		MSOP-8	DGK	R50F
REF5010I	10.0V	SO-8	D	REF5010
		MSOP-8	DGK	R50G

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

PARAMETER		REF50xx	UNIT
Input Voltage		+18	V
Output Short-Circuit		30	mA
Operating Temperature Range		–55 to +125	°C
Storage Temperature Range		–65 to +150	°C
Junction Temperature (T_J max)		+150	°C
ESD Rating	Human Body Model (HBM)	3000	V
	Charged Device Model (CDM)	1000	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS: PER DEVICE

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, I_{LOAD} = 0, C_L = 1µF, and V_{IN} = (V_{OUT} + 0.2V) to 18V, unless otherwise noted.

PARAMETER	CONDITIONS	PER DEVICE MIN	PER DEVICE TYP	PER DEVICE MAX	UNIT
REF5020 (V_{OUT} = 2.048V)(1)					
OUTPUT VOLTAGE					
Output Voltage V_{OUT}	2.7V < V_{IN} < 18V		2.048		V
Initial Accuracy: High-Grade		–0.05		0.05	%
Standard-Grade		–0.1		0.1	%
NOISE					
Output Voltage Noise	f = 0.1Hz to 10Hz		6		μV_{PP}
REF5025 (V_{OUT} = 2.5V)					
OUTPUT VOLTAGE					
Output Voltage V_{OUT}			2.5		V
Initial Accuracy: High-Grade		–0.05		0.05	%
Standard-Grade		–0.1		0.1	%
NOISE					
Output Voltage Noise	f = 0.1Hz to 10Hz		7.5		μV_{PP}
REF5030 (V_{OUT} = 3.0V)					
OUTPUT VOLTAGE					
Output Voltage V_{OUT}			3.0		V
Initial Accuracy: High-Grade		–0.05		0.05	%
Standard-Grade		–0.1		0.1	%
NOISE					
Output Voltage Noise	f = 0.1Hz to 10Hz		9		μV_{PP}
REF5040 (V_{OUT} = 4.096V)					
OUTPUT VOLTAGE					
Output Voltage V_{OUT}			4.096		V
Initial Accuracy: High-Grade		–0.05		0.05	%
Standard-Grade		–0.1		0.1	%
NOISE					
Output Voltage Noise	f = 0.1Hz to 10Hz		12		μV_{PP}
REF5045 (V_{OUT} = 4.5V)					
OUTPUT VOLTAGE					
Output Voltage V_{OUT}			4.5		V
Initial Accuracy: High-Grade		–0.05		0.05	%
Standard-Grade		–0.1		0.1	%
NOISE					
Output Voltage Noise	f = 0.1Hz to 10Hz		13.5		μV_{PP}
REF5050 (V_{OUT} = 5.0V)					
OUTPUT VOLTAGE					
Output Voltage V_{OUT}			5.0		V
Initial Accuracy: High-Grade		–0.05		0.05	%
Standard-Grade		–0.1		0.1	%
NOISE					
Output Voltage Noise	f = 0.1Hz to 10Hz		15		μV_{PP}
REF5010 (V_{OUT} = 10.0V)					
OUTPUT VOLTAGE					
Output Voltage V_{OUT}			10.0		V
Initial Accuracy: High-Grade		–0.05		0.05	%
Standard-Grade		–0.1		0.1	%
NOISE					
Output Voltage Noise	f = 0.1Hz to 10Hz		30		μV_{PP}

(1) For V_{OUT} ≤ 2.5V, the minimum supply voltage is 2.7V.

ELECTRICAL CHARACTERISTICS: ALL DEVICES

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, I_{LOAD} = 0, C_L = 1µF, and V_{IN} = (V_{OUT} + 0.2V) to 18V, unless otherwise noted.

PARAMETER		CONDITIONS	REF50xx MIN	REF50xx TYP	REF50xx MAX	UNIT
OUTPUT VOLTAGE TEMPERATURE DRIFT						
Output Voltage Temperature Drift	**dV_{OUT}/dT**					
High-Grade				**2.5**	**3**	**ppm/°C**
Standard-Grade				**3**	**8**	**ppm/°C**
LINE REGULATION						
Line Regulation	dV_{OUT}/dV_{IN}					
REF5020[1] Only		V_{IN} = 2.7V to 18V		0.1	1	ppm/V
All Other Devices		V_{IN} = V_{OUT} + 0.2V		0.1	1	ppm/V
Over Temperature				**0.2**	**1**	**ppm/V**
LOAD REGULATION						
Load Regulation	dV_{OUT}/d_{ILOAD}	–10mA < I_{LOAD} < +10mA				
REF5020 Only		V_{IN} = 3V		20	30	ppm/mA
All Other Devices		V_{IN} = V_{OUT} + 0.75V		20	30	ppm/mA
Over Temperature					**50**	**ppm/mA**
SHORT-CIRCUIT CURRENT						
Short-Circuit Current	I_{SC}	V_{OUT} = 0		25		mA
THERMAL HYSTERESIS [2]						
High-Grade	MSOP-8	Cycle 1		10		ppm
Standard-Grade	MSOP-8	Cycle 1		30		ppm
High-Grade	SO-8	Cycle 1		5		ppm
Standard-Grade	SO-8	Cycle 1		10		ppm
High-Grade	MSOP-8	Cycle 2		5		ppm
Standard-Grade	MSOP-8	Cycle 2		10		ppm
High-Grade	SO-8	Cycle 2		3		ppm
Standard-Grade	SO-8	Cycle 2		5		ppm
LONG-TERM STABILITY						
MSOP-8		0 to 1000 hours		50		ppm/1000 hr
MSOP-8		1000 to 2000 hours		5		ppm/1000 hr
SO-8		0 to 1000 hours		90		ppm/1000 hr
SO-8		1000 to 2000 hours		10		ppm/1000 hr
TEMP PIN						
Voltage Output		At T_A = +25°C		575		mV
Temperature Sensitivity				**2.64**		**mV/°C**
TURN-ON SETTLING TIME						
Turn-On Settling Time		To 0.1% with C_L = 1µF		200		µs
POWER SUPPLY						
Supply Voltage	V_S	See Note [1]	V_{OUT} + 0.2[1]		18	V
Quiescent Current				0.8	1	mA
Over Temperature					**1.2**	**mA**
TEMPERATURE RANGE						
Specified Range			–40		+125	°C
Operating Range			–55		+125	°C
Thermal Resistance	θ_{JA}					
MSOP-8				150		°C/W
SO-8				150		°C/W

(1) For V_{OUT} ≤ 2.5V, the minimal supply voltage is 2.7V.
(2) The thermal hysteresis procedure is explained in more detail in the *Application Information* section.

TYPICAL CHARACTERISTICS

At T_A = +25°C, I_{LOAD} = 0, and V_S = V_{OUT} + 0.2V, unless otherwise noted. For V_{OUT} ≤ 2.5V, the minimum supply voltage is 2.7V.

TEMPERATURE DRIFT (0°C to +85°C)

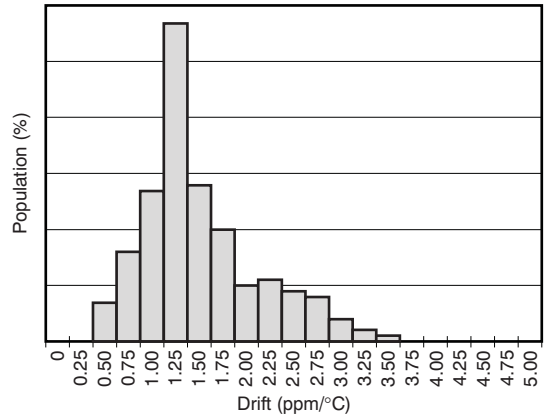


Figure 1.

TEMPERATURE DRIFT (–40°C to +125°C)

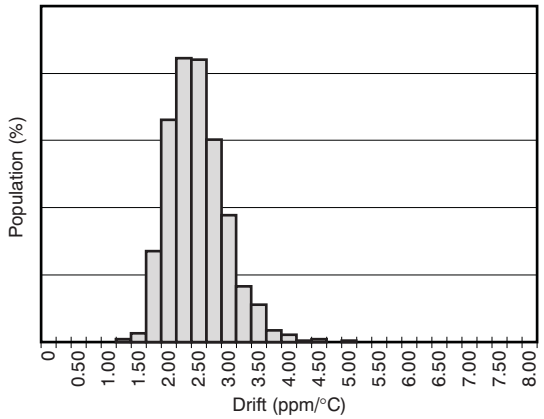


Figure 2.

OUTPUT VOLTAGE INITIAL ACCURACY

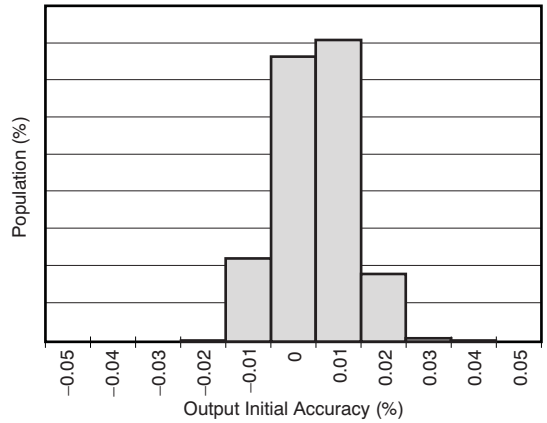


Figure 3.

OUTPUT VOLTAGE ACCURACY vs TEMPERATURE

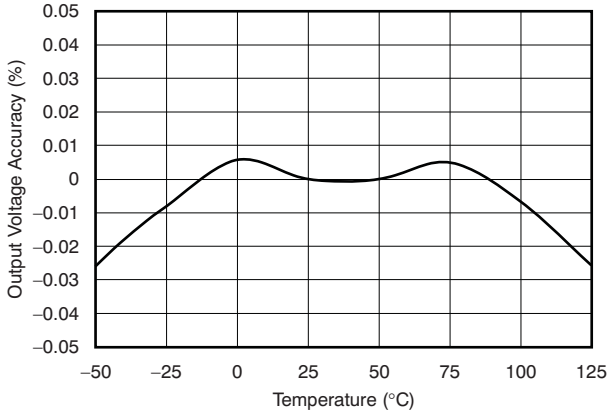


Figure 4.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

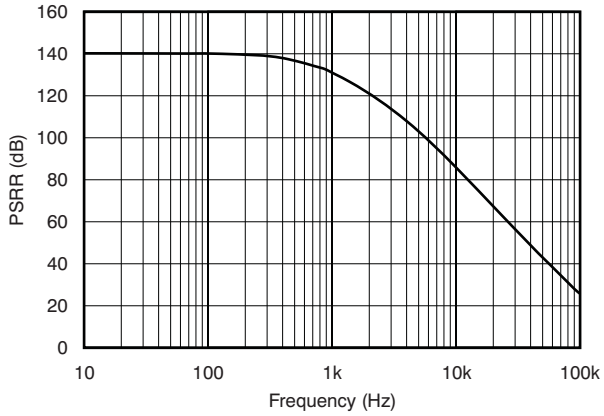


Figure 5.

DROPOUT VOLTAGE vs LOAD CURRENT

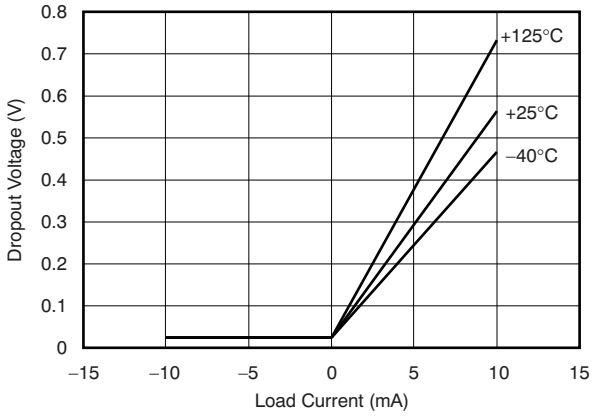


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, I_{LOAD} = 0, and V_S = V_{OUT} + 0.2V, unless otherwise noted. For V_{OUT} ≤ 2.5V, the minimum supply voltage is 2.7V.

REF5025 OUTPUT VOLTAGE vs LOAD CURRENT

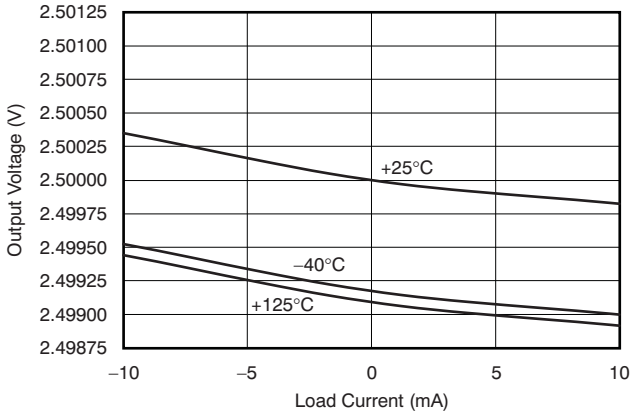


Figure 7.

TEMP PIN OUTPUT VOLTAGE vs TEMPERATURE

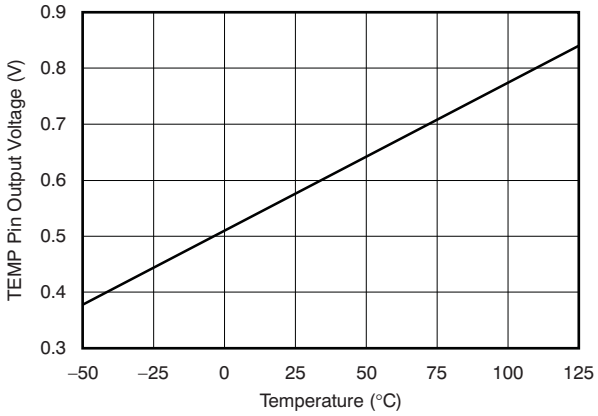


Figure 8.

QUIESCENT CURRENT vs TEMPERATURE

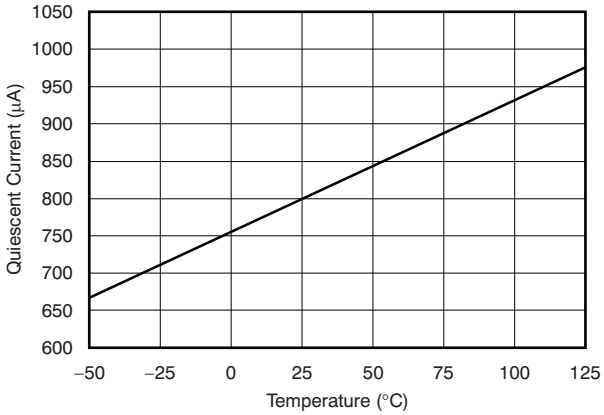


Figure 9.

QUIESCENT CURRENT vs INPUT VOLTAGE

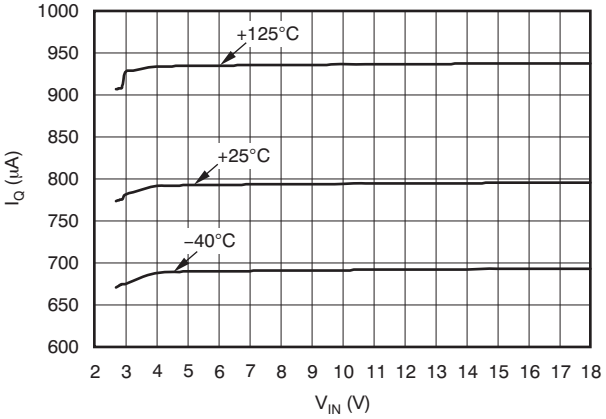


Figure 10.

LINE REGULATION vs TEMPERATURE

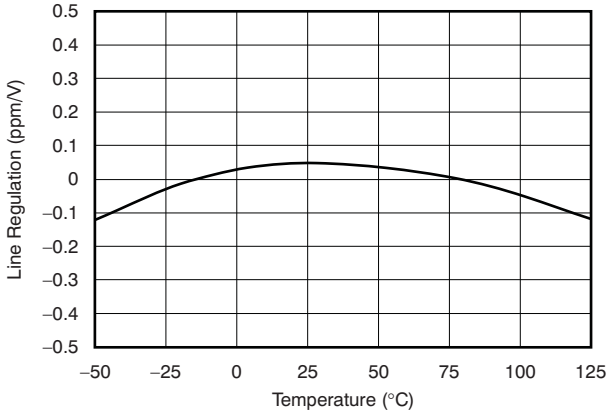


Figure 11.

SHORT-CIRCUIT CURRENT vs TEMPERATURE

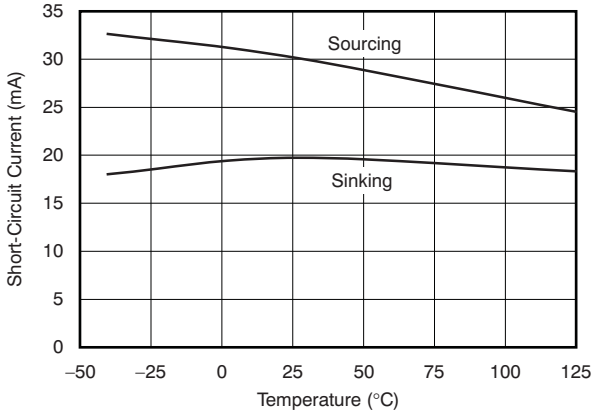


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, I_{LOAD} = 0, and V_S = V_{OUT} + 0.2V, unless otherwise noted. For V_{OUT} ≤ 2.5V, the minimum supply voltage is 2.7V.

NOISE

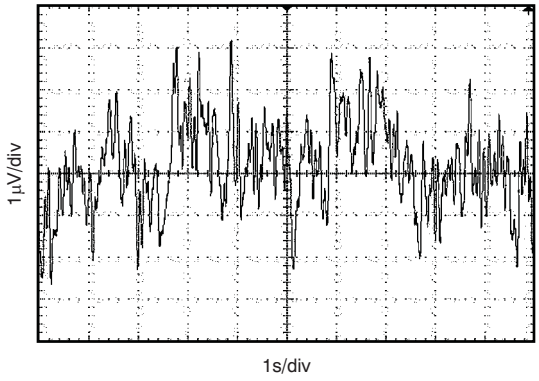


Figure 13.

STARTUP
(REF5025, C_L = 1µF)

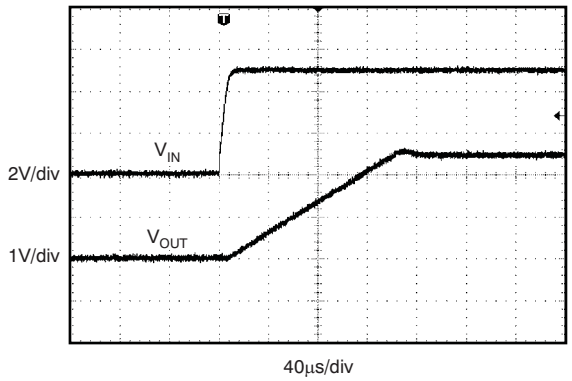


Figure 14.

STARTUP
(REF5025, C_L = 10µF)

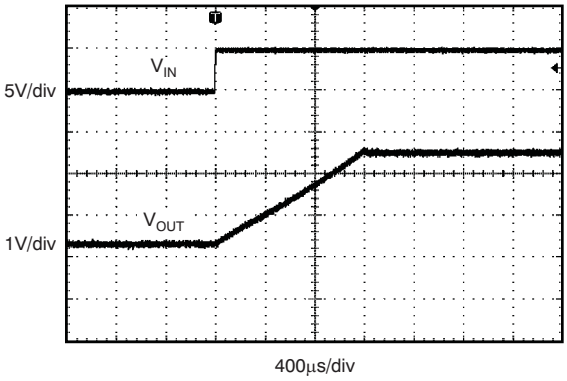


Figure 15.

LOAD TRANSIENT
(C_L = 1µF, I_{OUT} = 1mA)

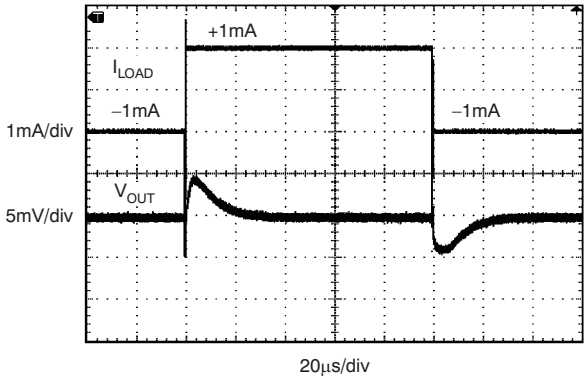


Figure 16.

LOAD TRANSIENT
(C_L = 1µF, I_{OUT} = 10mA)

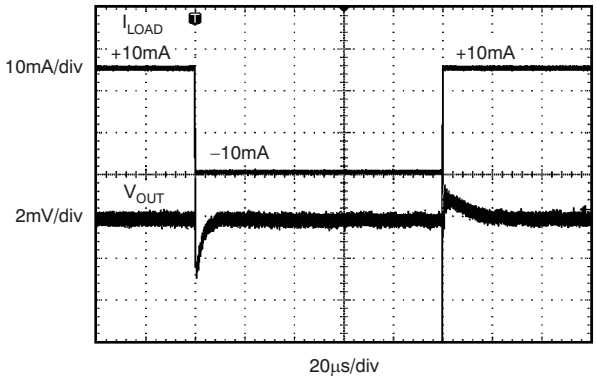


Figure 17.

LOAD TRANSIENT
(C_L = 10µF, I_{OUT} = 1mA)

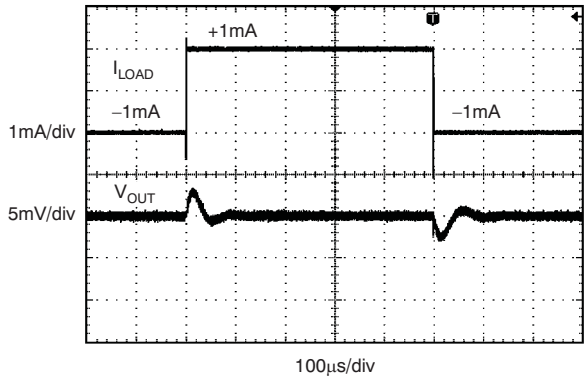


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, I_{LOAD} = 0, and V_S = V_{OUT} + 0.2V, unless otherwise noted. For V_{OUT} ≤ 2.5V, the minimum supply voltage is 2.7V.

LOAD TRANSIENT
(C_L = 10μF, I_{OUT} = 10mA)

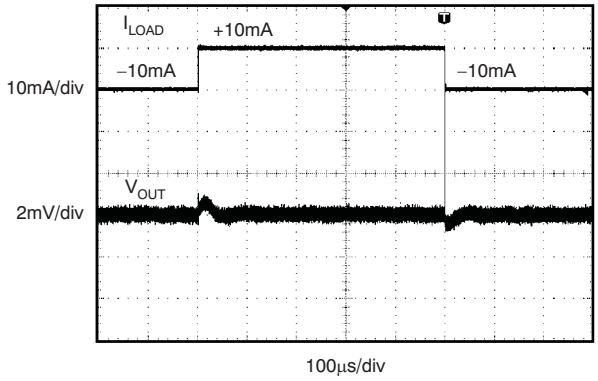


Figure 19.

LINE TRANSIENT
(C_L = 1μF)

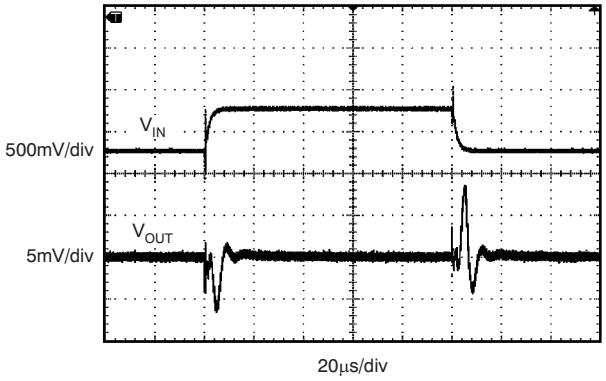


Figure 20.

LINE TRANSIENT
(C_L = 10μF)

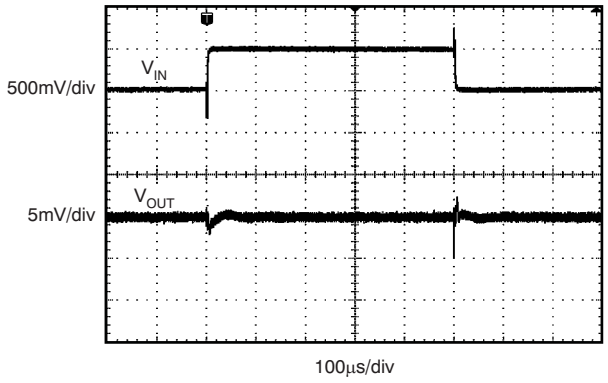


Figure 21.

REF50xx
LONG-TERM STABILITY (FIRST 1000 HOURS)

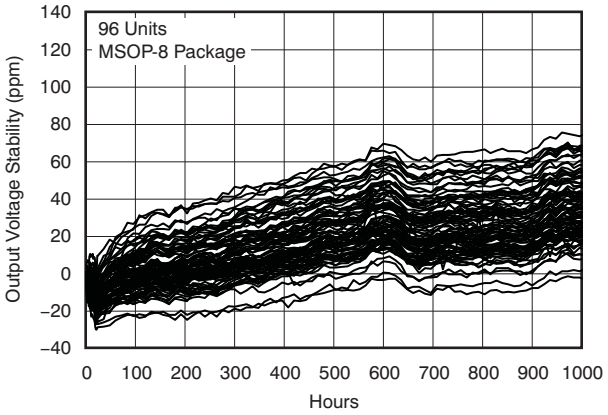


Figure 22.

REF50xx
LONG-TERM STABILITY (SECOND 1000 HOURS)

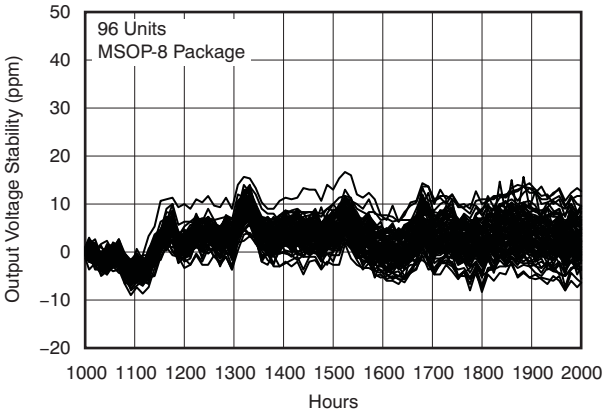


Figure 23.

REF50xx
LONG-TERM STABILITY (2000 HOURS)

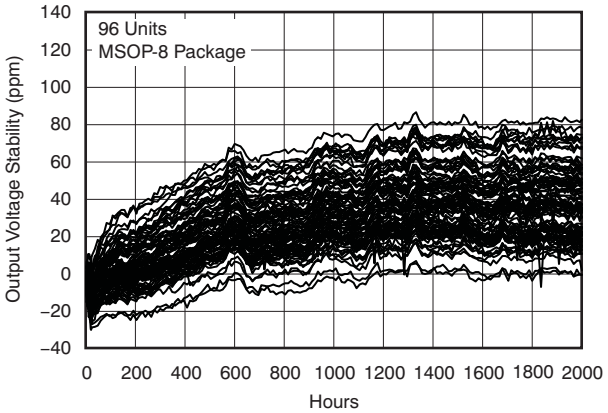


Figure 24.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, I_{LOAD} = 0, and V_S = V_{OUT} + 0.2V, unless otherwise noted. For V_{OUT} ≤ 2.5V, the minimum supply voltage is 2.7V.

REF50xx
LONG-TERM STABILITY (FIRST 1000 HOURS)

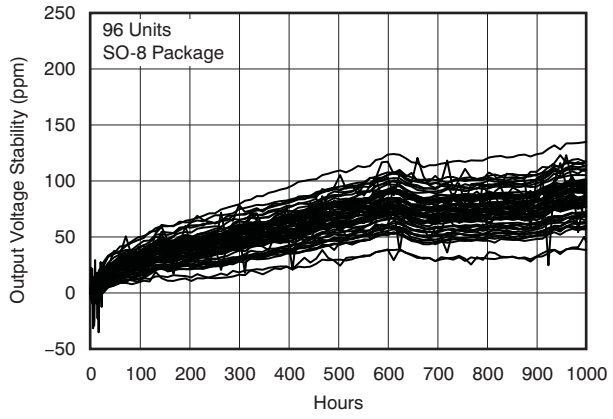


Figure 25.

REF50xx
LONG-TERM STABILITY (SECOND 1000 HOURS)

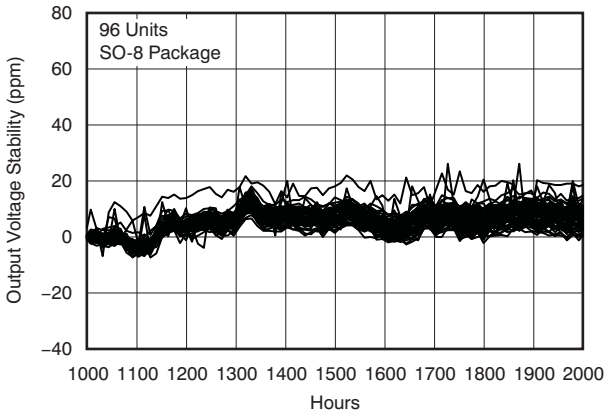


Figure 26.

REF50xx
LONG-TERM STABILITY (2000 HOURS)

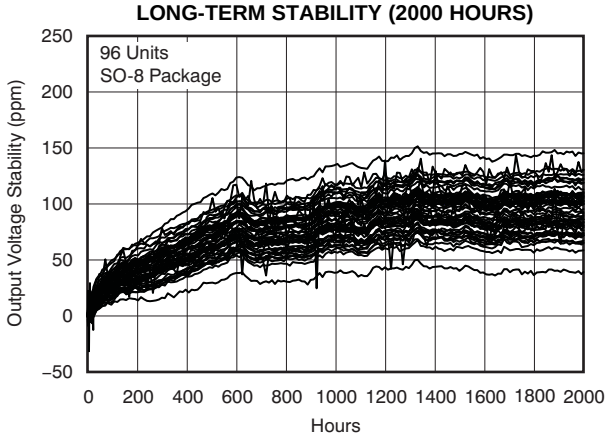


Figure 27.

APPLICATION INFORMATION

The REF50xx is family of low-noise, precision bandgap voltage references that are specifically designed for excellent initial voltage accuracy and drift. Figure 28 shows a simplified block diagram of the REF50xx.

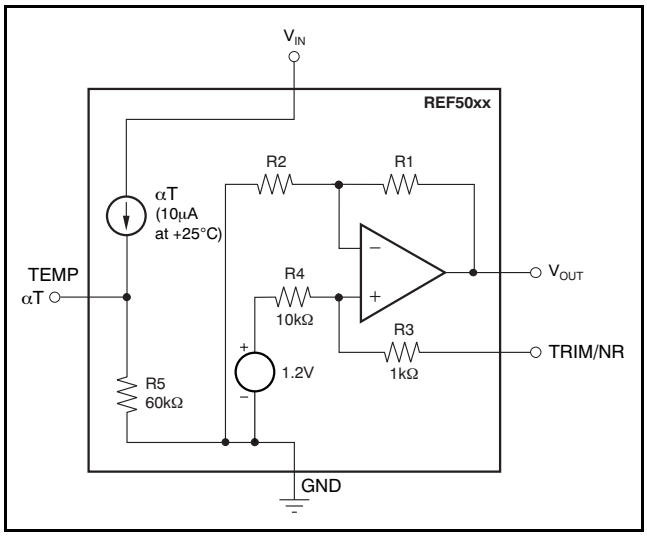


Figure 28. REF50xx Simplified Block Diagram

BASIC CONNECTIONS

Figure 29 shows the typical connections for the REF50xx. A supply bypass capacitor ranging between 1μF to 10μF is recommended. A 1μF to 50μF output capacitor (C_L) must be connected from V_{OUT} to GND. The ESR value of C_L must be less than or equal to 1.5Ω to ensure output stability. To minimize noise, the recommended ESR of C_L is between 1Ω and 1.5Ω.

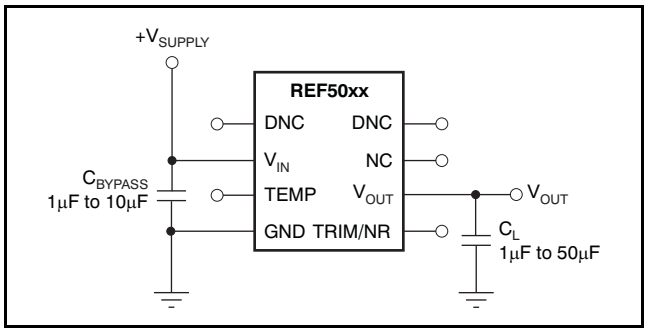


Figure 29. Basic Connections

SUPPLY VOLTAGE

The REF50xx family of voltage references features extremely low dropout voltage. With the exception of the REF5020, which has a minimum supply requirement of 2.7V, these references can be operated with a supply of 200mV above the output voltage in an unloaded condition. For loaded conditions, a typical dropout voltage versus load plot is shown in Figure 6 of the Typical Characteristics.

OUTPUT ADJUSTMENT USING THE TRIM/NR PIN

The REF50xx provides a very accurate, factory-trimmed voltage output. However, V_{OUT} can be adjusted using the trim and noise reduction pin (TRIM/NR, pin 5). Figure 30 shows a typical circuit that allows an output adjustment of ±15mV

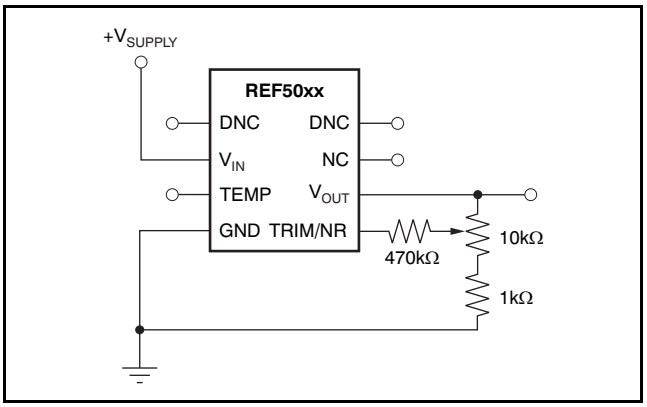


Figure 30. V_{OUT} Adjustment Using the TRIM/NR Pin

The REF50xx allows access to the bandgap through the TRIM/NR pin. Placing a capacitor from the TRIM/NR pin to GND (see Figure 31) in combination with the internal R_3 and R_4 resistors creates a low-pass filter. A capacitance of 1μF creates a low-pass filter with the corner frequency between 10Hz and 20Hz. Such a filter decreases the overall noise measured on the V_{OUT} pin by half. Higher capacitance results in a lower filter cutoff frequency, further reducing output noise. Note that use of this capacitor increases startup time.

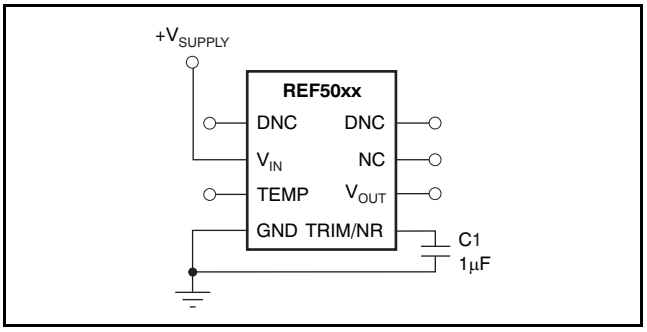


Figure 31. Noise Reduction Using the TRIM/NR Pin

TEMPERATURE DRIFT

The REF50xx is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by the following equation:

$$\text{Drift} = \left(\frac{V_{OUTMAX} - V_{OUTMIN}}{V_{OUT} \times \text{Temp Range}} \right) \times 10^6 (\text{ppm}) \quad (1)$$

The REF50xx features a maximum drift coefficient of 3ppm/°C for the high-grade version, and 8ppm/°C for the standard-grade.

THERMAL HYSTERESIS

Thermal hysteresis for the REF50xx is defined as the change in output voltage after operating the device at +25°C, cycling the device through the specified temperature range, and returning to +25°C. It can be expressed as Equation 2:

$$V_{HYST} = \left(\frac{|V_{PRE} - V_{POST}|}{V_{NOM}} \right) \bullet 10^6 (\text{ppm}) \quad (2)$$

Where:

V_{HYST} = thermal hysteresis (in units of ppm).

V_{NOM} = the specified output voltage.

V_{PRE} = output voltage measured at +25°C pretemperature cycling.

V_{POST} = output voltage measured after the device has been cycled from +25°C through the specified temperature range of –40°C to +125°C and returned to +25°C.

TEMPERATURE MONITORING

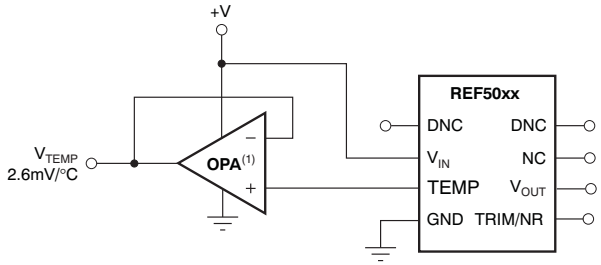
The temperature output terminal (TEMP, pin 3) provides a temperature-dependent voltage output with approximately 60kΩ source impedance. As seen in Figure 8, the output voltage follows the nominal relationship:

$V_{TEMP\ PIN} = 509mV + 2.64 \times T(°C)$

This pin indicates general chip temperature, accurate to approximately ±15°C. Although it is not generally suitable for accurate temperature measurements, it can be used to indicate temperature changes or for temperature compensation of analog circuitry. A temperature change of 30°C corresponds to an approximate 79mV change in voltage at the TEMP pin.

The TEMP pin has high output impedance (see Figure 28). Loading this pin with a low-impedance circuit induces a measurement error; however, it does not have any effect on V_{OUT} accuracy.

To avoid errors caused by low-impedance loading, buffer the TEMP pin output with a suitable low-temperature drift op amp, such as the OPA333, OPA335, or OPA376, as shown in Figure 32.



NOTE: (1) Low drift op amp, such as the OPA333, OPA335, or OPA376.

Figure 32. Buffering the TEMP Pin Output

POWER DISSIPATION

The REF50xx family is specified to deliver current loads of ±10mA over the specified input voltage range. The temperature of the device increases according to the equation:

$$T_J = T_A + P_D \times \theta_{JA} \quad (3)$$

Where:

T_J = Junction temperature (°C)

T_A = Ambient temperature (°C)

P_D = Power dissipated (W)

θ_{JA} = Junction-to-ambient thermal resistance (°C/W)

The REF50xx junction temperature must not exceed the absolute maximum rating of +150°C.

NOISE PERFORMANCE

Typical 0.1Hz to 10Hz voltage noise for each member of the REF50xx family is specified in the *Electrical Characteristics: Per Device* table. The noise voltage increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade performance.

For additional information about how to minimize noise and maximize performance in mixed-signal applications such as data converters, refer to the series of *Analog Applications Journal* articles entitled, *How a Voltage Reference Affects ADC Performance*. This three-part series is available for download from the TI website under three literature numbers: SLYT331, SLYT339, and SLYT355 for Part I, Part II, and Part III, respectively.

APPLICATION CIRCUITS

NEGATIVE REFERENCE VOLTAGE

For applications requiring a negative and positive reference voltage, the REF50xx and OPA735 can be used to provide a dual-supply reference from a 5V supply. Figure 33 shows the REF5025 used to provide a 2.5V supply reference voltage. The low drift performance of the REF50xx complements the low offset voltage and zero drift of the OPA735 to provide an accurate solution for split-supply applications. Care must be taken to match the temperature coefficients of R_1 and R_2.

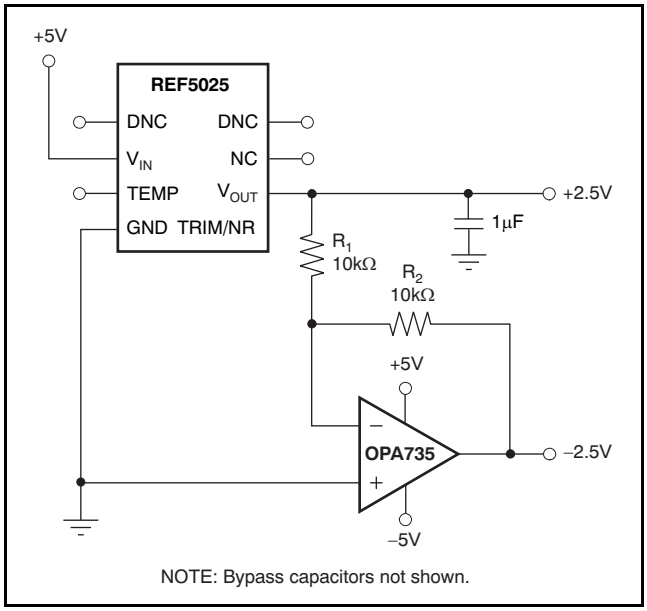


Figure 33. The REF5025 and OPA735 Create Positive and Negative Reference Voltages

DATA ACQUISITION

Data acquisition systems often require stable voltage references to maintain accuracy. The REF50xx family features low noise, very low drift, and high initial accuracy for high-performance data converters. Figure 34 shows the REF5040 in a basic data acquisition system.

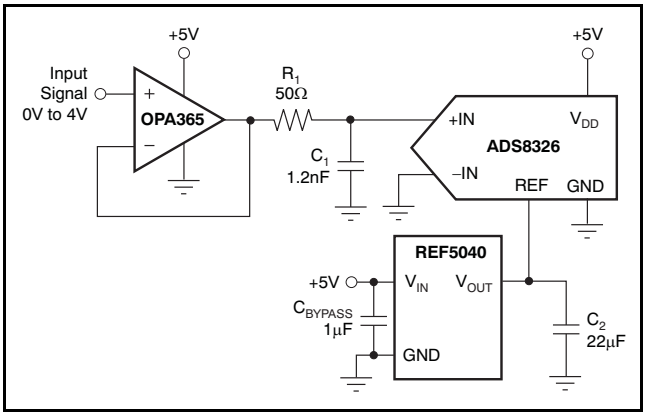


Figure 34. Basic Data Acquisition System

REVISION HISTORY

Changes from Revision D (April, 2009) to Revision E **Page**

- Updated *Features* list; added *Excellent Long-Term Stability* bullet 1
- Added *Thermal Hysteresis* parameters and specifications 4
- Added *Long-Term Stability* parameters and specifications 4
- Added Figure 22 through Figure 24 8
- Added Figure 25 through Figure 27 9
- Added *Thermal Hysteresis* section 11
- Revised *Noise Performance* section; added paragraph with links to applications articles 11

Changes from Revision C (December, 2008) to Revision D **Page**

- Removed all notes regarding MSOP-8 package status. MSOP-8 package released at time of document revision 1
- Changed *Storage Temperature Range* absolute minimum value from –55°C to –65°C 2
- Added test condition to *Line Regulation, All other devices* specification 4
- Added *Load Regulation* test condition and *Over Temperature* specifications 4
- Added typical characteristic graph, *Quiescent Current vs Input Voltage* (Figure 10) 6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF5010AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5010 A	Samples
REF5010AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50G	Samples
REF5010AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50G	Samples
REF5010AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5010 A	Samples
REF5010ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5010	Samples
REF5010IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50G	Samples
REF5010IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50G	Samples
REF5020AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020 A	Samples
REF5020AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020 A	Samples
REF5020AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50A	Samples
REF5020AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50A	Samples
REF5020AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020 A	Samples
REF5020AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020 A	Samples
REF5020ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF5020IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50A	Samples
REF5020IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50A	Samples
REF5020IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020	Samples
REF5020IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020	Samples
REF5025AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025 A	Samples
REF5025AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025 A	Samples
REF5025AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50B	Samples
REF5025AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50B	Samples
REF5025AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025 A	Samples
REF5025AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025 A	Samples
REF5025ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025	Samples
REF5025IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025	Samples
REF5025IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50B	Samples
REF5025IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50B	Samples
REF5025IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025	Samples
REF5025IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF5030AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030 A	Samples
REF5030AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030 A	Samples
REF5030AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50C	Samples
REF5030AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50C	Samples
REF5030AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030 A	Samples
REF5030ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030	Samples
REF5030IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50C	Samples
REF5030IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50C	Samples
REF5030IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030	Samples
REF5040AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040 A	Samples
REF5040AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040 A	Samples
REF5040AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50D	Samples
REF5040AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50D	Samples
REF5040AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040 A	Samples
REF5040ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF5040IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040	Samples
REF5040IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50D	Samples
REF5040IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50D	Samples
REF5040IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040	Samples
REF5040IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040	Samples
REF5045AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5045 A	Samples
REF5045AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5045 A	Samples
REF5045AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50E	Samples
REF5045AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50E	Samples
REF5045AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5045 A	Samples
REF5045ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5045	Samples
REF5045IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50E	Samples
REF5045IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50E	Samples
REF5045IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5045	Samples
REF5050AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050 A	Samples
REF5050AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050 A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF5050AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50F	Samples
REF5050AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50F	Samples
REF5050AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050 A	Samples
REF5050ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050	Samples
REF5050IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050	Samples
REF5050IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50F	Samples
REF5050IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50F	Samples
REF5050IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050	Samples
REF5050IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF REF5020, REF5025, REF5040, REF5050 :

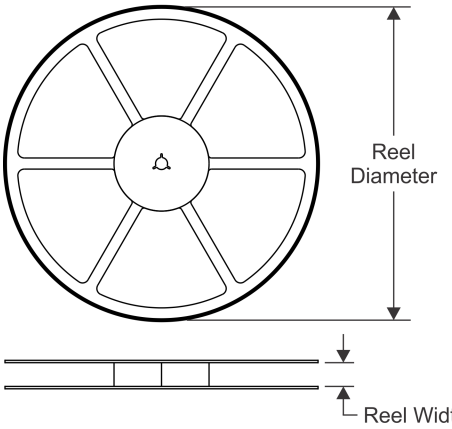
- Enhanced Product: REF5020-EP, REF5025-EP, REF5040-EP, REF5050-EP

NOTE: Qualified Version Definitions:

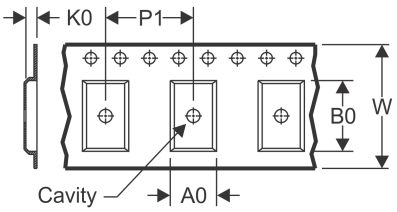
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

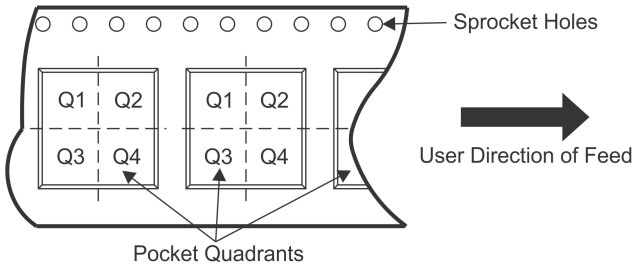


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

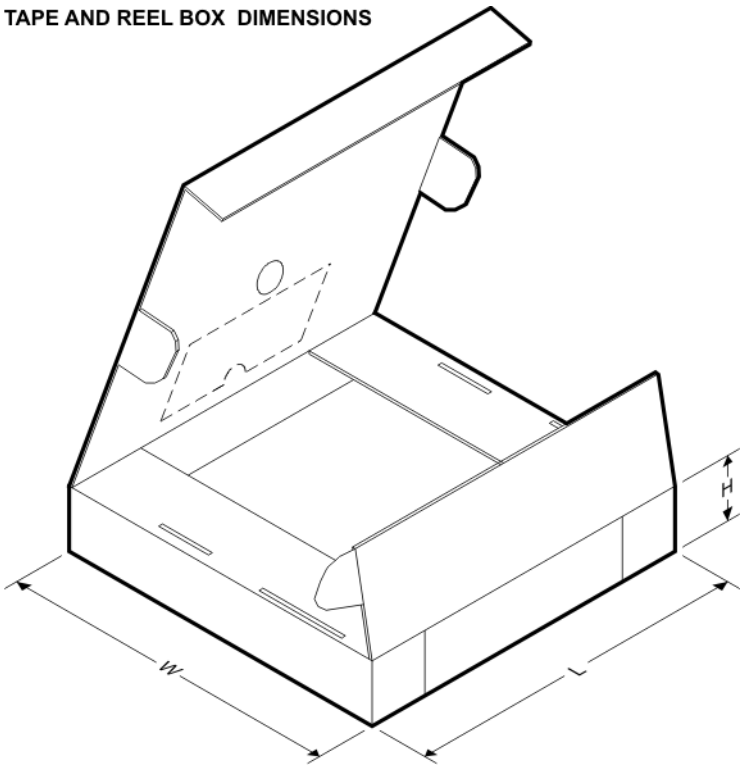


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF5010AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5010AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5010AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5010IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5010IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5020IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5025AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5025AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5025AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5025IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5025IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5025IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5030AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF5030AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5030AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5030IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5030IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5030IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5040AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5040AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5040AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5040IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5040IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5040IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5045AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5045AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5045AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5045IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5045IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5045IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5050AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5050AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5050AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5050IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5050IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5050IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

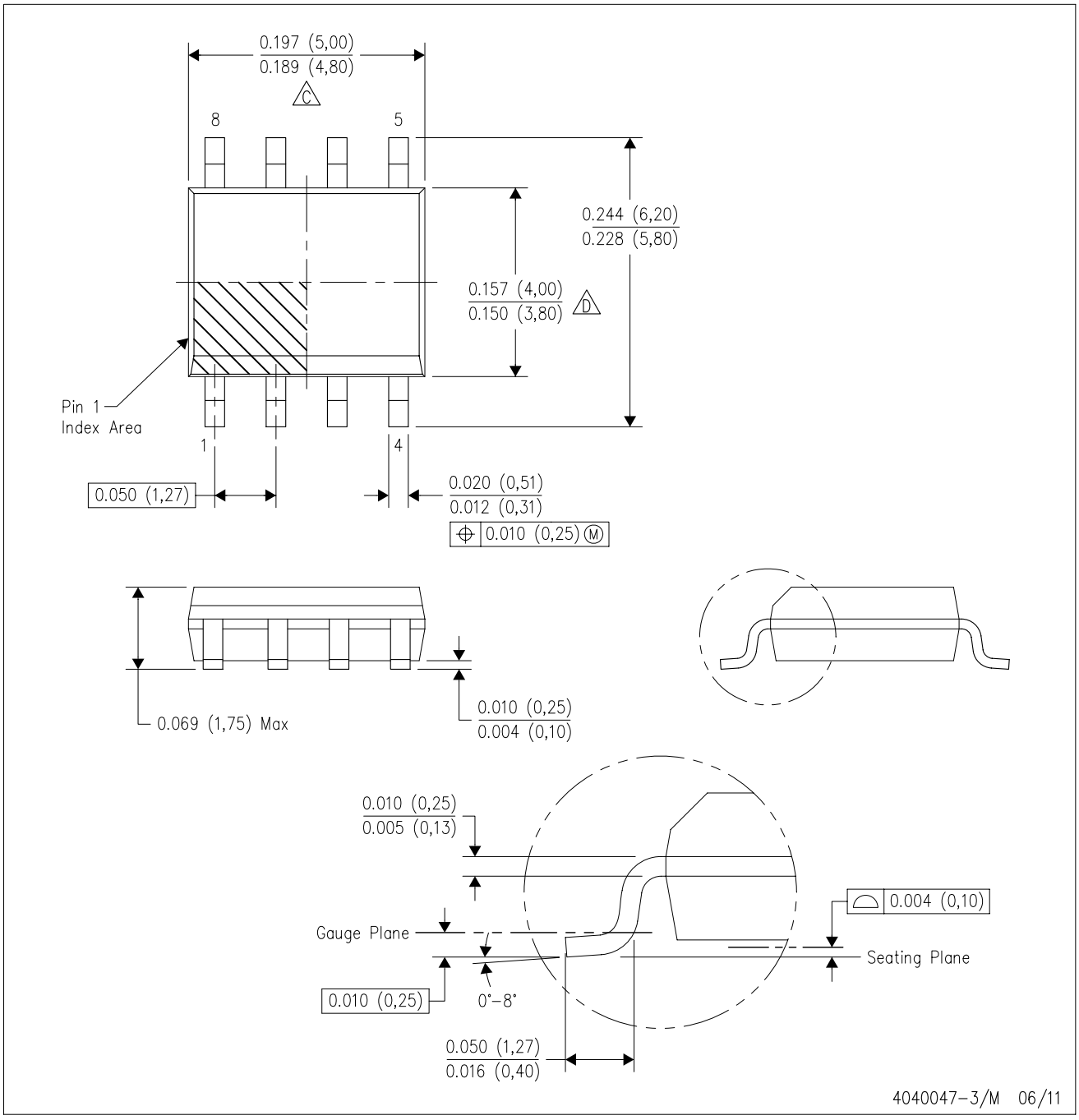


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF5010AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5010AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5010AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5010IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5010IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5020AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5020AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5020AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5020IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5020IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5020IDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5025AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5025AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5025AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5025IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5025IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5025IDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5030AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5030AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5030AIDR	SOIC	D	8	2500	367.0	367.0	35.0

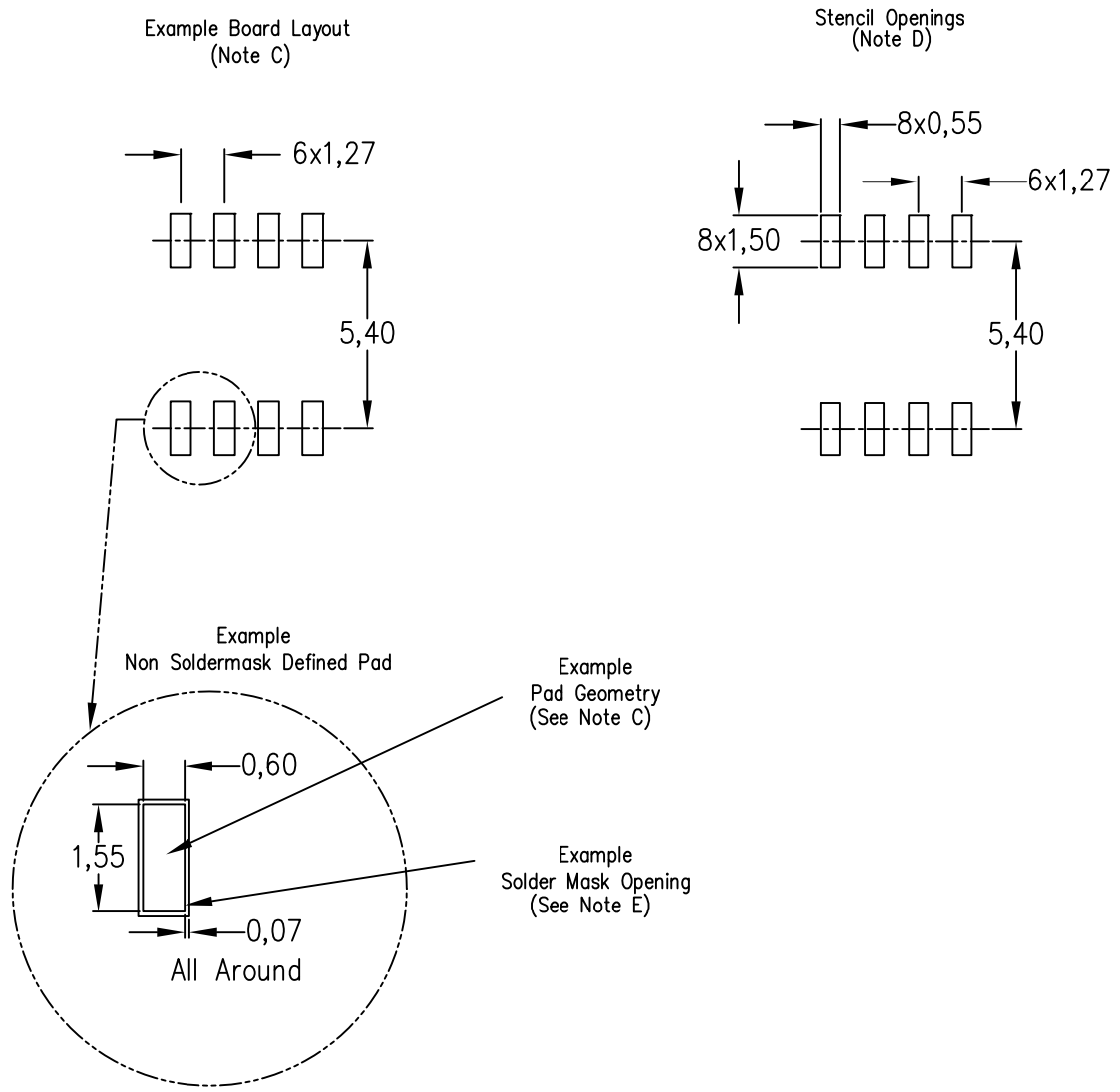
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF5030IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5030IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5030IDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5040AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5040AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5040AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5040IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5040IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5040IDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5045AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5045AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5045AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5045IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5045IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5045IDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5050AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5050AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5050AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5050IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5050IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5050IDR	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



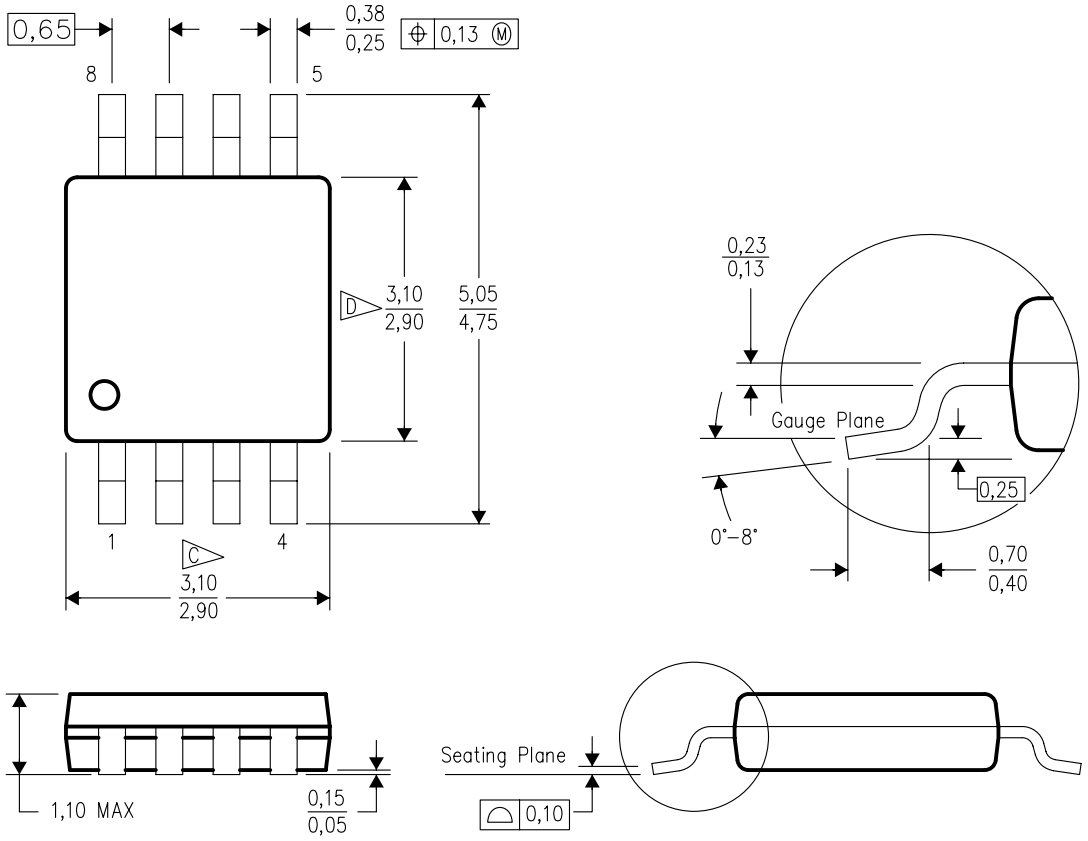
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

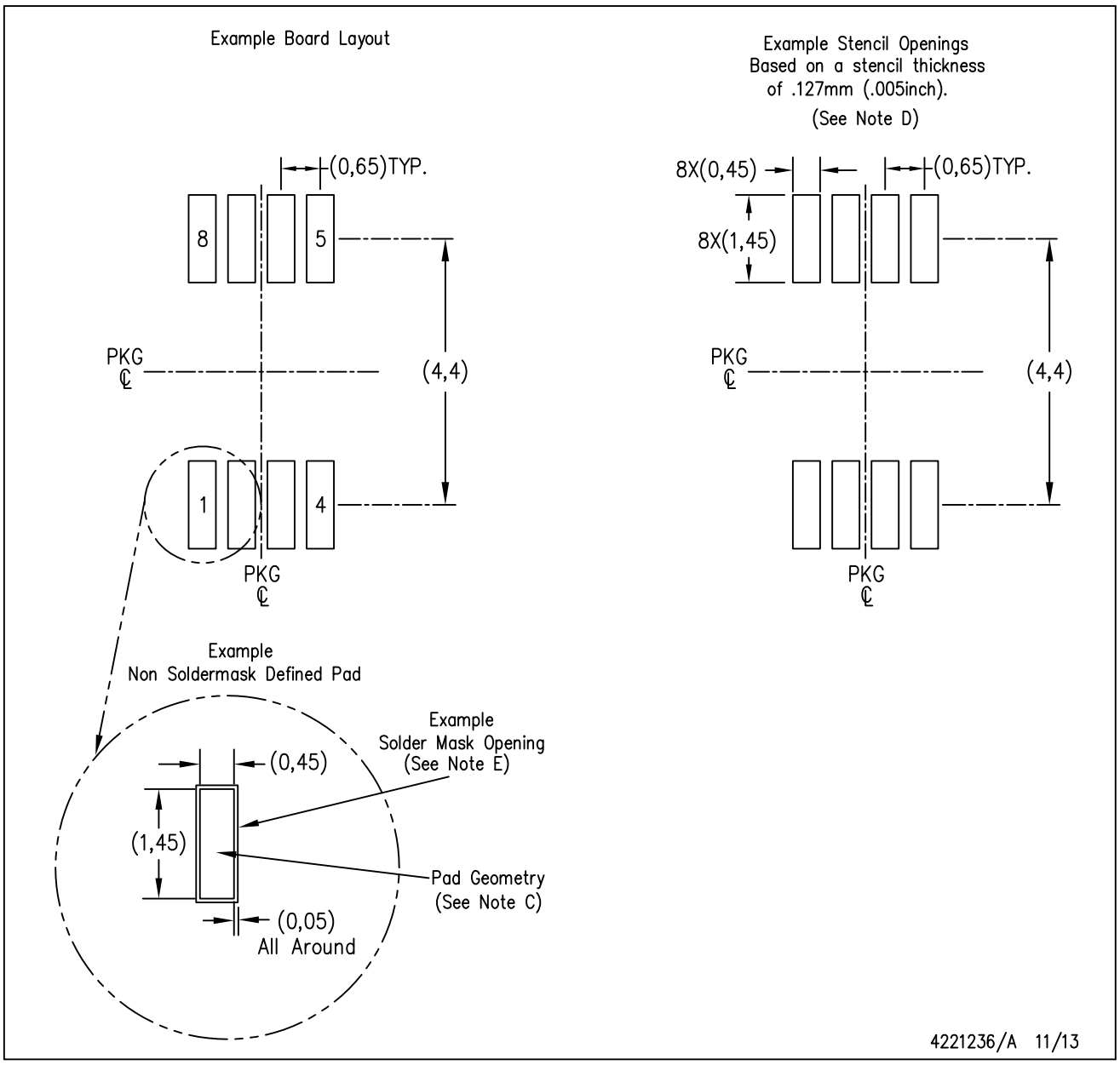
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265