Digital System Design and Lab: HW3

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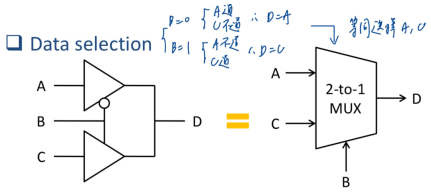
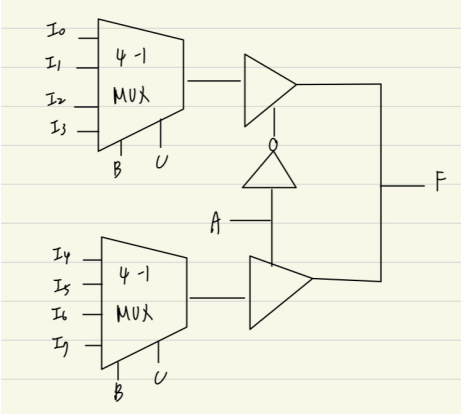
1

By lecture slide LEC-09 p.10-11, we knew that using two three-state buffers with one inverter could do data selection, and is equivalent to a 2-to-1 MUX:

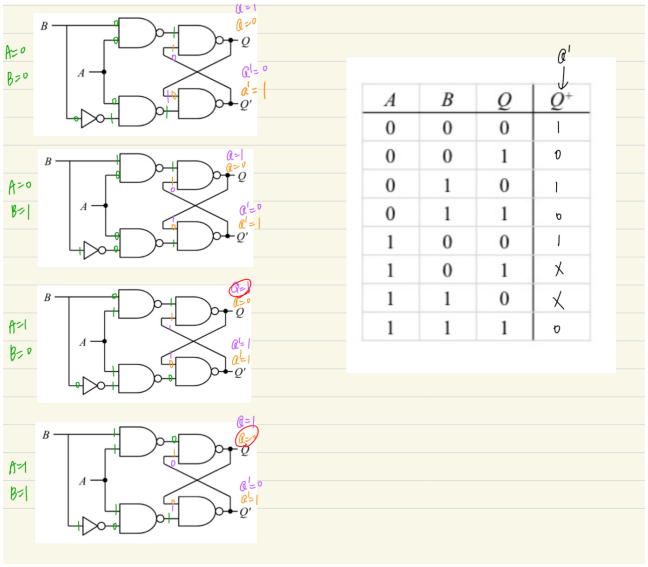


So, we can use the two 4-to-1 MUXs and this setting to implement the 8-to-1 MUX as follows:



2

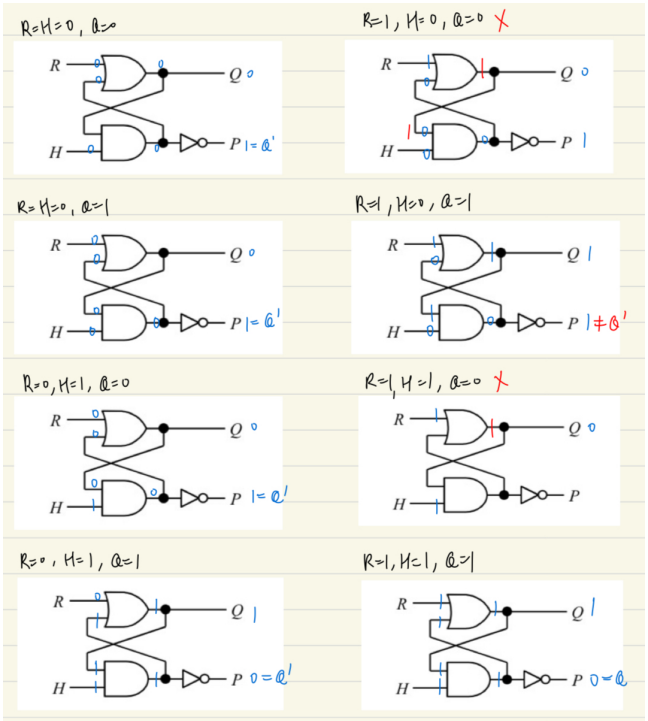
The derivation process and the resulting truth table are shown below:



A	B	Q	Q^+
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	X
1	1	0	X
1	1	1	0

3

The following is the different cases of the latch:



(1)

From the above cases, we can see that when $R = 1$ and $H = 0$, $P = 1 \neq Q' = 0$. Therefore, we should not let:

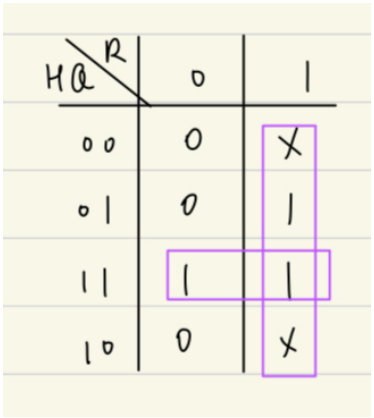
$$R = 1 \quad \text{and} \quad H = 0$$

(2)

The next-state table is shown below:

R	H	Q	Q+
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	X
1	0	1	1
1	1	0	X
1	1	1	1

And we can construct the K-map as follows:



Which would give us the characteristic equation:

$$Q^+ = R + H \cdot Q$$