实验报告

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专业	网络工程		课程名称	《计算机组成原理课程设计》	
任课老师	吴国华	指导老师	吴国华	机位号	
实验序号	5	实验名称	实验 5 存储器设计		
实验时间		实验地点	1-225	实验设备号	

一、实验设计与程序

1、 实验程序源代码及注释等

使用逻辑代码的 memory.v 模块

```
module memory(CLK,Reset,Mem_Addr,M_W_Data,Mem_Read,Mem_Write,M_R_Data );
	input [5:0] Mem_Addr;
	input CLK,Reset;
	input Mem_Write,Mem_Read;

	input [31:0]M_W_Data;
	output reg[31:0]M_R_Data;
	reg [7:0]REG_Files[0:31];


	//初始化存储器
	integer i;
	initial
	begin
		for (i = 0; i < 32; i = i + 1)
		REG_Files[i] = 0;
	end

	always@(posedge CLK or posedge Reset)

	begin
	  if (Reset)
		begin
		  for (i = 0; i < 32; i = i + 1)
		  REG_Files[i] <= 0;
		end
	  else if (Mem_Write)
```

```
            begin
                        REG_Files[Mem_Addr]<=M_W_Data[7:0];
                        REG_Files[Mem_Addr+1]<=M_W_Data[15:8];
                        REG_Files[Mem_Addr+2]<=M_W_Data[23:16];
                        REG_Files[Mem_Addr+3]<=M_W_Data[31:24];
            end
            else if(Mem_Read)
            begin
                        M_R_Data[7:0]<=REG_Files[Mem_Addr];
                        M_R_Data[15:8]<=REG_Files[Mem_Addr+1];
                        M_R_Data[23:16]<=REG_Files[Mem_Addr+2];
                        M_R_Data[31:24]<=REG_Files[Mem_Addr+3];
            end

            else
                        M_R_Data<=0;

        end
endmodule
```

顶层 top.v 模块

```
`timescale 1ns / 1ps

module top(
        input Mem_Read,             //读控制信号
        input Mem_Write,            //写控制信号
        input[7:2]Mem_Addr, //寄存器访问地址
        input[1:0]MUX,          //2 位输入选择器
        input Clk,
        input Reset,
        output reg[7:0]LED                      //LED 输出显示
);


        wire[31:0]M_R_Data; //存储器读出数据
        reg[31:0]M_W_Data;  //存储器写入数据

        RAM_B my_RAM(
                .clka(Clk), // input clka
                .wea(Mem_Write), // input [0 : 0] wea
                .addra(Mem_Addr), // input [5 : 0] addra
                .dina(M_W_Data), // input [31 : 0] dina
                .douta(M_R_Data) // output [31 : 0] douta
```

```
    );

    always @ (*)
    begin
        if(Reset)
        begin
        LED = 0;
        M_W_Data = 0;
        end
        else if (Mem_Read)
        begin       //读操作
            case(MUX)
                2'b00:      LED = M_R_Data[7:0];
                2'b01:      LED = M_R_Data[15:8];
                2'b10:      LED = M_R_Data[23:16];
                2'b11:      LED = M_R_Data[31:24];
                default:LED = 0;
            endcase
        end
        else if (Mem_Write)
        begin
            LED=0;
            case(MUX)
                2'b00:begin      M_W_Data = 32'h0000_000F;    end
                2'b01:begin      M_W_Data = 32'h0000_0DB0;    end
                2'b10:begin      M_W_Data = 32'h003C_C381;    end
                2'b11:beginM_W_Data = 32'hFFFF_FFFF;   end
                default:M_W_Data = 0;
            endcase
        end
    end

endmodule
```

底层 RAM_B 模块

```
RAM_B your_instance_name (
  .clka(clka), // input clka
  .wea(wea), // input [0 : 0] wea
  .addra(addra), // input [5 : 0] addra
  .dina(dina), // input [31 : 0] dina
  .douta(douta) // output [31 : 0] douta
);
```

二、实验仿真

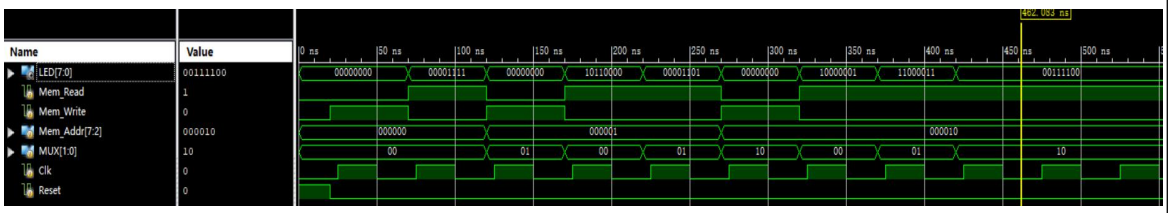
1、 仿真代码

```
`timescale 1ns / 1ps

module top_1;

	// Inputs
	reg Mem_Read;
	reg Mem_Write;
	reg [7:2] Mem_Addr;
	reg [1:0] MUX;
	reg Clk;
	reg Reset;

	// Outputs
	wire [7:0] LED;

	// Instantiate the Unit Under Test (UUT)
	top uut (
		.Mem_Read(Mem_Read),
		.Mem_Write(Mem_Write),
		.Mem_Addr(Mem_Addr),
		.MUX(MUX),
		.Clk(Clk),
		.Reset(Reset),
		.LED(LED)
	);
	initial Clk=0;
	always #25 Clk=~Clk;
	initial begin
		// Initialize Inputs
		Mem_Read = 0;
		Mem_Write = 0;
		Mem_Addr = 0;
		MUX = 0;
		Reset = 1;

		// Wait 100 ns for global reset to finish

	 #20;
		// Add stimulus here
		Mem_Read = 0;
		Mem_Write = 1;
		Mem_Addr = 0;
		MUX = 0;
```

```
Reset = 0;
#50;

Mem_Read = 1;
Mem_Write = 0;
Mem_Addr = 0;
MUX = 0;//00001111
#50;

Mem_Read = 0;
Mem_Write = 1;
Mem_Addr = 1;
MUX = 1;//
#50;

Mem_Read = 1;
Mem_Write = 0;
Mem_Addr = 1;
MUX = 0;//10110000
#50;

Mem_Read = 1;
Mem_Write = 0;
Mem_Addr = 1;
MUX = 1;//00001101
#50;

Mem_Read = 0;
Mem_Write = 1;
Mem_Addr = 2;
MUX = 2;//
#50;
Mem_Read = 1;
Mem_Write = 0;
Mem_Addr = 2;
MUX = 0;//1000_0001
#50;
Mem_Read = 1;
Mem_Write = 0;
Mem_Addr = 2;
MUX = 1;//1100_0011
#50;
Mem_Read = 1;
Mem_Write = 0;
```

```
        Mem_Addr = 2;
        MUX = 2;//0011_1100
        #50;
    end

endmodule
```

2、 仿真波形



3、 仿真结果分析

实验结果结果与真值表相同，仿真正确。

三、电路图