SOUTH EASTERN UNIVERSITY OF SRI LANKA

FIRST EXAMINATION IN BACHELOR OF INFORMATION AND COMMUNICATION TECHNOLOGY – 2021/2022

SEMESTER – I, APRIL/MAY 2024

CIS11032 – Logic Designing and Computer Organization

Index Number: _____ **Time Allowed:** 02 hours

Instructions:

- *Answer all questions.*
- *There are two parts in this question paper, Part A and Part B.*
- *Use the MCQ answer sheet provided to answer Part A.*

PART A

For each of the following questions, choose the best answer from the given options. Select only one answer per question.

01. Which logic gate produces **an output of 1 only** when all inputs are **0**?
    a) AND
    b) OR
    c) NOR
    d) NAND

02. The **binary** equivalent of the decimal **25.625** is:
    a) 111001.001_2
    b) 11001.011_2
    c) 11001.101_2
    d) 111001.101_2

03. The representation of hexadecimal $\mathbf{1AC_{16}}$ in **octal** is:
    a) 134_8
    b) 310_8
    c) 654_8
    d) 645_8

04. What is the **BCD** representation of the **decimal** number **25**?
    a) 0001 0101
    b) 0010 0101
    c) 0001 1001
    d) 0001 1010

05. What is the **Gray Code** equivalent for **decimal** number 7?
   a) 0111
   b) 0100
   c) 0101
   d) 1110

06. What is the **binary** representation of the **decimal** number **3.625**?
   a) 11.011
   b) 11.101
   c) 110.111
   d) 10.101

07. What is the result of the binary addition **1011 + 0101**?
   a) 10001
   b) 01110
   c) 10000
   d) 11010

08. What is the result of the binary subtraction **10101 - 1110**?
   a) 110
   b) 111
   c) 1101
   d) 1010

09. What is the result of the BCD addition $\mathbf{1001_{BCD} + 0110_{BCD}}$?
   a) $0000\ 1111_{BCD}$
   b) $0001\ 0011_{BCD}$
   c) $0001\ 1010_{BCD}$
   d) $0001\ 0101_{BCD}$

10. What is the complement of the expression **(AB' + C'D')**?
   a) (A' + B') + (C+D)
   b) A'B+CD
   c) (A'+B) . (C+D)
   d) (A'+B') . (C'+D')

11. Simplified expression for the Boolean expression **AB+ ABC+ ABC** is:
   a) ABC
   b) AB+ABC
   c) AB
   d) A

12. What is the primary function of the **Memory Buffer Register (MBR)**?
   a) Stores the address of the next instruction to be executed
   b) Holds the contents of the instruction currently being executed
   c) Temporarily stores data read from or written to the main memory
   d) Performs arithmetic and logical operations on data

13. Which component is responsible for interpreting and executing instructions in **Von Neumann architecture**?
    a) Arithmetic and Logic Unit (ALU)
    b) Control Unit
    c) Random Access Memory (RAM)
    d) Cache Memory

14. Which component of the CPU **temporarily holds data and instructions** during processing?
    a) ALU (Arithmetic Logic Unit)
    b) Control Unit
    c) Cache Memory
    d) Register

15. During which state of the instruction cycle does the CPU analyze the instruction to **determine the type of operation to be performed and operands to be used**?
    a) Instruction Operation Decoding
    b) Instruction Fetch
    c) Operand Fetch
    d) Instruction Address Calculation

16. What class do interrupts generated by **arithmetic overflow** fall into?
    a) Timer
    b) Input/Output
    c) Program
    d) Hardware

17. What is the purpose of the **address bus** in the system bus architecture?
    a) To transfer data between the CPU and memory
    b) To carry memory addresses for read and write operations
    c) To control the flow of data within the CPU
    d) To provide power to peripheral devices

18. In a 32-bit architecture, how many **bytes** are in a **word**?
    a) 2
    b) 4
    c) 8
    d) 16

19. Which access method requires **traversal through each record** until the desired data is found?
    a) Direct Access
    b) Random Access
    c) Indexed Access
    d) Sequential Access

20. How is data retrieved in an **associative access**?
    a) By specifying its memory address
    b) By searching for its content
    c) By using an index
    d) By following a predetermined sequence

21. Which type of memory is **non-volatile** and used to store the firmware of a computer?
    a) ROM
    b) RAM
    c) Cache Memory
    d) Secondary Storage

22. Which of the following best describes the purpose of **memory hierarchy** in computer systems?
    a) To ensure data consistency
    b) To provide storage for large programs
    c) To optimize memory access speed and cost
    d) To manage virtual memory

23. Which cache replacement algorithm prioritizes the retention of blocks that have been accessed **most recently**, regardless of their frequency of access?
    a) Least Frequently Used (LFU)
    b) First In First Out (FIFO)
    c) Least Recently Used (LRU)
    d) Most Recently Used (MRU)

24. Which architecture type tends to have a smaller and simpler instruction set, favoring **pipelining and parallelism** for performance?
    a) RISC (Reduced Instruction Set Computing)
    b) CISC (Complex Instruction Set Computing)
    c) SIMD (Single Instruction, Multiple Data)
    d) MIMD (Multiple Instruction, Multiple Data)

25. What is the primary difference between **dedicated and multiplexed** bus designs in computer architecture?
    a) Dedicated bus designs are slower than multiplexed bus designs.
    b) Dedicated bus designs use separate buses for each type of data transfer, while multiplexed bus designs share a single bus for multiple types of data transfer.
    c) Multiplexed bus designs are more complex than dedicated bus designs.
    d) Dedicated bus designs are used exclusively in parallel processing systems, while multiplexed bus designs are used in serial processing systems.

[25 Marks]

PART B

Question 01

a. Express **-116.125** in **32-bit Single Precision IEEE 754 binary** format.

(05 Marks)

b. Imagine you have a security system for a door that requires at least two out of three conditions to be met before allowing access. Conditions **A, B, and C** represent different access methods. The system allows access if **at least two** out of the three conditions are met. Indicate the **output Y** as **1** when access is **granted** and **0** when the access is **denied.**

I. Create a **truth table** for the above security system.

(05 Marks)

II. Derive the **Boolean expression** from the truth table in **SOP** form.

(05 Marks)

III. Simplify the Boolean expression obtained using **Boolean Algebraic Laws.**

(05 Marks)

IV. Draw a logic circuit for the **simplified** Boolean expression.

(05 Marks)

[25 Marks]

Question 02

a. Show that,

I. $XZ + \overline{X}\overline{Y} + \overline{Y}\overline{Z} = XZ + \overline{Y}$

II. $(A\overline{B}(C + BD) + \overline{A}\overline{B})C = \overline{B}C$

(10 Marks)

b. Simplify the following expressions using K-map

I. $F(A, B, C, D) = \Sigma(0,1,2,4,5,8,9,10,11)$

II. $F(A, B, C, D) = \Sigma(0,3,4,5,7,9,11,12,13,14) + \Sigma d(1,15)$

(10 Marks)

c. Illustrate the **instruction cycle with interrupt** including all important states using a **state diagram.**

(05 Marks)

[25 Marks]

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Question 03

a. Briefly explain **Belady's Anomaly** in cache replacement.

(04 Marks)

b. Imagine a cache with a capacity of **03** frames, and the following cache entries occur:
5, 0, 1, 2, 0, 3, 1, 2, 5, 2, 5, 3

I. Apply **First-In First-Out (FIFO)** cache replacement algorithm on the above cache entries considering that the frames are initially empty.

(07 Marks)

II. Apply **Least Frequently Used** (LFU) algorithm on the same cache entries.

(07 Marks)

III. Evaluate the best replacement algorithm from the above two in terms of **Hit Ratio**.

(07 Marks)

[25 Marks]

[Total 100 Marks]

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