# CIS11032 Logic Designing & Computer Organization

**Lesson 06 Bus Structures**

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# Lesson Learning Outcomes

At the completion of this lesson students should be able to,

- Understand the role and functionalities of System bus
- Identify the elements of bus design

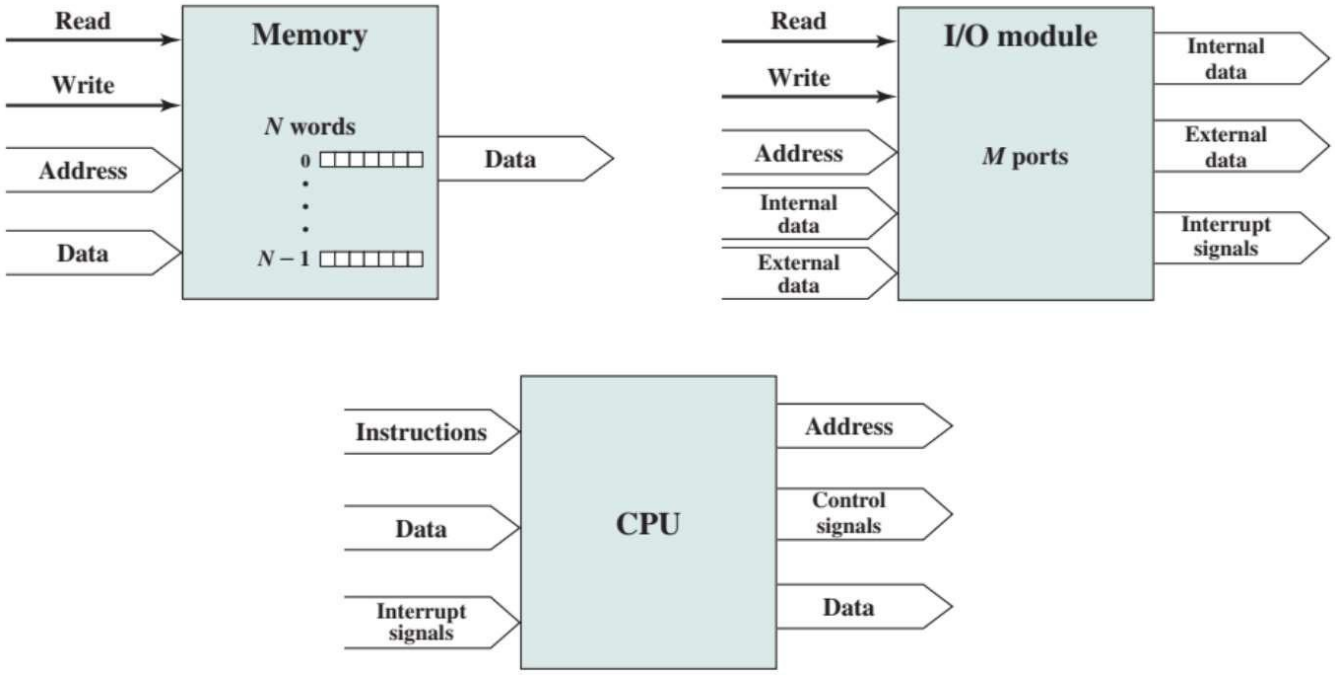
# COURSE OUTLINE

- Interconnection Structures
- Types of Transfer
- Bus Structures
  - System Bus
    - I. Data Lines
    - II. Address Lines
    - III. Control Lines
  - Bus Operation
- Multiple Bus
- Elements of Bus Design

# Interconnection Structures

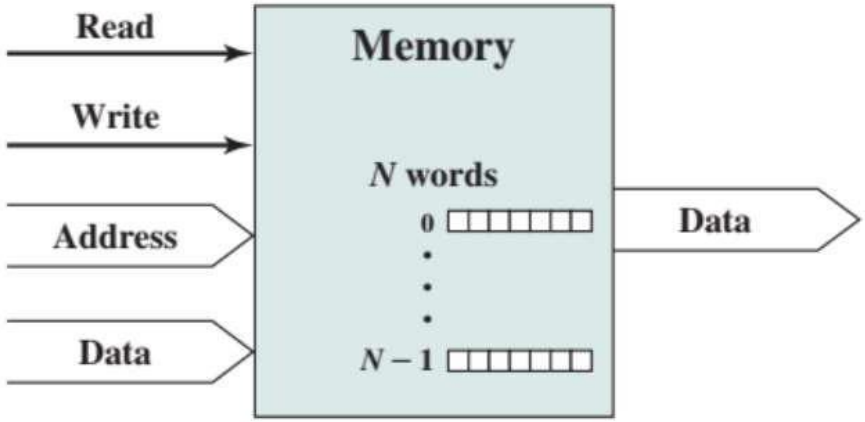
- A computer consists of a set of components or modules of three basic types (processor, memory, I/O) that communicate with each other.
- Thus, a path is essential for connecting the modules.
- The collection of such paths connecting the various modules is known as **Interconnection Structure**
- Therefore, the **interconnection structure** in a CPU (Central Processing Unit) refers to how different internal components (like ALU, registers, control unit, caches, etc.) and external components (memory, I/O devices) are connected and communicate with each other.

# Interconnection Structures Contd.



# Memory

- A memory module consists of N words of equal length where each word is assigned with a  unique numerical address.
- Data can either be read from or written to memory.



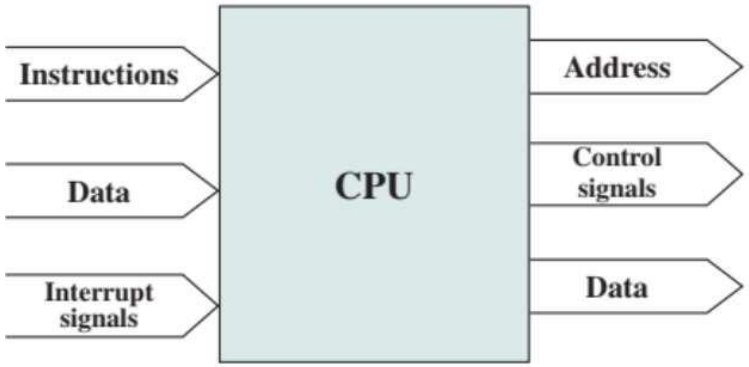
# I/O Module

- For a computer system, I/O is functionally similar to Memory
- Basically, there are 02 operations: **Read & Write**
- As I/O Module can control more than one device, a unique address is given to each of the interfaces of external device (a.k.a Ports)
- I/O Module also has data paths for data input, data output and interrupt signals (*sometimes*)

# The Processor

The processor,

- Reads in instructions and data
- Writes out data after processing,
- Uses control signals to control the overall operation of the system.
- Receives interrupt signals



# Transfer Types

In CPU interconnection, transfer types describe the kinds of data or control information moving across the internal paths.

These transfer types determine what is being sent and how it is being sent.

The Interconnection structure must be able to support the following transfers:

1. **Memory to processor**: The processor reads an instruction or a unit of data from memory.
2. **Processor to memory:** The processor writes a unit of data to memory.
3. **I/O to processor**: The processor reads data from an I/O device via an I/O module.
4. **Processor to I/O**: The processor sends data to the I/O device.
5. **I/O to or from memory**: For these two cases, an I/O module is allowed to exchange data directly with memory, without going through the processor, using direct memory access.

# Transfer Types

Based on this, the transfer types are classified as follows:

| Transfer Type | Source | Destination | Example |
|---|---|---|---|
| Memory Transfer | CPU | Main Memory | Load/store instruction |
| I/O Transfer | CPU | I/O Device | Read from disk |
| Instruction Transfer | Main Memory | CPU | Fetch next instruction |
| Interrupt Transfer | Device/CPU | CPU | Handle keyboard interrupt |
| Control Transfer | CPU Components | CPU Components | Start, stop, reset operations |
| Internal Data Transfer | Register File, ALU | Cache, Memory | Result storage |
| Cache Transfer | Cache Levels | Memory or Cache | Cache miss or update |

# Bus Structures

- A bus is a communication pathway connecting two or more devices.
- It can be seen as a **bundle of wires** or conductors that carry different types of signals.
- A key characteristic of a bus is that it is a shared transmission medium.
- Only one device can successfully transmit at a time.
- Multiple transmissions at a time would overlap and get garbled.
- A bus is a **broadcast device**.

A **bus structure** is a way of **organizing the connections** between different components of a computer system — like the CPU, memory, and I/O devices — using a **shared communication pathway** called a **bus**.

# Bus Structures contd.

- A typical bus consists of multiple communication pathways (or lines) where each line is capable of transmitting signals representing binary 1 and binary 0
- Over time, a sequence of binary digits can be transmitted across a single line
- Computer systems contain a number of different buses that provide pathways between components at various levels of the computer system hierarchy.
- The Bus that connects the major components of a computer is known as **System Bus**
- A system bus is the main communication highway inside a computer that connects the CPU, main memory (RAM), and input/output devices. It carries data, memory addresses, and control signals between these components, allowing them to work together.

# System Bus

- A system bus is composed of multiple separate lines each having a particular function
- The bus lines can be classified into 03 functional groups: :
    1. Data Lines / Data Bus
    2. Address Lines / Address Bus
    3. Control Lines /Control Bus

# 1. Data Lines

- Provide a path for moving data among system module.
- Collection of data lines is known as **Data Bus.**
- The data bus may consist of 32, 64, 128, or even more separate lines.
- The number of lines is referred as "**Width of Data Bus**"
- The width of the data bus is a key factor in determining overall system performance

# 2. Address Lines

- They are used to designate the source or destination of the data on the data bus.
- If the processor wishes to read a word of data from memory, it puts the address of the desired word on the Address lines
- The maximum possible memory capacity of the system is determined by the width of Address Bus.
- The address lines are generally also used to address I/O ports, where the higher-order bits are used to select a particular module on the bus, and the lower-order bits select a memory location or I/O port within the module.

# 3. Control Lines

- They are used to control the access to and the use of both the data and address lines.
- They transmit both command and timing information among system modules
- Timing signals indicate the validity of data and address information.
- Command signals specify operations to be performed.

# Control Lines Contd.

- Memory write: causes data on the bus to be written into the addressed location
- Memory read: causes data from the addressed location to be placed on the bus
- I/O write: causes data on the bus to be output to the addressed I/O port
- I/O read: causes data from the addressed I/O port to be placed on the bus
- Transfer ACK: indicates that data have been accepted from or placed on the bus

# Control Lines Contd.

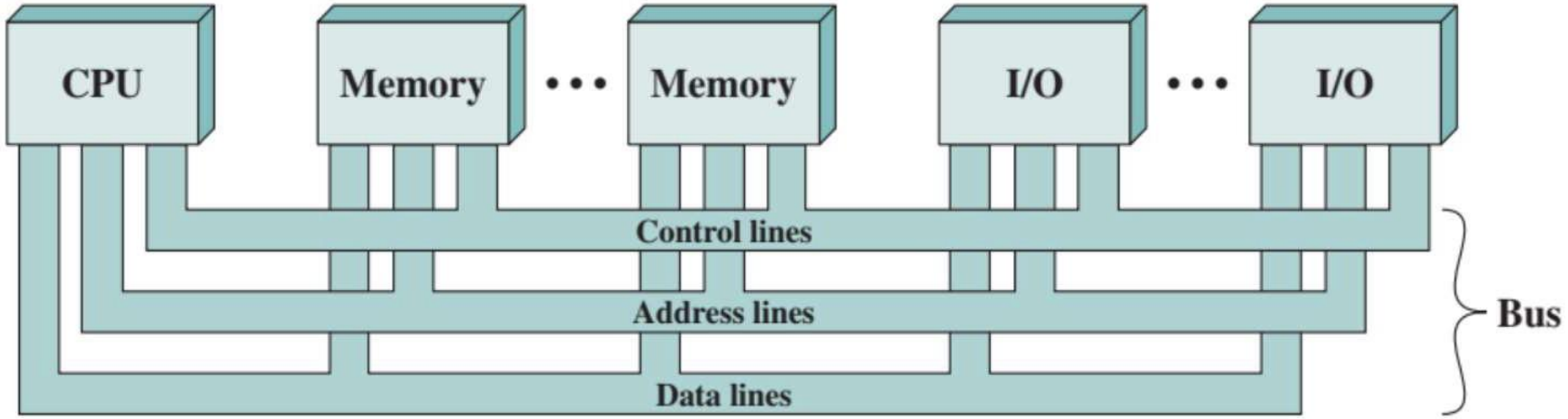
- Bus request: indicates that a module needs to gain control of the bus
- Bus grant: indicates that a requesting module has been granted control of the bus
- Interrupt request: indicates that an interrupt is pending
- Interrupt ACK: acknowledges that the pending interrupt has been recognized
- Clock: is used to synchronize operations
- Reset: Initializes all modules.

# How the bus is operated?

- If one module wishes to send data to another:
  1)obtain the use of the bus
  2)transfer data via the bus
- If one module wishes to request data from another module:
  1)obtain the use of the bus
  2)transfer a request to the other module over the appropriate control and address lines.

*It must then wait for that second module to send the data.

# The System Bus

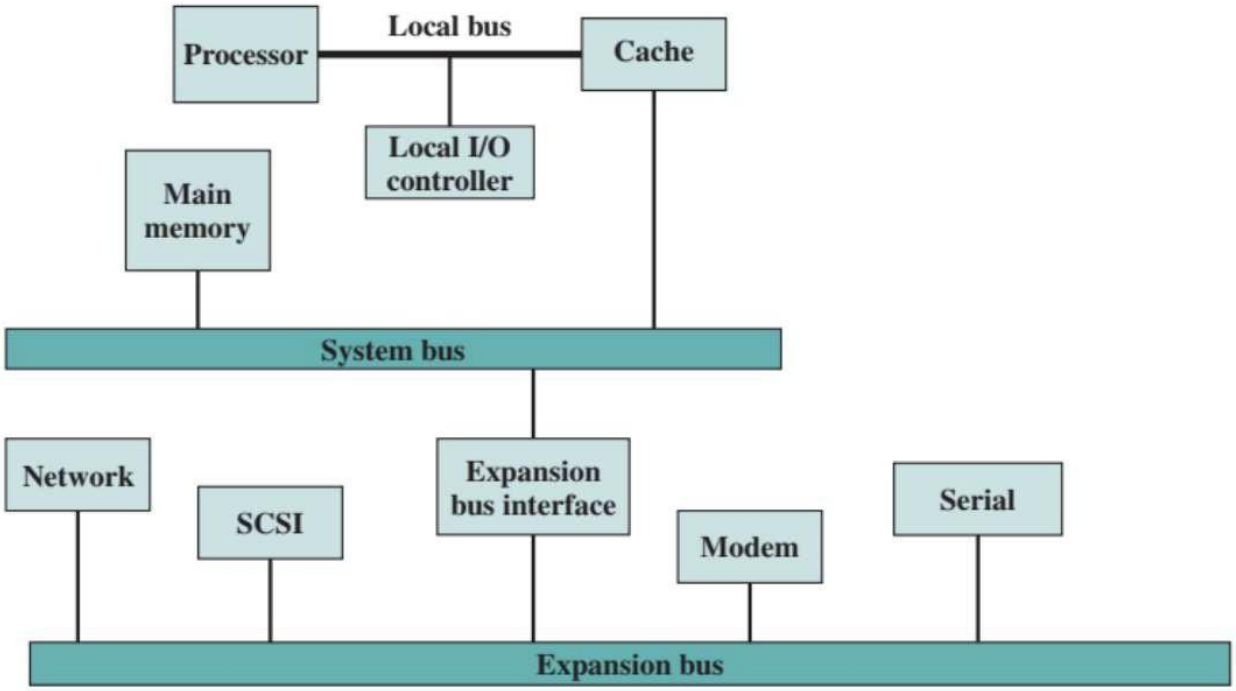


# Multiple Bus

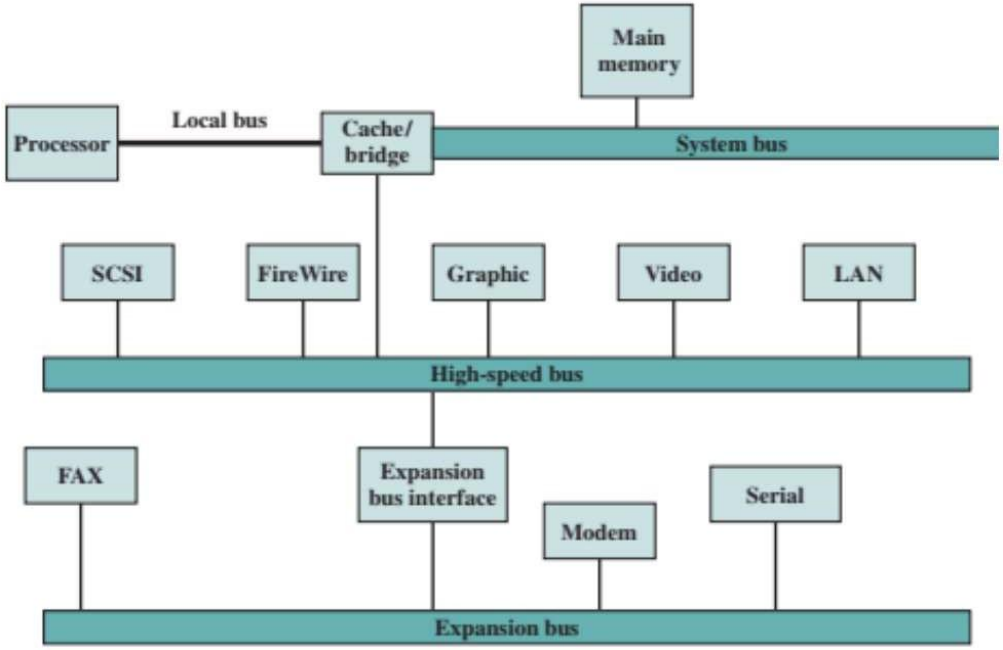
- If a great number of devices are connected to the bus, performance will suffer.
- Reasons
  - If more devices are attached to the bus, the greater the bus length and hence the greater the propagation delay. This delay determines the time it takes for devices to coordinate the use of the bus.
  - The bus may become a bottleneck as the aggregate data transfer demand approaches the capacity of the bus. This problem can be countered to some extent by increasing the data rate that the bus can carry and by using wider buses

**Use Multiple Buses**

# Traditional Bus Structure



# High Performance Architecture



# Elements of Bus Design

| | |
|---|---|
| **Type** | **Bus Width** |
| Dedicated | Address |
| Multiplexed | Data |
| **Method of Arbitration** | **Data Transfer Type** |
| Centralized | Read |
| Distributed | Write |
| **Timing** | Read-modify-write |
| Synchronous | Read-after-write |
| Asynchronous | Block |

**Submission Link**: https://forms.gle/mMdcru6Eu6ZQGMFt5

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# Thankyou