CHANGE HISTORY

1. Rev01 8-30-2016. Based on BCM943907WAE2 Rev 03 with these changes:
   a) New S1 (SB-WBM-N07P, instead of SB-WBM-N07). It has BT I2S brought out, and 3 BT ADC pins depricated
   b) BT I2S connected to Port 3 of AK4961 codec
   c) Added C98 and R93
   d) layout changes (added shield)
   e) the rework for Rev 03 incorporated as C94 and C97.
   f) Changed R62 to 22k, Added R94, C99
      (To delay HIB_REG_ON_IN.)
2. Rev02 9-15-2016. To bringout BT UART/JTAG, added TP13,14,23-26.
3. Rev 1.0 Oct 11, 2016
   a) Renamed to CYW943907WAE3, and setting to rev 1.0
   b) added R95 and connecting power to U6.D10
   c) added R96

   NOV 17 - 2016
   a) Removed J13 and associated components (c89,c90,c95,c96,c55,c27) and nets
   b) Removed J11 and associated components (R91) and nets
   c) removed TP23-26
   d) added L14

   NOV 25 - 2016
   a) Make R39=10k
   b) Make R38=1k. Populate it. Disconnect it from BT_JTAG_SEL net and rename this new node to VDD_PU
   c) Add more nets to J14 as shown now
   d) Add new header J15 (same PN as J14) and wire it up as shown
   e) Remove TP4, Tp6 and TP9

   Dec 13 - 2016
   a) Re-arranged nets on J14 and J15 to make routing easier
   b) Removed R27 and C26.

4 P102 - Mar 22 2017 [bom change only]
   1) Changed L1 and L2 to 0.3pF (0201)
   2) Changed C35 to 1.5nF (0201)
   3) Changed C86 to 0 ohms (0201)

5 June 16 2017 Based on CYW943907WAE3 Rev P102. New PCB SPIN
   Board Renamed as CYW943907WAE4

   1. Added C100-104
   2. Removed C82
   3. Removed D1 (installing U13 instead as noted below)
   4. Removed D2.
   5. Added J19 (sdio chasis)
   6. Changed J6 pn (relaced 4-pin with 6-pin)
   7. Removed R1, R5
   8. Added R100-R116
   9 Added R97-98
   10. Removed SW5
   11. Added U12 (FRAM), U13 (LED)
   12. Changed U2 to Cypress 32MB sflash
   13. Rewired J14, and re-labeled as BT Uart
   14. Changed PCB pn to *-0020, and sch pn to *-0020
   15. Changed silk screen for SW2 from Multi to V-
   16. Removed TP7,8,15,19-21 and renamed the nets to SDIO_*
   17. Rewired SW7 (Play/Pause) circuit as shown (Now driven by GPIO_11 instead of *GPIO_24. Now logic is active High)
   18. Added R117-121, TP31.
   19. Changed C69 to 22uF. Removed C70.
   20. Added R27,C26,C27,C55, TP32-36
   21. Added R122-125
   22. Populated R33 and depopulated R34
   23. Added J20, R128
   24. Added R126, R127. Codec power down moved to GPIO_21 (PWM3) from GPIO_12
       GPIO_12 is now connected to Codec XTI input for supplying 2nd clock source.
   25. Added D3, D4, R129 and R130 for active ant indication

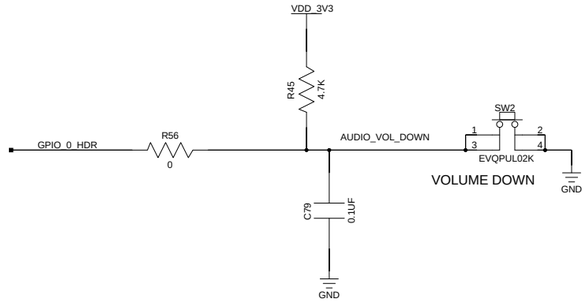
GPIO FUNCTIONALITY FROM BCM43907 PERSPECTIVE

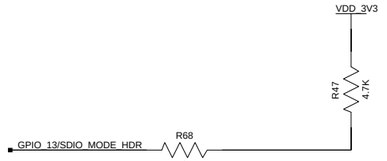
Actual PAD Names on BCM43907 WLCSP PKG	GPIO Definition on BCM43907 GCI Bus ---2nd # is---- FUNCTION TABLE	Input or Output from BCM43907	Description of Functionality
GPIO_0	GPIO_0 1	Input	AUDIO_VOL_DOWN
GPIO_1	GPIO_1 1	Output	43907 Wakes up BT IC (BT_DEV_WAKE)
GPIO_2	GPIO_2 1*	NC - JTAG	Not Used ----- JTAG_TCK - 4 Debug
GPIO_3	GPIO_3 1*	NC - JTAG	Not Used ----- JTAG_TMS - 4 Debug
GPIO_4	GPIO_4 1*	NC - JTAG	Not Used ----- JTAG_TDI - 4 Debug
GPIO_5	GPIO_5 1*	NC - JTAG	Not Used ----- JTAG_TDO - 4 Debug
GPIO_6	GPIO_6 1*	NC - JTAG	Not Used ----- JTAG_TRST_L - 4 Debug
GPIO_7	GPIO_7 1	Input	AUDIO_FWD_SW
GPIO_8	GPIO_8 1	Input	TAP_SEL
GPIO_9	GPIO_9 1	Input	AUDIO_VOL_UP_SW
GPIO_10	GPIO_10 1	Input	AUTH IC RESET
GPIO_11	GPIO_11 1	NC	Audio Play/Pause
GPIO_12	GPIO_12 1	Input	2nd CLOCK for CODEC (XTI)
GPIO_13	GPIO_13 1	Input	
GPIO_14	GPIO_14 1	Input	BT IC Wakes up 43907 (BT_HOST_WAKE)
GPIO_15	GPIO_15 1	Input	43907 Reset to BT IC (LOW = RESET BT 707)
GPIO_16	GPIO_16 1	Output	Battery Charger Interrupt
PWM_0	GPIO_18 3	Input	Enable +3.3V SW Regulator PSM mode (Power Save Mode)
PWM_1	GPIO_19 3	Output	Enable +2.0V SW Regulator
PWM_2	GPIO_20 3	Output	Enable +1.8V LDO
PWM_3	GPIO_21 3	Input	CODEC PDN
PWM_4	GPIO_22 3	Input	Enable Red LED (U13)
PWM_5	GPIO_23 3	Input	AUDIO_BCK_SW
SPI_0_CLK	GPIO_25 3	Input	FRAM
SPI_0_MISO	GPIO_24 3	Input	FRAM
SPI_0_MOSI	GPIO_26 3	IN / OUT	FRAM
SPI_0_CS	GPIO_27 3	IN / OUT	FRAM
I2C0_SDATA	GPIO_28 3	IN / OUT	I2C0
I2C0_CLK	GPIO_29 3	IN / OUT	I2C0

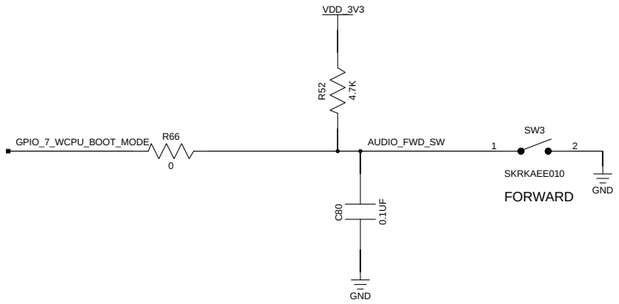
DOCUMENT	PRINTED CIRCUIT BOARD
SCHEMATIC DIAGRAM 630-90492-01	600-90492-01

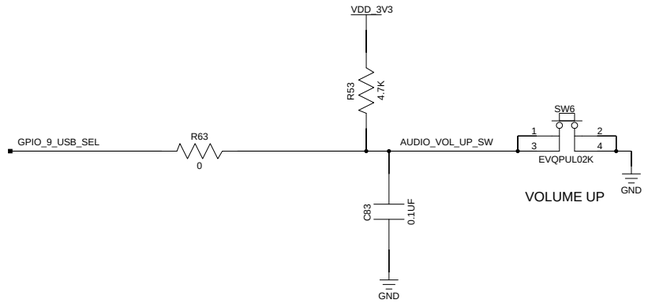
Approvals		Cypress Company Confidential		
Designer	Date			
Reviewer	Date	SIZE B	TITLE CYW943907WAE4 1	
Reviewer	Date	Designer Gurmail	Drawing Number 630-90492-01	Version Rev1.0
Reviewer	Date	DATE 6/16/2017	SHEET 1 OF 8	

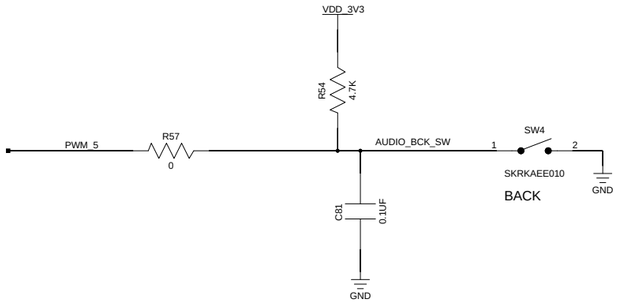
AUDIO SWITCHES ARRAY

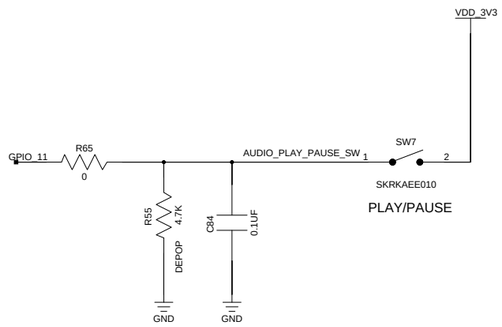












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B	CYW943907WAE4	2
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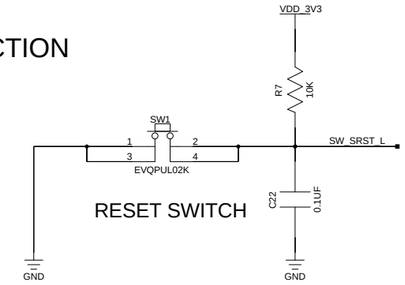
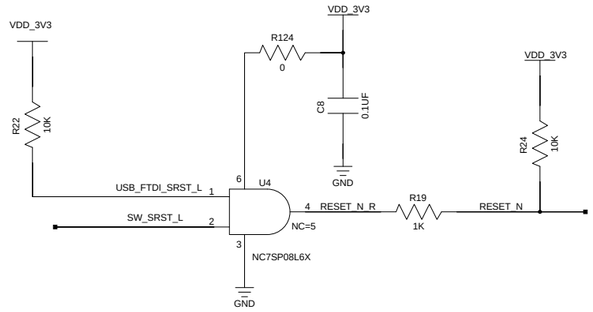
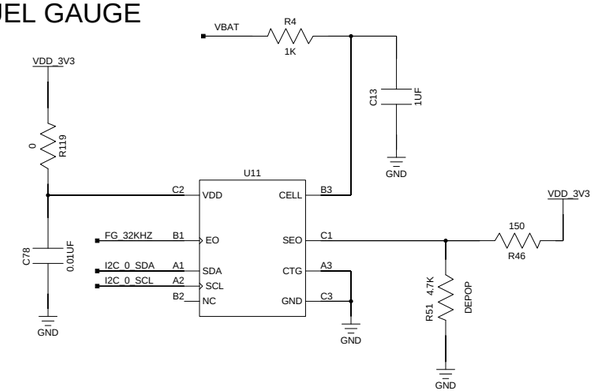
RESET FUNCTION



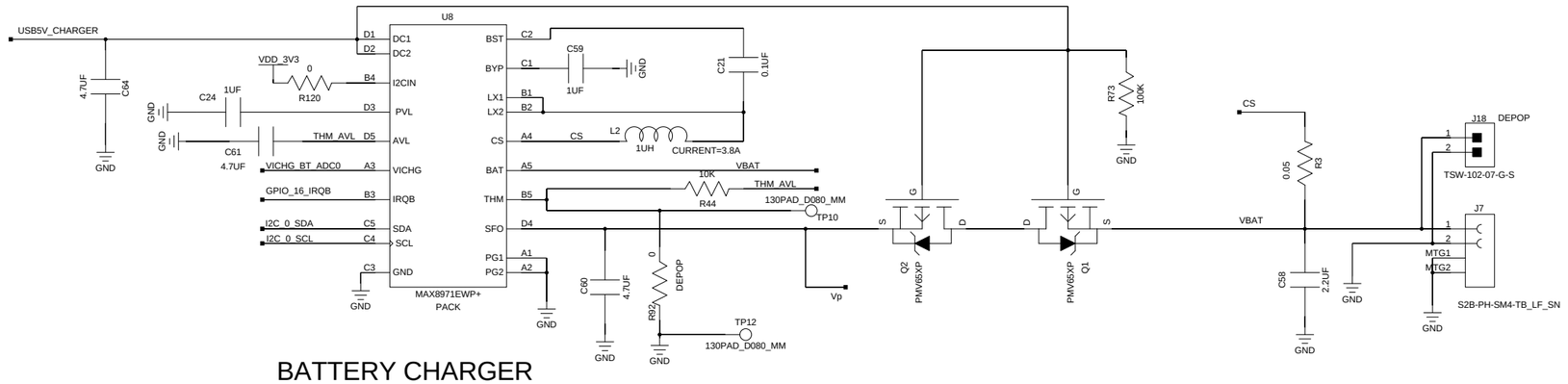
RESET SWITCH

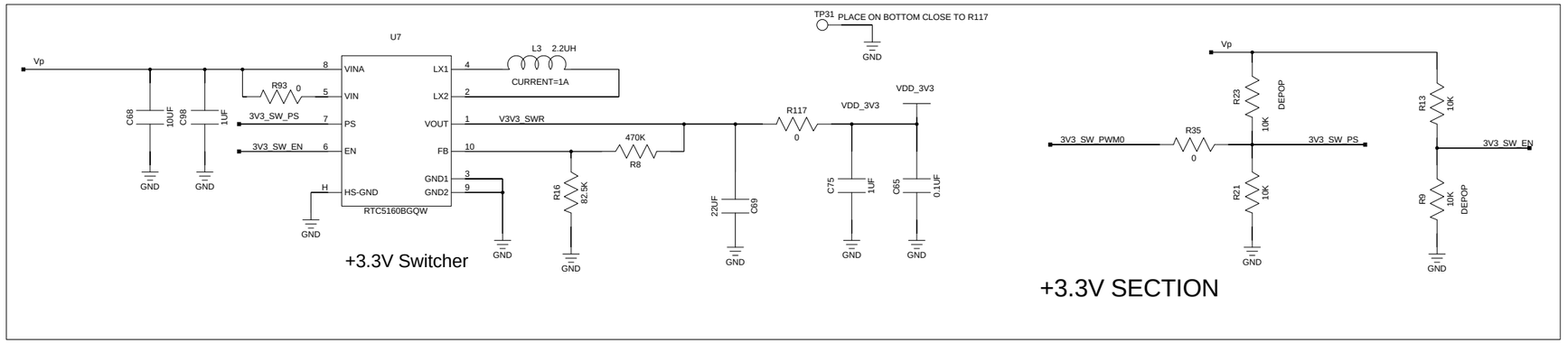
BATTERY FUEL GAUGE

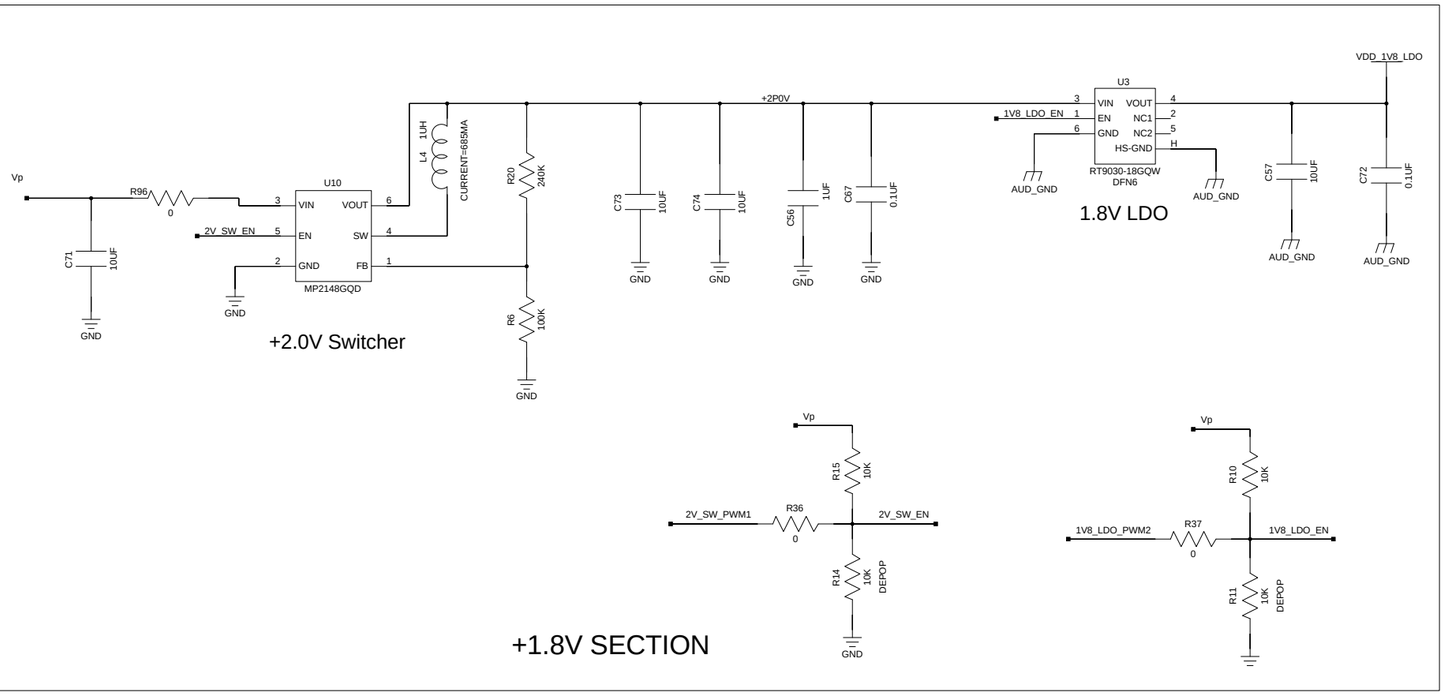




BATTERY CHARGER







Power Supplies

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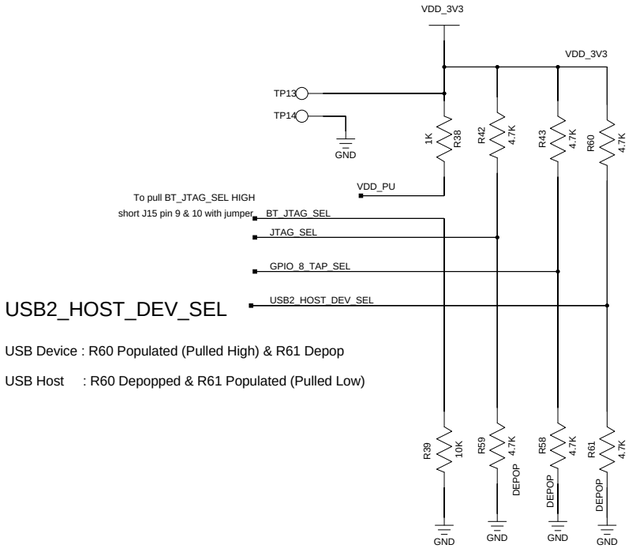
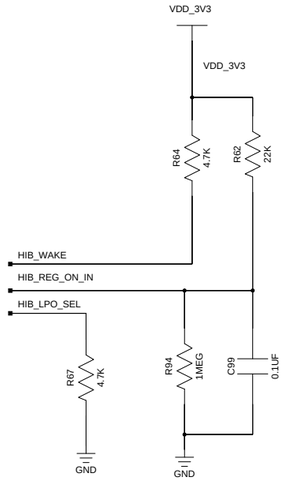


USB2_HOST_DEV_SEL

USB Device : R60 Populated (Pulled High) & R61 Depop

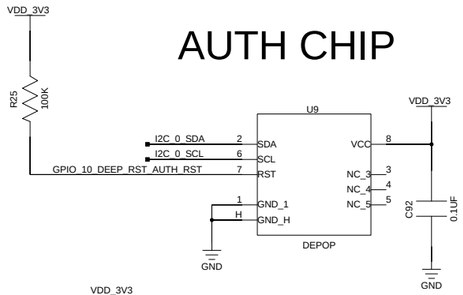
USB Host : R60 Depopped & R61 Populated (Pulled Low)



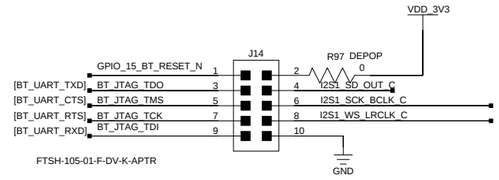
HIBERNATION STRAPPING

Pin	Strap Function	Strap Pull	
		Chip Default	Board Default
GPIO_1	gSPI Mode	0	
GPIO_7	WCPU Boot Mode : 0 = TCROM Boot 1 = TCMSRAM Boot	0	1 REFER TO AUDIO SWITCHES ARRAY
GPIO_9	USB/HSIC Sel : 0 = HSIC PHY 1 = USB PHY	0	1 REFER TO AUDIO SWITCHES ARRAY
GPIO_11	ACPU Boot Mode : 0 = SOCROM Boot 1 = SOCSRAM Boot	0	
GPIO_13	SDIO Mode : 0 = SDIO Device 1 = SDIO Host	0	
RF_SW_CTRL_5	Host DAP Clock Sel	0	
RF_SW_CTRL_7	Host RSRC Init	0	

AUTH CHIP



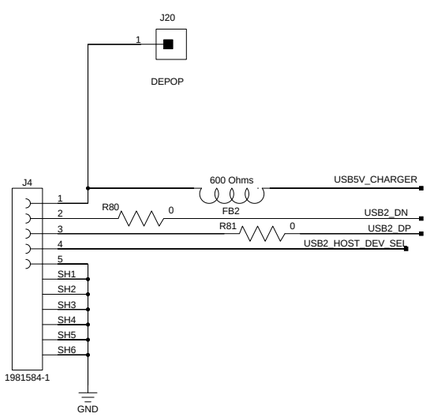
Display 2.54mm Header



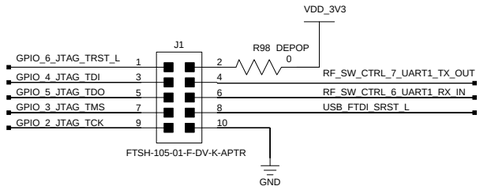
BT UART, WLAN I2S1 Micro Header

BT UART lines mulitplexed on BT JTAG signals as shown on Page5.

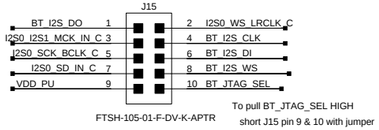
BT JTAG /UART can be driven by external host when 43907 is not using the BT UART interface inside the module U1



Micro USB



WLAN JTAG/UART1 Micro Header



BT I2S, WLAN I2S0 Micro Header

Straps + SFLASH + MISC

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General Vp decoupling

U1 contains BCM43907 (WLAN) and BCM20706A2 BT ICs

When WLAN is in reset, BT uart may be used.
Likewise, when BT is in reset, WLAN uart may be used.
Leave this interface unconnected when both WLAN and BT are operating.

U1
SB-WBM-N07P
LGA170_0.56mm

BCM43907 (WLAN)
BCM20707 (BT)
ALT FUNC. BT_JTAG

BCM43907 (WLAN)
BCM20707 (BT)

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SIZE	TITLE	
B	CYW943907WAE4	5
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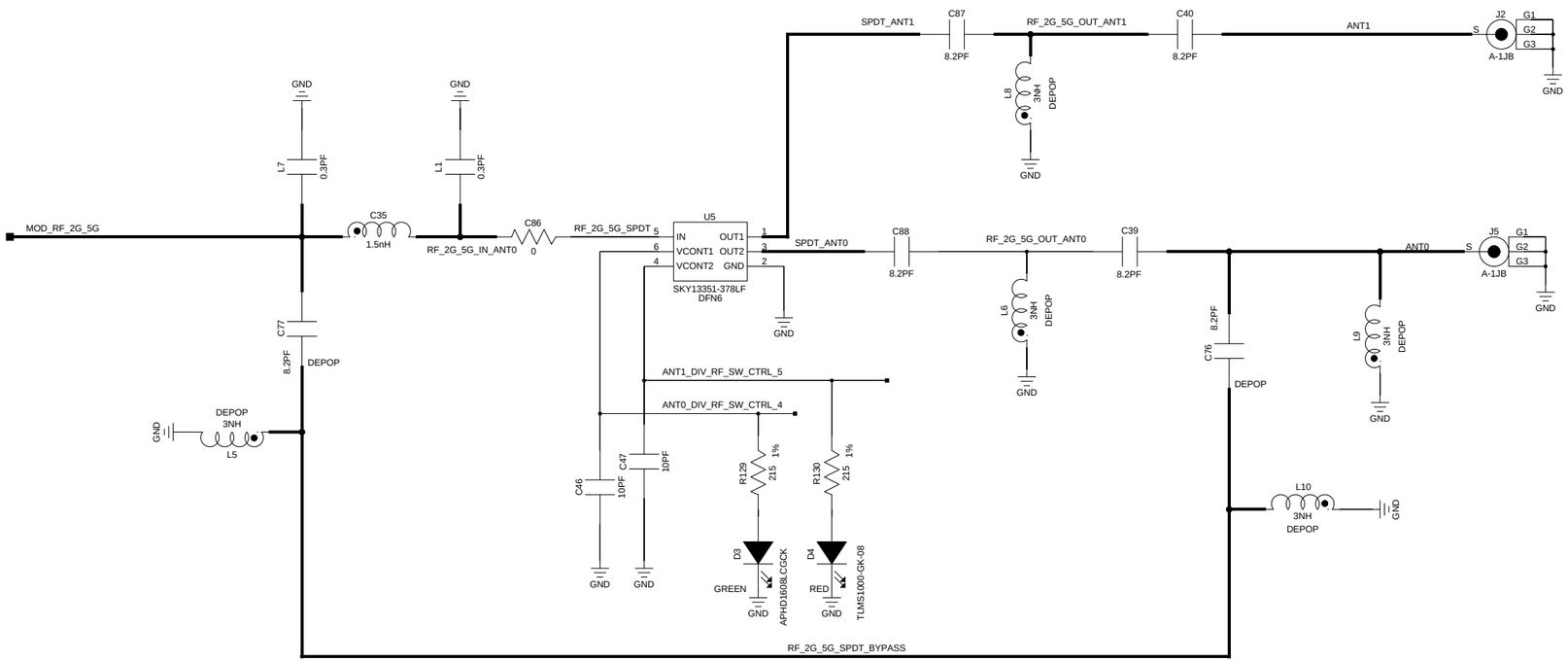

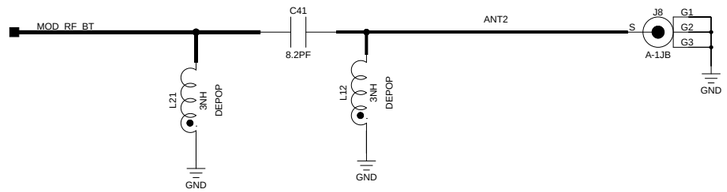

U5 2G/5G SPDT Antenna Diversity Switch Control Table		
MODE OF OPERATION Ant Diversity	ANT0_DIV_RF_SW_CTRL_4 SPDT (U5 VCONT1)	ANT1_DIV_RF_SW_CTRL_5 DPDT (U5 VCONT2)
RF_2G_5G to Ant0	1	0
RF_2G_5G to Ant1	0	1

ALL OTHER STATES UNDEFINED

ANTENNA DIVERSITY

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B	CYW943907WAE4 6	
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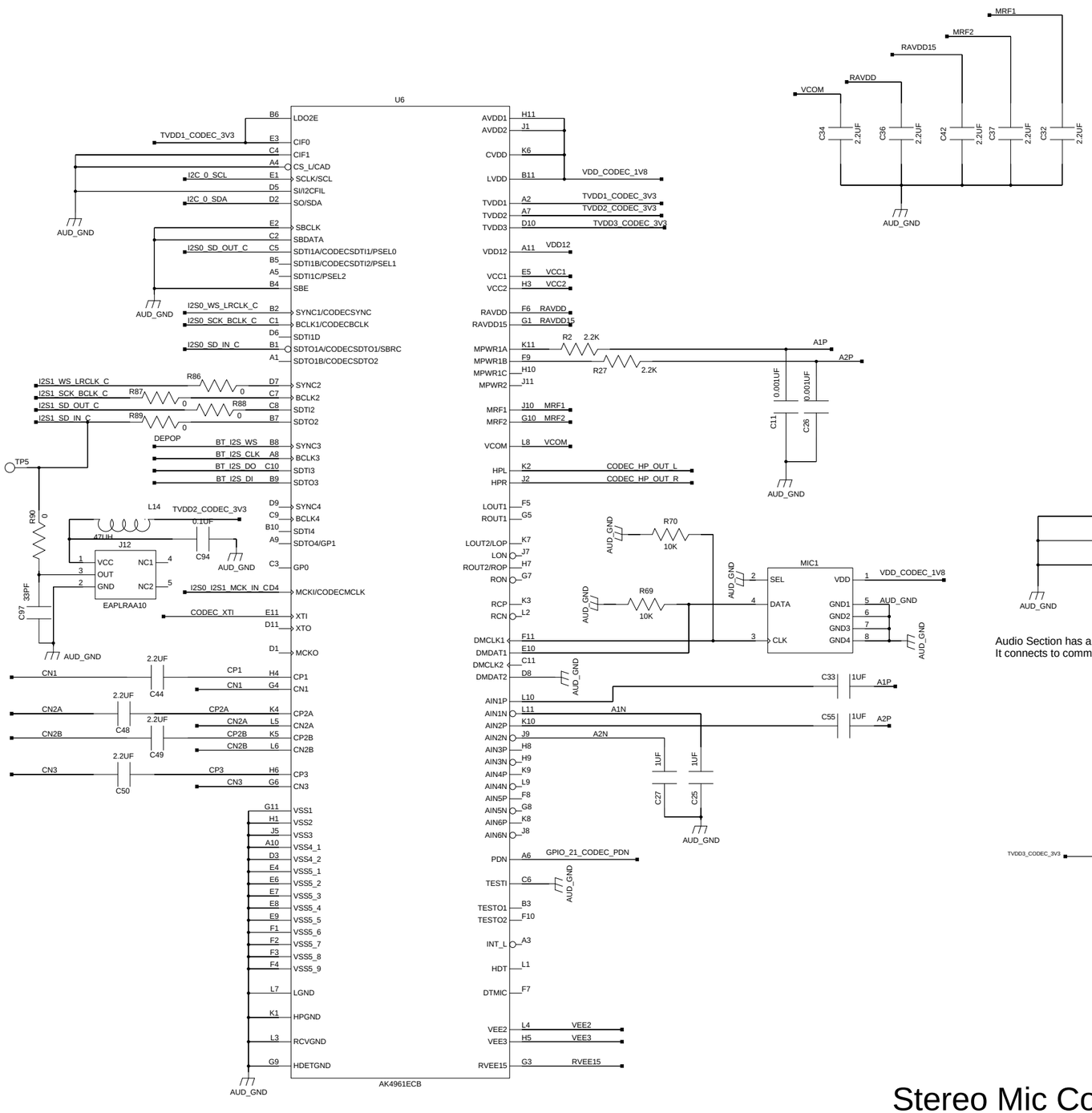
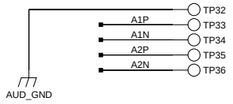


Audio Section has a separate Audio GND to isolate from noise of other sections.
It connects to common GND (GND) with a 0 Ohms Resistors

AUDIO CODEC

Stereo Mic Connection



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SIZE	TITLE	
B	CYW943907WAE4	7
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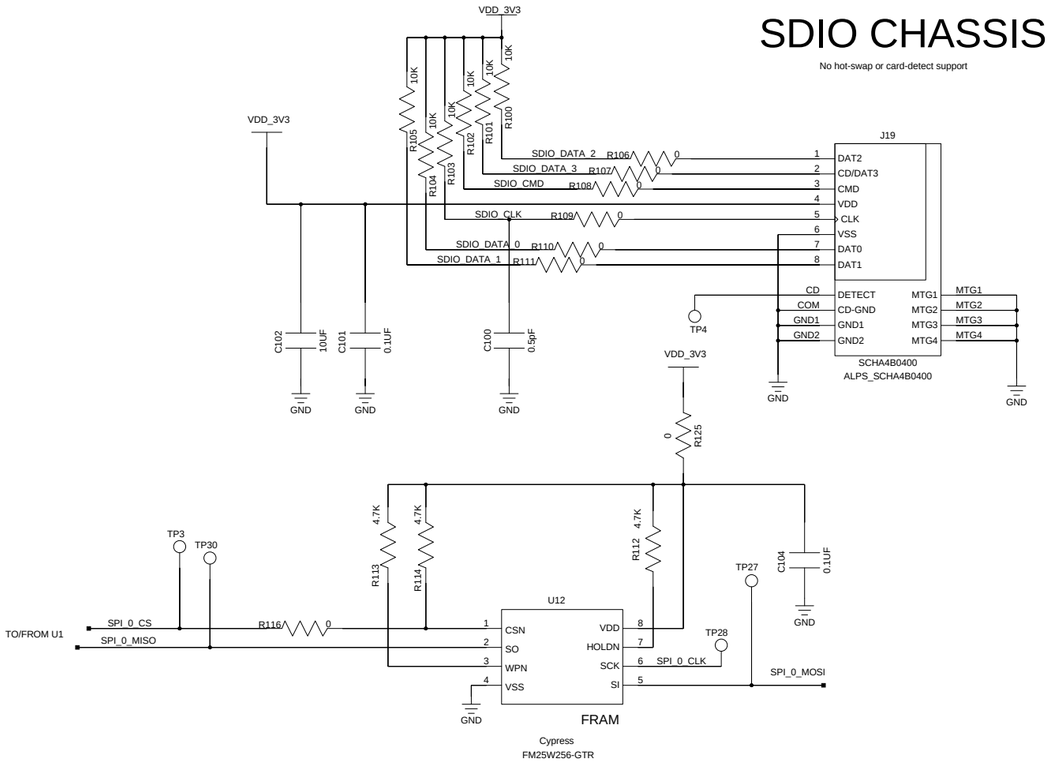
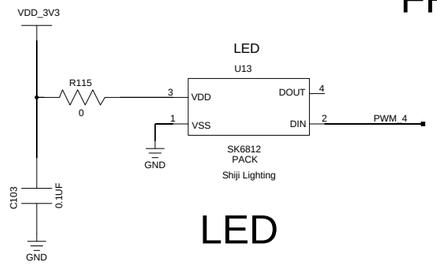
SDIO CHASSIS

No hot-swap or card-detect support

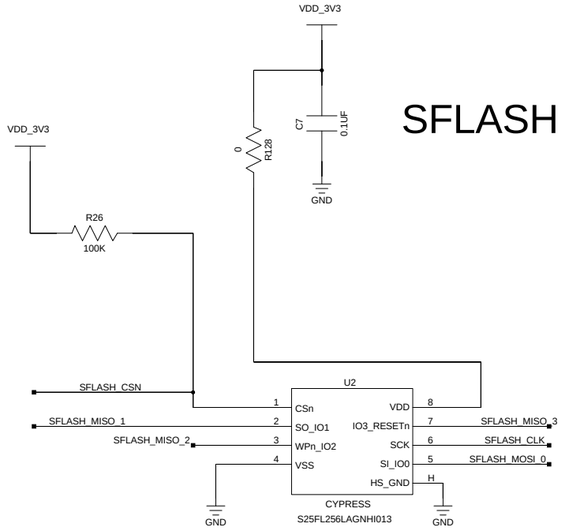


FRAM



LED

SFLASH 32MB



SFLASH, FRAM, SDIO CHASSIS, LED

Cypress

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		8
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