CS47L24

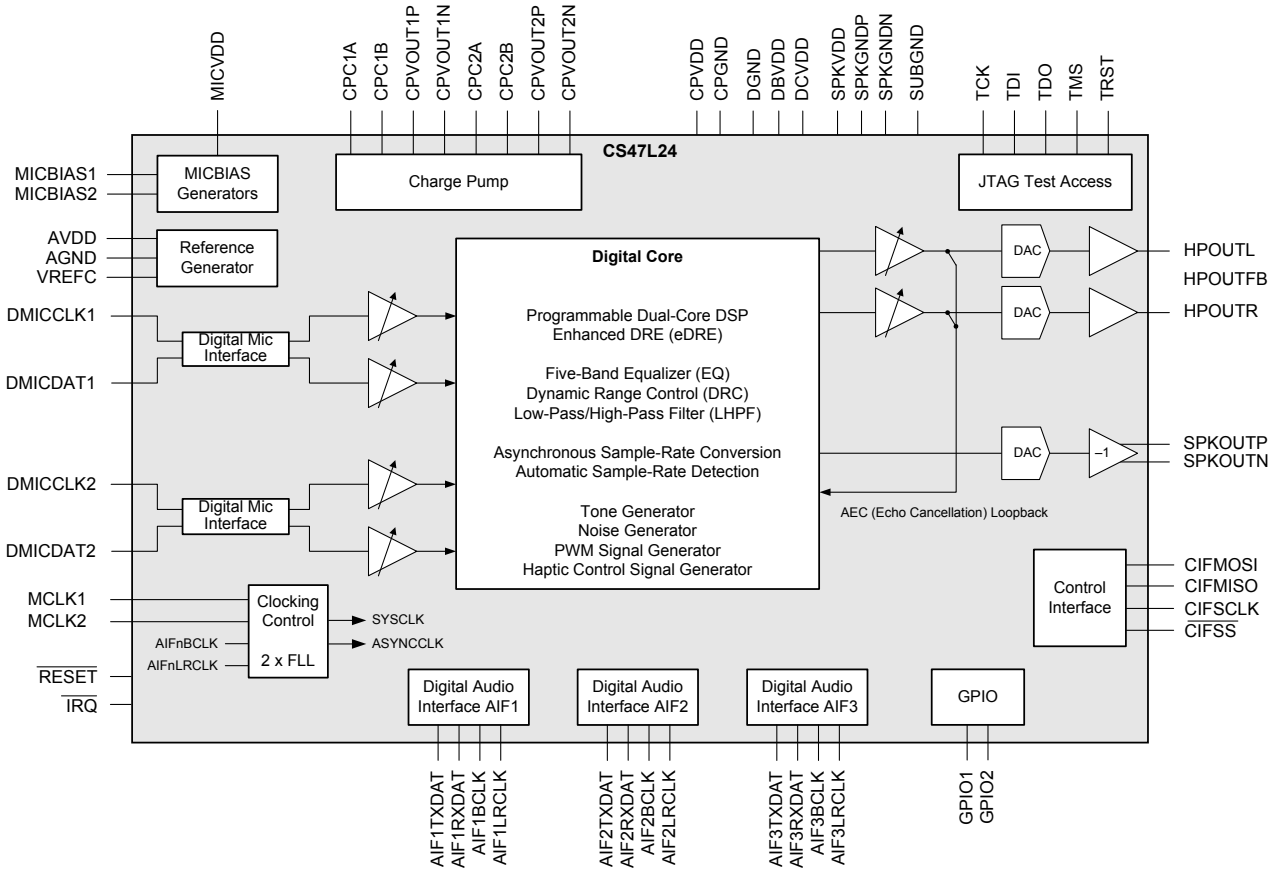
Low Power Audio Hub for Wearable Technology

Features

- 300 MIPS, 300MMAC dual-core audio-signal processor
- Enhanced DRE processing (eDRE) for 121dB SNR
- Fixed function signal-processing functions
  - — Dynamic range control, fully parametric EQs
  - — Tone, noise, PWM, haptic control signal generators
- Multichannel asynchronous sample-rate conversion
- Integrated multichannel 24-bit hi-fi audio hub codec
  - — 121-dB SNR headphone playback (48 kHz)
- Four digital microphone inputs (two stereo interfaces)
- Stereo headphone/earpiece/line output driver
  - — 33 mW into 32-Ω load at 1% THD+N
- Mono 2W Class D speaker output driver
- Three full digital audio interfaces
  - — Standard sample rates from 8kHz up to 192kHz
  - — TDM support on all AIFs
- Flexible clocking, derived from MCLKn or AIFn
- Two low-power frequency-locked loops (FLLs) support reference clocks down to 32 kHz
- Configurable functions on two GPIO pins
- Integrated regulators and charge pumps
- Small W-CSP package, 0.4-mm ball array

Applications

- Portable accessories and wearable technology
- Smartphones and multimedia handsets
- Speech-recognition applications



Description

The CS47L24 is a highly integrated, low-power audio hub for wearable technology and other portable audio devices. It combines an advanced DSP feature set with a flexible, high-performance audio hub codec.

The CS47L24 digital core combines a dual-core, 300MMAC DSP system, with a variety of power-efficient fixed-function audio-processing blocks. These are supported by a fully flexible, all-digital mixing and routing engine with sample rate converters for wide use-case flexibility. The programmable DSP cores support a range of advanced audio processing features, including multimic noise suppression, acoustic-echo cancellation (AEC), and voice recognition functions. The Enhanced DRE (eDRE) software is included with the CS47L24; additional software packages can be chosen according to the requirements of the target application.

Three digital audio interfaces are provided, each supporting a wide range of standard audio sample rates and serial interface formats. Automatic sample-rate detection enables seamless wideband/narrowband voice-call handover.

The headphone/line output driver provides stereo ground-referenced or mono BTL output. 121dB SNR, and noise levels as low as 0.8 µVRMS, offer hi-fi quality line or headphone output. A mono Class D output driver is incorporated; supporting up to 2-W audio output. A signal generator for controlling haptics devices is included; vibe actuators can connect directly to the Class D speaker output or via an external driver connected to a GPIO output. All inputs, outputs, and system interfaces can function concurrently.

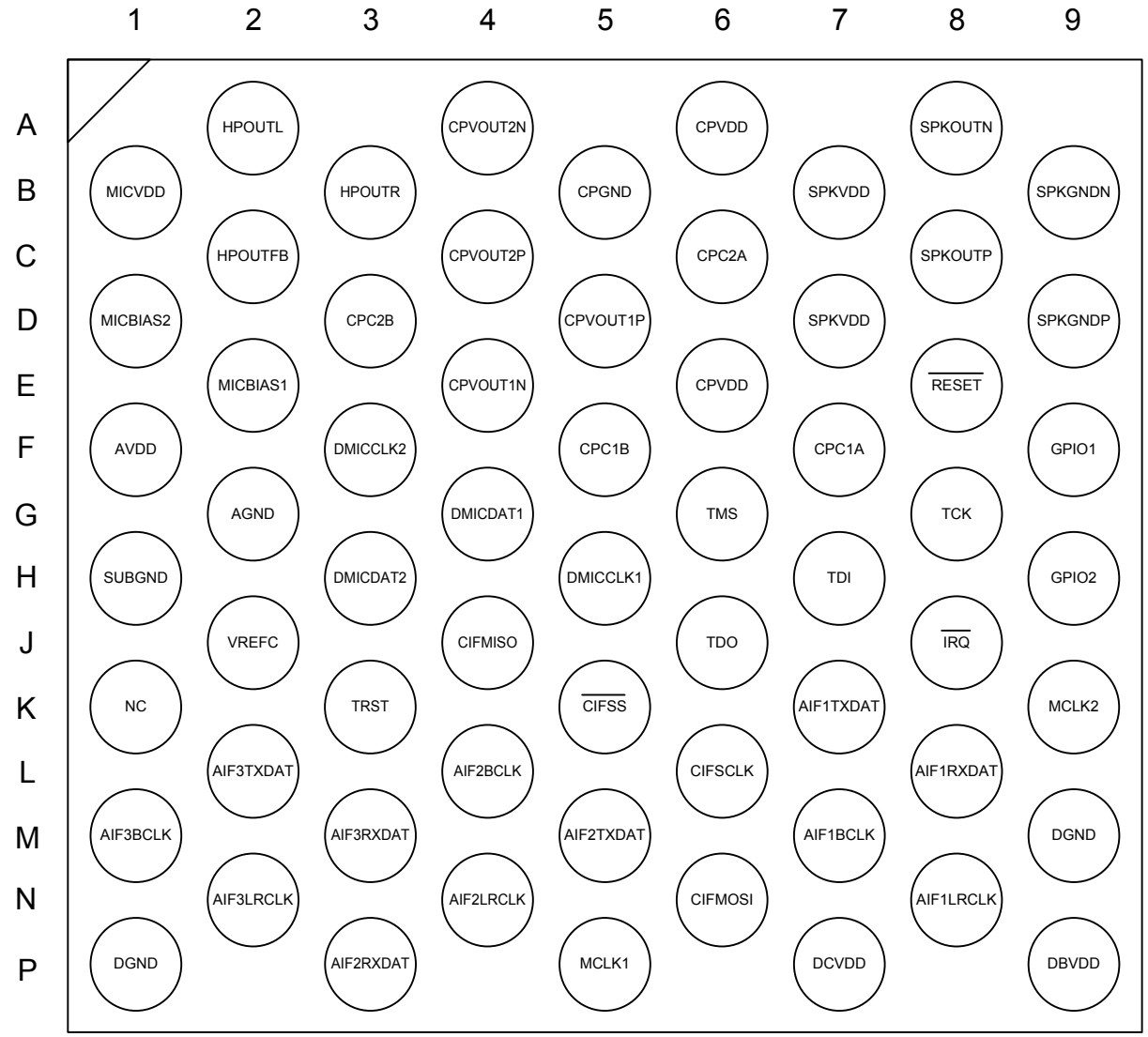
The CS47L24 supports up to four digital microphone inputs. Microphone activity detection with interrupt is available.

The CS47L24 power, clocking and output driver architectures are all designed to maximize battery life in voice, music, and standby modes. The CS47L24 is powered from 1.8- and 1.2-V external supplies. Separate MICVDD input can be supported, for microphone operation above 1.8 V. An additional supply is required for the Class D speaker drivers (typically direct connection to 4.2-V battery).

Two integrated FLLs provide support for a wide range of system clock frequencies. The CS47L24 is configured using an SPI™ control interface. The fully CS47L24 differential internal analog architecture, minimal analog signal paths, and on-chip RF noise filters ensure a very high degree of noise immunity.

TABLE OF CONTENTS

PIN CONFIGURATION



TOP VIEW – CS47L24

ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
CS47L24-CWZ	-40°C to +85°C	W-CSP (Pb-free)	MSL1	260°C
CS47L24-CWZR	-40°C to +85°C	W-CSP (Pb-free, Tape and reel)	MSL1	260°C

Note:
Reel quantity = 7000

PIN DESCRIPTION

A description of each pin on the CS47L24 is provided below.

Note that a table detailing the associated power domain for every input and output pin is provided on the following page.

Note that, where multiple pins share a common name, these pins should be tied together on the PCB.

All Digital Output pins are CMOS outputs, unless otherwise stated.

PIN NO	NAME	TYPE	DESCRIPTION
G2	AGND	Supply	Analogue ground (Return path for AVDD and MICVDD)
M7	AIF1BCLK	Digital Input / Output	Audio interface 1 bit clock
N8	AIF1LRCLK	Digital Input / Output	Audio interface 1 left / right clock
L8	AIF1RXDAT	Digital Input	Audio interface 1 RX digital audio data
K7	AIF1TXDAT	Digital Output	Audio interface 1 TX digital audio data
L4	AIF2BCLK	Digital Input / Output	Audio interface 2 bit clock
N4	AIF2LRCLK	Digital Input / Output	Audio interface 2 left / right clock
P3	AIF2RXDAT	Digital Input	Audio interface 2 RX digital audio data
M5	AIF2TXDAT	Digital Output	Audio interface 2 TX digital audio data
M1	AIF3BCLK	Digital Input / Output	Audio interface 3 bit clock
N2	AIF3LRCLK	Digital Input / Output	Audio interface 3 left / right clock
M3	AIF3RXDAT	Digital Input	Audio interface 3 RX digital audio data
L2	AIF3TXDAT	Digital Output	Audio interface 3 TX digital audio data
F1	AVDD	Supply	Analogue supply
J4	CIFMISO	Digital Output	Control interface Master In Slave Out. The pin configuration is selectable CMOS or 'Wired OR'.
N6	CIFMOSI	Digital Input	Control interface Master Out Slave In data.
L6	CIFSCLK	Digital Input	Control interface clock input
K5	$\overline{\text{CIFSS}}$	Digital Input	Control interface Slave Select (SS)
F7	CPC1A	Analogue Output	Charge pump fly-back capacitor 1 pin
F5	CPC1B	Analogue Output	Charge pump fly-back capacitor 1 pin
C6	CPC2A	Analogue Output	Charge pump fly-back capacitor 2 pin
D3	CPC2B	Analogue Output	Charge pump fly-back capacitor 2 pin
B5	CPGND	Supply	Charge pump ground (Return path for CPVDD)
A6, E6	CPVDD	Supply	Supply for Charge Pump
E4	CPVOUT1N	Analogue Output	Charge pump negative output 1 decoupling pin
D5	CPVOUT1P	Analogue Output	Charge pump positive output 1 decoupling pin
A4	CPVOUT2N	Analogue Output	Charge pump negative output 2 decoupling pin
C4	CPVOUT2P	Analogue Output	Charge pump positive output 2 decoupling pin
P9	DBVDD	Supply	Digital buffer (I/O) supply
P7	DCVDD	Supply	Digital core supply
M9, P1	DGND	Supply	Digital ground (Return path for DCVDD and DBVDD)
H5	DMICCLK1	Digital Output	Digital MIC clock output 1
F3	DMICCLK2	Digital Output	Digital MIC clock output 2
G4	DMICDAT1	Digital Input	Digital MIC data input 1
H3	DMICDAT2	Digital Input	Digital MIC data input 2
F9	GPIO1	Digital Input / Output	General Purpose pin GPIO1. The output configuration is selectable CMOS or Open Drain.
H9	GPIO2	Digital Input / Output	General Purpose pin GPIO2. The output configuration is selectable CMOS or Open Drain.
C2	HPOUTFB	Analogue Input	HPOUTL and HPOUTR ground feedback pin
A2	HPOUTL	Analogue Output	Left headphone output
B3	HPOUTR	Analogue Output	Right headphone output
J8	$\overline{\text{IRQ}}$	Digital Output	Interrupt Request (IRQ) output (default is active low). The pin configuration is selectable CMOS or Open Drain.
P5	MCLK1	Digital Input	Master clock 1
K9	MCLK2	Digital Input	Master clock 2

PIN NO	NAME	TYPE	DESCRIPTION
E2	MICBIAS1	Analogue Output	Microphone bias 1
D1	MICBIAS2	Analogue Output	Microphone bias 2
B1	MICVDD	Supply	Microphone bias supply (input to MICBIASn regulators).
E8	$\overline{\text{RESET}}$	Digital Input	Digital Reset input (active low)
B9	SPKGNDN	Supply	Speaker driver ground (Return path for SPKVDD). See note.
D9	SPKGNDP	Supply	Speaker driver ground (Return path for SPKVDD). See note.
A8	SPKOUTN	Analogue Output	Speaker negative output
C8	SPKOUTP	Analogue Output	Speaker positive output
B7, D7	SPKVDD	Supply	Speaker driver supply
H1	SUBGND	Supply	Substrate ground
G8	TCK	Digital Input	JTAG clock input. Internal pull-down holds this pin at logic 0 for normal operation.
H7	TDI	Digital Input	JTAG data input. Internal pull-down holds this pin at logic 0 for normal operation.
J6	TDO	Digital Output	JTAG data output
G6	TMS	Digital Input	JTAG mode select input. Internal pull-down holds this pin at logic 0 for normal operation.
K3	TRST	Digital Input	JTAG Test Access Port reset (active low). Internal pull-down holds this pin at logic 0 for normal operation.
J2	VREFC	Analogue Output	Bandgap reference decoupling capacitor connection
K1	NC		No Connection

Note:

Separate P/N ground connections are provided for each speaker driver channel; this provides flexible support for current monitoring and output protection circuits. If this option is not used, then the respective ground connections should be tied together on the PCB.

The following table identifies the power domain and ground reference associated with each of the input / output pins.

PIN NO	NAME	POWER DOMAIN	GROUND DOMAIN
M7	AIF1BCLK	DBVDD	DGND
N8	AIF1LRCLK	DBVDD	DGND
L8	AIF1RXDAT	DBVDD	DGND
K7	AIF1TXDAT	DBVDD	DGND
L4	AIF2BCLK	DBVDD	DGND
N4	AIF2LRCLK	DBVDD	DGND
P3	AIF2RXDAT	DBVDD	DGND
M5	AIF2TXDAT	DBVDD	DGND
M1	AIF3BCLK	DBVDD	DGND
N2	AIF3LRCLK	DBVDD	DGND
M3	AIF3RXDAT	DBVDD	DGND
L2	AIF3TXDAT	DBVDD	DGND
J4	CIFMISO	DBVDD	DGND
N6	CIFMOSI	DBVDD	DGND
L6	CIFSCLK	DBVDD	DGND
K5	$\overline{\text{CIFSS}}$	DBVDD	DGND
H5	DMICCLK1	MICVDD, MICBIAS1, MICBIAS2 The DMICCLK1 power domain is selectable using IN1_DMIC_SUP	AGND
F3	DMICCLK2	MICVDD, MICBIAS1, MICBIAS2 The DMICCLK2 power domain is selectable using IN2_DMIC_SUP	AGND
G4	DMICDAT1	MICVDD, MICBIAS1, MICBIAS2 The DMICDAT1 power domain is selectable using IN1_DMIC_SUP	AGND
H3	DMICDAT2	MICVDD, MICBIAS1, MICBIAS2 The DMICDAT2 power domain is selectable using IN2_DMIC_SUP	AGND
F9	GPIO1	DBVDD	DGND
H9	GPIO2	DBVDD	DGND
C2	HPOUTFB	CPVDD (Ground noise rejection)	CPGND
A2	HPOUTL	CPVDD	CPGND
B3	HPOUTR	CPVDD	CPGND
J8	$\overline{\text{IRQ}}$	DBVDD	DGND
P5	MCLK1	DBVDD	DGND
K9	MCLK2	DBVDD	DGND
E2	MICBIAS1	MICVDD	AGND
D1	MICBIAS2	MICVDD	AGND
E8	$\overline{\text{RESET}}$	DBVDD	DGND
A8	SPKOUTN	SPKVDD	SPKGNDN
C8	SPKOUTP	SPKVDD	SPKGNDP
G8	TCK	DBVDD	DGND
H7	TDI	DBVDD	DGND
J6	TDO	DBVDD	DGND
G6	TMS	DBVDD	DGND
K3	TRST	DBVDD	DGND

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus Logic tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (DCVDD)	-0.3V	MIN (1.6V, AVDD+0.6V)
Supply voltages (CPVDD)	-0.3V	2.5V
Supply voltages (DBVDD, AVDD, MICVDD)	-0.3V	5.0V
Supply voltages (SPKVDD)	-0.3V	6.0V
Voltage range digital inputs	SUBGND - 0.3V	DBVDD + 0.3V
Voltage range digital inputs (DMICDATn)	SUBGND - 0.3V	MICVDD + 0.3V
Voltage range analogue inputs (HPOUTFB)	SUBGND - 0.3V	SUBGND + 0.3V
Ground (AGND, DGND, CPGND, SPKGND)	SUBGND - 0.3V	SUBGND + 0.3V
Operating temperature range, T_A	-40ºC	+85ºC
Operating junction temperature, T_J	-40ºC	+125ºC
Storage temperature after soldering	-65ºC	+150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core) See note 2	DCVDD	1.14	1.2	1.26	V
Digital supply range (I/O)	DBVDD	1.71	1.8	2.75	V
Charge Pump supply range	CPVDD	1.71	1.8	1.89	V
Analogue supply range See note 2	AVDD	1.71	1.8	1.89	V
Microphone Bias supply	MICVDD	1.71		3.6	V
Speaker supply range	SPKVDD	2.4		5.5	V
Ground See note 1	DGND, AGND, CPGND, SPKGNDN, SPKGNDP, SUBGND		0		V
Power supply rise time See notes 3, 4, 5	DCVDD	10		2000	µs
	All other supplies	10			
Operating temperature range	T_A	-40		85	°C

Notes:

1. The impedance between DGND, AGND, CPGND and SUBGND should be less than 0.1Ω.The impedance between SPKGND and SUBGND should be less than 0.2Ω.
2. AVDD must be supplied before or simultaneously to DCVDD. DCVDD must not be powered if AVDD is not present. There are no other power sequencing requirements.
3. If the DCVDD rise time exceeds 2ms, then $\overline{\text{RESET}}$ must be asserted (low) during the rise, and held asserted until after DCVDD is within the recommended operating limits.
4. The specified minimum power supply rise times assume a minimum decoupling capacitance of 100nF per pin. However, Cirrus Logic strongly advises that the recommended decoupling capacitors are present on the PCB and that appropriate layout guidelines are observed.
5. The specified minimum power supply rise times also assume a maximum PCB inductance of 10nH between decoupling capacitor and pin.

ELECTRICAL CHARACTERISTICS

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Microphone Input Signal Level (DMICDAT1, DMICDAT2)						
Full-scale input signal level (0dBFS signal to digital core)		0dB gain		-6		dBFS

Note:

The digital microphone input signal level is measured in dBFS, where 0dBFS is a signal level equal to the full-scale range (FSR) of the PDM input. The FSR is defined as the amplitude of a 1kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively - this is the largest 1kHz sine wave that will fit in the digital output range without clipping.

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Line / Headphone / Earpiece Output Driver (HPOUTL, HPOUTR)						
Load resistance		Normal operation, Single-ended mode	6			Ω
		Normal operation, Differential (BTL) mode	15			
		Device survival with load applied indefinitely	0			
Load capacitance		Direct connection, Normal Mode			500	pF
		Direct connection, Mono Mode (BTL)			200	
		Connection via 16Ω series resistor			2	nF
Speaker Output Driver (SPKOUTP+SPKOUTN)						
Load resistance		Normal operation	4			Ω
		Device survival with load applied indefinitely	0			
Load capacitance					200	pF
Digital Speaker Output (SPKDAT)						
Full-scale output level (0dBFS digital core output)		0dB gain		-6		dBFS

Note:

The digital output signal level is measured in dBFS, where 0dBFS is a signal level equal to the full-scale range (FSR) of the PDM output. The FSR is defined as the amplitude of a 1kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively - this is the largest 1kHz sine wave that will fit in the digital output range without clipping.

Test Conditions

DBVDD = CPVDD = AVDD = 1.8V, MICVDD = 2.2V, DCVDD = 1.2V, SPKVDD = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Line / Headphone / Earpiece Output Driver (HPOUTL, HPOUTR)						
DC offset at Load		Single-ended mode		0.1		mV
		Differential (BTL) mode		0.2		
Speaker Output Driver (SPKOUTP+SPKOUTN)						
DC offset at Load				10		mV
SPKVDD leakage current				1		µA
DAC to Line Output (HPOUTL, HPOUTR; Load = 10kΩ, 50pF)						
Full-scale output signal level	V_{OUT}	0dBFS input	1 0			Vrms dBV
Signal to Noise Ratio (A-weighted)	SNR	Output signal = 1Vrms	106	115		dB
		Output signal = 1Vrms, eDRE software enabled		121		
Dynamic Range (A-weighted)	DR	-60dBFS input		115		dB
Total Harmonic Distortion	THD	0dBFS input		-93	-84	dB
Total Harmonic Distortion + Noise	THD+N	0dBFS input		-92		dB
Channel separation (Left/Right)				110		dB
Output noise floor (A-weighted)		eDRE software enabled		0.9		μV_{RMS}
PSRR (DBVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		105		dB
		100mV (peak-peak) 10kHz		75		
PSRR (MICVDD)	PSRR	100mV (peak-peak) 217Hz		112		dB
		100mV (peak-peak) 10kHz		102		
PSRR (DCVDD)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		114		
PSRR (SPKVDD)	PSRR	100mV (peak-peak) 217Hz		111		dB
		100mV (peak-peak) 10kHz		103		

Test Conditions

DBVDD = CPVDD = AVDD = 1.8V, MICVDD = 2.2V, DCVDD = 1.2V, SPKVDD = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Headphone Output (HPOUTL, HPOUTR, R_L = 32Ω, Short Circuit Protection disabled)						
Maximum output power	P_O	0.1% THD+N		30		mW
Signal to Noise Ratio (A-weighted)	SNR	Output signal = 1Vrms	106	115		dB
		Output signal = 1Vrms, eDRE software enabled		121		
Dynamic Range (A-weighted)	DR	-60dBFS input		115		dB
Total Harmonic Distortion	THD	P_O = 20mW		-92	-82	dB
Total Harmonic Distortion + Noise	THD+N	P_O = 20mW		-90		dB
Total Harmonic Distortion	THD	P_O = 5mW		-91		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 5mW		-88		dB
Channel separation (Left/Right)				94		dB
Output noise floor (A-weighted)		eDRE software enabled		0.9		μV_{RMS}
PSRR (DBVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		105		dB
		100mV (peak-peak) 10kHz		75		
PSRR (MICVDD)	PSRR	100mV (peak-peak) 217Hz		112		dB
		100mV (peak-peak) 10kHz		102		
PSRR (DCVDD)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		114		
PSRR (SPKVDD)	PSRR	100mV (peak-peak) 217Hz		111		dB
		100mV (peak-peak) 10kHz		103		
DAC to Headphone Output (HPOUTL, HPOUTR, R_L = 16Ω, Short Circuit Protection disabled; eDRE enabled)						
Maximum output power	P_O	0.1% THD+N		39		mW
Signal to Noise Ratio (A-weighted)	SNR	Output signal = 1Vrms	106	115		dB
		Output signal = 1Vrms, eDRE software enabled		121		
Dynamic Range (A-weighted)	DR	-60dBFS input		115		dB
Total Harmonic Distortion	THD	P_O = 20mW		-88	-78	dB
Total Harmonic Distortion + Noise	THD+N	P_O = 20mW		-87		dB
Total Harmonic Distortion	THD	P_O = 5mW		-88		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 5mW		-86		dB
Channel separation (Left/Right)				92		dB
Output noise floor (A-weighted)		eDRE software enabled		0.9		μV_{RMS}
PSRR (DBVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		105		dB
		100mV (peak-peak) 10kHz		75		
PSRR (MICVDD)	PSRR	100mV (peak-peak) 217Hz		112		dB
		100mV (peak-peak) 10kHz		102		
PSRR (DCVDD)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		114		
PSRR (SPKVDD)	PSRR	100mV (peak-peak) 217Hz		111		dB
		100mV (peak-peak) 10kHz		103		

Test Conditions

DBVDD = CPVDD = AVDD = 1.8V, MICVDD = 2.2V, DCVDD = 1.2V, SPKVDD = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Earpiece Output (HPOUTL, HPOUTR, Mono Mode, R_L = 32Ω BTL, Short Circuit Protection disabled)						
Maximum output power	P_O	0.1% THD+N		97		mW
Signal to Noise Ratio (A-weighted)	SNR	Output signal = 1.41Vrms		115		dB
		Output signal = 1.41Vrms, eDRE software enabled		126		
Dynamic Range (A-weighted)	DR	-60dBFS input		115		dB
Total Harmonic Distortion	THD	P_O = 75mW		-88		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 75mW		-86		dB
Total Harmonic Distortion	THD	P_O = 5mW		-90		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 5mW		-88		dB
Output noise floor (A-weighted)		eDRE software enabled		0.7		μV_{RMS}
PSRR (DBVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		102		dB
		100mV (peak-peak) 10kHz		101		
PSRR (MICVDD)	PSRR	100mV (peak-peak) 217Hz		109		dB
		100mV (peak-peak) 10kHz		107		
PSRR (DCVDD)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		109		
PSRR (SPKVDD)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		105		
DAC to Earpiece Output (HPOUTL, HPOUTR, Mono Mode, R_L = 16Ω BTL, Short Circuit Protection disabled)						
Maximum output power	P_O	0.1% THD+N		110		mW
Signal to Noise Ratio (A-weighted)	SNR	Output signal = 1.41Vrms		115		dB
		Output signal = 1.41Vrms, eDRE software enabled		126		
Dynamic Range (A-weighted)	DR	-60dBFS input		115		dB
Total Harmonic Distortion	THD	P_O = 75mW		-85		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 75mW		-83		dB
Total Harmonic Distortion	THD	P_O = 5mW		-86		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 5mW		-85		dB
Output noise floor (A-weighted)		eDRE software enabled		0.7		μV_{RMS}
PSRR (DBVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		102		dB
		100mV (peak-peak) 10kHz		101		
PSRR (MICVDD)	PSRR	100mV (peak-peak) 217Hz		109		dB
		100mV (peak-peak) 10kHz		107		
PSRR (DCVDD)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		109		
PSRR (SPKVDD)	PSRR	100mV (peak-peak) 217Hz		110		dB
		100mV (peak-peak) 10kHz		105		

Test Conditions

DBVDD = CPVDD = AVDD = 1.8V, MICVDD = 2.2V, DCVDD = 1.2V, SPKVDD = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Speaker Output (SPKOUTP+SPKOUTN; Load = 8Ω, 22µH, BTL)						
Maximum output power	P_O	SPKVDD = 5.0V, 1% THD+N		1.4		W
		SPKVDD = 4.2V, 1% THD+N		1.0		
		SPKVDD = 3.6V, 1% THD+N		0.7		
Signal to Noise Ratio (A-weighted)	SNR	Output signal = 2.83Vrms	85	95		dB
Dynamic Range (A-weighted)	DR	-60dBFS input		95		dB
Total Harmonic Distortion	THD	P_O = 1.0W		-40		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 1.0W		-40		dB
Total Harmonic Distortion	THD	P_O = 0.5W		-70	-59	dB
Total Harmonic Distortion + Noise	THD+N	P_O = 0.5W		-69		dB
Output noise floor (A-weighted)				51	158	μV_{RMS}
PSRR (DBVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		76		dB
		100mV (peak-peak) 10kHz		65		
PSRR (MICVDD)	PSRR	100mV (peak-peak) 217Hz		81		dB
		100mV (peak-peak) 10kHz		82		
PSRR (DCVDD)	PSRR	100mV (peak-peak) 217Hz		84		dB
		100mV (peak-peak) 10kHz		88		
PSRR (SPKVDD)	PSRR	100mV (peak-peak) 217Hz		69		dB
		100mV (peak-peak) 10kHz		70		
DAC to Speaker Output (SPKOUTP+SPKOUTN; Load = 4Ω, 15µH, BTL)						
Maximum output power	P_O	SPKVDD = 5.0V, 1% THD+N		2.7		W
		SPKVDD = 4.2V, 1% THD+N		1.9		
		SPKVDD = 3.6V, 1% THD+N		1.4		
Signal to Noise Ratio (A-weighted)	SNR	Output signal = 2.83Vrms		95		dB
Dynamic Range (A-weighted)	DR	-60dBFS input		95		dB
Total Harmonic Distortion	THD	P_O = 1.0W		-70		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 1.0W		-69		dB
Total Harmonic Distortion	THD	P_O = 0.5W		-69		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 0.5W		-68		dB
Output noise floor (A-weighted)				51		μV_{RMS}
PSRR (DBVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		76		dB
		100mV (peak-peak) 10kHz		65		
PSRR (MICVDD)	PSRR	100mV (peak-peak) 217Hz		81		dB
		100mV (peak-peak) 10kHz		82		
PSRR (DCVDD)	PSRR	100mV (peak-peak) 217Hz		84		dB
		100mV (peak-peak) 10kHz		88		
PSRR (SPKVDD)	PSRR	100mV (peak-peak) 217Hz		69		dB
		100mV (peak-peak) 10kHz		70		

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input / Output (except DMICDATn and DMICCLKn)						
Input HIGH Level	V_{IH}	V_{DBVDD} = 1.71V to 1.98V	0.75 × V_{DBVDD}			V
		V_{DBVDD} = 2.25V to 2.75V	0.8 × V_{DBVDD}			
Input LOW Level	V_{IL}	V_{DBVDD} = 1.71V to 1.98V			0.3 × V_{DBVDD}	V
		V_{DBVDD} = 2.25V to 2.75V			0.25 × V_{DBVDD}	
Note that digital input pins should not be left unconnected or floating.						
Output HIGH Level (I_{OH} = 1mA)	V_{OH}	V_{DBVDD} = 1.71V to 1.98V	0.75 × V_{DBVDD}			V
		V_{DBVDD} = 2.25V to 2.75V	0.65 × V_{DBVDD}			
Output LOW Level (I_{OL} = 1mA)	V_{OL}	V_{DBVDD} = 1.71V to 1.98V			0.25 × V_{DBVDD}	V
		V_{DBVDD} = 2.25V to 2.75V			0.3 × V_{DBVDD}	
Input capacitance					5	pF
Input leakage			-10		10	µA
Pull-up / pull-down resistance (where applicable)			42		56	kΩ
Digital Microphone Input / Output (DMICDATn and DMICCLKn) **DMICDATn and DMICCLKn are each referenced to a selectable supply, V_{SUP}, according to the INn_DMIC_SUP registers**						
DMICDATn input HIGH Level	V_{IH}		0.65 × V_{SUP}			V
DMICDATn input LOW Level	V_{IL}				0.35 × V_{SUP}	V
DMICCLKn output HIGH Level	V_{OH}	I_{OH} = 1mA	0.8 × V_{SUP}			V
DMICCLKn output LOW Level	V_{OL}	I_{OL} = -1mA			0.2 × V_{SUP}	V
Input capacitance				25		pF
Input leakage			-1		1	µA
General Purpose Input / Output (GPIOn)						
Clock output frequency		GPIO pin configured as OPCLK or FLL output			50	MHz

Test Conditions

fs ≤ 48kHz

With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC Interpolation Filters						
Passband		+/- 0.05dB	0		0.454 fs	
		-6dB		0.5 fs		
Passband ripple					+/- 0.05	dB
Stopband			0.546 fs			
Stopband attenuation		f > 0.546 fs	85			dB
Group delay					1.5	ms

Test Conditions

DBVDD = CPVDD = AVDD = 1.8V, MICVDD = 2.2V, DCVDD = 1.2V, SPKVDD = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Bias (MICBIAS1, MICBIAS2) Note - No capacitor on MICBIASn Note - In regulator mode, it is required that V_{MICVDD} - $V_{MICBIAS}$ > 200mV						
Minimum Bias Voltage	$V_{MICBIAS}$	Regulator mode (MICBn_BYPASS=0) Load current ≤ 1.0mA		1.5		V
Maximum Bias Voltage				2.8		V
Bias Voltage output step size				0.1		V
Bias Voltage accuracy			-5%		+5%	V
Bias Current		Regulator mode (MICBn_BYPASS=0), V_{MICVDD} - $V_{MICBIAS}$ >200mV			2.4	mA
		Bypass mode (MICBn_BYPASS=1)			5.0	
Output Noise Density		Regulator mode (MICBn_BYPASS=0), MICBn_LVL = 4h, Load current = 1mA, Measured at 1kHz		40		nV/√Hz
Integrated noise voltage		Regulator mode (MICBn_BYPASS=0), MICBn_LVL = 4h, Load current = 1mA, 100Hz to 7kHz, A-weighted		2.5		µVrms
Power Supply Rejection Ratio (DBVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		100		dB
		100mV (peak-peak) 10kHz		80		
Power Supply Rejection Ratio (MICVDD)	PSRR	100mV (peak-peak) 217Hz		82		dB
		100mV (peak-peak) 10kHz		44		
Power Supply Rejection Ratio (DCVDD)	PSRR	100mV (peak-peak) 217Hz		102		dB
		100mV (peak-peak) 10kHz		94		
Power Supply Rejection Ratio (SPKVDD)	PSRR	100mV (peak-peak) 217Hz		99		dB
		100mV (peak-peak) 10kHz		92		
Load capacitance		Regulator mode (MICBn_BYPASS=0), MICBn_EXT_CAP=0			50	pF
		Regulator mode (MICBn_BYPASS=0), MICBn_EXT_CAP=1	1.8	4.7		µF
Output discharge resistance		MICBn_ENA=0, MICBn_DISCH=1		2		kΩ
Frequency Locked Loop (FLL1, FLL2)						
Output frequency			39		156	MHz
Lock Time		F_{REF} = 32kHz, F_{OUT} = 147.456MHz		10		ms
		F_{REF} = 12MHz, F_{OUT} = 147.456MHz		1		
RESET pin Input						
RESET input pulse width (To trigger a Hardware Reset, the RESET input must be asserted for longer than this duration)			1			µs

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

Device Reset Thresholds						
AVDD Reset Threshold	V_{AVDD}	V_{AVDD} rising			1.56	V
		V_{AVDD} falling	0.92		1.55	
DCVDD Reset Threshold	V_{DCVDD}	V_{DCVDD} rising			1.04	V
		V_{DCVDD} falling	0.49		0.64	
DBVDD Reset Threshold	V_{DBVDD}	V_{DBVDD} rising			1.54	V
		V_{DBVDD} falling	0.58		1.52	
Note that the reset thresholds are derived from simulations only, across all operational and process corners. Device performance is not assured outside the voltage ranges defined in the “Recommended Operating Conditions” section. Refer to this section for the CS47L24 power-up sequencing requirements.						

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum full scale output signal and the output with no input signal applied. (Note that this is measured without any mute function enabled.)
2. Total Harmonic Distortion (dB) – THD is the ratio of the RMS sum of the harmonic distortion products in the specified bandwidth (see note below) relative to the RMS amplitude of the fundamental (i.e., test frequency) output.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the ratio of the RMS sum of the harmonic distortion products plus noise in the specified bandwidth (see note below) relative to the RMS amplitude of the fundamental (i.e., test frequency) output.
4. Power Supply Rejection Ratio (dB) - PSRR is the ratio of a specified power supply variation relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.
5. Common Mode Rejection Ratio (dB) – CMRR is the ratio of a specified input signal (applied to both sides of a differential input), relative to the output signal that results from it.
6. Channel Separation (L/R) (dB) – left-to-right and right-to-left channel separation is the difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
7. Multi-Path Crosstalk (dB) – is the difference in level between the output of the active path and the measured signal level in the idle path at the test signal frequency. The active path is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the specified idle path.
8. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.
9. All performance measurements are specified with a 20kHz low pass ‘brick-wall’ filter and, where noted, an A-weighted filter. Failure to use these filters will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out-of-band noise.

TYPICAL PERFORMANCE

TYPICAL POWER CONSUMPTION

Test Conditions:

DCVDD = 1.2V, DBVDD = MICVDD = CPVDD = AVDD = 1.8V, SPKVDD = 4.2V,
SYSCLK = 12.288MHz (direct MCLK1 input), T_A = +25ºC.

OPERATING MODE	TEST CONDITIONS	SUPPLY CURRENT (1.2V)	SUPPLY CURRENT (1.8V)	SUPPLY CURRENT (4.2V)	TOTAL POWER
Music Playback to Headphone					
AIF1 to DAC to HPOUT (stereo), fs=48kHz, 24-bit I2S, Slave mode, Load = 32Ω, eDRE enabled.	Quiescent	1.54mA	0.75mA	0.0mA	3.19mW
	1kHz sine wave, P_O=10mW	1.59mA	38.2mA	0.0mA	70.6mW
Music Playback to Speaker					
AIF1 to DAC to SPKOUT, fs=48kHz, 24-bit I2S, Slave mode, Load = 8Ω, 22µH, BTL, eDRE enabled	Quiescent	1.26mA	0.08mA	0.00mA	1.65mW
	1kHz sine wave, P_O=700mW	1.28mA	1.03mA	197mA	833mW
Full Duplex Speakerphone Voice Call					
Digital Mic to AIF1 (out), AIF (in) to DAC to SPKOUT, fs=8kHz, 16-bit I2S, Slave mode. MEMS microphone powered from 1.8V MICBIAS output (regulator bypass mode enabled). DMICCLK = 3.072MHz. Speaker load = 8Ω, BTL.	Quiescent	0.77mA	1.28mA	1.29mA	8.63mW
Stereo Line Record					
Digital Mic to AIF1, fs=48kHz, 24-bit I2S, Slave mode. MEMS microphone powered from 1.8V MICBIAS output (regulator bypass mode enabled). DMICCLK = 3.072MHz.	1kHz sine wave, -1dBFS out	1.2mA	1.5mA	0.0mA	4.1mW
Off					
Leakage current only, all clocks disabled, thermal protection disabled, DSP firmware memory disabled.		0.04mA	0.00mA	0.00mA	0.06mW

TYPICAL SIGNAL LATENCY

OPERATING MODE	TEST CONDITIONS			LATENCY
	INPUT	OUTPUT	DIGITAL CORE	
AIF to DAC Stereo Path				
Digital input (AIFn) to analogue output (HPOUT). Signal is routed via the digital core ASRC function in the asynchronous test cases only.	fs = 48kHz	fs = 48kHz	Synchronous	358µs
	fs = 44.1kHz	fs = 44.1kHz	Synchronous	391µs
	fs = 16kHz	fs = 16kHz	Synchronous	720µs
	fs = 8kHz	fs = 8kHz	Synchronous	1428µs
	fs = 8kHz	fs = 44.1kHz	Asynchronous	1940µs
	fs = 16kHz	fs = 44.1kHz	Asynchronous	1240µs
DMIC to AIF Stereo Path				
Digital input (INn) to digital output (AIFn). Digital core High Pass filter included in signal path.	fs = 48kHz	fs = 48kHz	Synchronous	236µs
	fs = 44.1kHz	fs = 44.1kHz	Synchronous	260µs
	fs = 16kHz	fs = 16kHz	Synchronous	732µs
	fs = 8kHz	fs = 8kHz	Synchronous	1543µs

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK & FREQUENCY LOCKED LOOP (FLL)

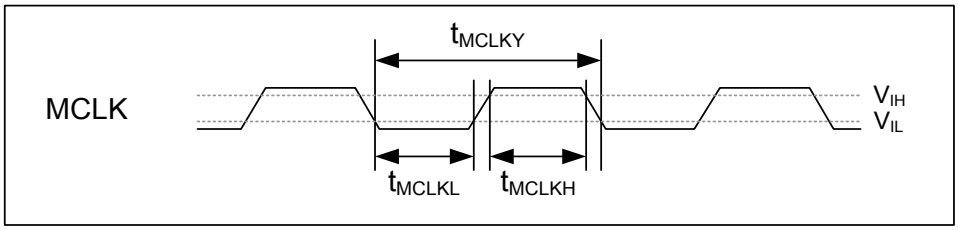


Figure 1 Master Clock Timing

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Master Clock Timing (MCLK1, MCLK2)					
MCLK cycle time	MCLK as input to FLL, FLLn_REFCLK_DIV=00	74			ns
	MCLK as input to FLL, FLLn_REFCLK_DIV=01	37			
	MCLK as input to FLL, FLLn_REFCLK_DIV=10	18			
	MCLK as input to FLL, FLLn_REFCLK_DIV=11	12.5			
	MCLK as direct SYSCLK or ASYNCCLK source	40			
MCLK duty cycle	MCLK as input to FLL	80:20		20:80	%
	MCLK as direct SYSCLK or ASYNCCLK source	60:40		40:60	
Frequency Locked Loops (FLL1, FLL2)					
FLL input frequency	FLLn_REFCLK_DIV=00	0.032		13.5	MHz
	FLLn_REFCLK_DIV=01	0.064		27	
	FLLn_REFCLK_DIV=10	0.128		54	
	FLLn_REFCLK_DIV=11	0.256		80	
FLL synchroniser input frequency	FLLn_SYNCCLK_DIV=00	0.032		13.5	MHz
	FLLn_SYNCCLK_DIV=01	0.064		27	
	FLLn_SYNCCLK_DIV=10	0.128		54	
	FLLn_SYNCCLK_DIV=11	0.256		80	

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal Clocking					
SYSCLK frequency	SYSCLK_FREQ=000, SYSCLK_FRAC=0	-1%	6.144	+1%	MHz
	SYSCLK_FREQ=000, SYSCLK_FRAC=1	-1%	5.6448	+1%	
	SYSCLK_FREQ=001, SYSCLK_FRAC=0	-1%	12.288	+1%	
	SYSCLK_FREQ=001, SYSCLK_FRAC=1	-1%	11.2896	+1%	
	SYSCLK_FREQ=010, SYSCLK_FRAC=0	-1%	24.576	+1%	
	SYSCLK_FREQ=010, SYSCLK_FRAC=1	-1%	22.5792	+1%	
	SYSCLK_FREQ=011, SYSCLK_FRAC=0	-1%	49.152	+1%	
	SYSCLK_FREQ=011, SYSCLK_FRAC=1	-1%	45.1584	+1%	
	SYSCLK_FREQ=100, SYSCLK_FRAC=0	-1%	73.728	+1%	
	SYSCLK_FREQ=100, SYSCLK_FRAC=1	-1%	67.7376	+1%	
	SYSCLK_FREQ=101, SYSCLK_FRAC=0	-1%	98.304	+1%	
	SYSCLK_FREQ=101, SYSCLK_FRAC=1	-1%	90.3168	+1%	
	SYSCLK_FREQ=110, SYSCLK_FRAC=0	-1%	147.456	+1%	
	SYSCLK_FREQ=110, SYSCLK_FRAC=1	-1%	135.4752	+1%	
ASYNCCLK frequency	ASYNC_CLK_FREQ=000	-1%	6.144	+1%	MHz
		-1%	5.6448	+1%	
	ASYNC_CLK_FREQ=001	-1%	12.288	+1%	
		-1%	11.2896	+1%	
	ASYNC_CLK_FREQ=010	-1%	24.576	+1%	
		-1%	22.5792	+1%	
	ASYNC_CLK_FREQ=011	-1%	49.152	+1%	
		-1%	45.1584	+1%	

Note:

When MCLK1 or MCLK2 is selected as a source for SYSCLK or ASYNCCLK (either directly or via one of the FLLs), the frequency must be within 1% of the applicable SYSCLK_FREQ or ASYNCCLK_FREQ register setting.

AUDIO INTERFACE TIMING

DIGITAL MICROPHONE (DMIC) INTERFACE TIMING

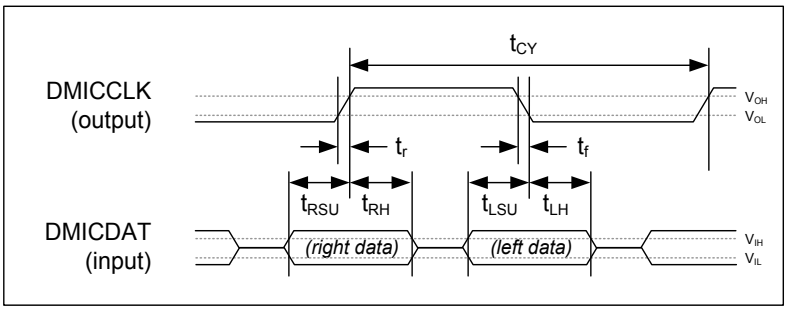


Figure 2 Digital Microphone Interface Timing

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital Microphone Interface Timing					
DMICCLKn cycle time	t_{CY}	160	163	1432	ns
DMICCLKn duty cycle		45		55	%
DMICCLKn rise/fall time (25pF load, 1.8V supply - see note)	t_r, t_f	5		30	ns
DMICDATn (Left) setup time to falling DMICCLK edge	t_{LSU}	15			ns
DMICDATn (Left) hold time from falling DMICCLK edge	t_{LH}	0			ns
DMICDATn (Right) setup time to rising DMICCLK edge	t_{RSU}	15			ns
DMICDATn (Right) hold time from rising DMICCLK edge	t_{RH}	0			ns

Notes:

DMICDATn and DMICCLKn are each referenced to a selectable supply, V_{SUP}.

The applicable supply is selected using the INn_DMIC_SUP registers.

DIGITAL AUDIO INTERFACE - MASTER MODE

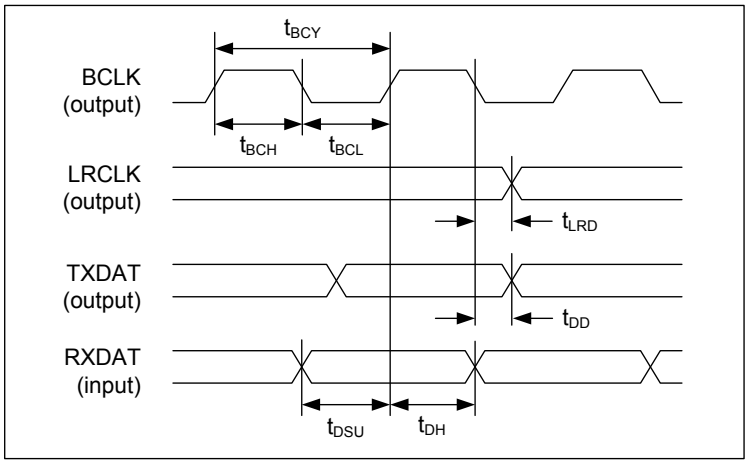


Figure 3 Audio Interface Timing - Master Mode

Note that BCLK and LRCLK outputs can be inverted if required; Figure 3 shows the default, non-inverted polarity.

Test Conditions

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.
C_{LOAD} = 15pF to 25pF (output pins). BCLK slew (10% to 90%) = 3.7ns to 5.6ns.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Master Mode					
AIFnBCLK cycle time	t_{BCY}	40			ns
AIFnBCLK pulse width high	t_{BCH}	18			ns
AIFnBCLK pulse width low	t_{BCL}	18			ns
AIFn[TX/RX]LRCLK propagation delay from BCLK falling edge	t_{LRD}	0		8.3	ns
AIFnTXDAT propagation delay from BCLK falling edge	t_{DD}	0		5	ns
AIFnRXDAT setup time to BCLK rising edge	t_{DSU}	9.2			ns
AIFnRXDAT hold time from BCLK rising edge	t_{DH}	0			ns
Audio Interface Timing - Master Mode, Slave LRCLK					
AIFnLRCLK setup time to BCLK rising edge	t_{LRSU}	14			ns
AIFnLRCLK hold time from BCLK rising edge	t_{LRH}	0			ns

Note:

The descriptions above assume non-inverted polarity of AIFnBCLK.

DIGITAL AUDIO INTERFACE - SLAVE MODE

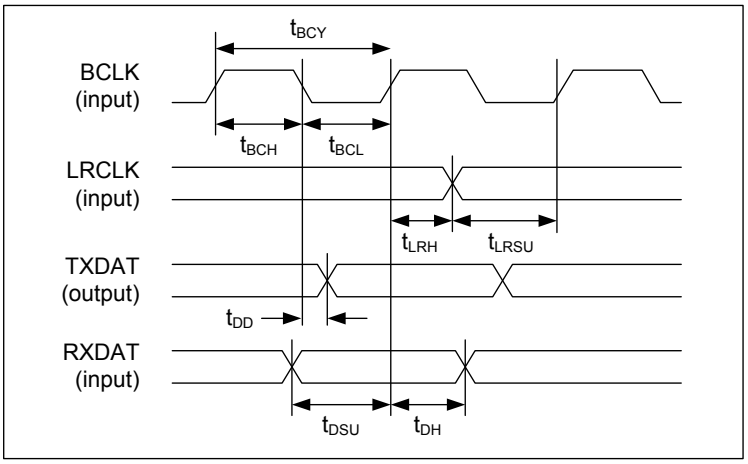


Figure 4 Audio Interface Timing - Slave Mode

Note that BCLK and LRCLK inputs can be inverted if required; Figure 4 shows the default, non-inverted polarity.

Test Conditions

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Slave Mode						
AIFnBCLK cycle time		t_{BCY}	40			ns
AIFnBCLK pulse width high	BCLK as direct SYSCLK or ASYNCCLK source	t_{BCH}	16			ns
	All other conditions		14			
AIFnBCLK pulse width low	BCLK as direct SYSCLK or ASYNCCLK source	t_{BCL}	16			ns
	All other conditions		14			
Audio Interface Timing - Slave Mode C_{LOAD} = 15pF (output pins). BCLK slew (10% to 90%) = 3ns.						
AIFn[TX/RX]LRCLK set-up time to BCLK rising edge		t_{LRSU}	7			ns
AIFn[TX/RX]LRCLK hold time from BCLK rising edge		t_{LRH}	0			ns
AIFnTXDAT propagation delay from BCLK falling edge		t_{DD}	0		10.7	ns
AIFnRXDAT set-up time to BCLK rising edge		t_{DSU}	2			ns
AIFnRXDAT hold time from BCLK rising edge		t_{DH}	0			ns
Audio Interface Timing - Slave Mode C_{LOAD} = 25pF (output pins). BCLK slew (10% to 90%) = 6ns.						
AIFn[TX/RX]LRCLK set-up time to BCLK rising edge		t_{LRSU}	7			ns
AIFn[TX/RX]LRCLK hold time from BCLK rising edge		t_{LRH}	0			ns
AIFnTXDAT propagation delay from BCLK falling edge		t_{DD}	0		12.7	ns
AIFnRXDAT set-up time to BCLK rising edge		t_{DSU}	2			ns
AIFnRXDAT hold time from BCLK rising edge		t_{DH}	0			ns
Audio Interface Timing - Slave Mode, Master LRCLK						
AIFn[TX/RX]LRCLK propagation delay from BCLK falling edge C_{LOAD} = 15pF (output pins). BCLK slew (10% to 90%) = 3ns.		t_{LRD}			14.8	ns
AIFn[TX/RX]LRCLK propagation delay from BCLK falling edge C_{LOAD} = 25pF (output pins). BCLK slew (10% to 90%) = 6ns.					15.9	

Notes:

The descriptions above assume non-inverted polarity of AIFnBCLK.

When AIFnBCLK or AIFnLRCLK is selected as a source for SYSCLK or ASYNCCLK (either directly or via one of the FLLs), the frequency must be within 1% of the applicable SYSCLK_FREQ or ASYNCCLK_FREQ register setting.

DIGITAL AUDIO INTERFACE - TDM MODE

When TDM operation is used on the AIFnTXDAT pins, it is important that two devices do not attempt to drive the AIFnTXDAT pin simultaneously. To support this requirement, the AIFnTXDAT pins can be configured to be tri-stated when not outputting data.

The timing of the AIFnTXDAT tri-stating at the start and end of the data transmission is described in Figure 5 below.

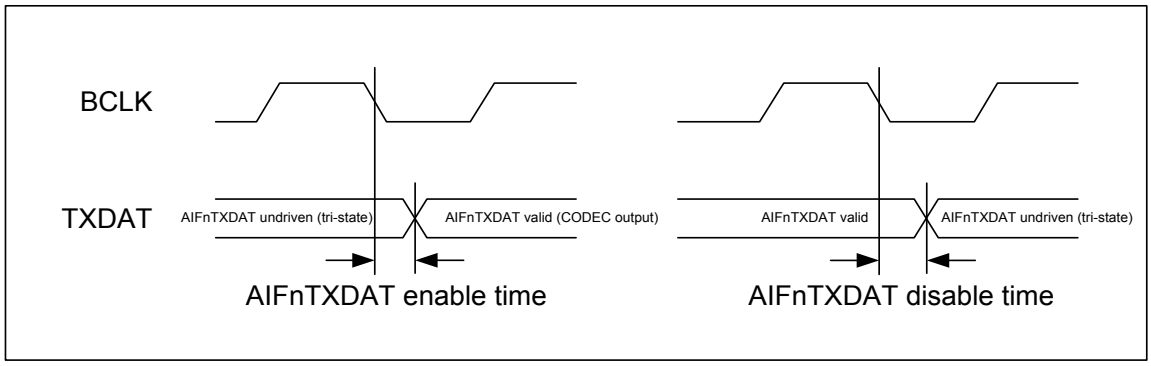


Figure 5 Audio Interface Timing - TDM Mode

Test Conditions

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.

PARAMETER	MIN	TYP	MAX	UNIT
TDM Timing - Master Mode C_{LOAD} (AIFnTXDAT) = 15pF to 25pF. BCLK slew (10% to 90%) = 3.7ns to 5.6ns.				
AIFnTXDAT enable time from BCLK falling edge	0			ns
AIFnTXDAT disable time from BCLK falling edge			6	ns
TDM Timing - Slave Mode C_{LOAD} (AIFnTXDAT) = 15pF). BCLK slew (10% to 90%) = 3ns.				
AIFnTXDAT enable time from BCLK falling edge	2			ns
AIFnTXDAT disable time from BCLK falling edge			10.7	ns
TDM Timing - Slave Mode C_{LOAD} (AIFnTXDAT) = 25pF). BCLK slew (10% to 90%) = 6ns				
AIFnTXDAT enable time from BCLK falling edge	2			ns
AIFnTXDAT disable time from BCLK falling edge			12.7	ns

CONTROL INTERFACE TIMING

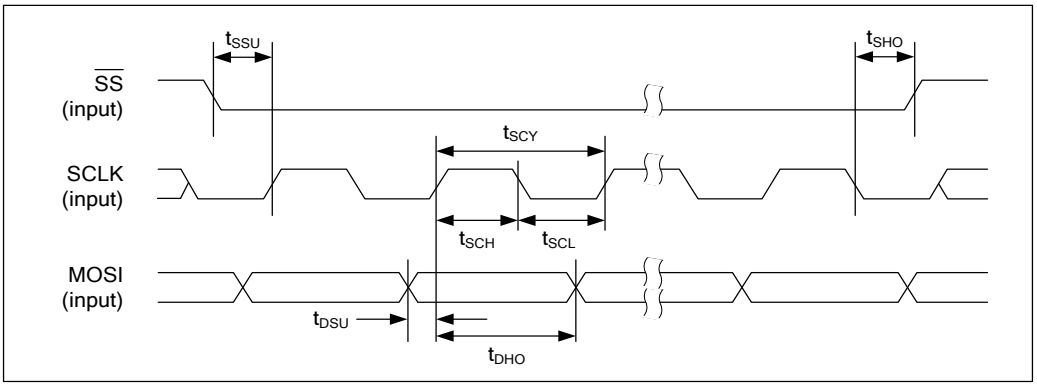


Figure 6 Control Interface Timing - 4-wire (SPI) Control Mode (Write Cycle)

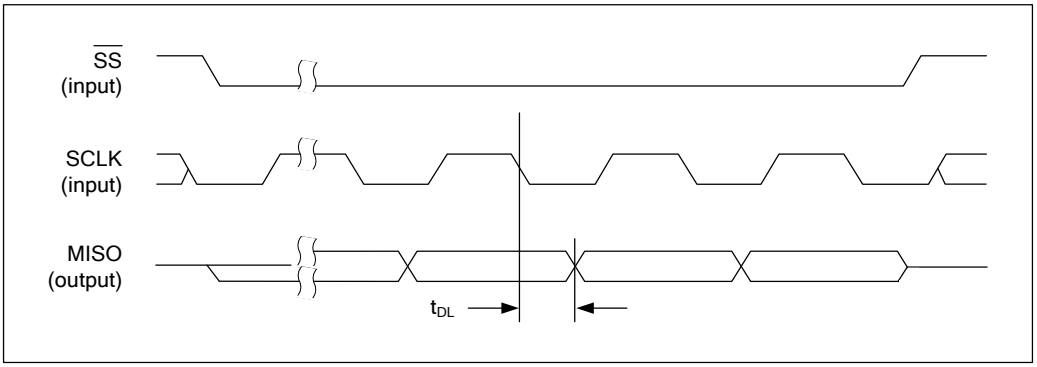


Figure 7 Control Interface Timing - 4-wire (SPI) Control Mode (Read Cycle)

Test Conditions

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
SS falling edge to SCLK rising edge		t_{SSU}	2.6			ns
SCLK falling edge to SS rising edge		t_{SHO}	0			ns
SCLK pulse cycle time	SYSCLK disabled (SYSCLK_ENA=0)	t_{SCY}	38.4			ns
	SYSCLK_ENA=1 and SYSCLK_FREQ = 000		76.8			
	SYSCLK_ENA=1 and SYSCLK_FREQ > 000		38.4			
SCLK pulse width low		t_{SCL}	15.3			ns
SCLK pulse width high		t_{SCH}	15.3			ns
MOSI to SCLK set-up time		t_{DSU}	1.5			ns
MOSI to SCLK hold time		t_{DHO}	1.7			ns
SCLK falling edge to MISO transition	SCLK slew (90% to 10%) = 5ns, C_{LOAD} (MISO) = 25pF	t_{DL}	0		11.9	ns

JTAG INTERFACE TIMING

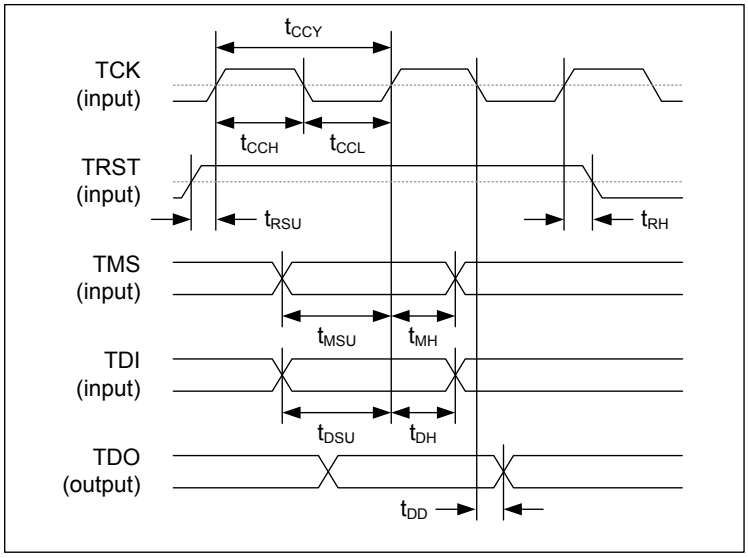


Figure 8 JTAG Interface Timing

Test Conditions

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.
C_{LOAD} = 25pF (output pins). TCK slew (20% to 80%) = 5ns.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
JTAG Interface Timing					
TCK cycle time	T_{CCY}	50			ns
TCK pulse width high	T_{CCH}	20			ns
TCK pulse width low	T_{CCL}	20			ns
TMS setup time to TCK rising edge	T_{MSU}	1			ns
TMS hold time from TCK rising edge	T_{MH}	2			ns
TDI setup time to TCK rising edge	T_{DSU}	1			ns
TDI hold time from TCK rising edge	T_{DH}	2			ns
TDO propagation delay from TCK falling edge	T_{DD}	0		17	ns
TRST setup time to TCK rising edge	T_{RSU}	3			ns
TRST hold time from TCK rising edge	T_{RH}	3			ns
TRST pulse width low		20			ns

DEVICE DESCRIPTION

INTRODUCTION

The CS47L24 is a highly integrated low-power audio hub for wearable technology and other portable devices. It provides flexible, high-performance audio interfacing for handheld devices in a small and cost-effective package. It provides exceptional levels of performance and signal processing capability, suitable for a wide variety of mobile and handheld devices.

The CS47L24 digital core provides an extensive programmable capability for signal processing algorithms. Cirrus Logic® Enhanced DRE processing (eDRE) software is included with the CS47L24; additional functions such as multi-mic noise suppression, acoustic echo cancellation (AEC), and voice recognition are also possible. A number of fixed-function processing capabilities are incorporated, enabling low/high pass filtering, parametric equalisation (EQ), and dynamic range control (DRC). Highly flexible digital mixing, including stereo full-duplex asynchronous sample rate conversion, provides use-case flexibility across a broad range of system architectures. A signal generator for controlling haptics vibe actuators is included.

The CS47L24 provides multiple digital audio interfaces, in order to provide independent and fully asynchronous connections to different processors (e.g., application processor, baseband processor and wireless transceiver).

A flexible clocking arrangement supports a wide variety of external clock references, including clocking derived from the digital audio interface. Two integrated Frequency Locked Loop (FLL) circuits provide additional flexibility.

Unused circuitry can be disabled under software control, in order to save power; low leakage currents enable extended standby/off time in portable battery-powered applications.

Comprehensive Interrupt (IRQ) logic and status readback are provided. Versatile input/output functionality on two GPIO pins is also provided.

HI-FI AUDIO CODEC

The CS47L24 is a high-performance low-power audio CODEC with a predominantly digital architecture. The audio CODEC is controlled directly via register access over an SPI control interface. The simple analogue architecture, combined with the integrated tone generator, enables simple device configuration and testing, minimising debug time and reducing software effort.

Two stereo microphone interfaces are provided, supporting up to four channels of digital microphone input. Interface clocking rates of 768kHz up to 3.072MHz support a wide range of low power vs. high performance operating requirements. The MICBIAS circuits can provide regulation of the digital microhone power rails; they can also be used as switches, enabling power gating of the external microphones.

The CS47L24 incorporates three DACs, providing a dedicated DAC for each analogue output channel. All of the mixing, equalisation, filtering, gain and other audio processing options can be configured independently for each channel; this allows each signal path to be individually tailored for the load characteristics and application requirements.

The analogue outputs comprise a 33mW (121dB SNR) stereo headphone amplifier with ground-referenced output, and a mono Class D speaker driver capable of delivering 2W into a 4Ω load. All outputs have integrated pop and click suppression features.

The headphone output drivers are powered from an integrated charge pump. The ground-referenced outputs deliver high quality, power efficient headphone playback, without any requirement for DC blocking capacitors. Ground loop feedback is incorporated, providing rejection of noise on the ground connections. A mono mode is available on the headphone outputs; this configures the drivers as differential (BTL) outputs, suitable for an earpiece or hearing aid coil.

The Class D speaker driver delivers excellent power efficiency. High PSRR, low leakage and optimised supply voltage ranges enable powering from switching regulators or directly from the battery. Battery current consumption is minimised across a wide variety of voice communication and multimedia playback use cases.

DIGITAL AUDIO CORE

The CS47L24 audio core is an entirely digital architecture, with audio effects available on all signal paths, regardless of the respective source or destination. The digital mixing desk allows different audio effects to be applied simultaneously on many independent paths, whilst also supporting a variety of sample rates concurrently. This helps support many new audio use-cases. Soft mute and un-mute control allows smooth transitions between use-cases without interrupting existing audio streams elsewhere.

The dual-core DSP system provides an extensive capability for programmable signal processing algorithms. Cirrus Logic's Enhanced DRE (eDRE) software is included with the CS47L24; additional software packages can be chosen according to the requirements of the target application. The CS47L24 can support many advanced audio processing features, including multi-mic noise suppression, acoustic echo cancellation (AEC), and voice recognition functions. User-programmed solutions can also be implemented.

Highly flexible digital mixing, including mixing between audio interfaces, is possible. The CS47L24 performs multi-channel full-duplex asynchronous sample rate conversion, providing use-case flexibility across a broad range of system architectures. Automatic sample rate detection is provided, enabling seamless wideband/narrowband voice call handover.

Dynamic Range Controller (DRC) functions are available for optimising audio signal levels. In playback modes, the DRC can be used to maximise loudness, while limiting the signal level to avoid distortion, clipping or battery droop, in particular for high-power output drivers such as speaker amplifiers. In record modes, the DRC assists in applications where the signal level is unpredictable.

The 5-band parametric equaliser (EQ) functions can be used to compensate for the frequency characteristics of the output transducers. EQ functions can be cascaded to provide additional frequency control. Programmable high-pass and low-pass filters are also available for general filtering applications such as removal of wind and other low-frequency noise.

DIGITAL INTERFACES

Three serial digital audio interfaces (AIFs) each support PCM, TDM and I2S data formats for compatibility with most industry-standard chipsets. AIF1 supports eight input/output channels; AIF2 supports six input/output channels; AIF3 supports two input/output channels. Bidirectional operation at sample rates up to 192kHz is supported.

Four digital PDM input channels are available (two stereo interfaces); these are typically used for digital microphones, powered from the integrated MICBIAS power supply regulators.

The CS47L24 is equipped with a SPI control interface, operating up to 26MHz. This is primarily used for control register access, but it can also support buffered audio data transfers associated with voice command software.

OTHER FEATURES

The CS47L24 incorporates two 1kHz tone generators which can be used for ‘beep’ functions through any of the audio signal paths. The phase relationship between the two generators is configurable, providing flexibility in creating differential signals, or for test scenarios.

A white noise generator is provided, which can be routed within the digital core. The noise generator can provide ‘comfort noise’ in cases where silence (digital mute) is not desirable.

Two Pulse Width Modulation (PWM) signal generators are incorporated. The duty cycle of each PWM signal can be modulated by an audio source, or can be set to a fixed value using a control register setting. The PWM signal generators can be output directly on a GPIO pin.

The CS47L24 provides 2 GPIO pins, supporting selectable input/output functions for interfacing, detection of external hardware, and to provide logic outputs to other devices. Comprehensive Interrupt (IRQ) functionality is also provided for monitoring internal and external event conditions.

A signal generator for controlling haptics devices is included, compatible with both Eccentric Rotating Mass (ERM) and Linear Resonant Actuator (LRA) haptic devices. The haptics signal generator is highly configurable, and can execute programmable drive event profiles, including reverse drive control. An external vibe actuator can be driven directly by the Class D speaker output.

The CS47L24 is powered from 1.8V and 1.2V external supplies. A separate supply (4.2V) is typically required for the Class D speaker driver. An integrated Charge Pump circuit generates positive and negative supply rails for the headphone drivers. Two MICBIAS regulators support powering and switching of external digital microphones.

System clocking can be derived from the MCLK1 or MCLK2 input pins. Alternatively, the audio interfaces (configured in Slave mode), can be used to provide a clock reference. Two integrated Frequency Locked Loop (FLL) circuits provide support for a wide range of clocking configurations, including the use of a 32kHz input clock reference.

INPUT SIGNAL PATH

The CS47L24 provides two stereo digital input paths, supporting up to four digital microphone inputs.

The digital input paths interface directly with external digital microphones; a separate microphone interface clock is provided for 2 separate stereo pairs of digital microphones. Digital delay can be applied to any of the digital input paths; this can be used for phase adjustment of any digital input, including directional control of multiple microphones.

Two microphone bias (MICBIAS) generators are available, which provide a low noise reference voltage, suitable for powering digital microphones.

Digital volume control is available on the microphone inputs, with programmable ramp control for smooth, glitch-free operation. The input signal paths and control registers are illustrated in Figure 9.

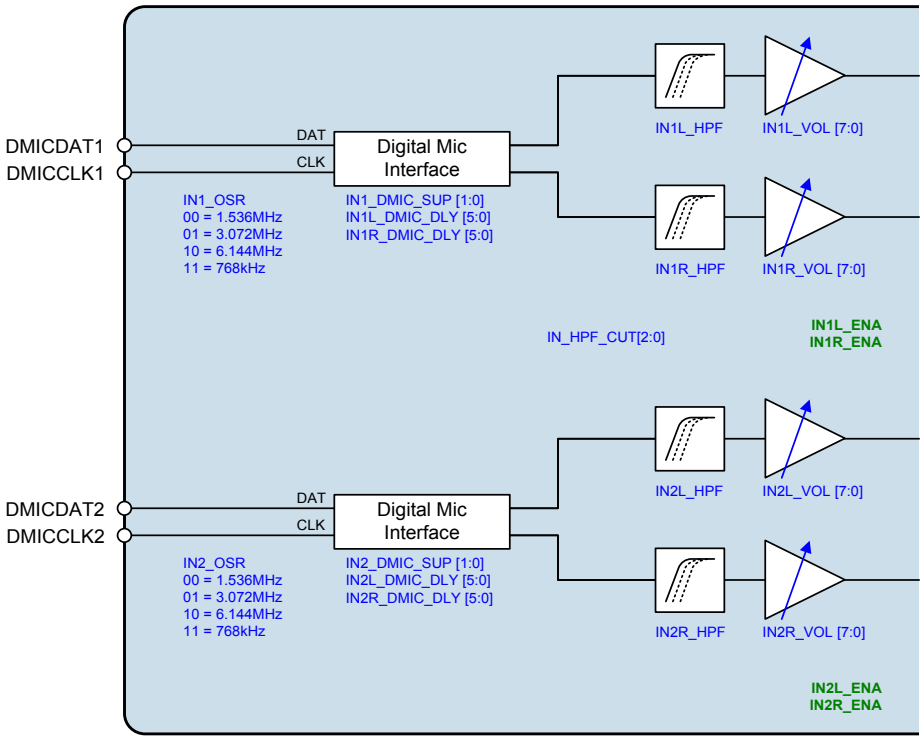


Figure 9 Input Signal Paths

DIGITAL MICROPHONE INPUT

Up to four digital microphones can be connected to the CS47L24. Two channels of audio data are multiplexed on the DMICDAT1 and DMICDAT2 pins. Each of these stereo interfaces is clocked using the respective DMICCLK1 or DMICCLK2 pin.

When digital microphone input is enabled, the CS47L24 outputs a clock signal on the applicable DMICCLK*n* pin(s). The DMICCLK*n* frequency is controlled by the respective IN*n*_OSR register, as described in Table 1. See Table 3 for details of the IN*n*_OSR registers.

Note that, if the 768kHz DMICCLKn frequency is selected for one or more of the digital microphone input paths, then the Input Path sample rate (all input paths) is valid in the range 8kHz to 16kHz only.

Note that the DMICCLK*n* frequencies noted in Table 1 assume that the SYSCLK frequency is a multiple of 6.144MHz (SYSCLK_FRAC=0). If the SYSCLK frequency is a multiple of 5.6448MHz (SYSCLK_FRAC=1), then the DMICCLK*n* frequencies will be scaled accordingly.

CONDITION	DMICCLKn FREQUENCY	SIGNAL PASSBAND
IN*n*_OSR = 00	1.536MHz	up to 20kHz
IN*n*_OSR = 01	3.072MHz	up to 20kHz
IN*n*_OSR = 10	6.144MHz	up to 96kHz
IN*n*_OSR = 11	768kHz	up to 8kHz

Table 1 DMICCLK Frequency

The microphone bias (MICBIAS) generators provide a configurable low noise output voltage, suitable for powering digital microphones. The MICBIAS generators are powered from the MICVDD supply. Powering the microphones directly from MICVDD (instead of MICBIASn) is also supported. However, the MICBIAS outputs are recommended, as these offer better noise performance and independent enable/disable control.

The voltage reference for each digital microphone interface is selectable, using the IN*n*_DMIC_SUP registers. Each interface may be referenced to MICVDD, or to the MICBIAS1 or MICBIAS2 levels.

A pair of digital microphones is connected as illustrated in Figure 10. The microphones must be configured to ensure that the Left mic transmits a data bit when DMICCLK is high, and the Right mic transmits a data bit when DMICCLK is low. The CS47L24 samples the digital microphone data at the end of each DMICCLK phase. Each microphone must tri-state its data output when the other microphone is transmitting.

Note that the CS47L24 provides integrated pull-down resistors on the DMICDAT1 and DMICDAT2 pins. This provides a flexible capability for interfacing with other devices.

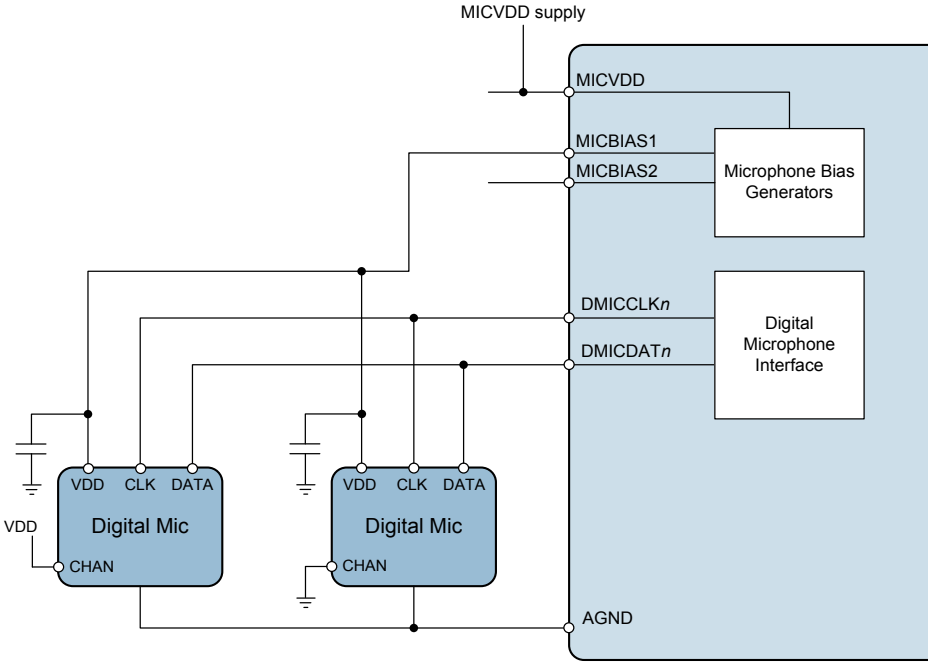


Figure 10 Digital Microphone Input

Two digital microphone channels are interleaved on DMICDAT*n*. The digital microphone interface timing is illustrated in Figure 11. Each microphone must tri-state its data output when the other microphone is transmitting.

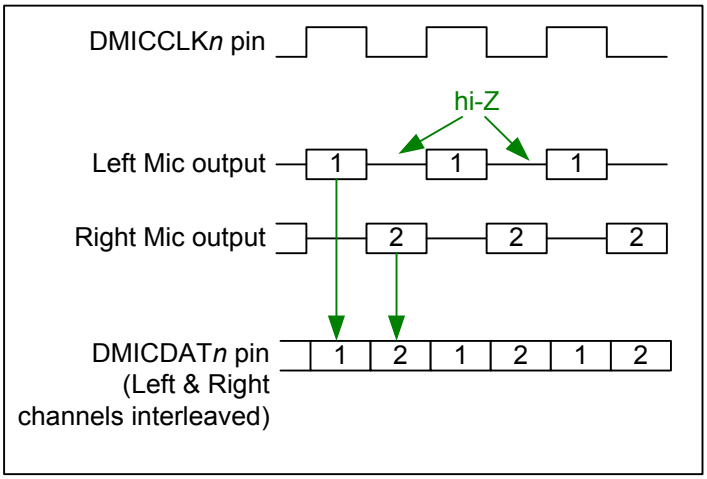


Figure 11 Digital Microphone Interface Timing

When digital microphone input is enabled, the CS47L24 outputs a clock signal on the applicable DMICCLK pin(s). The DMICCLK frequency is selectable, as described in Table 1.

Note that SYSCLK must be present and enabled when using the Digital Microphone inputs; see "Clocking and Sample Rates" for details of SYSCLK and the associated register control fields.

INPUT SIGNAL PATH ENABLE

The input signal paths are enabled using the register bits described in Table 2. The respective bit(s) must be enabled for digital input on the respective input path(s).

The input signal paths are muted by default. It is recommended that de-selecting the mute should be the final step of the path enable control sequence. Similarly, the mute should be selected as the first step of the path disable control sequence. The input signal path mute functions are controlled using the register bits described in Table 4.

The system clock, SYSCLK, must be configured and enabled before any audio path is enabled. The ASYNCCLK clock may also be required, depending on the path configuration. See "Clocking and Sample Rates" for details of the system clocks.

The CS47L24 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the input signal paths. If an attempt is made to enable an input signal path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error condition can be monitored using the GPIO and/or Interrupt functions. See "General Purpose Input / Output" and "Interrupts" for further details.

The status bits in Register R769 indicate the status of each of the input signal paths. If an Underclocked Error condition occurs, then these bits provide readback of which input signal path(s) have been successfully enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R768 (0300h) Input Enables	3	IN2L_ENA	0	Input Path 2 (Left) Enable 0 = Disabled 1 = Enabled
	2	IN2R_ENA	0	Input Path 2 (Right) Enable 0 = Disabled 1 = Enabled
	1	IN1L_ENA	0	Input Path 1 (Left) Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	IN1R_ENA	0	Input Path 1 (Right) Enable 0 = Disabled 1 = Enabled
R769 (0301h) Input Enables Status	3	IN2L_ENA_STS	0	Input Path 2 (Left) Enable Status 0 = Disabled 1 = Enabled
	2	IN2R_ENA_STS	0	Input Path 2 (Right) Enable Status 0 = Disabled 1 = Enabled
	1	IN1L_ENA_STS	0	Input Path 1 (Left) Enable Status 0 = Disabled 1 = Enabled
	0	IN1R_ENA_STS	0	Input Path 1 (Right) Enable Status 0 = Disabled 1 = Enabled

Table 2 Input Signal Path Enable

INPUT SIGNAL PATH SAMPLE RATE CONTROL

The input signal paths may be selected as input to the digital mixers or signal processing functions within the CS47L24 digital core. The sample rate for the input signal paths is configured using the IN_RATE register - see Table 21 within the "Digital Core" section.

Note that sample rate conversion is required when routing the input signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

INPUT SIGNAL PATH CONFIGURATION

A configurable high pass filter (HPF) is provided on the left and right channels of each input path. The applicable cut-off frequency is selected using the IN_HPF_CUT register. The filter can be enabled on each path independently using the IN*nx*_HPF bits.

The voltage reference for the digital microphone input/output pins is selectable using the IN*n*_DMIC_SUP registers - each interface may be referenced to MICVDD, or to the MICBIAS1 or MICBIAS2 levels.

The DMICCLKn frequency for each stereo input path can be configured using the INn_OSR register bits.

A digital delay may be applied to any of the digital microphone input channels. This feature can be used for phase adjustment of any digital input, including directional control of multiple microphones. The delay is controlled using the INnL_DMIC_DLY and INnR_DMIC_DLY registers.

The input signal paths are configured using the register bits described in Table 3.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R780 (030Ch) HPF Control	2:0	IN_HPF_CUT [2:0]	010	Input Path HPF Select Controls the cut-off frequency of the input path HPF circuits. 000 = 2.5Hz 001 = 5Hz 010 = 10Hz 011 = 20Hz 100 = 40Hz All other codes are Reserved
R784 (0310h) IN1L	15	IN1L_HPF	0	Input Path 1 (Left) HPF Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
Control	14:13	IN1_OSR [1:0]	01	Input Path 1 DMIC Oversample Rate Controls the DMICCLK1 frequency: 00 = 1.536MHz 01 = 3.072MHz 10 = 6.144MHz 11 = 768kHz When IN1_OSR=11, the Input Path sample rate (for all input paths) must be in the range 8kHz to 16kHz.
	12:11	IN1_DMIC_SUP [1:0]	00	Input Path 1 DMIC Reference Select (Sets the DMICDAT1 and DMICCLK1 logic levels) 00 = MICVDD 01 = MICBIAS1 10 = MICBIAS2 11 = Reserved
R786 (0312h) DMIC1L Control	5:0	IN1L_DMIC_DLY [5:0]	00h	Input Path 1 (Left) Digital Delay LSB = 1 sample, Range is 0 to 63. (Sample rate is controlled by IN1_OSR.)
R788 (0314h) IN1R Control	15	IN1R_HPF	0	Input Path 1 (Right) HPF Enable 0 = Disabled 1 = Enabled
R790 (0316h) DMIC1R Control	5:0	IN1R_DMIC_DLY [5:0]	00h	Input Path 1 (Right) Digital Delay LSB = 1 sample, Range is 0 to 63. (Sample rate is controlled by IN1_OSR.)
R792 (0318h) IN2L Control	15	IN2L_HPF	0	Input Path 2 (Left) HPF Enable 0 = Disabled 1 = Enabled
	14:13	IN2_OSR [1:0]	01	Input Path 2 DMIC Oversample Rate Controls the DMICCLK2 frequency: 00 = 1.536MHz 01 = 3.072MHz 10 = 6.144MHz 11 = 768kHz When IN2_OSR=11, the Input Path sample rate (for all input paths) must be in the range 8kHz to 16kHz.
	12:11	IN2_DMIC_SUP [1:0]	00	Input Path 2 DMIC Reference Select (Sets the DMICDAT2 and DMICCLK2 logic levels) 00 = MICVDD 01 = MICBIAS1 10 = MICBIAS2 11 = Reserved
R794 (031Ah) DMIC2L Control	5:0	IN2L_DMIC_DLY [5:0]	00h	Input Path 2 (Left) Digital Delay LSB = 1 sample, Range is 0 to 63. (Sample rate is controlled by IN2_OSR.)
R796 (031Ch) IN2R Control	15	IN2R_HPF	0	Input Path 2 (Right) HPF Enable 0 = Disabled 1 = Enabled
R798 (031Eh) DMIC2R Control	5:0	IN2R_DMIC_DLY [5:0]	00h	Input Path 2 (Right) Digital Delay LSB = 1 sample, Range is 0 to 63. (Sample rate is controlled by IN2_OSR.)

Table 3 Input Signal Path Configuration

INPUT SIGNAL PATH DIGITAL VOLUME CONTROL

A digital volume control is provided on each of the input signal paths, providing -64dB to +31.5dB gain control in 0.5dB steps. An independent mute control is also provided for each input signal path.

Whenever the gain or mute setting is changed, the signal path gain is ramped up or down to the new settings at a programmable rate. For increasing gain (or un-mute), the rate is controlled by the IN_VI_RAMP register. For decreasing gain (or mute), the rate is controlled by the IN_VD_RAMP register. Note that the IN_VI_RAMP and IN_VD_RAMP registers should not be changed while a volume ramp is in progress.

The IN_VU bits control the loading of the input signal path digital volume and mute controls. When IN_VU is set to 0, the digital volume and mute settings will be loaded into the respective control register, but will not actually change the signal path gain. The digital volume and mute settings on all of the input signal paths are updated when a 1 is written to IN_VU. This makes it possible to update the gain of multiple signal paths simultaneously.

Note that, although the digital volume control registers provide 0.5dB steps, the internal circuits provide signal gain adjustment in 0.125dB steps. This allows a very high degree of gain control, and smooth volume ramping under all operating conditions.

The 0dBFS level of the IN1/IN2 digital input paths is not equal to the 0dBFS level of the CS47L24 digital core. The maximum digital input signal level is -6dBFS (see “Electrical Characteristics”). Under 0dBFS gain conditions, a -6dBFS input signal corresponds to a 0dBFS input to the CS47L24 digital core functions.

The digital volume control register fields are described in Table 4 and Table 5.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R777 (0309h) Input Volume Ramp	6:4	IN_VD_RAMP [2:0]	010	Input Volume Decreasing Ramp Rate (seconds/6dB) 000 = 0ms 001 = 0.5ms 010 = 1ms 011 = 2ms 100 = 4ms 101 = 8ms 110 = 15ms 111 = 30ms This register should not be changed while a volume ramp is in progress.
	2:0	IN_VI_RAMP [2:0]	010	Input Volume Increasing Ramp Rate (seconds/6dB) 000 = 0ms 001 = 0.5ms 010 = 1ms 011 = 2ms 100 = 4ms 101 = 8ms 110 = 15ms 111 = 30ms This register should not be changed while a volume ramp is in progress.
R785 (0311h) ADC Digital Volume 1L	9	IN_VU		Input Signal Paths Volume and Mute Update Writing a 1 to this bit will cause the Input Signal Paths Volume and Mute settings to be updated simultaneously
	8	IN1L_MUTE	1	Input Path 1 (Left) Digital Mute 0 = Un-mute 1 = Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:0	IN1L_VOL [7:0]	80h	Input Path 1 (Left) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 5 for volume range)
R789 (0315h) ADC Digital Volume 1R	9	IN_VU		Input Signal Paths Volume and Mute Update Writing a 1 to this bit will cause the Input Signal Paths Volume and Mute settings to be updated simultaneously
	8	IN1R_MUTE	1	Input Path 1 (Right) Digital Mute 0 = Un-mute 1 = Mute
	7:0	IN1R_VOL [7:0]	80h	Input Path 1 (Right) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 5 for volume range)
R793 (0319h) ADC Digital Volume 2L	9	IN_VU		Input Signal Paths Volume and Mute Update Writing a 1 to this bit will cause the Input Signal Paths Volume and Mute settings to be updated simultaneously
	8	IN2L_MUTE	1	Input Path 2 (Left) Digital Mute 0 = Un-mute 1 = Mute
	7:0	IN2L_VOL [7:0]	80h	Input Path 2 (Left) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 5 for volume range)
R797 (031Dh) ADC Digital Volume 2R	9	IN_VU		Input Signal Paths Volume and Mute Update Writing a 1 to this bit will cause the Input Signal Paths Volume and Mute settings to be updated simultaneously
	8	IN2R_MUTE	1	Input Path 2 (Right) Digital Mute 0 = Un-mute 1 = Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:0	IN2R_VOL [7:0]	80h	Input Path 2 (Right) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 5 for volume range)

Table 4 Input Signal Path Digital Volume Control

Input Volume Register	Volume (dB)	Input Volume Register	Volume (dB)	Input Volume Register	Volume (dB)	Input Volume Register	Volume (dB)
00h	-64.0	40h	-32.0	80h	0.0	C0h	Reserved
01h	-63.5	41h	-31.5	81h	0.5	C1h	Reserved
02h	-63.0	42h	-31.0	82h	1.0	C2h	Reserved
03h	-62.5	43h	-30.5	83h	1.5	C3h	Reserved
04h	-62.0	44h	-30.0	84h	2.0	C4h	Reserved
05h	-61.5	45h	-29.5	85h	2.5	C5h	Reserved
06h	-61.0	46h	-29.0	86h	3.0	C6h	Reserved
07h	-60.5	47h	-28.5	87h	3.5	C7h	Reserved
08h	-60.0	48h	-28.0	88h	4.0	C8h	Reserved
09h	-59.5	49h	-27.5	89h	4.5	C9h	Reserved
0Ah	-59.0	4Ah	-27.0	8Ah	5.0	CAh	Reserved
0Bh	-58.5	4Bh	-26.5	8Bh	5.5	CBh	Reserved
0Ch	-58.0	4Ch	-26.0	8Ch	6.0	CCh	Reserved
0Dh	-57.5	4Dh	-25.5	8Dh	6.5	CDh	Reserved
0Eh	-57.0	4Eh	-25.0	8Eh	7.0	CEh	Reserved
0Fh	-56.5	4Fh	-24.5	8Fh	7.5	CFh	Reserved
10h	-56.0	50h	-24.0	90h	8.0	D0h	Reserved
11h	-55.5	51h	-23.5	91h	8.5	D1h	Reserved
12h	-55.0	52h	-23.0	92h	9.0	D2h	Reserved
13h	-54.5	53h	-22.5	93h	9.5	D3h	Reserved
14h	-54.0	54h	-22.0	94h	10.0	D4h	Reserved
15h	-53.5	55h	-21.5	95h	10.5	D5h	Reserved
16h	-53.0	56h	-21.0	96h	11.0	D6h	Reserved
17h	-52.5	57h	-20.5	97h	11.5	D7h	Reserved
18h	-52.0	58h	-20.0	98h	12.0	D8h	Reserved
19h	-51.5	59h	-19.5	99h	12.5	D9h	Reserved
1Ah	-51.0	5Ah	-19.0	9Ah	13.0	DAh	Reserved
1Bh	-50.5	5Bh	-18.5	9Bh	13.5	DBh	Reserved
1Ch	-50.0	5Ch	-18.0	9Ch	14.0	DCh	Reserved
1Dh	-49.5	5Dh	-17.5	9Dh	14.5	DDh	Reserved
1Eh	-49.0	5Eh	-17.0	9Eh	15.0	DEh	Reserved
1Fh	-48.5	5Fh	-16.5	9Fh	15.5	DFh	Reserved
20h	-48.0	60h	-16.0	A0h	16.0	E0h	Reserved
21h	-47.5	61h	-15.5	A1h	16.5	E1h	Reserved
22h	-47.0	62h	-15.0	A2h	17.0	E2h	Reserved
23h	-46.5	63h	-14.5	A3h	17.5	E3h	Reserved
24h	-46.0	64h	-14.0	A4h	18.0	E4h	Reserved
25h	-45.5	65h	-13.5	A5h	18.5	E5h	Reserved
26h	-45.0	66h	-13.0	A6h	19.0	E6h	Reserved
27h	-44.5	67h	-12.5	A7h	19.5	E7h	Reserved
28h	-44.0	68h	-12.0	A8h	20.0	E8h	Reserved
29h	-43.5	69h	-11.5	A9h	20.5	E9h	Reserved
2Ah	-43.0	6Ah	-11.0	AAh	21.0	EAh	Reserved
2Bh	-42.5	6Bh	-10.5	ABh	21.5	EBh	Reserved
2Ch	-42.0	6Ch	-10.0	ACh	22.0	ECh	Reserved
2Dh	-41.5	6Dh	-9.5	ADh	22.5	EDh	Reserved
2Eh	-41.0	6Eh	-9.0	AEh	23.0	EEh	Reserved
2Fh	-40.5	6Fh	-8.5	AFh	23.5	EFh	Reserved
30h	-40.0	70h	-8.0	B0h	24.0	F0h	Reserved
31h	-39.5	71h	-7.5	B1h	24.5	F1h	Reserved
32h	-39.0	72h	-7.0	B2h	25.0	F2h	Reserved
33h	-38.5	73h	-6.5	B3h	25.5	F3h	Reserved
34h	-38.0	74h	-6.0	B4h	26.0	F4h	Reserved
35h	-37.5	75h	-5.5	B5h	26.5	F5h	Reserved
36h	-37.0	76h	-5.0	B6h	27.0	F6h	Reserved
37h	-36.5	77h	-4.5	B7h	27.5	F7h	Reserved
38h	-36.0	78h	-4.0	B8h	28.0	F8h	Reserved
39h	-35.5	79h	-3.5	B9h	28.5	F9h	Reserved
3Ah	-35.0	7Ah	-3.0	BAh	29.0	FAh	Reserved
3Bh	-34.5	7Bh	-2.5	BBh	29.5	FBh	Reserved
3Ch	-34.0	7Ch	-2.0	BCh	30.0	FCh	Reserved
3Dh	-33.5	7Dh	-1.5	BDh	30.5	FDh	Reserved
3Eh	-33.0	7Eh	-1.0	BEh	31.0	FEh	Reserved
00.	-32.5	7Fh	-0.5	BFh	31.5	FFh	Reserved

Table 5 Input Signal Path Digital Volume Range

DIGITAL MICROPHONE INTERFACE PULL-DOWN

The CS47L24 provides integrated pull-down resistors on the DMICDAT1 and DMICDAT2 pins. This provides a flexible capability for interfacing with other devices.

Each of the pull-down resistors can be configured independently using the register bits described in Table 6. Note that, if the DMICDAT1 or DMICDAT2 digital microphone input paths are disabled, then the pull-down will be disabled on the respective pin.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3106 (0C22h) Misc Pad Ctrl 3	1	DMICDAT2_PD	0	DMICDAT2 Pull-Down Control 0 = Disabled 1 = Enabled
	0	DMICDAT1_PD	0	DMICDAT1 Pull-Down Control 0 = Disabled 1 = Enabled

Table 6 Digital Microphone Interface Pull-Down Control

DIGITAL CORE

The CS47L24 digital core provides extensive mixing and processing capabilities for multiple signal paths. The configuration is highly flexible, and virtually every conceivable input/output connection can be supported between the available processing blocks.

The digital core provides parametric equalisation (EQ) functions, dynamic range control (DRC), low-pass / high-pass filters (LHPF), and programmable DSP capability. The DSP can support functions such as wind noise, side-tone or other programmable filters, also dynamic range control and compression, or virtual surround sound and other audio enhancements.

The CS47L24 supports multiple signal paths through the digital core. Stereo full-duplex sample rate conversion is provided to allow digital audio to be routed between input (DMIC) paths, output (DAC) paths, and Digital Audio Interfaces (AIF1, AIF2 and AIF3) operating at different sample rates and/or referenced to asynchronous clock domains.

The DSP functions are highly programmable, using application-specific control sequences. It should be noted that the DSP configuration data is lost whenever the DCVDD power domain is removed; the DSP configuration data must be downloaded to the CS47L24 each time the device is powered up.

The procedure for configuring the CS47L24 DSP functions is tailored to each customer's application; please contact your local Cirrus Logic representative for more details.

The CS47L24 incorporates two 1kHz tone generators which can be used for 'beep' functions through any of the audio signal paths. A white noise generator is incorporated, to provide 'comfort noise' in cases where silence (digital mute) is not desirable.

A haptic signal generator is provided, for use with external haptic devices (e.g., mechanical vibration actuators). Two Pulse Width Modulation (PWM) signal generators are also provided; the PWM waveforms can be modulated by an audio source within the digital core, and can be output on a GPIO pin.

An overview of the digital core processing and mixing functions is provided in Figure 12. An overview of the external digital interface paths is provided in Figure 13.

The control registers associated with the digital core signal paths are shown in Figure 14 through to Figure 29. The full list of digital mixer control registers is provided in the "Register Map" section (Register R1600 through to R3000). Generic register definitions are provided in Table 7.

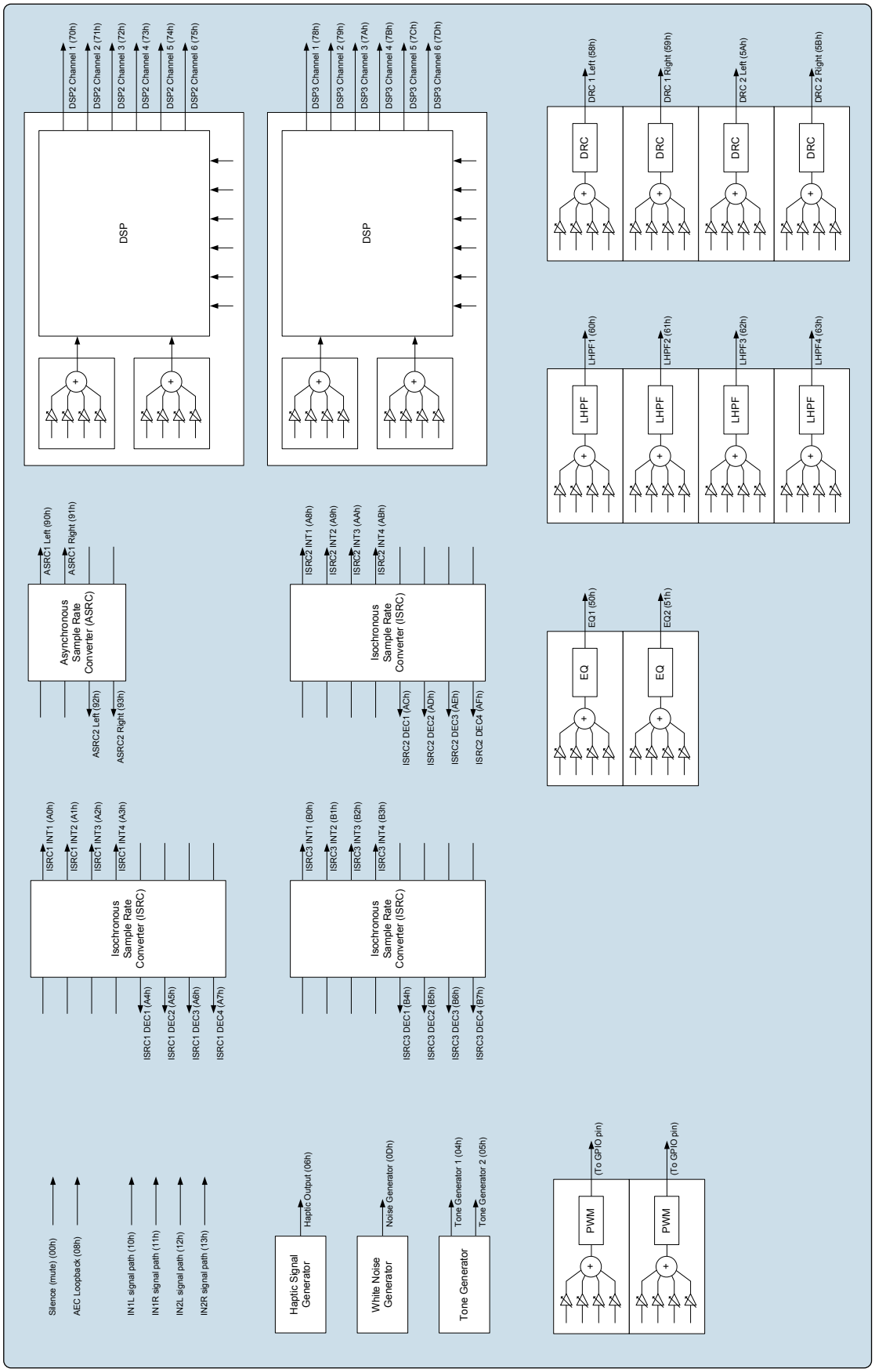


Figure 12 Digital Core - Internal Signal Processing

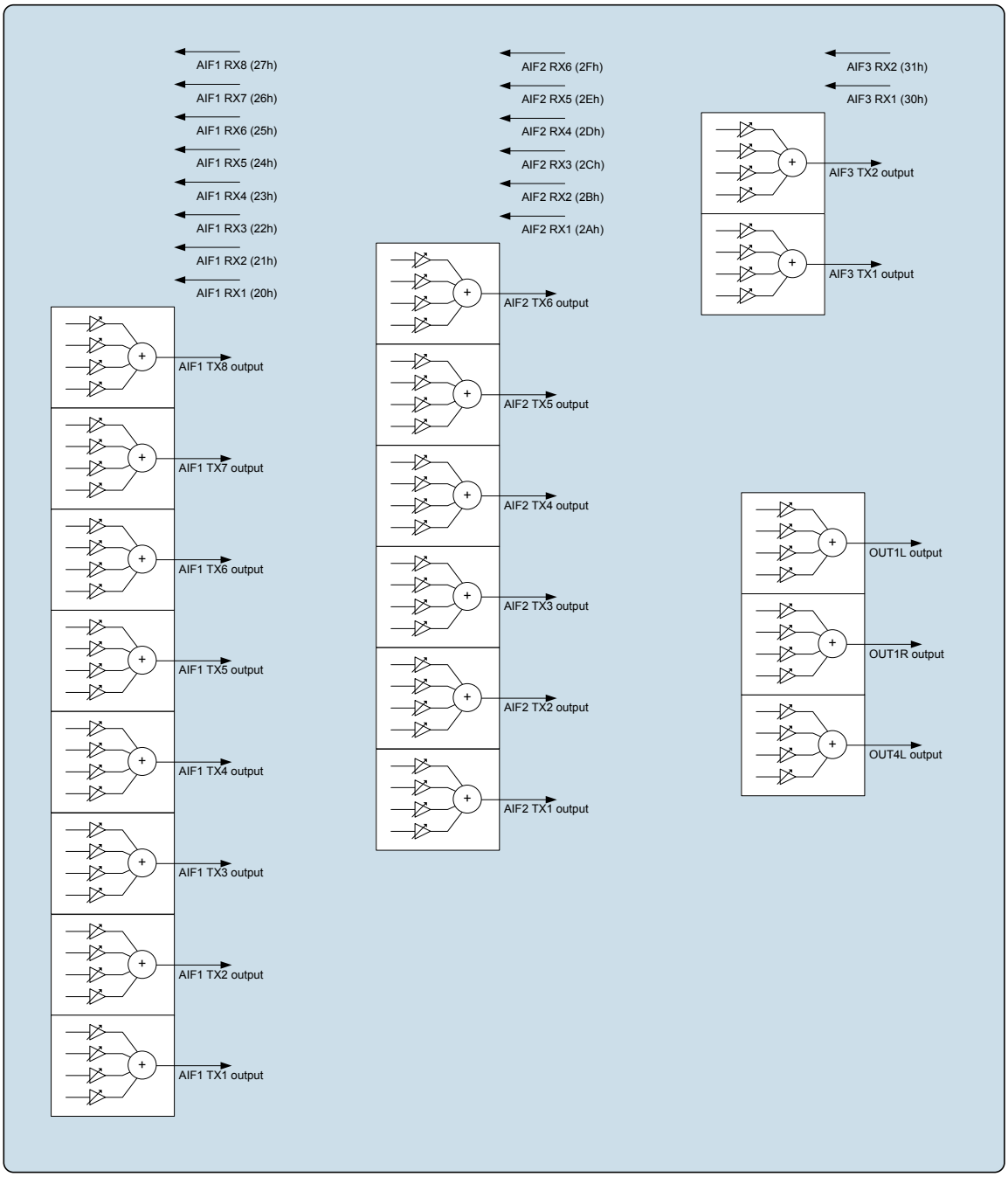


Figure 13 Digital Core - External Digital Interfaces

DIGITAL CORE MIXERS

The CS47L24 provides an extensive digital mixing capability. The digital core signal processing blocks and audio interface paths are illustrated in Figure 12 and Figure 13.

A 4-input digital mixer is associated with many of these functions, as illustrated. The digital mixer circuit is identical in each instance, providing up to 4 selectable input sources, with independent volume control on each input.

The control registers associated with the digital core signal paths are shown in Figure 14 through to Figure 29. The full list of digital mixer control registers is provided in the “Register Map” section (Register R1600 through to R3000).

Further description of the associated control registers is provided below. Generic register definitions are provided in Table 7.

The digital mixer input sources are selected using the associated *_SRC*n* registers; the volume control is implemented via the associated *_VOL*n* registers.

The ASRC, ISRC, and DSP Aux Input functions support selectable input sources, but do not incorporate any digital mixing. The respective input source (*_SRC*n*) registers are identical to those of the digital mixers.

The *_SRC*n* registers select the input source(s) for the respective mixer or signal processing block. Note that the selected input source(s) must be configured for the same sample rate as the block(s) to which they are connected. Sample rate conversion functions are available to support flexible interconnectivity - see “Asynchronous Sample Rate Converter (ASRC)” and “Isochronous Sample Rate Converter (ISRC)”.

A status bit associated with each of the configurable input sources provides readback for the respective signal path. If an Underclocked Error condition occurs, then these bits provide readback of which signal path(s) have been successfully enabled.

The generic register definition for the digital mixers is provided in Table 7.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1600 (0640h) to R3000 (0BB8h)	15	*_STSn Valid for every digital core function input (digital mixers, DSP Aux inputs, ASRC & ISRC inputs).	0	[Digital Core function] input *n* status 0 = Disabled 1 = Enabled
	7:1	*_VOLn Valid for every digital mixer input.	40h	[Digital Core mixer] input *n* volume -32dB to +16dB in 1dB steps 00h to 20h = -32dB 21h = -31dB 22h = -30dB ... (1dB steps) 40h = 0dB ... (1dB steps) 50h = +16dB 51h to 7Fh = +16dB
	7:0	*_SRCn Valid for every digital core function input (digital mixers, DSP Aux inputs, ASRC & ISRC inputs).	00h	[Digital Core function] input *n* source select 00h = Silence (mute) 04h = Tone generator 1 05h = Tone generator 2 06h = Haptic generator 08h = AEC loopback 0Dh = Noise generator 10h = IN1L signal path 11h = IN1R signal path 12h = IN2L signal path 13h = IN2R signal path 20h = AIF1 RX1 21h = AIF1 RX2 22h = AIF1 RX3 23h = AIF1 RX4 24h = AIF1 RX5 25h = AIF1 RX6 26h = AIF1 RX7 27h = AIF1 RX8 28h = AIF2 RX1 29h = AIF2 RX2 2Ah = AIF2 RX3 2Bh = AIF2 RX4 2Ch = AIF2 RX5 2Dh = AIF2 RX6

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
				30h = AIF3 RX1 31h = AIF3 RX2 50h = EQ1 51h = EQ2 58h = DRC1 Left 59h = DRC1 Right 5Ah = DRC2 Left 5Bh = DRC2 Right 60h = LHPF1 61h = LHPF2 62h = LHPF3 63h = LHPF4 70h = DSP2 channel 1 71h = DSP2 channel 2 72h = DSP2 channel 3 73h = DSP2 channel 4 74h = DSP2 channel 5 75h = DSP2 channel 6 78h = DSP3 channel 1 79h = DSP3 channel 2 7Ah = DSP3 channel 3 7Bh = DSP3 channel 4 7Ch = DSP3 channel 5 7Dh = DSP3 channel 6 90h = ASRC1 Left 91h = ASRC1 Right 92h = ASRC2 Left 93h = ASRC2 Right A0h = ISRC1 INT1 A1h = ISRC1 INT2 A2h = ISRC1 INT3 A3h = ISRC1 INT4 A4h = ISRC1 DEC1 A5h = ISRC1 DEC2 A6h = ISRC1 DEC3 A7h = ISRC1 DEC4 A8h = ISRC2 INT1 A9h = ISRC2 INT2 AAh = ISRC2 INT3 ABh = ISRC2 INT4 ACh = ISRC2 DEC1 ADh = ISRC2 DEC2 AEh = ISRC2 DEC3 AFh = ISRC2 DEC4 B0h = ISRC3 INT1 B1h = ISRC3 INT2 B2h = ISRC3 INT3 B3h = ISRC3 INT4 B4h = ISRC3 DEC1 B5h = ISRC3 DEC2 B6h = ISRC3 DEC3 B7h = ISRC3 DEC4

Table 7 Digital Core Mixer Control Registers

DIGITAL CORE INPUTS

The digital core comprises multiple input paths as illustrated in Figure 14. Any of these inputs may be selected as a source to the digital mixers or signal processing functions within the CS47L24 digital core.

Note that the outputs from other blocks within the Digital Core may also be selected as input to the digital mixers or signal processing functions within the CS47L24 digital core. Those input sources, which are not shown in Figure 14, are described separately in other sections of the “Digital Core” description.

The bracketed numbers in Figure 14, e.g.,”(10h)” indicate the corresponding *_SRC*n* register setting for selection of that signal as an input to another digital core function.

The sample rate for the input signal paths is configured using the applicable IN_RATE or AIFn_RATE register - see Table 21. Note that sample rate conversion is required when routing the input signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

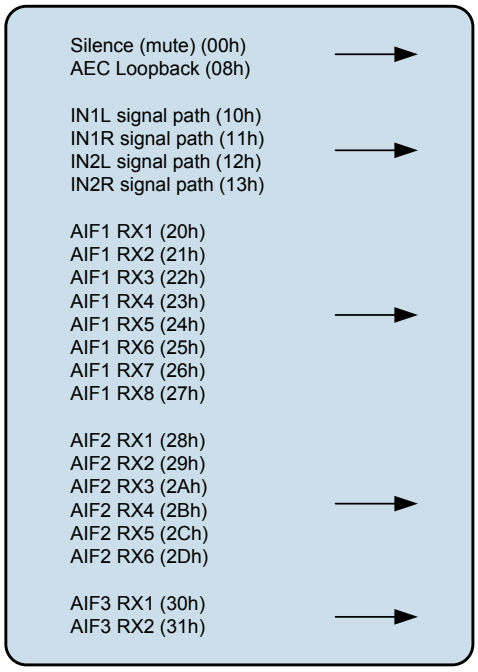


Figure 14 Digital Core Inputs

DIGITAL CORE OUTPUT MIXERS

The digital core comprises multiple output paths. The output paths associated with AIF1, AIF2 and AIF3 are illustrated in Figure 15. The output paths associated with OUT1 and OUT4L are illustrated in Figure 16. (Note that OUT2, OUT3, and OUT4R are not implemented on this device.)

A 4-input mixer is associated with each output. The 4 input sources are selectable in each case, and independent volume control is provided for each path.

The AIF1, AIF2 and AIF3 output mixer control registers (see Figure 15) are located at register addresses R1792 (700h) through to R1935 (78Fh). The OUT1 and OUT4L output mixer control registers (see Figure 16) are located at addresses R1664 (680h) through to R1719 (6BFh).

The full list of digital mixer control registers is provided in the “Register Map” section (Register R1600 through to R3000). Generic register definitions are provided in Table 7.

The *_SRC*n* registers select the input source(s) for the respective mixers. Note that the selected input source(s) must be configured for the same sample rate as the mixer to which they are connected. Sample rate conversion functions are available to support flexible interconnectivity - see “Asynchronous Sample Rate Converter (ASRC)” and “Isochronous Sample Rate Converter (ISRC)”.

The sample rate for the output signal paths is configured using the applicable OUT_RATE, or AIFn_RATE register - see Table 21. Note that sample rate conversion is required when routing the output signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

The CS47L24 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the output mixer paths. If an attempt is made to enable an output mixer path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error condition can be monitored using the GPIO and/or Interrupt functions. See “General Purpose Input / Output” and “Interrupts” for further details.

The status bits in Registers R1600 to R3000 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

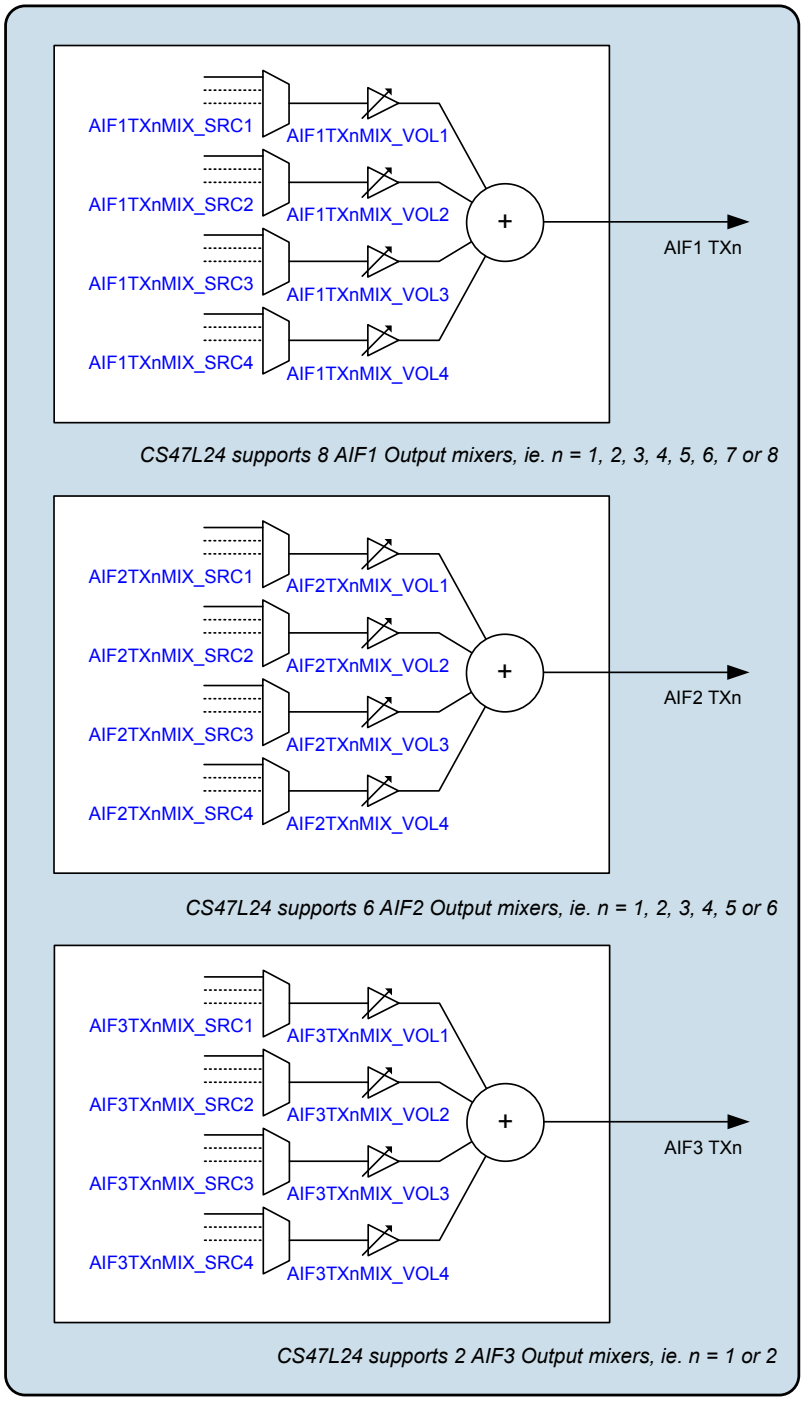


Figure 15 Digital Core AIF Outputs

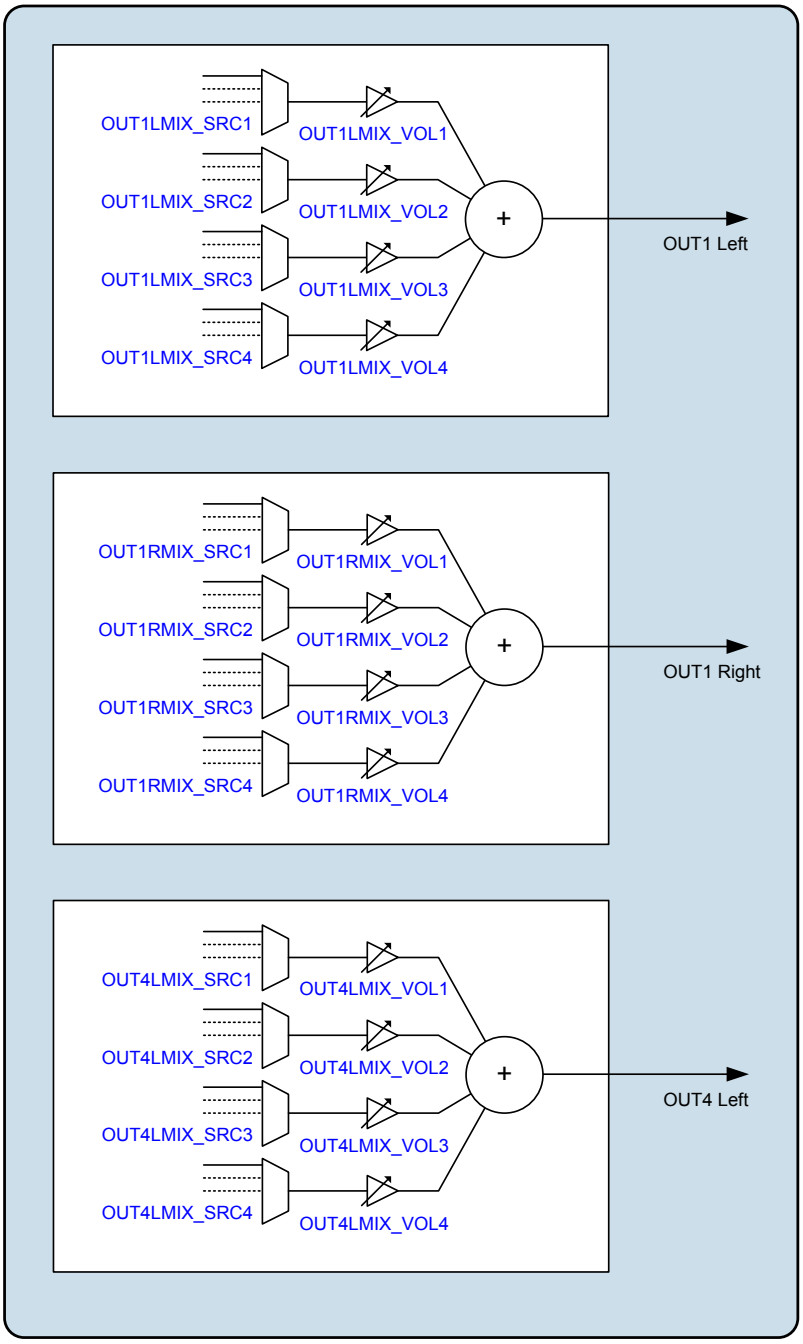


Figure 16 Digital Core OUT1 and OUT4L Outputs

5-BAND PARAMETRIC EQUALISER (EQ)

The digital core provides two EQ processing blocks as illustrated in Figure 17. A 4-input mixer is associated with each EQ. The 4 input sources are selectable in each case, and independent volume control is provided for each path. Each EQ block supports 1 output.

The EQ provides selective control of 5 frequency bands as described below.

The low frequency band (Band 1) filter can be configured either as a peak filter or a shelving filter. When configured as a shelving filter, it provides adjustable gain below the Band 1 cut-off frequency. As a peak filter, it provides adjustable gain within a defined frequency band that is centred on the Band 1 frequency.

The mid frequency bands (Band 2, Band 3, Band 4) filters are peak filters, which provide adjustable gain around the respective centre frequency.

The high frequency band (Band 5) filter is a shelving filter, which provides adjustable gain above the Band 5 cut-off frequency.

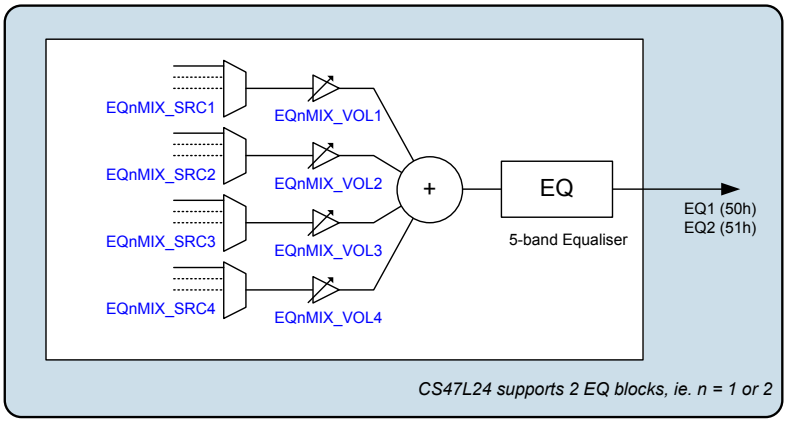


Figure 17 Digital Core EQ Blocks

The EQ1 and EQ2 mixer control registers (see Figure 17) are located at register addresses R2176 (880h) through to R2191 (88Eh).

The full list of digital mixer control registers is provided in the “Register Map” section (Register R1600 through to R3000). Generic register definitions are provided in Table 7.

The *_SRC*n* registers select the input source(s) for the respective EQ processing blocks. Note that the selected input source(s) must be configured for the same sample rate as the EQ to which they are connected. Sample rate conversion functions are available to support flexible interconnectivity - see “Asynchronous Sample Rate Converter (ASRC)” and “Isochronous Sample Rate Converter (ISRC)”.

The bracketed numbers in Figure 17, e.g.,”(50h)” indicate the corresponding *_SRC*n* register setting for selection of that signal as an input to another digital core function.

The sample rate for the EQ function is configured using the FX_RATE register - see Table 21. Note that the EQ, DRC and LHPF functions must all be configured for the same sample rate.

The EQ function supports audio sample rates in the range 8kHz to 192kHz. When the DRC is enabled, the maximum sample rate for the EQ, DRC and LHPF functions is 96kHz.

Sample rate conversion is required when routing the EQ signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

The control registers associated with the EQ functions are described in Table 9.

The cut-off or centre frequencies for the 5-band EQ are set using the coefficients held in the registers identified in Table 8. These coefficients are derived using tools provided in Cirrus Logic’s WISCE™ evaluation board control software; please contact your local Cirrus Logic representative for more details.

EQ	REGISTER ADDRESSES
EQ1	R3602 (0E10h) to R3620 (0E24h)
EQ2	R3624 (0E28h) to R3642 (0E3Ah)

Table 8 EQ Coefficient Registers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3585 (0E01h) FX_Ctrl2	15:4	FX_STS [11:0]	00h	LHPF, DRC, EQ Enable Status Indicates the status of each of the respective signal processing functions. [11] = Reserved [10] = Reserved [9] = EQ2 [8] = EQ1 [7] = DRC2 (Right) [6] = DRC2 (Left) [5] = DRC1 (Right) [4] = DRC1 (Left) [3] = LHPF4 [2] = LHPF3 [1] = LHPF2 [0] = LHPF1 Each bit is coded as: 0 = Disabled 1 = Enabled
R3600 (0E10h) EQ1_1	15:11	EQ1_B1_GAIN [4:0]	01100	EQ1 Band 1 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	10:6	EQ1_B2_GAIN [4:0]	01100	EQ1 Band 2 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	5:1	EQ1_B3_GAIN [4:0]	01100	EQ1 Band 3 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	0	EQ1_ENA	0	EQ1 Enable 0 = Disabled 1 = Enabled
R3601 (0E11h) EQ1_2	15:11	EQ1_B4_GAIN [4:0]	01100	EQ1 Band 4 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	10:6	EQ1_B5_GAIN [4:0]	01100	EQ1 Band 5 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	0	EQ1_B1_MODE	0	EQ1 Band 1 Mode 0 = Shelving filter 1 = Peak filter
R3602 (0E12h) to R3620 (E24h)	15:0	EQ1_B1_* EQ1_B2_* EQ1_B3_* EQ1_B4_* EQ1_B5_*		EQ1 Frequency Coefficients Refer to WISCE evaluation board control software for the deriviation of these field values.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3622 (0E26h) EQ2_1	15:11	EQ2_B1_GAIN [4:0]	01100	EQ2 Band 1 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	10:6	EQ2_B2_GAIN [4:0]	01100	EQ2 Band 2 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	5:1	EQ2_B3_GAIN [4:0]	01100	EQ2 Band 3 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	0	EQ2_ENA	0	EQ2 Enable 0 = Disabled 1 = Enabled
R3623 (0E27h) EQ2_2	15:11	EQ2_B4_GAIN [4:0]	01100	EQ2 Band 4 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	10:6	EQ2_B5_GAIN [4:0]	01100	EQ2 Band 5 Gain -12dB to +12dB in 1dB steps (see Table 10 for gain range)
	0	EQ2_B1_MODE	0	EQ2 Band 1 Mode 0 = Shelving filter 1 = Peak filter
R3624 (0E28h) to R3642 (E3Ah)	15:0	EQ2_B1_* EQ2_B2_* EQ2_B3_* EQ2_B4_* EQ2_B5_*		EQ2 Frequency Coefficients Refer to WISCE evaluation board control software for the deriviation of these field values.

Table 9 EQ Enable and Gain Control

EQ GAIN SETTING	GAIN (dB)
00000	-12
00001	-11
00010	-10
00011	-9
00100	-8
00101	-7
00110	-6
00111	-5
01000	-4
01001	-3
01010	-2
01011	-1
01100	0
01101	+1
01110	+2
01111	+3
10000	+4
10001	+5
10010	+6
10011	+7
10100	+8
10101	+9
10110	+10
10111	+11
11000	+12
11001 to 11111	Reserved

Table 10 EQ Gain Control Range

The CS47L24 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the commanded EQ and digital mixing functions. If an attempt is made to enable an EQ signal path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error can be monitored using the GPIO and/or Interrupt functions. See “General Purpose Input / Output” and “Interrupts” for further details.

The FX_STS field in Register R3585 indicates the status of each of the EQ, DRC and LHPF signal paths. If an Underclocked Error condition occurs, then this register provides readback of which EQ, DRC or LHPF signal path(s) have been successfully enabled.

The status bits in Registers R1600 to R3000 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

DYNAMIC RANGE CONTROL (DRC)

The digital core provides two stereo Dynamic Range Control (DRC) processing blocks as illustrated in Figure 18. A 4-input mixer is associated with each DRC input channel. The 4 input sources are selectable in each case, and independent volume control is provided for each path. The stereo DRC blocks support 2 outputs each.

The function of the DRC is to adjust the signal gain in conditions where the input amplitude is unknown or varies over a wide range, e.g. when recording from microphones built into a handheld system, or to restrict the dynamic range of an output signal path.

The DRC can apply Compression and Automatic Level Control to the signal path. It incorporates ‘anti-clip’ and ‘quick release’ features for handling transients in order to improve intelligibility in the presence of loud impulsive noises.

The DRC also incorporates a Noise Gate function, which provides additional attenuation of very low-level input signals. This means that the signal path is quiet when no signal is present, giving an improvement in background noise level under these conditions.

A Signal Detect function is provided within the DRC; this can be used to detect the presence of an audio signal, and used

to trigger other events. The Signal Detect function can be used as an Interrupt event, or as a GPIO output, or used to trigger the Control Write Sequencer (note - DRC1 only).

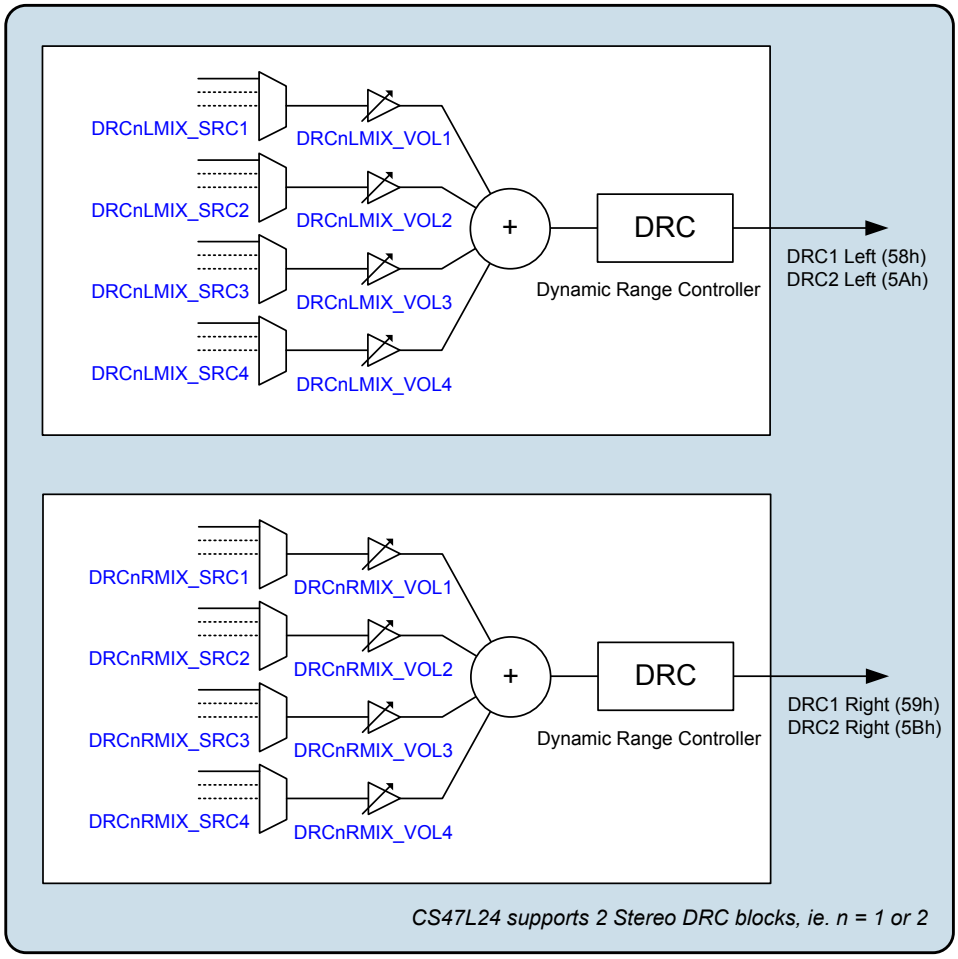


Figure 18 Dynamic Range Control (DRC) Block

The DRC1 and DRC2 mixer control registers (see Figure 18) are located at register addresses R2240 (8C0h) through to R2271 (08DFh).

The full list of digital mixer control registers is provided in the “Register Map” section (Register R1600 through to R3000). Generic register definitions are provided in Table 7.

The *_SRC*n* registers select the input source(s) for the respective DRC processing blocks. Note that the selected input source(s) must be configured for the same sample rate as the DRC to which they are connected. Sample rate conversion functions are available to support flexible interconnectivity - see “Asynchronous Sample Rate Converter (ASRC)” and “Isochronous Sample Rate Converter (ISRC)”.

The bracketed numbers in Figure 18, e.g.,”(58h)” indicate the corresponding *_SRC*n* register setting for selection of that signal as an input to another digital core function.

The sample rate for the DRC function is configured using the FX_RATE register - see Table 21. Note that the EQ, DRC and LHPF functions must all be configured for the same sample rate.

The DRC function supports audio sample rates in the range 8kHz to 96kHz. Higher sample rates (up to 192kHz) may be selected using FX_RATE, provided that the DRC function is disabled.

Sample rate conversion is required when routing the DRC signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

The DRC functions are enabled using the control registers described in Table 11.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3712 (0E80h) DRC1 ctrl1	1	DRC1L_ENA	0	DRC1 (Left) Enable 0 = Disabled 1 = Enabled
	0	DRC1R_ENA	0	DRC1 (Right) Enable 0 = Disabled 1 = Enabled
R3721 (0E89h) DRC2 ctrl1	1	DRC2L_ENA	0	DRC2 (Left) Enable 0 = Disabled 1 = Enabled
	0	DRC2R_ENA	0	DRC2 (Right) Enable 0 = Disabled 1 = Enabled

Table 11 DRC Enable

The following description of the DRC is applicable to each of the DRCs. The associated register control fields are described in Table 13 and Table 14 for DRC1 and DRC2 respectively.

DRC COMPRESSION / EXPANSION / LIMITING

The DRC supports two different compression regions, separated by a “Knee” at a specific input amplitude. In the region above the knee, the compression slope DRCn_HI_COMP applies; in the region below the knee, the compression slope DRCn_LO_COMP applies. (Note that ‘n’ identifies the applicable DRC 1 or 2.)

The DRC also supports a noise gate region, where low-level input signals are heavily attenuated. This function can be enabled or disabled according to the application requirements. The DRC response in this region is defined by the expansion slope DRCn_NG_EXP.

For additional attenuation of signals in the noise gate region, an additional “knee” can be defined (shown as “Knee2” in Figure 19). When this knee is enabled, this introduces an infinitely steep drop-off in the DRC response pattern between the DRCn_LO_COMP and DRCn_NG_EXP regions.

The overall DRC compression characteristic in “steady state” (i.e. where the input amplitude is near-constant) is illustrated in Figure 19.

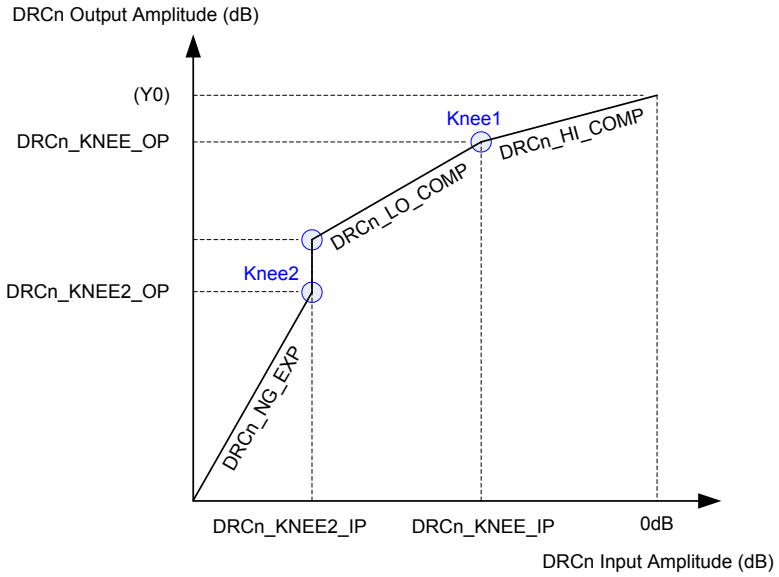


Figure 19 DRC Response Characteristic

The slope of the DRC response is determined by register fields DRCn_HI_COMP and DRCn_LO_COMP. A slope of 1 indicates constant gain in this region. A slope less than 1 represents compression (i.e. a change in input amplitude produces only a smaller change in output amplitude). A slope of 0 indicates that the target output amplitude is the same across a range of input amplitudes; this is infinite compression.

When the noise gate is enabled, the DRC response in this region is determined by the DRCn_NG_EXP register. A slope of 1 indicates constant gain in this region. A slope greater than 1 represents expansion (i.e., a change in input amplitude produces a larger change in output amplitude).

When the DRCn_KNEE2_OP knee is enabled ("Knee2" in Figure 19), this introduces the vertical line in the response pattern illustrated, resulting in infinitely steep attenuation at this point in the response.

The DRC parameters are listed in Table 12.

REF	PARAMETER	DESCRIPTION
1	DRCn_KNEE_IP	Input level at Knee1 (dB)
2	DRCn_KNEE_OP	Output level at Knee2 (dB)
3	DRCn_HI_COMP	Compression ratio above Knee1
4	DRCn_LO_COMP	Compression ratio below Knee1
5	DRCn_KNEE2_IP	Input level at Knee2 (dB)
6	DRCn_NG_EXP	Expansion ratio below Knee2
7	DRCn_KNEE2_OP	Output level at Knee2 (dB)

Table 12 DRC Response Parameters

The noise gate is enabled when the DRCn_NG_ENA register is set. When the noise gate is not enabled, parameters 5, 6, 7 above are ignored, and the DRCn_LO_COMP slope applies to all input signal levels below Knee1.

The DRCn_KNEE2_OP knee is enabled when the DRCn_KNEE2_OP_ENA register is set. When this bit is not set, then parameter 7 above is ignored, and the Knee2 position always coincides with the low end of the DRCn_LO_COMP region.

The "Knee1" point in Figure 19 is determined by register fields DRCn_KNEE_IP and DRCn_KNEE_OP.

Parameter Y0, the output level for a 0dB input, is not specified directly, but can be calculated from the other parameters, using the equation:

Y0 = DRCn_KNEE_OP - (DRCn_KNEE_IP x DRCn_HI_COMP)

GAIN LIMITS

The minimum and maximum gain applied by the DRC is set by register fields DRCn_MINGAIN, DRCn_MAXGAIN and DRCn_NG_MINGAIN. These limits can be used to alter the DRC response from that illustrated in Figure 19. If the range between maximum and minimum gain is reduced, then the extent of the dynamic range control is reduced.

The minimum gain in the Compression regions of the DRC response is set by DRCn_MINGAIN. The mimimum gain in the Noise Gate region is set by DRCn_NG_MINGAIN. The minimum gain limit prevents excessive attenuation of the signal path.

The maximum gain limit set by DRCn_MAXGAIN prevents quiet signals (or silence) from being excessively amplified.

DYNAMIC CHARACTERISTICS

The dynamic behaviour determines how quickly the DRC responds to changing signal levels. Note that the DRC responds to the average (RMS) signal amplitude over a period of time.

The DRCn_ATK determines how quickly the DRC gain decreases when the signal amplitude is high. The DRCn_DCY determines how quickly the DRC gain increases when the signal amplitude is low.

These register fields are described in Table 13. Note that the register defaults are suitable for general purpose microphone use.

ANTI-CLIP CONTROL

The DRC includes an Anti-Clip feature to avoid signal clipping when the input amplitude rises very quickly. This feature uses a feed-forward technique for early detection of a rising signal level. Signal clipping is avoided by dynamically increasing the gain attack rate when required. The Anti-Clip feature is enabled using the DRCn_ANTICLIP bit.

Note that the feed-forward processing increases the latency in the input signal path.

Note that the Anti-Clip feature operates entirely in the digital domain. It cannot be used to prevent signal clipping in the analogue domain nor in the source signal. Analogue clipping can only be prevented by reducing the analogue signal gain or by adjusting the source signal.

QUICK RELEASE CONTROL

The DRC includes a Quick-Release feature to handle short transient peaks that are not related to the intended source signal. For example, in handheld microphone recording, transient signal peaks sometimes occur due to user handling, key presses or accidental tapping against the microphone. The Quick Release feature ensures that these transients do not cause the intended signal to be masked by the longer time constant of DRCn_DCY.

The Quick-Release feature is enabled by setting the DRCn_QR bit. When this bit is enabled, the DRC measures the crest factor (peak to RMS ratio) of the input signal. A high crest factor is indicative of a transient peak that may not be related to the intended source signal. If the crest factor exceeds the level set by DRCn_QR_THR, then the normal decay rate (DRCn_DCY) is ignored and a faster decay rate (DRCn_QR_DCY) is used instead.

SIGNAL ACTIVITY DETECT

The DRC incorporates a configurable signal detect function, allowing the signal level at the DRC input to be monitored and to be used to trigger other events. This can be used to detect the presence of a microphone signal on an digital microphone channel, or can be used to detect an audio signal received over the digital audio interface.

The DRC Signal Detect function is enabled by setting DRCn_SIG_DET register bit. (Note that the respective DRCn must also be enabled.) The detection threshold is either a Peak level (Crest Factor) or an RMS level, depending on the DRCn_SIG_DET_MODE register bit. When Peak level is selected, the threshold is determined by DRCn_SIG_DET_PK, which defines the applicable Crest Factor (Peak to RMS ratio) threshold. If RMS level is selected, then the threshold is set using DRCn_SIG_DET_RMS.

The DRC Signal Detect function is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see “Interrupts”.

The DRC Signal Detect signal can be output directly on a GPIO pin as an external indication of the Signal Detection. See “General Purpose Input / Output” to configure a GPIO pin for this function.

The Control Write Sequencer can be triggered by the DRC1 Signal Detect function. This is enabled using the DRC1_WSEQ_SIG_DET_ENA register bit. See “Control Write Sequencer” for further details.

Note that signal detection is supported on DRC1 and DRC2, but the triggering of the Control Write Sequencer is available on DRC1 only.

GPIO OUTPUTS FROM DRC

The Dynamic Range Control (DRC) circuit provides a number of status outputs, which can be output directly on a GPIO pin as an external indication of the DRC Status. See “General Purpose Input / Output” to configure a GPIO pin for these functions.

Each of the DRC status outputs is described below.

The DRC Signal Detect flag indicates that a signal is present on the respective signal path. The threshold level for signal detection is configurable using the register fields are described in Table 13 and Table 14.

The DRC Anti-Clip flag indicates that the DRC Anti-Clip function has been triggered. In this event, the DRC gain is decreasing in response to a rising signal level. The flag is asserted until the DRC gain stablises.

The DRC Decay flag indicates that the DRC gain is increasing in response to a low level signal input. The flag is asserted until the DRC gain stabilises.

The DRC Noise Gate flag indicates that the DRC Noise Gate function has been triggered, indicating that an idle condition has been detected in the signal path.

The DRC Quick Release flag indicates that the DRC Quick Release function has been triggered. In this event, the DRC gain is increasing rapidly following detection of a short transient peak. The flag is asserted until the DRC gain stabilises.

DRC REGISTER CONTROLS

The DRC control registers are described in Table 13 and Table 14 for DRC1 and DRC2 respectively.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3585 (0E01h) FX_Ctrl2	15:4	FX_STS [11:0]	00h	LHPF, DRC, EQ Enable Status Indicates the status of each of the respective signal processing functions. [11] = Reserved [10] = Reserved [9] = EQ2 [8] = EQ1 [7] = DRC2 (Right) [6] = DRC2 (Left) [5] = DRC1 (Right) [4] = DRC1 (Left) [3] = LHPF4 [2] = LHPF3 [1] = LHPF2 [0] = LHPF1 Each bit is coded as: 0 = Disabled 1 = Enabled
R3712 (0E80h) DRC1 ctrl1	15:11	DRC1_SIG_DET_RMS [4:0]	00h	DRC1 Signal Detect RMS Threshold. This is the RMS signal level for signal detect to be indicated when DRC1_SIG_DET_MODE=1. 00h = -30dB 01h = -31.5dB …. (1.5dB steps) 1Eh = -75dB 1Fh = -76.5dB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	10:9	DRC1_SIG_DET_PK [1:0]	00	DRC1 Signal Detect Peak Threshold. This is the Peak/RMS ratio, or Crest Factor, level for signal detect to be indicated when DRC1_SIG_DET_MODE=0. 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB
	8	DRC1_NG_ENA	0	DRC1 Noise Gate Enable 0 = Disabled 1 = Enabled
	7	DRC1_SIG_DET_MODE	0	DRC1 Signal Detect Mode 0 = Peak threshold mode 1 = RMS threshold mode
	6	DRC1_SIG_DET	0	DRC1 Signal Detect Enable 0 = Disabled 1 = Enabled
	5	DRC1_KNEE2_OP_ENA	0	DRC1 KNEE2_OP Enable 0 = Disabled 1 = Enabled
	4	DRC1_QR	1	DRC1 Quick-release Enable 0 = Disabled 1 = Enabled
	3	DRC1_ANTICLIP	1	DRC1 Anti-clip Enable 0 = Disabled 1 = Enabled
	2	DRC1_WSEQ_SIG_DET_ENA	0	DRC1 Signal Detect Write Sequencer Select 0 = Disabled 1 = Enabled
R3713 (0E81h) DRC1 ctrl2	12:9	DRC1_ATK [3:0]	0100	DRC1 Gain attack rate (seconds/6dB) 0000 = Reserved 0001 = 181us 0010 = 363us 0011 = 726us 0100 = 1.45ms 0101 = 2.9ms 0110 = 5.8ms 0111 = 11.6ms 1000 = 23.2ms 1001 = 46.4ms 1010 = 92.8ms 1011 = 185.6ms 1100 to 1111 = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	8:5	DRC1_DCY [3:0]	1001	DRC1 Gain decay rate (seconds/6dB) 0000 = 1.45ms 0001 = 2.9ms 0010 = 5.8ms 0011 = 11.6ms 0100 = 23.25ms 0101 = 46.5ms 0110 = 93ms 0111 = 186ms 1000 = 372ms 1001 = 743ms 1010 = 1.49s 1011 = 2.97s 1100 to1111 = Reserved
	4:2	DRC1_MINGAIN [2:0]	100	DRC1 Minimum gain to attenuate audio signals 000 = 0dB 001 = -12dB 010 = -18dB 011 = -24dB 100 = -36dB 101 = Reserved 11X = Reserved
	1:0	DRC1_MAXGAIN [1:0]	11	DRC1 Maximum gain to boost audio signals (dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 36dB
R3714 (0E82h) DRC1 ctrl3	15:12	DRC1_NG_MINGAIN [3:0]	0000	DRC1 Minimum gain to attenuate audio signals when the noise gate is active. 0000 = -36dB 0001 = -30dB 0010 = -24dB 0011 = -18dB 0100 = -12dB 0101 = -6dB 0110 = 0dB 0111 = 6dB 1000 = 12dB 1001 = 18dB 1010 = 24dB 1011 = 30dB 1100 = 36dB 1101 to 1111 = Reserved
	11:10	DRC1_NG_EXP [1:0]	00	DRC1 Noise Gate slope 00 = 1 (no expansion) 01 = 2 10 = 4 11 = 8
	9:8	DRC1_QR_THR [1:0]	00	DRC1 Quick-release threshold (crest factor in dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:6	DRC1_QR_DCY [1:0]	00	DRC1 Quick-release decay rate (seconds/6dB) 00 = 0.725ms 01 = 1.45ms 10 = 5.8ms 11 = Reserved
	5:3	DRC1_HI_COMP [2:0]	011	DRC1 Compressor slope (upper region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 0 110 = Reserved 111 = Reserved
	2:0	DRC1_LO_COMP [2:0]	000	DRC1 Compressor slope (lower region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 0 101 = Reserved 11X = Reserved
R3715 (0E83h) DRC1 ctrl4	10:5	DRC1_KNEE_IP [5:0]	000000	DRC1 Input signal level at the Compressor 'Knee'. 000000 = 0dB 000001 = -0.75dB 000010 = -1.5dB … (-0.75dB steps) 111100 = -45dB 111101 = Reserved 11111X = Reserved
	4:0	DRC1_KNEE_OP [4:0]	00000	DRC1 Output signal at the Compressor 'Knee'. 00000 = 0dB 00001 = -0.75dB 00010 = -1.5dB … (-0.75dB steps) 11110 = -22.5dB 11111 = Reserved
R3716 (0E84h) DRC1 ctrl5	9:5	DRC1_KNEE2_IP [4:0]	00000	DRC1 Input signal level at the Noise Gate threshold 'Knee2'. 00000 = -36dB 00001 = -37.5dB 00010 = -39dB … (-1.5dB steps) 11110 = -81dB 11111 = -82.5dB Only applicable when DRC1_NG_ENA = 1.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	4:0	DRC1_KNEE2_OP [4:0]	00000	DRC1 Output signal at the Noise Gate threshold 'Knee2'. 00000 = -30dB 00001 = -31.5dB 00010 = -33dB … (-1.5dB steps) 11110 = -75dB 11111 = -76.5dB Only applicable when DRC1_KNEE2_OP_ENA = 1.

Table 13 DRC1 Control Registers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3585 (0E01h) FX_Ctrl2	15:4	FX_STS [11:0]	00h	LHPF, DRC, EQ Enable Status Indicates the status of each of the respective signal processing functions. [11] = Reserved [10] = Reserved [9] = EQ2 [8] = EQ1 [7] = DRC2 (Right) [6] = DRC2 (Left) [5] = DRC1 (Right) [4] = DRC1 (Left) [3] = LHPF4 [2] = LHPF3 [1] = LHPF2 [0] = LHPF1 Each bit is coded as: 0 = Disabled 1 = Enabled
R3721 (0E89h) DRC2 ctrl1	15:11	DRC2_SIG_DET_RMS [4:0]	00h	DRC2 Signal Detect RMS Threshold. This is the RMS signal level for signal detect to be indicated when DRC2_SIG_DET_MODE=1. 00h = -30dB 01h = -31.5dB …. (1.5dB steps) 1Eh = -75dB 1Fh = -76.5dB
	10:9	DRC2_SIG_DET_PK [1:0]	00	DRC2 Signal Detect Peak Threshold. This is the Peak/RMS ratio, or Crest Factor, level for signal detect to be indicated when DRC2_SIG_DET_MODE=0. 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB
	8	DRC2_NG_ENA	0	DRC2 Noise Gate Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7	DRC2_SIG_DET_MODE	0	DRC2 Signal Detect Mode 0 = Peak threshold mode 1 = RMS threshold mode
	6	DRC2_SIG_DET	0	DRC2 Signal Detect Enable 0 = Disabled 1 = Enabled
	5	DRC2_KNEE2_OP_ENA	0	DRC2 KNEE2_OP Enable 0 = Disabled 1 = Enabled
	4	DRC2_QR	1	DRC2 Quick-release Enable 0 = Disabled 1 = Enabled
	3	DRC2_ANTICLIP	1	DRC2 Anti-clip Enable 0 = Disabled 1 = Enabled
R3722 (0E8Ah) DRC2 ctrl2	12:9	DRC2_ATK [3:0]	0100	DRC2 Gain attack rate (seconds/6dB) 0000 = Reserved 0001 = 181us 0010 = 363us 0011 = 726us 0100 = 1.45ms 0101 = 2.9ms 0110 = 5.8ms 0111 = 11.6ms 1000 = 23.2ms 1001 = 46.4ms 1010 = 92.8ms 1011 = 185.6ms 1100 to 1111 = Reserved
	8:5	DRC2_DCY [3:0]	1001	DRC2 Gain decay rate (seconds/6dB) 0000 = 1.45ms 0001 = 2.9ms 0010 = 5.8ms 0011 = 11.6ms 0100 = 23.25ms 0101 = 46.5ms 0110 = 93ms 0111 = 186ms 1000 = 372ms 1001 = 743ms 1010 = 1.49s 1011 = 2.97s 1100 to1111 = Reserved
	4:2	DRC2_MINGAIN [2:0]	100	DRC2 Minimum gain to attenuate audio signals 000 = 0dB 001 = -12dB (default) 010 = -18dB 011 = -24dB 100 = -36dB 101 = Reserved 11X = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1:0	DRC2_MAXGAIN [1:0]	11	DRC2 Maximum gain to boost audio signals (dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 36dB
R3723 (0E8Bh) DRC2 ctrl3	15:12	DRC2_NG_MING AIN [3:0]	0000	DRC2 Minimum gain to attenuate audio signals when the noise gate is active. 0000 = -36dB 0001 = -30dB 0010 = -24dB 0011 = -18dB 0100 = -12dB 0101 = -6dB 0110 = 0dB 0111 = 6dB 1000 = 12dB 1001 = 18dB 1010 = 24dB 1011 = 30dB 1100 = 36dB 1101 to 1111 = Reserved
	11:10	DRC2_NG_EXP [1:0]	00	DRC2 Noise Gate slope 00 = 1 (no expansion) 01 = 2 10 = 4 11 = 8
	9:8	DRC2_QR_THR [1:0]	00	DRC2 Quick-release threshold (crest factor in dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB
	7:6	DRC2_QR_DCY [1:0]	00	DRC2 Quick-release decay rate (seconds/6dB) 00 = 0.725ms 01 = 1.45ms 10 = 5.8ms 11 = Reserved
	5:3	DRC2_HI_COMP [2:0]	011	DRC2 Compressor slope (upper region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 0 110 = Reserved 111 = Reserved
	2:0	DRC2_LO_COMP [2:0]	000	DRC2 Compressor slope (lower region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 0 101 = Reserved 11X = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3724 (0E8Ch) DRC2 ctrl4	10:5	DRC2_KNEE_IP [5:0]	000000	DRC2 Input signal level at the Compressor 'Knee'. 000000 = 0dB 000001 = -0.75dB 000010 = -1.5dB … (-0.75dB steps) 111100 = -45dB 111101 = Reserved 11111X = Reserved
	4:0	DRC2_KNEE_OP [4:0]	00000	DRC2 Output signal at the Compressor 'Knee'. 00000 = 0dB 00001 = -0.75dB 00010 = -1.5dB … (-0.75dB steps) 11110 = -22.5dB 11111 = Reserved
R3725 (0E8Dh) DRC2 ctrl5	9:5	DRC2_KNEE2_IP [4:0]	00000	DRC2 Input signal level at the Noise Gate threshold 'Knee2'. 00000 = -36dB 00001 = -37.5dB 00010 = -39dB … (-1.5dB steps) 11110 = -81dB 11111 = -82.5dB Only applicable when DRC2_NG_ENA = 1.
	4:0	DRC2_KNEE2_OP [4:0]	00000	DRC2 Output signal at the Noise Gate threshold 'Knee2'. 00000 = -30dB 00001 = -31.5dB 00010 = -33dB … (-1.5dB steps) 11110 = -75dB 11111 = -76.5dB Only applicable when DRC2_KNEE2_OP_ENA = 1.

Table 14 DRC2 Control Registers

The CS47L24 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the commanded DRC and digital mixing functions. If an attempt is made to enable a DRC signal path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error can be monitored using the GPIO and/or Interrupt functions. See "General Purpose Input / Output" and "Interrupts" for further details.

The FX_STS field in Register R3585 indicates the status of each of the EQ, DRC and LHPF signal paths. If an Underclocked Error condition occurs, then this register provides readback of which EQ, DRC or LHPF signal path(s) have been successfully enabled.

The status bits in Registers R1600 to R3000 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

LOW PASS / HIGH PASS DIGITAL FILTER (LHPF)

The digital core provides four Low Pass Filter (LPF) / High Pass Filter (HPF) processing blocks as illustrated in Figure 20. A 4-input mixer is associated with each filter. The 4 input sources are selectable in each case, and independent volume control is provided for each path. Each Low/High Pass Filter (LHPF) block supports 1 output.

The Low Pass Filter / High Pass Filter can be used to remove unwanted 'out of band' noise from a signal path. Each filter can be configured either as a Low Pass filter or High Pass filter.

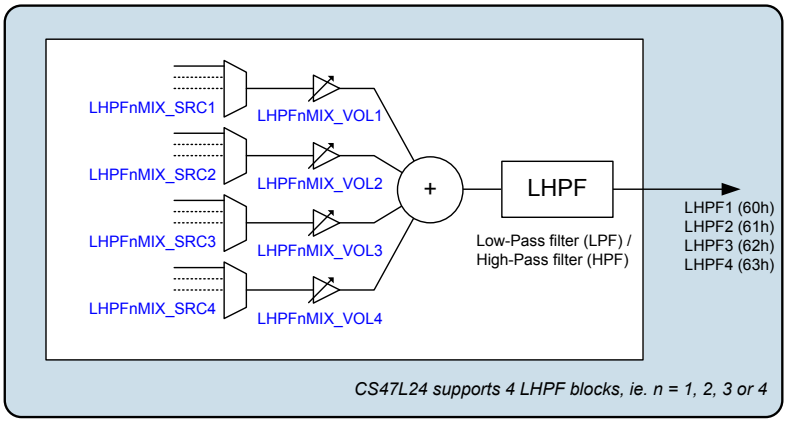


Figure 20 Digital Core LPF/HPF Blocks

The LHPF1, LHPF2, LHPF3 and LHPF4 mixer control registers (see Figure 20) are located at register addresses R2304 (900h) through to R2335 (91Fh).

The full list of digital mixer control registers is provided in the "Register Map" section (Register R1600 through to R3000). Generic register definitions are provided in Table 7.

The *_SRC*n* registers select the input source(s) for the respective LHPF processing blocks. Note that the selected input source(s) must be configured for the same sample rate as the LHPF to which they are connected. Sample rate conversion functions are available to support flexible interconnectivity - see "Asynchronous Sample Rate Converter (ASRC)" and "Isochronous Sample Rate Converter (ISRC)".

The bracketed numbers in Figure 20, e.g.,"(60h)" indicate the corresponding *_SRC*n* register setting for selection of that signal as an input to another digital core function.

The sample rate for the LHPF function is configured using the FX_RATE register - see Table 21. Note that the EQ, DRC and LHPF functions must all be configured for the same sample rate.

The LHPF function supports audio sample rates in the range 8kHz to 192kHz. When the DRC is enabled, the maximum sample rate for the EQ, DRC and LHPF functions is 96kHz.

Sample rate conversion is required when routing the LHPF signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

The control registers associated with the LHPF functions are described in Table 15.

The cut-off frequencies for the LHPF blocks are set using the coefficients held in registers R3777, R3781, R3785 and R3789 for LHPF1, LHPF2, LHPF3 and LHPF4 respectively. These coefficients are derived using tools provided in Cirrus Logic's WISCE™ evaluation board control software; please contact your local Cirrus Logic representative for more details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3585 (0E01h) FX_Ctrl2	15:4	FX_STS [11:0]	00h	LHPF, DRC, EQ Enable Status Indicates the status of each of the respective signal processing functions. [11] = Reserved [10] = Reserved [9] = EQ2 [8] = EQ1 [7] = DRC2 (Right) [6] = DRC2 (Left) [5] = DRC1 (Right) [4] = DRC1 (Left) [3] = LHPF4 [2] = LHPF3 [1] = LHPF2 [0] = LHPF1 Each bit is coded as: 0 = Disabled 1 = Enabled
R3776 (0EC0h) HPLPF1_1	1	LHPF1_MODE	0	Low/High Pass Filter 1 Mode 0 = Low-Pass 1 = High-Pass
	0	LHPF1_ENA	0	Low/High Pass Filter 1 Enable 0 = Disabled 1 = Enabled
R3777 (0EC1h) HPLPF1_2	15:0	LHPF1_COEFF [15:0]	0000h	Low/High Pass Filter 1 Frequency Coefficient Refer to WISCE evaluation board control software for the deriviation of this field value.
R3780 (0EC4h) HPLPF2_1	1	LHPF2_MODE	0	Low/High Pass Filter 2 Mode 0 = Low-Pass 1 = High-Pass
	0	LHPF2_ENA	0	Low/High Pass Filter 2 Enable 0 = Disabled 1 = Enabled
R3781 (0EC5h) HPLPF2_2	15:0	LHPF2_COEFF [15:0]	0000h	Low/High Pass Filter 2 Frequency Coefficient Refer to WISCE evaluation board control software for the deriviation of this field value.
R3784 (0EC8h) HPLPF3_1	1	LHPF3_MODE	0	Low/High Pass Filter 3 Mode 0 = Low-Pass 1 = High-Pass
	0	LHPF3_ENA	0	Low/High Pass Filter 3 Enable 0 = Disabled 1 = Enabled
R3785 (0EC9h) HPLPF3_2	15:0	LHPF3_COEFF [15:0]	0000h	Low/High Pass Filter 3 Frequency Coefficient Refer to WISCE evaluation board control software for the deriviation of this field value.
R3788 (0ECCh) HPLPF4_1	1	LHPF4_MODE	0	Low/High Pass Filter 4 Mode 0 = Low-Pass 1 = High-Pass
	0	LHPF4_ENA	0	Low/High Pass Filter 4 Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3789 (0ECDh) HPLPF4_2	15:0	LHPF4_COEFF [15:0]	0000h	Low/High Pass Filter 4 Frequency Coefficient Refer to WISCE evaluation board control software for the deriviation of this field value.

Table 15 Low Pass Filter / High Pass Filter Control

The CS47L24 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the commanded LHPF and digital mixing functions. If an attempt is made to enable an LHPF signal path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error can be monitored using the GPIO and/or Interrupt functions. See “General Purpose Input / Output” and “Interrupts” for further details.

The FX_STS field in Register R3585 indicates the status of each of the EQ, DRC and LHPF signal paths. If an Underclocked Error condition occurs, then this register provides readback of which EQ, DRC or LHPF signal path(s) have been successfully enabled.

The status bits in Registers R1600 to R3000 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

DIGITAL CORE DSP

The digital core provides two programmable DSP processing blocks as illustrated in Figure 21. Each block supports 8 inputs (Left, Right, Aux1, Aux2, … Aux6). A 4-input mixer is associated with the Left and Right inputs, providing further expansion of the number of input paths. Each of the input sources is selectable, and independent volume control is provided for Left and Right input mixer channels. Each DSP block supports 6 outputs.

The functionality of the DSP processing blocks is not fixed, and a wide range of audio enhancements algorithms may be performed. The procedure for configuring the CS47L24 DSP functions is tailored to each customer’s application; please contact your local Cirrus Logic representative for more details.

For details of the DSP Firmware requirements relating to clocking, register access, and code execution, refer to the “DSP Firmware Control” section.

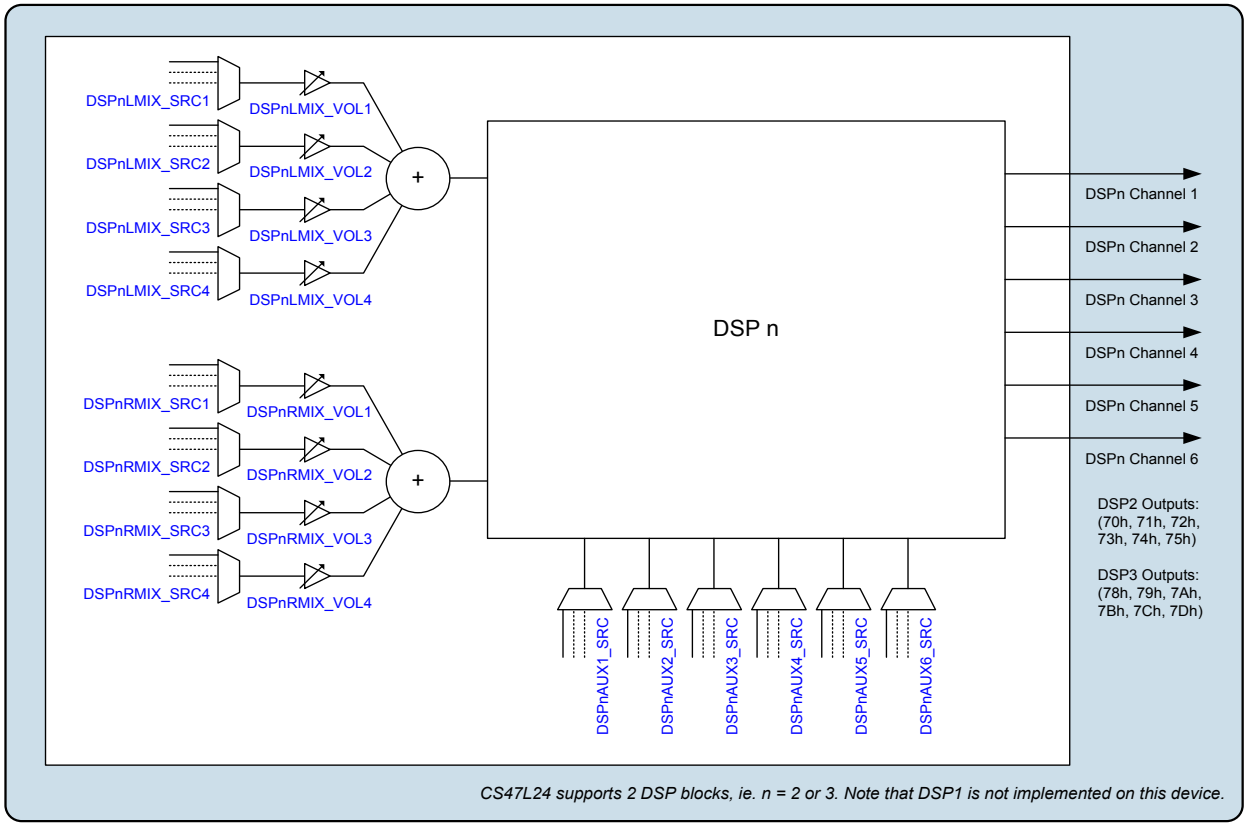


Figure 21 Digital Core DSP Blocks

The DSP2 and DSP3 mixer / input control registers (see Figure 21) are located at register addresses R2432 (980h) through to R2552 (9F8h). (Note that DSP1 is not implemented on this device.)

The full list of digital mixer control registers is provided in the “Register Map” section (Register R1600 through to R3000). Generic register definitions are provided in Table 7.

The *_SRC*n* registers select the input source(s) for the respective DSP processing blocks. Note that the selected input source(s) must be configured for the same sample rate as the DSP to which they are connected. Sample rate conversion functions are available to support flexible interconnectivity - see “Asynchronous Sample Rate Converter (ASRC)” and “Isochronous Sample Rate Converter (ISRC)”.

The bracketed numbers in Figure 21, e.g.,”(68h)” indicate the corresponding *_SRC*n* register setting for selection of that signal as an input to another digital core function.

The sample rate for each of the DSP functions is configured using the respective DSPn_RATE registers - see Table 21. Sample rate conversion is required when routing the DSPn signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

The CS47L24 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the commanded DSP mixing functions. If an attempt is made to enable a DSP mixer path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error condition can be monitored using the GPIO and/or Interrupt functions. See “General Purpose Input / Output” and “Interrupts” for further details.

The status bits in Registers R1600 to R3000 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

The CS47L24 supports up to eight DSP Status flags as outputs from the DSP blocks. These are configurable within the DSP to provide external indication of the required function(s). The DSP Status flags can be read using the DSP_IRQn_STS registers described in Table 66 (see “Interrupts”).

The DSP Status flags are inputs to the Interrupt control circuit and can be used to trigger an interrupt event - see “Interrupts”.

The DSP Status flags can be output directly on a GPIO pin as an external indication of the DSP Status. See “General Purpose Input / Output” to configure a GPIO pin for this function.

The DSP_IRQn_STS fields are read-only bits. These bits can be set (or reset) by writing to the DSP_IRQn fields, as described in Table 16. This facility can be used to allow a DSP core to generate an interrupt to the host processor. The DSP interrupt registers are asserted on the rising and falling edges of the respective DSP_IRQn fields.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3393 (0D41h) ADSP2 IRQ0	1	DSP_IRQ2	0	DSP IRQ2 0 = Not asserted 1 = Asserted This bit can be set/reset by a DSP core in order to generate a DSP_IRQ2_EINTn interrupt to the host processor.
	0	DSP_IRQ1	0	DSP IRQ1 0 = Not asserted 1 = Asserted This bit can be set/reset by a DSP core in order to generate a DSP_IRQ1_EINTn interrupt to the host processor.
R3394 (0D42h) ADSP2 IRQ1	1	DSP_IRQ4	0	DSP IRQ4 0 = Not asserted 1 = Asserted This bit can be set/reset by a DSP core in order to generate a DSP_IRQ4_EINTn interrupt to the host processor.
	0	DSP_IRQ3	0	DSP IRQ3 0 = Not asserted 1 = Asserted This bit can be set/reset by a DSP core in order to generate a DSP_IRQ3_EINTn interrupt to the host processor.
R3395 (0D43h) ADSP2 IRQ2	1	DSP_IRQ6	0	DSP IRQ6 0 = Not asserted 1 = Asserted This bit can be set/reset by a DSP core in order to generate a DSP_IRQ6_EINTn interrupt to the host processor.
	0	DSP_IRQ5	0	DSP IRQ5 0 = Not asserted 1 = Asserted This bit can be set/reset by a DSP core in order to generate a DSP_IRQ5_EINTn interrupt to the host processor.
R3396 (0D44h) ADSP2 IRQ3	1	DSP_IRQ8	0	DSP IRQ8 0 = Not asserted 1 = Asserted This bit can be set/reset by a DSP core in order to generate a DSP_IRQ8_EINTn interrupt to the host processor.
	0	DSP_IRQ7	0	DSP IRQ7 0 = Not asserted 1 = Asserted This bit can be set/reset by a DSP core in order to generate a DSP_IRQ7_EINTn interrupt to the host processor.

Table 16 DSP Interrupts

TONE GENERATOR

The CS47L24 incorporates two 1kHz tone generators which can be used for 'beep' functions through any of the audio signal paths. The phase relationship between the two generators is configurable, providing flexibility in creating differential signals, or for test scenarios.

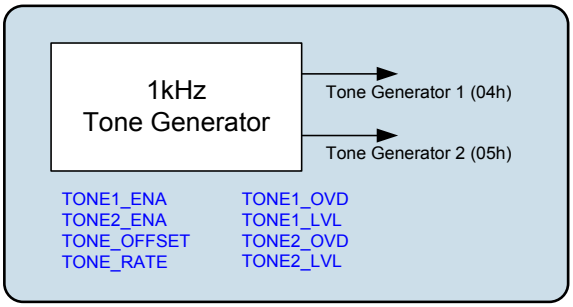


Figure 22 Digital Core Tone Generator

The tone generators can be selected as input to any of the digital mixers or signal processing functions within the CS47L24 digital core. The bracketed numbers in Figure 22, e.g.,"(04h)" indicate the corresponding *_SRC*n* register setting for selection of that signal as an input to another digital core function.

The sample rate for the tone generators is configured using the TONE_RATE register - see Table 21. Note that sample rate conversion is required when routing the tone generator output(s) to any signal chain that is asynchronous and/or configured for a different sample rate.

The tone generators are enabled using the TONE1_ENA and TONE2_ENA register bits as described in Table 17. The phase relationship is configured using TONE_OFFSET.

The tone generators can also provide a configurable DC signal level, for use as a test signal. The DC output is selected using the TONEn_OVD register bits, and the DC signal amplitude is configured using the TONEn_LVL registers, as described in Table 17.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (0020h) Tone Generator 1	9:8	TONE_OFFSET [1:0]	00	Tone Generator Phase Offset Sets the phase of Tone Generator 2 relative to Tone Generator 1 00 = 0 degrees (in phase) 01 = 90 degrees ahead 10 = 180 degrees ahead 11 = 270 degrees ahead
	5	TONE2_OVD	0	Tone Generator 2 Override 0 = Disabled (1kHz tone output) 1 = Enabled (DC signal output) The DC signal level, when selected, is configured using TONE2_LVL[23:0]
	4	TONE1_OVD	0	Tone Generator 1 Override 0 = Disabled (1kHz tone output) 1 = Enabled (DC signal output) The DC signal level, when selected, is configured using TONE1_LVL[23:0]
	1	TONE2_ENA	0	Tone Generator 2 Enable 0 = Disabled 1 = Enabled
	0	TONE1_ENA	0	Tone Generator 1 Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R33 (0021h) Tone Generator 2	15:0	TONE1_LVL [23:8]	1000h	Tone Generator 1 DC output level TONE1_LVL [23:8] is coded as 2's complement. Bits [23:20] contain the integer portion; bits [19:0] contain the fractional portion. The digital core 0dBFS level corresponds to 1000_00h (+1) or F000_00h (-1).
R34 (0022h) Tone Generator 3	7:0	TONE1_LVL [7:0]	00h	Tone Generator 1 DC output level TONE1_LVL [23:8] is coded as 2's complement. Bits [23:20] contain the integer portion; bits [19:0] contain the fractional portion. The digital core 0dBFS level corresponds to 1000_00h (+1) or F000_00h (-1).
R35 (0023h) Tone Generator 4	15:0	TONE2_LVL [23:8]	1000h	Tone Generator 2 DC output level TONE2_LVL [23:8] is coded as 2's complement. Bits [23:20] contain the integer portion; bits [19:0] contain the fractional portion. The digital core 0dBFS level corresponds to 1000_00h (+1) or F000_00h (-1).
R36 (0024h) Tone Generator 5	7:0	TONE2_LVL [7:0]	00h	Tone Generator 2 DC output level TONE2_LVL [23:8] is coded as 2's complement. Bits [23:20] contain the integer portion; bits [19:0] contain the fractional portion. The digital core 0dBFS level corresponds to 1000_00h (+1) or F000_00h (-1).

Table 17 Tone Generator Control

NOISE GENERATOR

The CS47L24 incorporates a white noise generator, which can be routed within the digital core. The main purpose of the noise generator is to provide 'comfort noise' in cases where silence (digital mute) is not desirable.

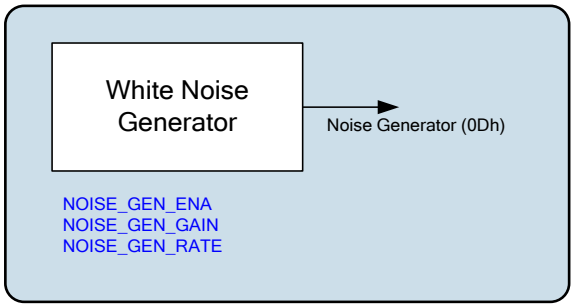


Figure 23 Digital Core Noise Generator

The noise generator can be selected as input to any of the digital mixers or signal processing functions within the CS47L24 digital core. The bracketed number (0Dh) in Figure 23 indicates the corresponding *_SRC*n* register setting for selection of the noise generator as an input to another digital core function.

The sample rate for the noise generator is configured using the NOISE_GEN_RATE register - see Table 21. Note that sample rate conversion is required when routing the noise generator output to any signal chain that is asynchronous and/or configured for a different sample rate.

The noise generator is enabled using the NOISE_GEN_ENA register bit as described in Table 18. The signal level is configured using NOISE_GEN_GAIN.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R112 (0070h) Comfort Noise Generator	5	NOISE_GEN_ENA	0	Noise Generator Enable 0 = Disabled 1 = Enabled
	4:0	NOISE_GEN_GAIN [4:0]	00h	Noise Generator Signal Level 00h = -114dBFS 01h = -108dBFS 02h = -102dBFS …(6dB steps) 11h = -6dBFS 12h = 0dBFS All other codes are Reserved

Table 18 Noise Generator Control

HAPTIC SIGNAL GENERATOR

The CS47L24 incorporates a signal generator for use with haptic devices (e.g., mechanical vibration actuators). The haptic signal generator is compatible with both Eccentric Rotating Mass (ERM) and Linear Resonant Actuator (LRA) haptic devices.

The haptic signal generator is highly configurable, and includes the capability to execute a programmable event profile comprising three distinct operating phases.

The resonant frequency of the haptic signal output (for LRA devices) is selectable, providing support for many different actuator components.

The haptic signal generator is a digital signal generator which is incorporated within the digital core of the CS47L24. The haptic signal may be routed, via one of the digital core output mixers, to the Class D speaker output for connection to the external haptic device, as illustrated in Figure 24.

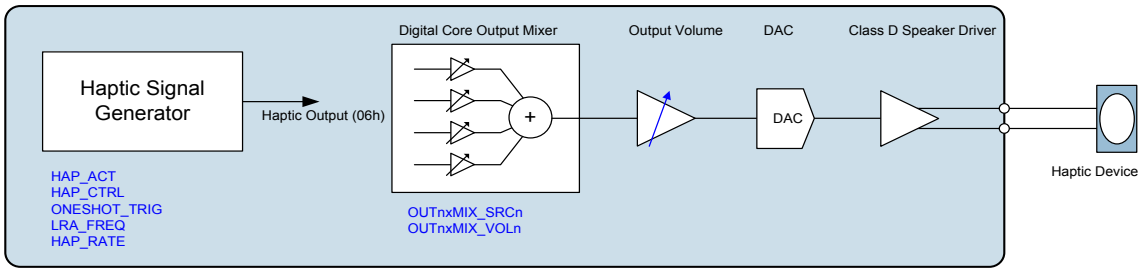


Figure 24 Digital Core Haptic Signal Generator

The bracketed number (06h) in Figure 24 indicates the corresponding *_SRC*n* register setting for selection of the haptic signal generator as an input to another digital core function.

The haptic signal generator is selected as input to one of the digital core output mixers by setting the *_SRC*n* register of the applicable output mixer to (06h).

The sample rate for the haptic signal generator is configured using the HAP_RATE register - see Table 21. Note that sample rate conversion is required when routing the haptic signal generator output to any signal chain that is asynchronous and/or configured for a different sample rate.

The haptic signal generator is configured for an ERM or LRA actuator using the HAP_ACT register bit. The required resonant frequency is configured using the LRA_FREQ field. (Note that the resonant frequency is only applicable to LRA actuators.)

The signal generator can be enabled in Continuous mode or configured for One-Shot mode using the HAP_CTRL register, as described in Table 19. In One-Shot mode, the output is triggered by writing to the ONESHOT_TRIG bit.

In One-Shot mode, the signal generator profile comprises the distinct phases (1, 2, 3). The duration and intensity of each output phase is programmable.

In Continuous mode, the signal intensity is controlled using the PHASE2_INTENSITY field only.

In the case of an ERM actuator (HAP_ACT = 0), the haptic output is a DC signal level, which may be positive or negative, as selected by the *_INTENSITY registers.

For an LRA actuator (HAP_ACT = 1), the haptic output is an AC signal; selecting a negative signal level corresponds to a 180 degree phase inversion. In some applications, phase inversion may be desirable during the final phase, to halt the physical motion of the haptic device.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R144 (0090h) Haptics Control 1	4	ONESHOT_TRIG	0	Haptic One-Shot Trigger Writing '1' starts the one-shot profile (i.e., Phase 1, Phase 2, Phase 3)
	3:2	HAP_CTRL [1:0]	00	Haptic Signal Generator Control 00 = Disabled 01 = Continuous 10 = One-Shot 11 = Reserved
	1	HAP_ACT	0	Haptic Actuator Select 0 = Eccentric Rotating Mass (ERM) 1 = Linear Resonant Actuator (LRA)
R145 (0091h) Haptics Control 2	14:0	LRA_FREQ [14:0]	7FFFh	Haptic Resonant Frequency Selects the haptic signal frequency (LRA actuator only, HAP_ACT = 1) Haptic Frequency (Hz) = System Clock / (2 x (LRA_FREQ+1)) where System Clock = 6.144MHz or 5.6448MHz, derived by division from SYSCLK or ASYNCCLK. If HAP_RATE<1000, then SYSCLK is the clock source, and the applicable System Clock frequency is determined by SYSCLK. If HAP_RATE>=1000, then ASYNCCLK is the clock source, and the applicable System Clock frequency is determined by ASYNCCLK. Valid for Haptic Frequency in the range 100Hz to 250Hz For 6.144MHz System Clock: 77FFh = 100Hz 4491h = 175Hz 2FFFh = 250Hz For 5.6448MHz System Clock: 6E3Fh = 100Hz 3EFFh = 175Hz 2C18h = 250Hz
R146 (0092h) Haptics phase 1 intensity	7:0	PHASE1_INTENSITY [7:0]	00h	Haptic Output Level (Phase 1) Selects the signal intensity of Phase 1 in one-shot mode. Coded as 2's complement. Range is +/- Full Scale (FS). For ERM actuator, this selects the DC signal level for the haptic output. For LRA actuator, this selects the AC peak amplitude; Negative values correspond to a 180 degree phase shift.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R147 (0093h) Haptics Control phase 1 duration	8:0	PHASE1_DURATION [8:0]	000h	Haptic Output Duration (Phase 1) Selects the duration of Phase 1 in one-shot mode. 000h = 0ms 001h = 0.625ms 002h = 1.25ms … (0.625ms steps) 1FFh = 319.375ms
R148 (0094h) Haptics phase 2 intensity	7:0	PHASE2_INTENSITY [7:0]	00h	Haptic Output Level (Phase 2) Selects the signal intensity in Continuous mode or Phase 2 of one-shot mode. Coded as 2's complement. Range is +/- Full Scale (FS). For ERM actuator, this selects the DC signal level for the haptic output. For LRA actuator, this selects the AC peak amplitude; Negative values correspond to a 180 degree phase shift.
R149 (0095h) Haptics phase 2 duration	10:0	PHASE2_DURATION [10:0]	000h	Haptic Output Duration (Phase 2) Selects the duration of Phase 2 in one-shot mode. 000h = 0ms 001h = 0.625ms 002h = 1.25ms … (0.625ms steps) 7FFh = 1279.375ms
R150 (0096h) Haptics phase 3 intensity	7:0	PHASE3_INTENSITY [7:0]	00h	Haptic Output Level (Phase 3) Selects the signal intensity of Phase 3 in one-shot mode. Coded as 2's complement. Range is +/- Full Scale (FS). For ERM actuator, this selects the DC signal level for the haptic output. For LRA actuator, this selects the AC peak amplitude; Negative values correspond to a 180 degree phase shift.
R151 (0097h) Haptics phase 3 duration	8:0	PHASE3_DURATION [8:0]	000h	Haptic Output Duration (Phase 3) Selects the duration of Phase 3 in one-shot mode. 000h = 0ms 001h = 0.625ms 002h = 1.25ms … (0.625ms steps) 1FFh = 319.375ms
R152 (0098h) Haptics Status	0	ONESHOT_STS	0	Haptic One-Shot status 0 = One-Shot event not in progress 1 = One-Shot event in progress

Table 19 Haptic Signal Generator Control

PWM GENERATOR

The CS47L24 incorporates two Pulse Width Modulation (PWM) signal generators as illustrated in Figure 25. The duty cycle of each PWM signal can be modulated by an audio source, or can be set to a fixed value using a control register setting.

A 4-input mixer is associated with each PWM generator. The 4 input sources are selectable in each case, and independent volume control is provided for each path.

The PWM signal generators can be output directly on a GPIO pin. See “General Purpose Input / Output” to configure a GPIO pin for this function.

Note that the PWM output should always be disabled whenever the system clock, SYSCLK, is disabled. Failure to do this may result in a persistent logic ‘1’ DC output from the PWM generator. See “Clocking and Sample Rates” for details of system clocking and the associated control requirements.

Note that the PWM signal generators cannot be selected as input to the digital mixers or signal processing functions within the CS47L24 digital core.

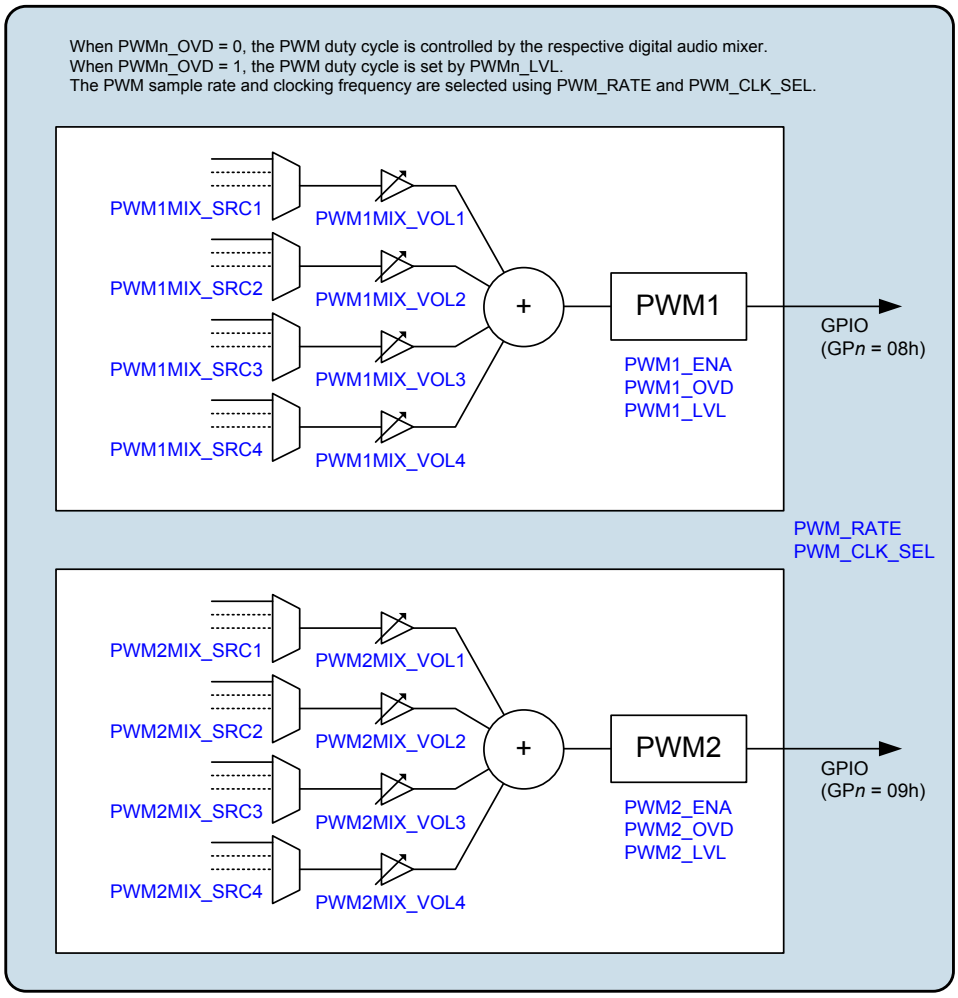


Figure 25 Digital Core Pulse Width Modulation (PWM) Generator

The PWM1 and PWM2 mixer control registers (see Figure 25) are located at register addresses R1600 (640h) through to R1615 (64Fh).

The full list of digital mixer control registers is provided in the “Register Map” section (Register R1600 through to R3000). Generic register definitions are provided in Table 7.

The *_SRC*n* registers select the input source(s) for the respective mixers. Note that the selected input source(s) must be configured for the same sample rate as the mixer to which they are connected. Sample rate conversion functions are available to support flexible interconnectivity - see “Asynchronous Sample Rate Converter (ASRC)” and “Isochronous Sample Rate Converter (ISRC)”.

The PWM sample rate (cycle time) is configured using the PWM_RATE register - see Table 21. Note that sample rate conversion is required when linking the PWM generators to any signal chain that is asynchronous and/or configured for a different sample rate.

The PWM generators are enabled using PWM1_ENA and PWM2_ENA respectively, as described in Table 20.

Under default conditions (PWM*n*_OVD = 0), the duty cycle of the PWM generators is controlled by an audio signal path; a 4-input mixer is associated with each PWM generator, as illustrated in Figure 25.

When the PWM*n*_OVD bit is set, the duty cycle of the respective PWM generator is set to a fixed ratio; in this case, the duty cycle ratio is configurable using the PWM*n*_LVL registers.

The PWM generator clock frequency is selected using PWM_CLK_SEL. For best performance, this register should be set to the highest available setting. Note that the PWM generator clock must not be set to a higher frequency than SYSCLK (if PWM_RATE<1000) or ASYNCCLK (if PWM_RATE≥1000).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R48 (0030h) PWM Drive 1	10:8	PWM_CLK_SEL [2:0]	000	PWM Clock Select 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) All other codes are Reserved The frequencies in brackets apply for 44.1kHz-related sample rates only. PWM_CLK_SEL controls the resolution of the PWM generator; higher settings correspond to higher resolution. The PWM Clock must be less than or equal to SYSCLK (if PWM_RATE<1000) or less than or equal to ASYNCCLK (if PWM_RATE>=1000).
	5	PWM2_OVD	0	PWM2 Generator Override 0 = Disabled (PWM duty cycle is controlled by audio source) 1 = Enabled (PWM duty cycle is controlled by PWM2_LVL).
	4	PWM1_OVD	0	PWM1 Generator Override 0 = Disabled (PWM1 duty cycle is controlled by audio source) 1 = Enabled (PWM1 duty cycle is controlled by PWM1_LVL).
	1	PWM2_ENA	0	PWM2 Generator Enable 0 = Disabled 1 = Enabled
	0	PWM1_ENA	0	PWM1 Generator Enable 0 = Disabled 1 = Enabled
R49 (0031h) PWM Drive 2	9:0	PWM1_LVL [9:0]	100h	PWM1 Override Level Sets the PWM1 duty cycle when PWM1_OVD=1. Coded as 2's complement. 000h = 50% duty cycle 200h = 0% duty cycle
R50 (0032h) PWM Drive 3	9:0	PWM2_LVL [9:0]	100h	PWM2 Override Level Sets the PWM2 duty cycle when PWM2_OVD=1. Coded as 2's complement. 000h = 50% duty cycle 200h = 0% duty cycle

Table 20 Pulse Width Modulation (PWM) Generator Control

The CS47L24 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the digital mixer paths. If an attempt is made to enable a PWM signal mixer path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error condition can be monitored using the GPIO and/or Interrupt functions. See “General Purpose Input / Output” and “Interrupts” for further details.

The status bits in Registers R1600 to R3000 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

SAMPLE RATE CONTROL

The CS47L24 supports multiple signal paths through the digital core. Stereo full-duplex sample rate conversion is provided to allow digital audio to be routed between interfaces operating at different sample rates and/or referenced to asynchronous clock domains.

Two independent clock domains are supported, referenced to SYSCLK and ASYNCCLK respectively, as described in “Clocking and Sample Rates”. Every digital signal path must be synchronised either to SYSCLK or to ASYNCCLK.

Up to five different sample rates may be in use at any time on the CS47L24. Three of these sample rates must be synchronised to SYSCLK; the remaining two, where required, must be synchronised to ASYNCCLK.

Sample rate conversion is required when routing any audio path between digital functions that are asynchronous and/or configured for different sample rates.

The Asynchronous Sample Rate Converter (ASRC) provides two stereo signal paths between the SYSCLK and ASYNCCLK domains. The ASRC is described later, and is illustrated in Figure 28.

There are three Isochronous Sample Rate Converters (ISRCs). These provide four signal paths each between sample rates on the SYSCLK domain, or between sample rates on the ASYNCCLK domain. The ISRCs are described later, and are illustrated in Figure 29.

The sample rate of different blocks within the CS47L24 digital core are controlled as illustrated in Figure 26 and Figure 27 - the *_RATE registers select the applicable sample rate for each respective group of digital functions.

The *_RATE registers should not be changed if any of the *_SRC*n* registers associated with the respective functions is non-zero. The associated *_SRC*n* registers should be cleared to 00h before writing new values to the *_RATE registers. A minimum delay of 125µs should be allowed between clearing the *_SRC*n* registers and writing to the associated *_RATE registers. See Table 21 for further details.

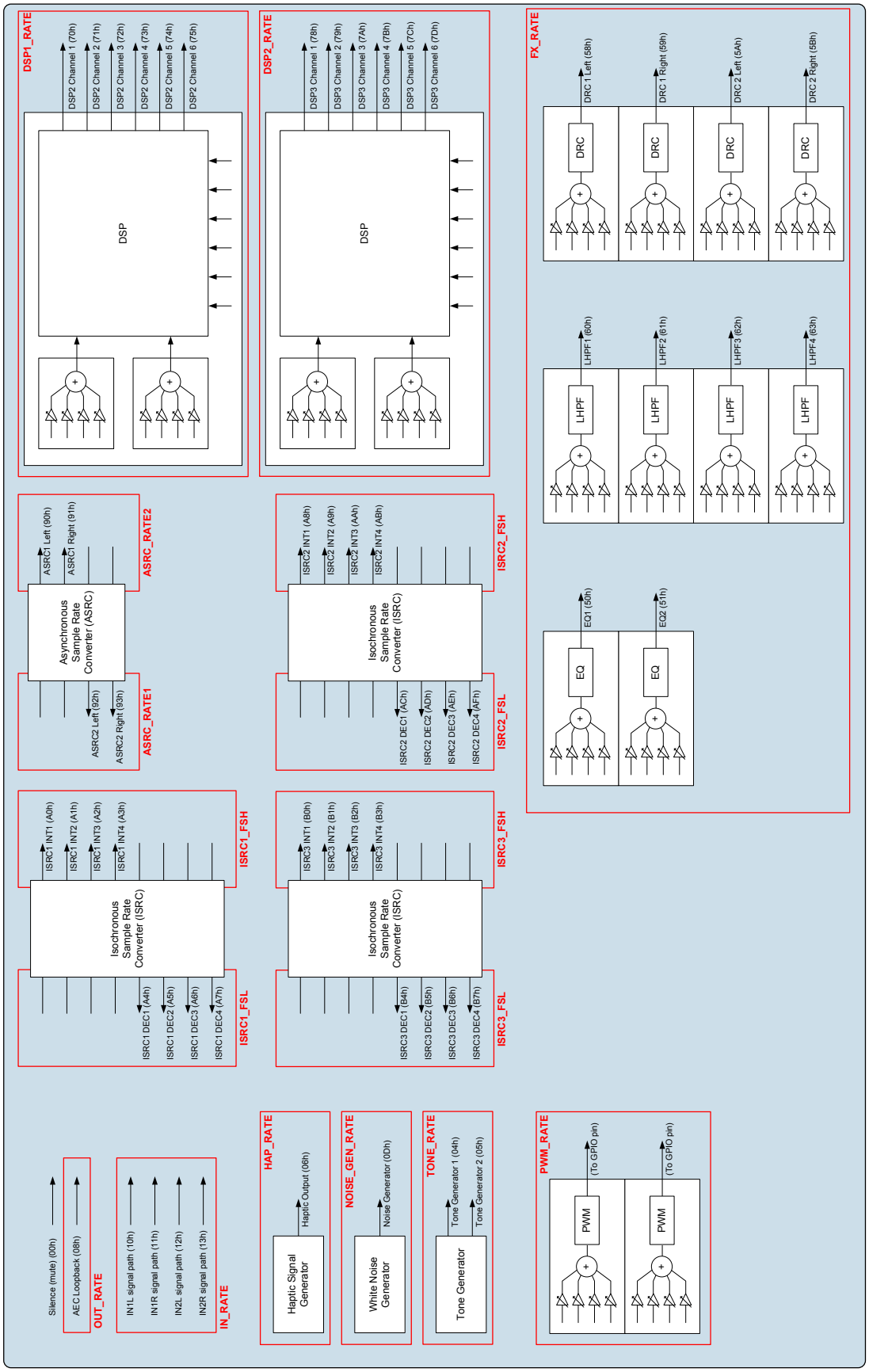


Figure 26 Digital Core Sample Rate Control (Internal Signal Processing)

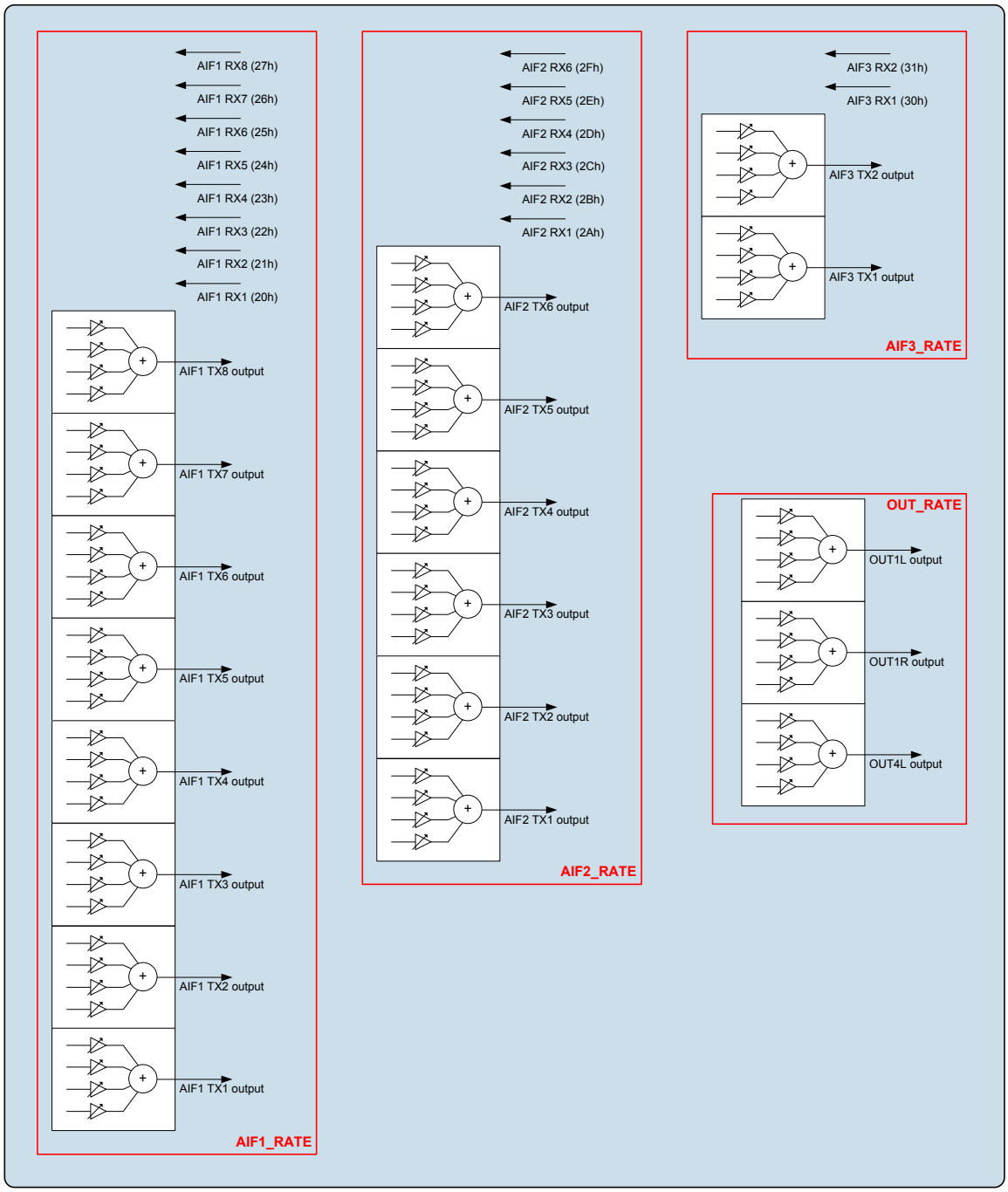


Figure 27 Digital Core Sample Rate Control (External Digital Interfaces)

The input signal paths may be selected as input to the digital mixers or signal processing functions. The sample rate for the input signal paths is configured using the IN_RATE register.

The output signal paths are derived from the respective output mixers. The sample rate for the output signal paths is configured using the OUT_RATE register. The sample rate of the AEC Loopback path is also set by the OUT_RATE register.

The AIFn RX inputs may be selected as input to the digital mixers or signal processing functions. The AIFn TX outputs are derived from the respective output mixers. The sample rates for digital audio interfaces (AIF1, AIF2 and AIF3) are configured using the AIF1_RATE, AIF2_RATE and AIF3_RATE registers respectively.

The EQ, LHPF and DRC functions can be enabled in any signal path within the digital core. The sample rate for these functions is configured using the FX_RATE register. Note that the EQ, DRC and LHPF functions must all be configured

for the same sample rate.

The DSPn functions can be enabled in any signal path within the digital core. The applicable sample rates are configured using the DSP2_RATE and DSP3_RATE registers.

The tone generators and noise generator can be selected as input to any of the digital mixers or signal processing functions. The sample rates for these sources are configured using the TONE_RATE and NOISE_GEN_RATE registers respectively.

The haptic signal generator can be used to control an external vibe actuator, which can be driven directly by the Class D speaker output. The sample rate for the haptic signal generator is configured using the HAP_RATE register.

The PWM signal generators can be modulated by an audio source, derived from the associated signal mixers. The sample rate (cycle time) for the PWM signal generators is configured using the PWM_RATE register.

The sample rate control registers are described in Table 21. Refer to the register descriptions for details of the valid selections in each case. Note that the input (DMIC) and output (DAC) signal paths must always be associated with the SYSCLK clocking domain; different sample rates may be selected concurrently, but both these rates must be synchronised to SYSCLK.

The control registers associated with the ASRC and ISRCs are described in Table 22 and Table 23 respectively within the following sections.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (0020h) Tone Generator 1	14:11	TONE_RATE [3:0]	0000	Tone Generator Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz.
R48 (0030h) PWM Drive 1	14:11	PWM_RATE [3:0]	0000	PWM Frequency (sample rate) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 4kHz to 192kHz. All PWM*n*MIX_SRC*m* registers should be set to 00h before changing PWM_RATE.
R112 0070h) Comfort Noise Generator	14:11	NOISE_GEN_RATE [3:0]	0000	Noise Generator Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 4kHz to 192kHz.
R144 0090h) Haptics Control 1	14:11	HAP_RATE [3:0]	0000	Haptic Signal Generator Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R776 (0308h) Input Rate	14:11	IN_RATE [3:0]	0000	Input Signal Paths Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. If 768kHz DMIC clock rate is selected on any of the input paths (INn_OSR=11), then the Input Signal Paths sample rate is valid in the range 8kHz to 16kHz only.
R1032 (0408h) Output Rate 1	14:11	OUT_RATE [3:0]	0000	Output Signal Paths Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. All OUT*n*xMIX_SRC*m* registers should be set to 00h before changing OUT_RATE.
R1283 (0503h) AIF1 Rate Ctrl	14:11	AIF1_RATE [3:0]	0000	AIF1 Audio Interface Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 4kHz to 192kHz. All AIF1TXMIX_SRC*n* registers should be set to 00h before changing AIF1_RATE.
R1347 (0543h) AIF2 Rate Ctrl	14:11	AIF2_RATE [3:0]	0000	AIF2 Audio Interface Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 4kHz to 192kHz. All AIF2TXMIX_SRC*n* registers should be set to 00h before changing AIF2_RATE.
R1411 (0583h) AIF3 Rate Ctrl	14:11	AIF3_RATE [3:0]	0000	AIF3 Audio Interface Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 4kHz to 192kHz. All AIF3TXMIX_SRC*n* registers should be set to 00h before changing AIF3_RATE.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3584 (0E00h) FX_Ctrl	14:11	FX_RATE [3:0]	0000	FX Sample Rate (EQ, LHPF, DRC) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. When the DRC is enabled, the maximum FX_RATE sample rate is 96kHz. All EQ*n*MIX_SRC*m*, DRC*n*xMIX_SRC*m*, and LHPF*n*MIX_SRC*m* registers should be set to 00h before changing FX_RATE.
R4608 (1200h) DSP2 Control 1	14:11	DSP2_RATE [3:0]	0000	DSP2 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 4kHz to 192kHz. All DSP2*x*MIX_SRC*n* registers should be set to 00h before changing DSP2_RATE.
R4864 (1300h) DSP3 Control 1	14:11	DSP3_RATE [3:0]	0000	DSP3 Sample Rate 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 4kHz to 192kHz. All DSP3*x*MIX_SRC*n* registers should be set to 00h before changing DSP3_RATE.

Table 21 Digital Core Sample Rate Control

ASYNCHRONOUS SAMPLE RATE CONVERTER (ASRC)

The CS47L24 supports multiple signal paths through the digital core. Two independent clock domains are supported, referenced to SYSCLK and ASYNCCLK respectively, as described in “Clocking and Sample Rates”. Every digital signal path must be synchronised either to SYSCLK or to ASYNCCLK.

The Asynchronous Sample Rate Converter (ASRC) provides two stereo signal paths between the SYSCLK and ASYNCCLK domains, as illustrated in Figure 28.

The sample rate on the SYSCLK domain is selected using the ASRC_RATE1 register - the rate can be set equal to SAMPLE_RATE_1, SAMPLE_RATE_2 or SAMPLE_RATE_3.

The sample rate on the ASYNCCLK domain is selected using the ASRC_RATE2 register - the rate can be set equal to ASYNC_SAMPLE_RATE_1 or ASYNC_SAMPLE_RATE_2.

See “Clocking and Sample Rates” for details of the sample rate control registers.

The ASRC_RATE1 and ASRC_RATE2 registers should not be changed if any of the respective *_SRC*n* registers is non-zero. The associated *_SRC*n* registers should be cleared to 00h before writing new values to ASRC_RATE1 or ASRC_RATE2. A minimum delay of 125µs should be allowed between clearing the *_SRC*n* registers and writing to the associated ASRC_RATE1 or ASRC_RATE2 registers. See Table 22 for further details.

The ASRC supports sample rates in the range 8kHz to 48kHz only. The applicable SAMPLE_RATE_n and ASYNC_SAMPLE_RATE_n registers must each select sample rates between 8kHz and 48kHz when any ASRC path is enabled.

The ASRC1 Left and ASRC1 Right paths convert from the SYSCLK domain to the ASYNCCLK domain. These paths are enabled using the ASRC1L_ENA and ASRC1R_ENA register bits respectively.

The ASRC2 Left and ASRC2 Right paths convert from the ASYNCCLK domain to the SYSCLK domain. These paths are enabled using the ASRC2L_ENA and ASRC2R_ENA register bits respectively.

Synchronisation (lock) between different clock domains is not instantaneous when the clocking or sample rate configurations are updated. The lock status of each ASRC path is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see “Interrupts”.

The ASRC Lock status of each ASRC path can be output directly on a GPIO pin as an external indication of ASRC Lock. See “General Purpose Input / Output” to configure a GPIO pin for this function.

The CS47L24 performs automatic checks to confirm that the SYSCLK or ASYNCCLK frequency is high enough to support the commanded ASRC and digital mixing functions. If an attempt is made to enable an ASRC signal path, and there are insufficient SYSCLK or ASYNCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error can be monitored using the GPIO and/or Interrupt functions. See “General Purpose Input / Output” and “Interrupts” for further details.

The status bits in Register R3809 indicate the status of each of the ASRC signal paths. If an Underclocked Error condition occurs, then these bits provide readback of which ASRC signal path(s) have been successfully enabled.

The status bits in Registers R1600 to R3000 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

The Asynchronous Sample Rate Converter (ASRC) signal paths and control registers are illustrated in Figure 28.

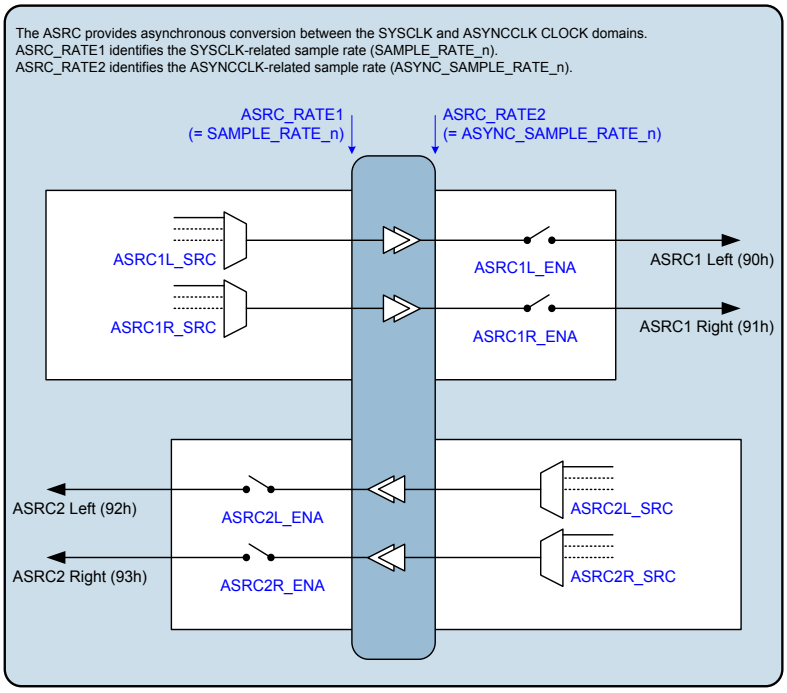


Figure 28 Asynchronous Sample Rate Converters (ASRCs)

The ASRC1 and ASRC2 input control registers (see Figure 28) are located at register addresses R2688 (A80h) through to R2712 (A98h).

The full list of digital mixer control registers is provided in the “Register Map” section (Register R1600 through to R3000). Generic register definitions are provided in Table 7.

The *_SRC*n* registers select the input source(s) for the respective ASRC processing blocks. Note that the selected input source(s) must be configured for the same sample rate as the ASRC to which they are connected.

The bracketed numbers in Figure 28, e.g.,"(90h)" indicate the corresponding *_SRC*n* register setting for selection of that signal as an input to another digital core function.

The register bits associated with the ASRCs are described in Table 22.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3808 (0EE0h) ASRC_ENABLE	3	ASRC2L_ENA	0	ASRC2 Left Enable (Left ASRC channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
	2	ASRC2R_ENA	0	ASRC2 Right Enable (Right ASRC channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
	1	ASRC1L_ENA	0	ASRC1 Left Enable (Left ASRC channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
	0	ASRC1R_ENA	0	ASRC1 Right Enable (Right ASRC channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
R3809 (0EE1h) ASRC_STATUS	3	ASRC2L_ENA_STS	0	ASRC2 Left Enable Status (Left ASRC channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
	2	ASRC2R_ENA_STS	0	ASRC2 Right Enable Status (Right ASRC channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
	1	ASRC1L_ENA_STS	0	ASRC1 Left Enable Status (Left ASRC channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
	0	ASRC1R_ENA_STS	0	ASRC1 Right Enable Status (Right ASRC channel from ASYNCCLK domain to SYSCLK domain) 0 = Disabled 1 = Enabled
R3810 (0EE2h) ASRC_RATE1	14:11	ASRC_RATE1 [3:0]	0000	ASRC Sample Rate select for SYSCLK domain 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 48kHz. The ASRC_IN1L_SRC and ASRC_IN1R_SRC registers should be set to 00h before ASRC_RATE1.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3811 (0EE3h) ASRC_RATE2	14:11	ASRC_RATE2 [3:0]	1000	ASRC Sample Rate select for ASYNCCLK domain 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 48kHz. The ASRC_IN2L_SRC and ASRC_IN2R_SRC registers should be set to 00h before ASRC_RATE2.

Table 22 Digital Core ASRC Control

ISOCHRONOUS SAMPLE RATE CONVERTER (ISRC)

The CS47L24 supports multiple signal paths through the digital core. The Isochronous Sample Rate Converters (ISRCs) provide sample rate conversion between synchronised sample rates on the SYSCLK clock domain, or between synchronised sample rates on the ASYNCCLK clock domain.

There are three Isochronous Sample Rate Converters (ISRCs). Each of these provides four signal paths between two different sample rates, as illustrated in Figure 29.

The sample rates associated with each ISRC can be set independently. Note that the two sample rates associated with any single ISRC must both be referenced to the same clock domain (SYSCLK or ASYNCCLK).

When an ISRC is used on the SYSCLK domain, then the associated sample rates may be selected from SAMPLE_RATE_1, SAMPLE_RATE_2 or SAMPLE_RATE_3.

When an ISRC is used on the ASYNCCLK domain, then the associated sample rates are ASYNC_SAMPLE_RATE_1 and ASYNC_SAMPLE_RATE_2.

See “Clocking and Sample Rates” for details of the sample rate control registers.

Each ISRC supports sample rates in the range 8kHz to 192kHz. The higher of the sample rates associated with each ISRC must be an integer multiple of the lower sample rate; all possible integer ratios are supported (i.e., up to 24).

Each ISRC converts between a sample rate selected by ISRCn_FSL and a sample rate selected by ISRCn_FSH, (where ‘n’ identifies the applicable ISRC 1, 2 or 3). Note that, in each case, the higher of the two sample rates must be selected by ISRCn_FSH.

The ISRC*n*_FSL and ISRC*n*_FSH registers should not be changed if any of the respective *_SRC*n* registers is non-zero. The associated *_SRC*n* registers should be cleared to 00h before writing new values to ISRC*n*_FSL or ISRC*n*_FSH. A minimum delay of 125µs should be allowed between clearing the *_SRC*n* registers and writing to the associated ISRC*n*_FSL or ISRC*n*_FSH registers. See Table 23 for further details.

The ISRCn ‘interpolation’ paths (increasing sample rate) are enabled using the ISRCn_INT1_ENA, ISRCn_INT2_ENA, ISRCn_INT3_ENA and ISRCn_INT4_ENA register bits.

The ISRCn ‘decimation’ paths (decreasing sample rate) are enabled using the ISRCn_DEC1_ENA, ISRCn_DEC2_ENA, ISRCn_DEC3_ENA and ISRCn_DEC4_ENA register bits.

A notch filter is provided in each of the ISRC paths; these are enabled using the ISRCn_NOTCH_ENA bits. The filter is configured automatically according to the applicable sample rate(s). It is recommended to enable the filter for typical applications. Disabling the filter will provide maximum ‘pass’ bandwidth, at the expense of degraded stopband attenuation.

The CS47L24 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the commanded ISRC and digital mixing functions. If an attempt is made to enable an ISRC signal path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error condition can be monitored using the GPIO and/or Interrupt functions. See “General Purpose Input / Output” and “Interrupts” for further details.

The status bits in Registers R1600 to R3000 indicate the status of each of the digital mixers. If an Underclocked Error condition occurs, then these bits provide readback of which mixer(s) have been successfully enabled.

The Isochronous Sample Rate Converter (ISRC) signal paths and control registers are illustrated in Figure 29.

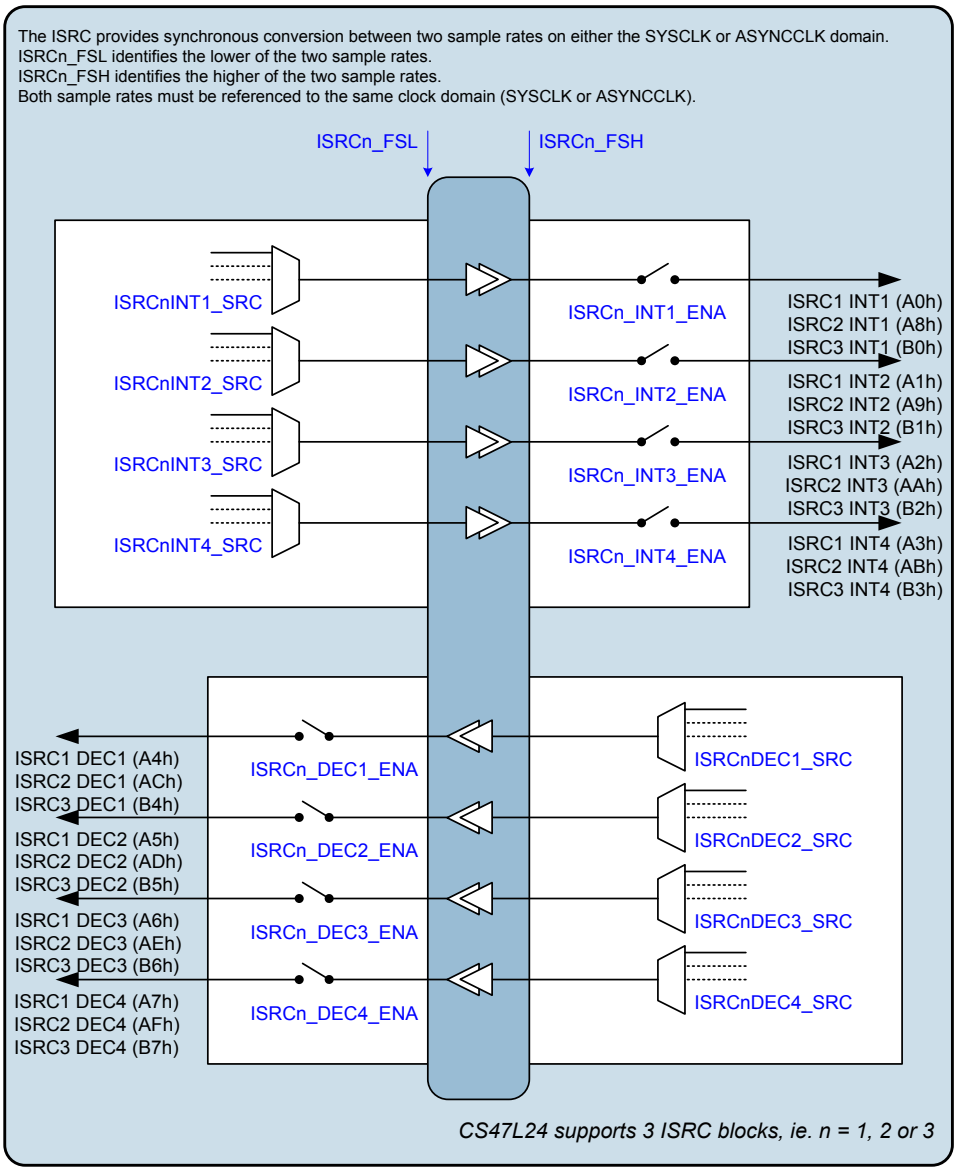


Figure 29 Isochronous Sample Rate Converters (ISRCs)

The ISRC input control registers (see Figure 29) are located at register addresses R2816 (B00h) through to R3000 (0BB8h).

The full list of digital mixer control registers is provided in the “Register Map” section (Register R1600 through to R3000). Generic register definitions are provided in Table 7.

The *_SRC registers select the input source(s) for the respective ISRC processing blocks. Note that the selected input source(s) must be configured for the same sample rate as the ISRC to which they are connected.

The bracketed numbers in Figure 29, e.g.,”(A4h)” indicate the corresponding *_SRC register setting for selection of that signal as an input to another digital core function.

The register bits associated with the ISRCs are described in Table 23.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3824 (0EF0h) ISRC 1 CTRL 1	14:11	ISRC1_FSH [3:0]	0000	ISRC1 High Sample Rate (Sets the higher of the ISRC1 sample rates) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. The ISRC1_FSH and ISRC1_FSL fields must both select sample rates referenced to the same clock domain (SYSCLK or ASYNCCLK). All ISRC1_DEC*n*_SRC registers should be set to 00h before changing ISRC1_FSH.
R3825 (0EF1h) ISRC 1 CTRL 2	14:11	ISRC1_FSL [3:0]	0000	ISRC1 Low Sample Rate (Sets the lower of the ISRC1 sample rates) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. The ISRC1_FSH and ISRC1_FSL fields must both select sample rates referenced to the same clock domain (SYSCLK or ASYNCCLK). All ISRC1_INT*n*_SRC registers should be set to 00h before changing ISRC1_FSL.
R3826 (0EF2h) ISRC 1 CTRL 3	15	ISRC1_INT1_ENA	0	ISRC1 INT1 Enable (Interpolation Channel 1 path from ISRC1_FSL rate to ISRC1_FSH rate) 0 = Disabled 1 = Enabled
	14	ISRC1_INT2_ENA	0	ISRC1 INT2 Enable (Interpolation Channel 2 path from ISRC1_FSL rate to ISRC1_FSH rate) 0 = Disabled 1 = Enabled
	13	ISRC1_INT3_ENA	0	ISRC1 INT3 Enable (Interpolation Channel 3 path from ISRC1_FSL rate to ISRC1_FSH rate) 0 = Disabled 1 = Enabled
	12	ISRC1_INT4_ENA	0	ISRC1 INT4 Enable (Interpolation Channel 4 path from ISRC1_FSL rate to ISRC1_FSH rate) 0 = Disabled 1 = Enabled
	9	ISRC1_DEC1_ENA	0	ISRC1 DEC1 Enable (Decimation Channel 1 path from ISRC1_FSH rate to ISRC1_FSL rate) 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	8	ISRC1_DEC2_ENA	0	ISRC1 DEC2 Enable (Decimation Channel 2 path from ISRC1_FSH rate to ISRC1_FSL rate) 0 = Disabled 1 = Enabled
	7	ISRC1_DEC3_ENA	0	ISRC1 DEC3 Enable (Decimation Channel 3 path from ISRC1_FSH rate to ISRC1_FSL rate) 0 = Disabled 1 = Enabled
	6	ISRC1_DEC4_ENA	0	ISRC1 DEC4 Enable (Decimation Channel 4 path from ISRC1_FSH rate to ISRC1_FSL rate) 0 = Disabled 1 = Enabled
	0	ISRC1_NOTCH_ENA	0	ISRC1 Notch Filter Enable 0 = Disabled 1 = Enabled It is recommended to enable the notch filter for typical applications.
R3827 (0EF3h) ISRC 2 CTRL 1	14:11	ISRC2_FSH [3:0]	0000	ISRC2 High Sample Rate (Sets the higher of the ISRC2 sample rates) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. The ISRC2_FSH and ISRC2_FSL fields must both select sample rates referenced to the same clock domain (SYSCLK or ASYNCCLK). All ISRC2_DEC*n*_SRC registers should be set to 00h before changing ISRC2_FSH.
R3828 (0EF4h) ISRC 2 CTRL 2	14:11	ISRC2_FSL [3:0]	0000	ISRC2 Low Sample Rate (Sets the lower of the ISRC2 sample rates) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. The ISRC2_FSH and ISRC2_FSL fields must both select sample rates referenced to the same clock domain (SYSCLK or ASYNCCLK). All ISRC2_INT*n*_SRC registers should be set to 00h before changing ISRC2_FSL.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3829 (0EF5h) ISRC 2 CTRL 3	15	ISRC2_INT1_ENA	0	ISRC2 INT1 Enable (Interpolation Channel 1 path from ISRC2_FSL rate to ISRC2_FSH rate) 0 = Disabled 1 = Enabled
	14	ISRC2_INT2_ENA	0	ISRC2 INT2 Enable (Interpolation Channel 2 path from ISRC2_FSL rate to ISRC2_FSH rate) 0 = Disabled 1 = Enabled
	13	ISRC2_INT3_ENA	0	ISRC2 INT3 Enable (Interpolation Channel 3 path from ISRC2_FSL rate to ISRC2_FSH rate) 0 = Disabled 1 = Enabled
	12	ISRC2_INT4_ENA	0	ISRC2 INT4 Enable (Interpolation Channel 4 path from ISRC2_FSL rate to ISRC2_FSH rate) 0 = Disabled 1 = Enabled
	9	ISRC2_DEC1_ENA	0	ISRC2 DEC1 Enable (Decimation Channel 1 path from ISRC2_FSH rate to ISRC2_FSL rate) 0 = Disabled 1 = Enabled
	8	ISRC2_DEC2_ENA	0	ISRC2 DEC2 Enable (Decimation Channel 2 path from ISRC2_FSH rate to ISRC2_FSL rate) 0 = Disabled 1 = Enabled
	7	ISRC2_DEC3_ENA	0	ISRC2 DEC3 Enable (Decimation Channel 3 path from ISRC2_FSH rate to ISRC2_FSL rate) 0 = Disabled 1 = Enabled
	6	ISRC2_DEC4_ENA	0	ISRC2 DEC4 Enable (Decimation Channel 4 path from ISRC2_FSH rate to ISRC2_FSL rate) 0 = Disabled 1 = Enabled
	0	ISRC2_NOTCH_ENA	0	ISRC2 Notch Filter Enable 0 = Disabled 1 = Enabled It is recommended to enable the notch filter for typical applications.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3830 (0EF6h) ISRC 3 CTRL 1	14:11	ISRC3_FSH [3:0]	0000	ISRC3 High Sample Rate (Sets the higher of the ISRC3 sample rates) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. The ISRC3_FSH and ISRC3_FSL fields must both select sample rates referenced to the same clock domain (SYSCLK or ASYNCCLK). All ISRC3_DEC*n*_SRC registers should be set to 00h before changing ISRC3_FSH.
R3831 (0EF7h) ISRC 3 CTRL 2	14:11	ISRC3_FSL [3:0]	0000	ISRC3 Low Sample Rate (Sets the lower of the ISRC3 sample rates) 0000 = SAMPLE_RATE_1 0001 = SAMPLE_RATE_2 0010 = SAMPLE_RATE_3 1000 = ASYNC_SAMPLE_RATE_1 1001 = ASYNC_SAMPLE_RATE_2 All other codes are Reserved. The selected sample rate is valid in the range 8kHz to 192kHz. The ISRC3_FSH and ISRC3_FSL fields must both select sample rates referenced to the same clock domain (SYSCLK or ASYNCCLK). All ISRC3_INT*n*_SRC registers should be set to 00h before changing ISRC3_FSL.
R3832 (0EF8h) ISRC 3 CTRL 3	15	ISRC3_INT1_ENA	0	ISRC3 INT1 Enable (Interpolation Channel 1 path from ISRC3_FSL rate to ISRC3_FSH rate) 0 = Disabled 1 = Enabled
	14	ISRC3_INT2_ENA	0	ISRC3 INT2 Enable (Interpolation Channel 2 path from ISRC3_FSL rate to ISRC3_FSH rate) 0 = Disabled 1 = Enabled
	13	ISRC3_INT3_ENA	0	ISRC3 INT3 Enable (Interpolation Channel 3 path from ISRC3_FSL rate to ISRC3_FSH rate) 0 = Disabled 1 = Enabled
	12	ISRC3_INT4_ENA	0	ISRC3 INT4 Enable (Interpolation Channel 4 path from ISRC3_FSL rate to ISRC3_FSH rate) 0 = Disabled 1 = Enabled
	9	ISRC3_DEC1_ENA	0	ISRC3 DEC1 Enable (Decimation Channel 1 path from ISRC3_FSH rate to ISRC3_FSL rate) 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	8	ISRC3_DEC2_ENA	0	ISRC3 DEC2 Enable (Decimation Channel 2 path from ISRC3_FSH rate to ISRC3_FSL rate) 0 = Disabled 1 = Enabled
	7	ISRC3_DEC3_ENA	0	ISRC3 DEC3 Enable (Decimation Channel 3 path from ISRC3_FSH rate to ISRC3_FSL rate) 0 = Disabled 1 = Enabled
	6	ISRC3_DEC4_ENA	0	ISRC3 DEC4 Enable (Decimation Channel 4 path from ISRC3_FSH rate to ISRC3_FSL rate) 0 = Disabled 1 = Enabled
	0	ISRC3_NOTCH_ENA	0	ISRC3 Notch Filter Enable 0 = Disabled 1 = Enabled It is recommended to enable the notch filter for typical applications.

Table 23 Digital Core ISRC Control

DSP FIRMWARE CONTROL

The CS47L24 digital core incorporates two DSP processing blocks, capable of running a wide range of audio enhancement functions. Different firmware configurations can be loaded onto each DSP, enabling the CS47L24 to be highly customised for specific application requirements. Synchronisation of different DSPs is supported, and shared data memory space is provided for the DSP2 and DSP3 blocks; these features enable enhanced processing capabilities for the associated DSPs.

Examples of the DSP functions include Virtual Surround Sound (VSS), Multiband Compressor (MBC), and the Cirrus Logic SoundClear™ suite of audio processing algorithms. Note that it is possible to implement more than one type of audio enhancement function on a single DSP; the precise combination(s) of functions will vary from one firmware configuration to another.

DSP firmware can be configured using Cirrus Logic-supplied software packages. A software programming guide can also be provided to assist users in developing their own software algorithms - please contact your local Cirrus Logic representative for further information.

In order to use the DSP blocks, the required firmware configuration must first be loaded onto the device by writing the appropriate files to the CS47L24 register map. The firmware configuration will comprise Program, Coefficient and Data content. In some cases, the Coefficient content must be derived using tools provided in Cirrus Logic's WISCE™ evaluation board control software.

Details of how to load the firmware configuration onto the CS47L24 are described below. Note that the WISCE™ evaluation board control software provides support for easy loading of Program, Coefficient and Data content onto the CS47L24. Please contact your local Cirrus Logic representative for more details of the WISCE™ evaluation board control software.

After loading the DSP firmware, the DSP functions must be enabled using the associated register control fields.

The audio signal paths connecting to/from the DSP processing blocks are configured as described in the "Digital Core" section. Note that the DSP firmware must be loaded and enabled before audio signal paths can be enabled.

DSP FIRMWARE MEMORY CONTROL

The DSP firmware memory is programmed by writing to the registers referenced in Table 24. Note that the DSP clock must be configured and enabled for the respective DSP block to support read/write access to these registers.

The CS47L24 Program, Coefficient and Data register memory space is described in Table 24. See "Register Map" for a definition of these register addresses. The shared DSP2/DSP3 memory space is implemented at two different register address locations; note that reading or writing at either address will access the same memory data.

If multiple DSPs write to a shared memory address at the same time, then the address at which the collision occurred will be reported in the DSP3_DUALMEM_COLLISION_ADDR register. Note that this field is coded in 24-bit DSP data word units, and is defined relative to the base address of the applicable shared memory area.

The DSP memory controller provides an input to the Interrupt Controller circuit. An interrupt event is triggered if a memory collision occurs. (Note that the DSP software should be written to ensure this never happens; the interrupt is intended for development purposes only.) See "Interrupts" for more details of the Interrupt event handling.

The Program firmware parameters are formatted as 40-bit words. For this reason, 3 x 16-bit register addresses are required for each 40-bit word.

The Coefficient and Data firmware parameters are formatted as 24-bit words. For this reason, 2 x 16-bit register addresses are required for each 24-bit word.

	DESCRIPTION	REGISTER ADDRESS		DSP MEMORY SIZE
DSP2	Program memory	20_0000h to 20_5FFFh	(24576 registers)	8k x 40-bit words
	Coefficient memory	28_0000h to 28_1FFFh	(8192 registers)	4k x 24-bit words
	X Data memory	29_0000h to 29_BFFFh	(49152 registers)	24k x 24-bit words
	X Data memory (Shared DSP2/DSP3)	2A_6000h to 2A_7FFFh	(8192 registers)	4k x 24-bit words
	Y Data memory	2A_8000h to 2B_3FFFh	(49152 registers)	24k x 24-bit words
DSP3	Program memory	30_0000h to 30_8FFFh	(36864 registers)	12k x 40-bit words
	Coefficient memory	38_0000h to 38_1FFFh	(8192 registers)	4k x 24-bit words
	X Data memory	39_0000h to 3A_1FFFh	(73728 registers)	36k x 24-bit words
	X Data memory (Shared DSP2/DSP3)	3A_6000h to 3A_7FFFh	(8192 registers)	4k x 24-bit words
	Y Data memory	3A_8000h to 3B_3FFFh	(49152 registers)	24k x 24-bit words

Table 24 DSP Program, Coefficient and Data Registers

Clocking is required for any functionality of the DSP processing blocks, including any register read/write operations associated with DSP firmware loading.

The clock source for each DSP is derived from SYSCLK, which must also be enabled. See “Clocking and Sample Rates” for details of how to configure SYSCLK.

The DSP clock frequency is selected using the DSPn_CLK_SEL register. Note that the DSP clock frequency must be less than or equal to the SYSCLK frequency. The frequencies must be integer-related (e.g., divide by 1, 2, 3 etc.).

The clock source for each DSP block is enabled using DSPn_SYS_ENA (where ‘n’ identifies the applicable DSP processing block 1 or 2). The clock must be enabled before (or simultaneous to) enabling the respective DSP Core or DMA channels. The clock must be disabled after (or simultaneous to) disabling the DSP Core and DMA channels.

The DSPn_CLK_SEL_STS fields provide readback of the clock frequency for the respective DSP cores. These can be used to confirm the clock frequency, in cases where code execution has a minimum clock frequency requirement. The DSPn_CLK_SEL_STS field is only valid when the respective DSP Clock is enabled; typical typical usage of this field would be for the DSP core itself to readback the clock status, and to take action as applicable (in particular, if the available clock does not meet the application requirements).

The DSPn_RAM_RDY status bits indicate when the respective DSP firmware memory registers are ready for read/write access. The respective DSP memories should not be accessed until this bit has been set.

The DSP RAM Ready flags are inputs to the Interrupt control circuit and can be used to trigger an interrupt event - see “Interrupts”.

The DSP RAM Ready flags can be output directly on a GPIO pin as an external indication of the DSP RAM Status. See “General Purpose Input / Output” to configure a GPIO pin for this function.

Under default register conditions, the DSP firmware memory contents are retained if the respective clock is disabled, and also during Hardware Reset and Software Reset; this is selectable using the DSPn_MEM_ENA register bits, as described below.

When DSPn_MEM_ENA = 1 (default), the DSP firmware memory is retained when the DSP clock is disabled (i.e., when DSPn_SYS_ENA = 0). It is also retained during Hardware Reset and Software Reset, provided DCVDD is held above its reset threshold.

When DSPn_MEM_ENA = 0, the DSP firmware memory is disabled (and the contents lost) when DSPn_SYS_ENA = 0. It is also disabled during Hardware Reset and Software Reset. Power consumption is reduced when the memory is disabled, but the DSP firmware must then be reloaded when required.

See the “Applications Information” section for a summary of the CS47L24 memory reset conditions.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4608 (1200h) DSP2 Control 1	4	DSP2_MEM_ENA	1	DSP2 Memory Control 0 = DSP2 memory is cleared when DSP2_SYS_ENA=0, and during Hardware Reset or Software Reset. 1 = DSP2 memory is retained when DSP2_SYS_ENA=0. DSP2 memory is retained during Hardware Reset and Software Reset.
	2	DSP2_SYS_ENA	0	DSP2 Clock Enable 0 = Disabled 1 = Enabled The DSP2 Clock must be enabled for DSP2 firmware register access, code execution, or DMA operation. The DSP2 Core must be reset (by writing DSP2_CORE_ENA=0) when disabling the DSP2 Clock.
R4609 (1201h) DSP2 Clocking 1	2:0	DSP2_CLK_SEL [2:0]	000	DSP2 Clock Frequency Select 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) 100 = 73.728MHz (67.7376MHz) 101 = 98.304MHz (90.3168MHz) 110 = 147.456MHz (135.4752MHz) 111 = Reserved The DSP2 Clock must be less than or equal to the SYSCLK frequency. The frequencies must also be integer-related (e.g., divide by 1, 2, 3 etc.). The frequencies in brackets apply for 44.1kHz-related sample rates only (i.e., SAMPLE_RATE_n = 01XXX).
R4612 (1204h) DSP2 Status 1	0	DSP2_RAM_RDY	0	DSP2 Memory Status 0 = Not ready 1 = Ready Note - DSP2 memory should not be accessed until this bit has been set.
R4614 (1206h) DSP2 Status 3	3:1	DSP2_CLK_SEL_STS [2:0	000	DSP2 Clock Frequency (Read only, Only valid when the respective DSP Clock is enabled) 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) 100 = 73.728MHz (67.7376MHz) 101 = 98.304MHz (90.3168MHz) 110 = 147.456MHz (135.4752MHz) 111 = Reserved The frequencies in brackets apply for 44.1kHz-related sample rates only (i.e., SAMPLE_RATE_n = 01XXX).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	DSP2_CLK_AVAIL	0	DSP2 Clock Availability (Read only) 0 = No Clock 1 = Clock Available Note – this bit exists for legacy software support only; it is not recommended for future designs, as the readback may be unreliable on the latest device architectures.
R4864 (1300h) DSP3 Control 1	4	DSP3_MEM_ENA	1	DSP3 Memory Control 0 = DSP3 memory is cleared when DSP3_SYS_ENA=0, and during Hardware Reset or Software Reset. 1 = DSP3 memory is retained when DSP3_SYS_ENA=0. DSP3 memory is retained during Hardware Reset and Software Reset.
	2	DSP3_SYS_ENA	0	DSP3 Clock Enable 0 = Disabled 1 = Enabled The DSP3 Clock must be enabled for DSP3 firmware register access, code execution, or DMA operation. The DSP3 Core must be reset (by writing DSP3_CORE_ENA=0) when disabling the DSP3 Clock.
R4865 (1301h) DSP3 Clocking 1	2:0	DSP3_CLK_SEL [2:0]	000	DSP3 Clock Frequency Select 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) 100 = 73.728MHz (67.7376MHz) 101 = 98.304MHz (90.3168MHz) 110 = 147.456MHz (135.4752MHz) 111 = Reserved The DSP3 Clock must be less than or equal to the SYSCLK frequency. The frequencies must also be integer-related (e.g., divide by 1, 2, 3 etc.). The frequencies in brackets apply for 44.1kHz-related sample rates only (i.e., SAMPLE_RATE_n = 01XXX).
R4868 (1304h) DSP3 Status 1	0	DSP3_RAM_RDY	0	DSP3 Memory Status 0 = Not ready 1 = Ready Note - DSP3 memory should not be accessed until this bit has been set.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4870 (1306h) DSP3 Status 3	3:1	DSP3_CLK_SEL_STS [2:0	000	DSP3 Clock Frequency (Read only, Only valid when the respective DSP Clock is enabled) 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) 100 = 73.728MHz (67.7376MHz) 101 = 98.304MHz (90.3168MHz) 110 = 147.456MHz (135.4752MHz) 111 = Reserved The frequencies in brackets apply for 44.1kHz-related sample rates only (i.e., SAMPLE_RATE_n = 01XXX).
	0	DSP3_CLK_AVAIL	0	DSP3 Clock Availability (Read only) 0 = No Clock 1 = Clock Available Note – this bit exists for legacy software support only; it is not recommended for future designs, as the readback may be unreliable on the latest device architectures.
R4871 (1307h) DSP3 Status 4	15:0	DSP3_DUALMEM_COLLISION_ADDR [15:0]	0000h	DSP3 Dual Memory Collision Address In the event of a DSP3 memory access collision, this field will report the address at which the collision occurred. The address is defined relative to the base address of the shared data memory. The LSB represents one 24-bit DSP memory word.

Table 25 DSP Clocking Control

DSP FIRMWARE EXECUTION

After the DSP firmware has been loaded, and the clocks configured, the DSP blocks are enabled using the DSPn_CORE_ENA register bits. When the DSP is configured and enabled, the firmware execution can be started by writing '1' to the respective DSPn_START bit.

Alternative methods to trigger the firmware execution can also be configured using the DSPn_START_IN_SEL register fields. Note that this provides the capability to synchronously trigger multiple DSP blocks.

Using the DSPn_START_IN_SEL registers, the DSP firmware execution can be linked to the respective DMA function, the IRQ2 status, or to configurable 'DSPn Start' signals from another DSP. The 'DSPn Start' signals are generated within the DSP cores, enabling any of the DSP blocks to trigger code execution in another DSP.

The DSPn_CORE_ENA bit must be set to '1' to enable firmware execution on the respective DSP block. Note that the usage of the DSPn_START bit may vary depending on the particular software that is being executed: in some applications (e.g., when an alternative trigger is selected using DSPn_START_IN_SEL), writing to the DSPn_START bit will not be required.

For read/write access to the DSP firmware memory registers, the respective firmware execution must be disabled by setting the DSPn_CORE_ENA bit to '0'.

The audio signal paths connecting to/from the DSP processing blocks are configured as described in the "Digital Core" section. Note that the DSP firmware must be loaded and enabled before audio signal paths can be enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4608 (1200h) DSP2 Control 1	1	DSP2_CORE_ENA	0	DSP2 Enable Controls the DSP2 firmware execution 0 = Disabled 1 = Enabled
	0	DSP2_START		DSP2 Start Write '1' to Start DSP2 firmware execution
R4664 (1238h) DSP2 External Start Select 1	3:0	DSP2_START_IN_SEL [3:0]	0h	DSP2 Firmware Execution control Selects the trigger for DSP2 firmware execution. 0 = DMA 5 = DSP3 Start 1 6 = DSP3 Start 2 11 = IRQ2 All other codes are Reserved. Note that the DSP2_START bit will also start the DSP2 firmware execution, regardless of this register setting.
R4864 (1300h) DSP3 Control 1	1	DSP3_CORE_ENA	0	DSP3 Enable Controls the DSP3 firmware execution 0 = Disabled 1 = Enabled
	0	DSP3_START		DSP3 Start Write '1' to Start DSP3 firmware execution
R4920 (1338h) DSP3 External Start Select 1	3:0	DSP3_START_IN_SEL [3:0]	0h	DSP3 Firmware Execution control Selects the trigger for DSP3 firmware execution. 0 = DMA 3 = DSP2 Start 1 4 = DSP2 Start 2 11 = IRQ2 All other codes are Reserved. Note that the DSP3_START bit will also start the DSP3 firmware execution, regardless of this register setting.

Table 26 DSP Firmware Execution

DSP DIRECT MEMORY ACCESS (DMA) CONTROL

Each DSP provides a multi-channel DMA function; this is configured using the registers described in Table 27.

There are 8 WDMA (DSP input) and 6 RDMA (DSP output) channels for each DSP; these are enabled using the DSPn_WDMA_CHANNEL_ENABLE and DSPn_RDMA_CHANNEL_ENABLE fields. The status of each WDMA channel is indicated in DSPn_WDMA_ACTIVE_CHANNELS.

The DMA can access the X data memory or Y data memory associated with the respective DSP. The applicable memory is selected using bit [15] of the respective *_START_ADDRESS register.

The start address of each DMA channel is configured as described in Table 27. Note that the required address is defined relative to the base address of the selected (X data or Y data) memory.

The buffer length of the DMA channels is configured using the DSPn_WDMA_BUFFER_LENGTH field. The selected buffer length applies to all enabled WDMA or RDMA channels.

Note that the start address registers, and WDMA buffer length registers, are defined in 24-bit DSP data word units. This means that the LSB of these fields represents one 24-bit DSP memory word. (Note that this differs from the CS47L24 register map layout, as described in Table 24).

The parameters of a DMA channel (i.e., Start Address or Offset Address) must not be changed whilst the respective DMA is enabled. All of the DMA channels must be disabled before changing the WDMA buffer length.

Each DMA channel uses a twin buffer mechanism to support uninterrupted data flow through the DSP. The buffers are called ‘ping’ and ‘pong’ respectively, and are of configurable size, as noted above. Data is transferred to/from each of the buffers in turn.

When the ‘ping’ input data buffer is full, the DSPn_PING_FULL bit will be asserted (set to ‘1’), and a ‘DSP Start’ signal will be generated. The ‘Start’ signal from the DMA is typically used to start Firmware execution, as noted in Table 26. Meanwhile, further DSP input data will be filling up the ‘pong’ buffer.

When the ‘pong’ input buffer is full, the DSPn_PONG_FULL bit will be asserted, and another ‘DSP Start’ signal will be generated. The DSP Firmware must take care to read the input data from the applicable buffer, in accordance with the DSPn_PING_FULL and DSPn_PONG_FULL status bits.

Twin buffers are also used on the DSP output (RDMA) channels. The output ‘ping’ buffers are emptied at the same time as the input ‘ping’ buffers are filled; the output ‘pong’ buffers are emptied at the same time as the input ‘pong’ buffers are filled.

Further details of the DMA are provided in the software programming guide - please contact your local Cirrus Logic representative if required.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4613 (1205h) DSP2 Status 2	15	DSP2_PING_FULL	0	DSP2 WDMA Ping Buffer Status 0 = Not Full 1 = Full
	14	DSP2_PONG_FULL	0	DSP2 WDMA Pong Buffer Status 0 = Not Full 1 = Full
	7:0	DSP2_WDMA_ACTIVE_CHANNELS [7:0]	00h	DSP2 WDMA Channel Status There are 8 WDMA channels; each bit of this field indicates the status of the respective WDMA channel. Each bit is coded as: 0 = Inactive 1 = Active
R4624 (1210h) to R4631 (1217h)	15:0	DSP2_START_ADDRESS_WDMA_BUFFER_n [15:0]	0000h	DSP2 WDMA Channel n Start Address Bit [15] = Memory select 0 = X Data memory 1 = Y Data memory Bits [14:0] = Address select The address is defined relative to the base address of the applicable data memory. The LSB represents one 24-bit DSP memory word. Note that the start address is also controlled by the respective DSP2_WDMA_CHANNEL_OFFSET bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4640 (1220h) to R4645 (1225h)	15:0	DSP2_START_ADDRESS_RDMA_BUFFER_n [15:0]	0000h	DSP2 RDMA Channel n Start Address Bit [15] = Memory select 0 = X Data memory 1 = Y Data memory Bits [14:0] = Address select The address is defined relative to the base address of the applicable data memory. The LSB represents one 24-bit DSP memory word. Note that the start address is also controlled by the respective DSP2_RDMA_CHANNEL_OFFSET bit.
R4656 (1230h) DSP2 WDMA Config 1	13:0	DSP2_WDMA_BUFFER_LENGTH [13:0]	0000h	DSP2 DMA Buffer Length Selects the amount of data transferred in each DMA channel. The LSB represents one 24-bit DSP memory word.
R4657 (1231h) DSP2 WDMA Config 2	7:0	DSP2_WDMA_CHANNEL_ENABLE [7:0]	00h	DSP2 WDMA Channel Enable There are 8 WDMA channels; each bit of this field enables the respective WDMA channel. Each bit is coded as: 0 = Disabled 1 = Enabled
R4658 (1232h) DSP2 WDMA Offset 1	7:0	DSP2_WDMA_CHANNEL_OFFSET [7:0]		DSP2 WDMA Channel Offset There are 8 WDMA channels; each bit of this field offsets the Start Address of the respective WDMA channel. Each bit is coded as: 0 = No offset 1 = Offset by 8000h
R4660 (1234h) DSP2 RDMA Config 1	5:0	DSP2_RDMA_CHANNEL_ENABLE [5:0]	00h	DSP2 RDMA Channel Enable There are 6 RDMA channels; each bit of this field enables the respective RDMA channel. Each bit is coded as: 0 = Disabled 1 = Enabled
R4661 (1235h) DSP2 RDMA Offset 1	5:0	DSP2_RDMA_CHANNEL_OFFSET [7:0]		DSP2 RDMA Channel Offset There are 6 RDMA channels; each bit of this field offsets the Start Address of the respective RDMA channel. Each bit is coded as: 0 = No offset 1 = Offset by 8000h
R4869 (1305h) DSP3 Status 2	15	DSP3_PING_FULL	0	DSP3 WDMA Ping Buffer Status 0 = Not Full 1 = Full
	14	DSP3_PONG_FULL	0	DSP3 WDMA Pong Buffer Status 0 = Not Full 1 = Full
	7:0	DSP3_WDMA_ACTIVE_CHANNELS [7:0]	00h	DSP3 WDMA Channel Status There are 8 WDMA channels; each bit of this field indicates the status of the respective WDMA channel. Each bit is coded as: 0 = Inactive 1 = Active

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4880 (1310h) to R4887 (1317h)	15:0	DSP3_START_ADDRESS_WDMA_BUFFER_n [15:0]		DSP3 WDMA Channel n Start Address Bit [15] = Memory select 0 = X Data memory 1 = Y Data memory Bits [14:0] = Address select The address is defined relative to the base address of the applicable data memory. The LSB represents one 24-bit DSP memory word. Note that the start address is also controlled by the respective DSP3_WDMA_CHANNEL_OFFSET bit.
R4896 (1320h) to R4901 (1325h)	15:0	DSP3_START_ADDRESS_RDMA_BUFFER_n [15:0]		DSP3 RDMA Channel n Start Address Bit [15] = Memory select 0 = X Data memory 1 = Y Data memory Bits [14:0] = Address select The address is defined relative to the base address of the applicable data memory. The LSB represents one 24-bit DSP memory word. Note that the start address is also controlled by the respective DSP3_RDMA_CHANNEL_OFFSET bit.
R4912 (1330h) DSP3 WDMA Config 1	13:0	DSP3_WDMA_BUFFER_LENGTH [13:0]	0000h	DSP3 DMA Buffer Length Selects the amount of data transferred in each DMA channel. The LSB represents one 24-bit DSP memory word.
R4913 (1331h) DSP3 WDMA Config 2	7:0	DSP3_WDMA_CHANNEL_ENABLE [7:0]	00h	DSP3 WDMA Channel Enable There are 8 WDMA channels; each bit of this field enables the respective WDMA channel. Each bit is coded as: 0 = Disabled 1 = Enabled
R4914 (1332h) DSP3 WDMA Offset 1	7:0	DSP3_WDMA_CHANNEL_OFFSET [7:0]		DSP3 WDMA Channel Offset There are 8 WDMA channels; each bit of this field offsets the Start Address of the respective WDMA channel. Each bit is coded as: 0 = No offset 1 = Offset by 8000h
R4916 (1334h) DSP3 RDMA Config 1	5:0	DSP3_RDMA_CHANNEL_ENABLE [5:0]	00h	DSP3 RDMA Channel Enable There are 6 RDMA channels; each bit of this field enables the respective RDMA channel. Each bit is coded as: 0 = Disabled 1 = Enabled
R4917 (1335h) DSP3 RDMA Offset 1	5:0	DSP3_RDMA_CHANNEL_OFFSET [7:0]		DSP3 RDMA Channel Offset There are 6 RDMA channels; each bit of this field offsets the Start Address of the respective RDMA channel. Each bit is coded as: 0 = No offset 1 = Offset by 8000h

Table 27 DSP Direct Memory Access (DMA) Control

DSP DEBUG SUPPORT

General purpose 'scratch' registers are provided for each DSP. These have no assigned function, and can be used to assist in algorithm development.

The JTAG interface provides test and debug access to the CS47L24, as described in the "JTAG Interface" section. The JTAG interface clock can be enabled independently for each DSP core, using the DSPn_DBG_CLK_ENA register bits.

When using the JTAG interface to access any DSP core, the respective DSPn_DBG_CLK_ENA, DSPn_SYS_ENA, and DSPn_CORE_ENA bits must all be set.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4608 (1200h) DSP2 Control 1	3	DSP2_DBG_CLK_ENA	0	DSP2 Debug Clock Enable 0 = Disabled 1 = Enabled
R4672 (1240h) DSP2 Scratch 0	15:0	DSP2_SCRATCH_0 [15:0]	0000h	DSP2 Scratch Register 0
R4673 (1241h) DSP2 Scratch 1	15:0	DSP2_SCRATCH_1 [15:0]	0000h	DSP2 Scratch Register 1
R4674 (1242h) DSP2 Scratch 2	15:0	DSP2_SCRATCH_2 [15:0]	0000h	DSP2 Scratch Register 2
R4675 (1243h) DSP2 Scratch 3	15:0	DSP2_SCRATCH_3 [15:0]	0000h	DSP2 Scratch Register 3
R4864 (1300h) DSP3 Control 1	3	DSP3_DBG_CLK_ENA	0	DSP3 Debug Clock Enable 0 = Disabled 1 = Enabled
R4928 (1340h) DSP3 Scratch 0	15:0	DSP3_SCRATCH_0 [15:0]	0000h	DSP3 Scratch Register 0
R4929 (1341h) DSP3 Scratch 1	15:0	DSP3_SCRATCH_1 [15:0]	0000h	DSP3 Scratch Register 1
R4930 (1342h) DSP3 Scratch 2	15:0	DSP3_SCRATCH_2 [15:0]	0000h	DSP3 Scratch Register 2
R4931 (1343h) DSP3 Scratch 3	15:0	DSP3_SCRATCH_3 [15:0]	0000h	DSP3 Scratch Register 3

Table 28 DSP Debug Support

DIGITAL AUDIO INTERFACE

The CS47L24 provides three audio interfaces, AIF1, AIF2 and AIF3. Each of these is independently configurable on the respective transmit (TX) and receive (RX) paths. AIF1 supports up to 8 channels of input and output signal paths; AIF2 supports up to 6 channels of input and output signal paths; AIF3 supports up to 2 channels of input and output signal paths.

The data source(s) for the audio interface transmit (TX) paths can be selected from any of the CS47L24 input signal paths, or from the digital core processing functions. The audio interface receive (RX) paths can be selected as inputs to any of the digital core processing functions or digital core outputs. See “Digital Core” for details of the digital core routing options.

The digital audio interfaces provide flexible connectivity for multiple processors and other audio devices. Typical connections include Applications Processor, Baseband Processor and Wireless Transceiver. A typical configuration is illustrated in Figure 30.

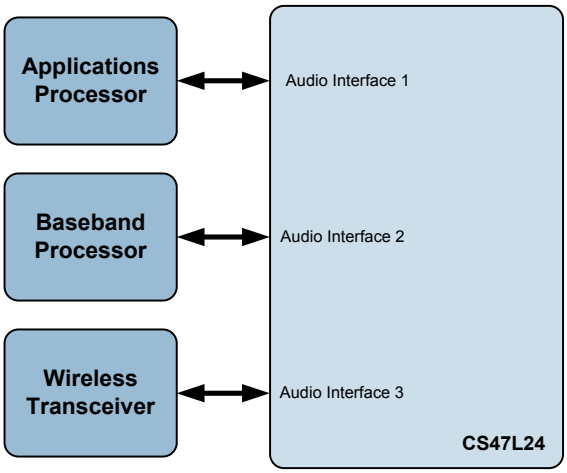


Figure 30 Typical AIF Connections

In the general case, the digital audio interface uses four pins:

- TXDAT: Data output
- RXDAT: Data input
- BCLK: Bit clock, for synchronisation
- LRCLK: Left/Right data alignment clock

In master interface mode, the clock signals BCLK and LRCLK are outputs from the CS47L24. In slave mode, these signals are inputs, as illustrated below.

Four different audio data formats are supported by the digital audio interface:

- DSP mode A
- DSP mode B
- I2S
- Left Justified

The Left Justified and DSP-B modes are valid in Master mode only (i.e., BCLK and LRCLK are outputs from the CS47L24). These modes cannot be supported in Slave mode.

All four of these modes are MSB first. Data words are encoded in 2’s complement format. Each of the audio interface modes is described in the following sections. Refer to the “Signal Timing Requirements” section for timing information.

Two variants of DSP mode are supported - ‘Mode A’ and ‘Mode B’. Mono PCM operation can be supported using the DSP modes.

MASTER AND SLAVE MODE OPERATION

The CS47L24 digital audio interfaces can operate as a master or slave as shown in Figure 31 and Figure 32. The associated control bits are described in “Digital Audio Interface Control”.

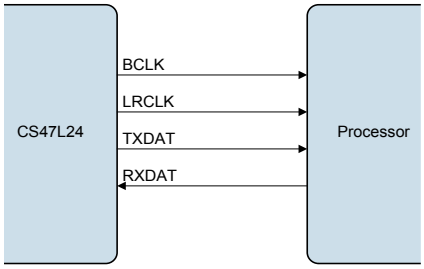


Figure 31 Master Mode

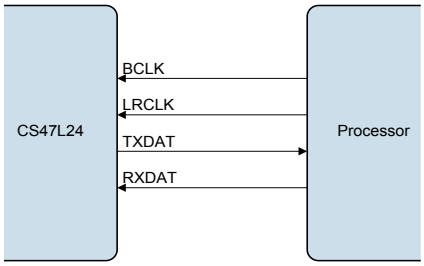


Figure 32 Slave Mode

AUDIO DATA FORMATS

The CS47L24 digital audio interfaces can be configured to operate in I^2S, Left-Justified, DSP-A or DSP-B interface modes. Note that Left-Justified and DSP-B modes are valid in Master mode only (i.e., BCLK and LRCLK are outputs from the CS47L24).

The digital audio interfaces also provide flexibility to support multiple ‘slots’ of audio data within each LRCLK frame. This flexibility allows multiple audio channels to be supported within a single LRCLK frame.

The data formats described in this section are generic descriptions, assuming only one stereo pair of audio samples per LRCLK frame. In these cases, the AIF is configured to transmit (or receive) in the first available position in each frame (i.e., the Slot 0 position).

The options for multi-channel operation are described in the following section (“AIF Timeslot Configuration”).

The audio data modes supported by the CS47L24 are described below. Note that the polarity of the BCLK and LRCLK signals can be inverted if required; the following descriptions all assume the default, non-inverted polarity of these signals.

In DSP mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK following a rising edge of LRCLK. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In master mode, the LRCLK output will resemble the frame pulse shown in Figure 33 and Figure 34. In slave mode, it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs at least one BCLK period before the rising edge of the next frame pulse.

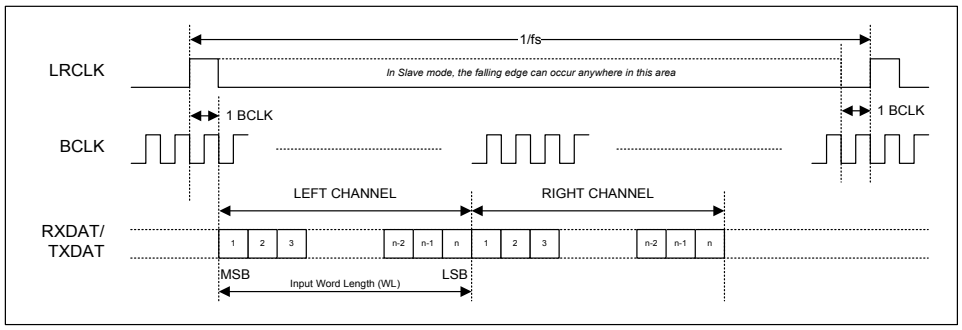


Figure 33 DSP Mode A Data Format

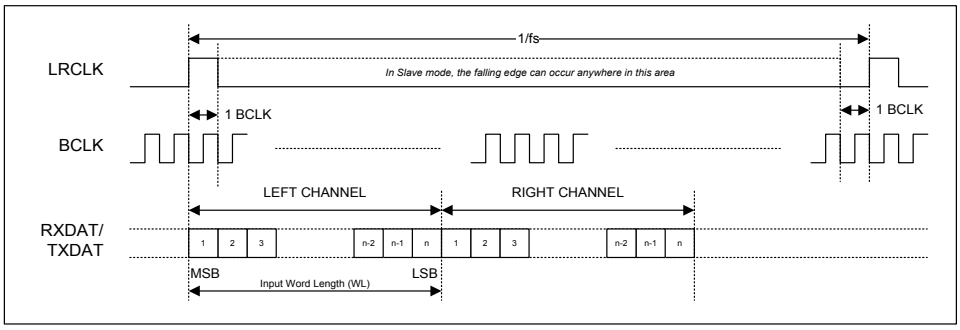


Figure 34 DSP Mode B Data Format

PCM operation is supported in DSP interface mode. CS47L24 data that is output on the Left Channel will be read as mono PCM data by the receiving equipment. Mono PCM data received by the CS47L24 will be treated as Left Channel data. This data may be routed to the Left/Right playback paths using the control fields described in the "Digital Core" section.

In I^2S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

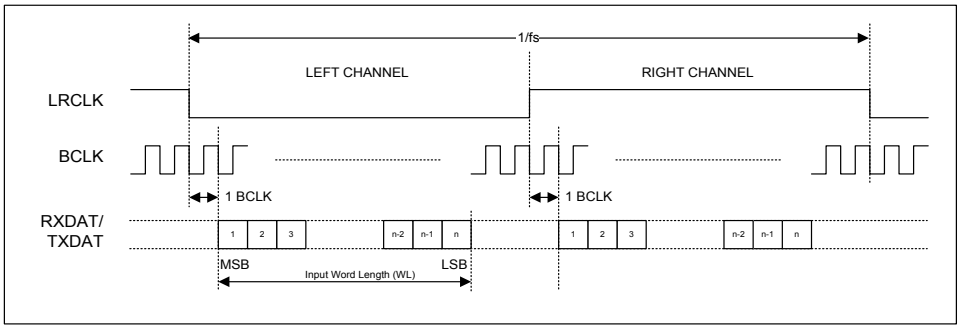


Figure 35 I2S Data Format (assuming n-bit word length)

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.

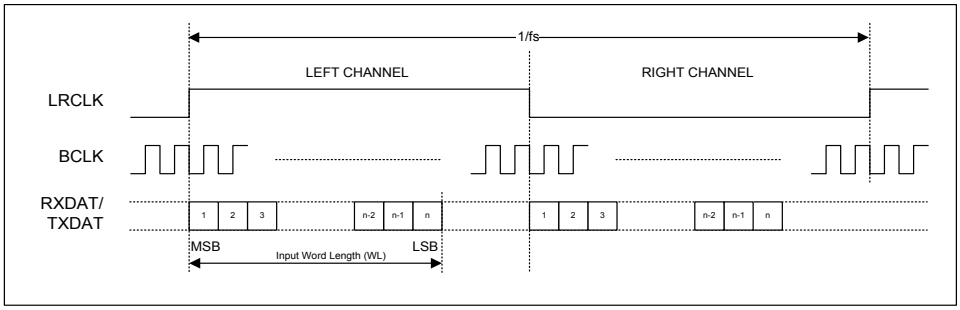


Figure 36 Left Justified Data Format (assuming n-bit word length)

AIF TIMESLOT CONFIGURATION

Digital audio interfaces AIF1 and AIF2 support multi-channel operation; AIF1 supports up to 8 channels of input and output signal paths; AIF2 supports up to 6 channels of input and output signal paths. A high degree of flexibility is provided to define the position of the audio samples within each LRCLK frame; the audio channel samples may be arranged in any order within the frame.

AIF3 also provides flexible configuration options, but supports only 1 stereo input and 1 stereo output path.

Note that, on each interface, all input and output channels must operate at the same sample rate (fs).

Each of the audio channels can be enabled or disabled independently on the transmit (TX) and receive (RX) signal paths. For each enabled channel, the audio samples are assigned to one timeslot within the LRCLK frame.

In DSP modes, the timeslots are ordered consecutively from the start of the LRCLK frame. In I2S and Left-Justified modes, the even-numbered timeslots are arranged in the first half of the LRCLK frame, and the odd-numbered timeslots are arranged in the second half of the frame.

The timeslots are assigned independently for the transmit (TX) and receive (RX) signal paths. There is no requirement to assign every available timeslot to an audio sample; some slots may be unused, if desired. Care is required, however, to ensure that no timeslot is allocated to more than one audio channel.

The number of BCLK cycles within a slot is configurable; this is the Slot Length. The number of valid data bits within a slot is also configurable; this is the Word Length. The number of BCLK cycles per LRCLK frame must be configured; it must be ensured that there are enough BCLK cycles within each LRCLK frame to transmit or receive all of the enabled audio channels.

Examples of the AIF Timeslot Configurations are illustrated in Figure 37 to Figure 40. One example is shown for each of the four possible data formats.

Figure 37 shows an example of DSP Mode A format. Four enabled audio channels are shown, allocated to timeslots 0 through to 3.

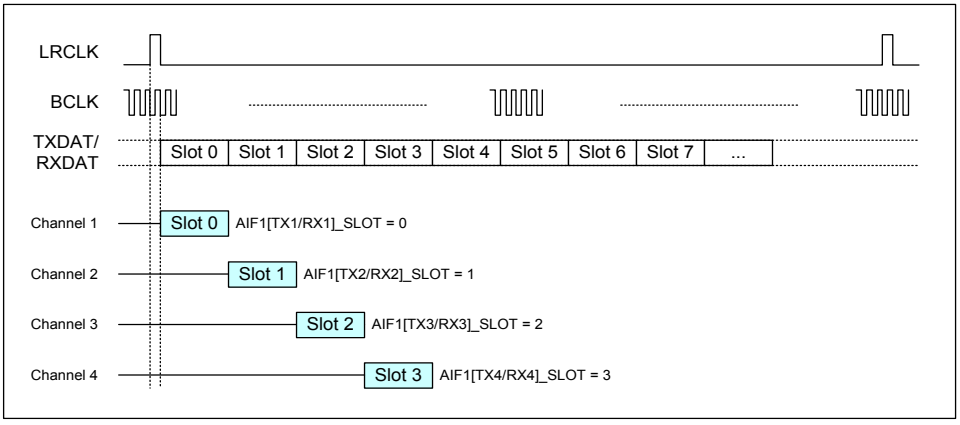


Figure 37 DSP Mode A Example

Figure 38 shows an example of DSP Mode B format. Six enabled audio channels are shown, with timeslots 4 and 5 ususued.

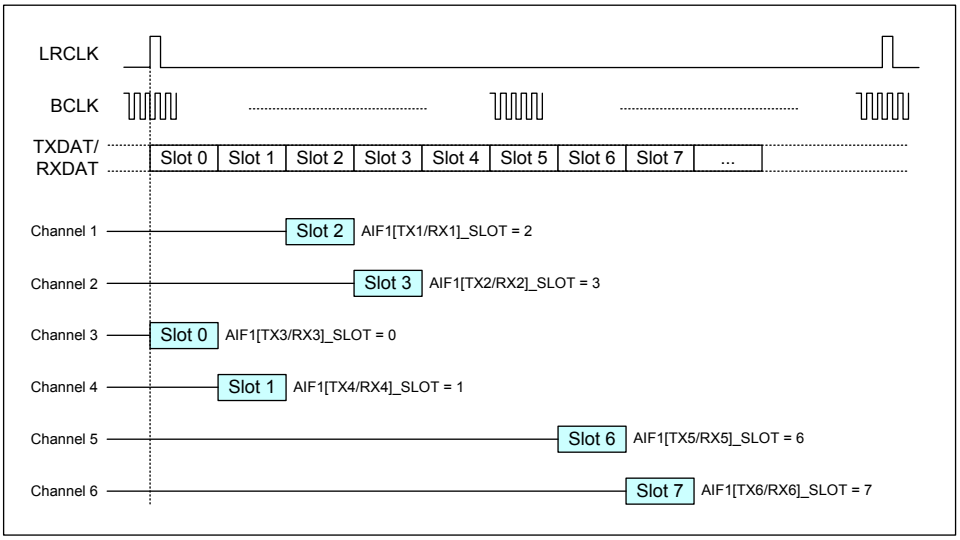


Figure 38 DSP Mode B Example

Figure 39 shows an example of I2S format. Four enabled channels are shown, allocated to timeslots 0 through to 3.

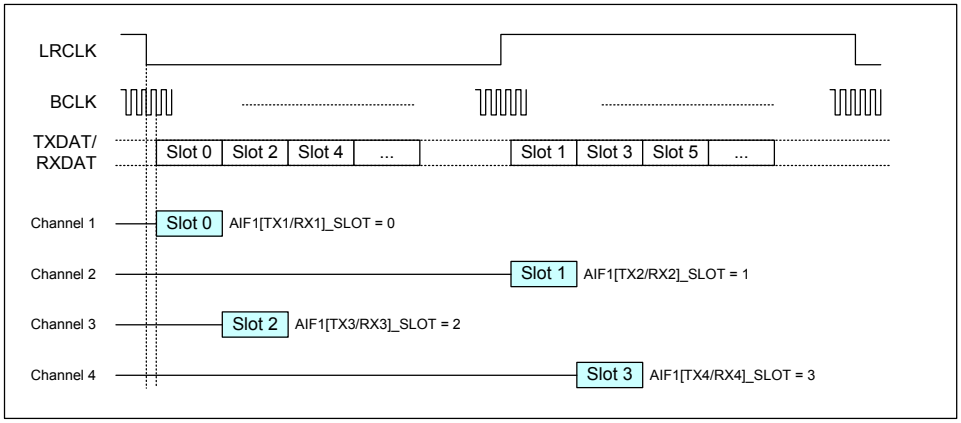


Figure 39 I2S Example

Figure 40 shows an example of Left Justified format. Six enabled channels are shown.

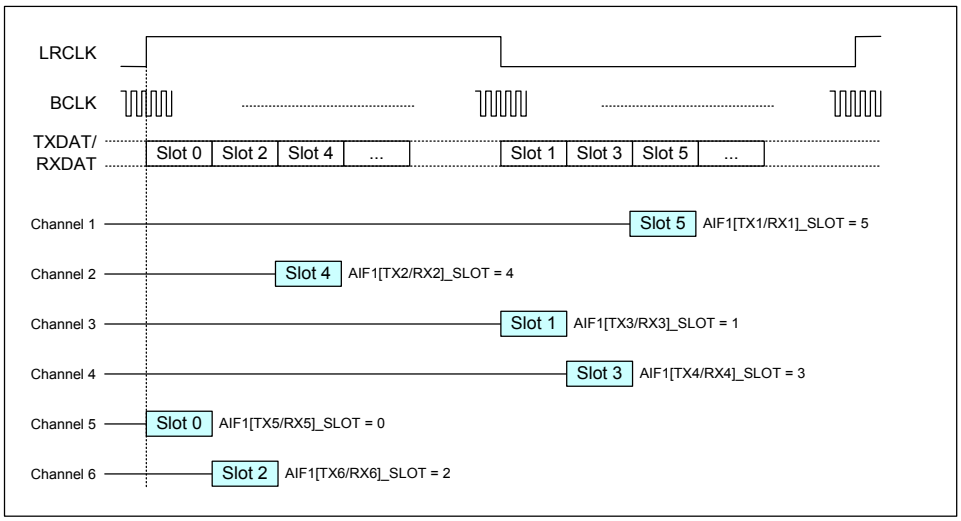


Figure 40 Left Justifed Example

TDM OPERATION BETWEEN THREE OR MORE DEVICES

The AIF operation described above illustrates how multiple audio channels can be interleaved on a single TXDAT or RXDAT pin. The interface uses Time Division Multiplexing (TDM) to allocate time periods to each of the audio channels in turn.

This form of TDM is implemented between two devices, using the electrical connections illustrated in Figure 31 or Figure 32.

It is also possible to implement TDM between three or more devices. This allows one CODEC to receive audio data from two other devices simultaneously on a single audio interface, as illustrated in Figure 41, Figure 42 and Figure 43.

The CS47L24 provides full support for TDM operation. The TXDAT pin can be tri-stated when not transmitting data, in order to allow other devices to transmit on the same wire. The behaviour of the TXDAT pin is configurable, to allow maximum flexibility to interface with other devices in this way.

Typical configurations of TDM operation between three devices are illustrated in Figure 41, Figure 42 and Figure 43.

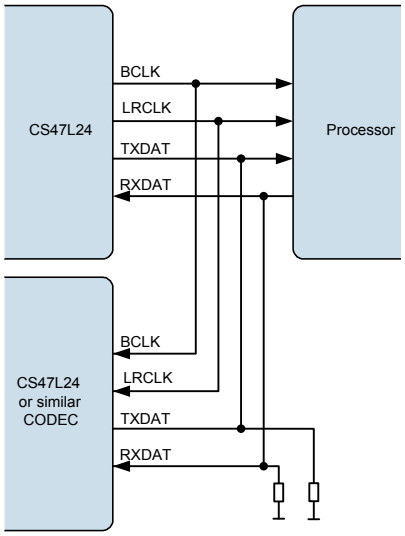


Figure 41 TDM with CS47L24 as Master

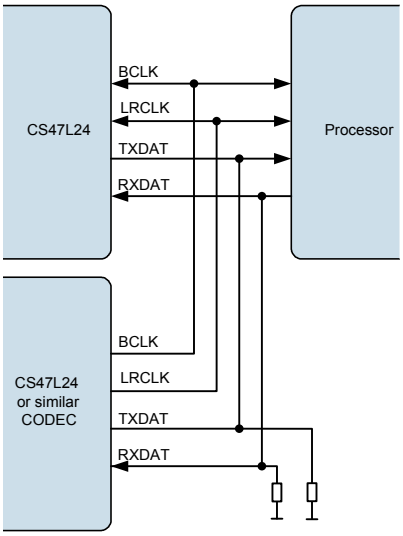


Figure 42 TDM with Other CODEC as Master

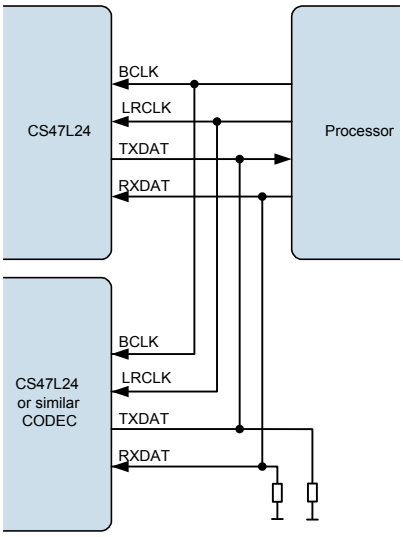


Figure 43 TDM with Processor as Master

Note:

The CS47L24 is a 24-bit device. If the user operates the CS47L24 in 32-bit mode then the 8 LSBs will be ignored on the receiving side and not driven on the transmitting side. It is therefore recommended to add a pull-down resistor if necessary to the RXDAT line and the TXDAT line in TDM mode.

DIGITAL AUDIO INTERFACE CONTROL

This section describes the configuration of the CS47L24 digital audio interface paths.

AIF1 supports up to 8 input signal paths and up to 8 output signal paths; AIF2 supports up to 6 channels of input and output signal paths; AIF3 supports up to 2 channels of input and output signal paths. The digital audio interfaces AIF1, AIF2 and AIF3 can be configured as Master or Slave interfaces; mixed master/slave configurations are also possible.

Each input and output signal path can be independently enabled or disabled. The AIF output (TX) and AIF input (RX) paths use shared BCLK and LRCLK control signals.

The digital audio interface supports flexible data formats, selectable word-length, configurable timeslot allocations and TDM tri-state control.

The audio interfaces can be re-configured whilst enabled, including changes to the LRCLK frame length and the channel timeslot configurations. Care is required to ensure that any 'on-the-fly' re-configuration does not cause corruption to the active signal paths. Wherever possible, it is recommended to disable all channels before changing the AIF configuration.

As noted in the applicable register descriptions, some of the AIF control fields are locked and cannot be updated whilst AIF channels are enabled; this is to ensure continuity of the respective BCLK and LRCLK signals.

AIF SAMPLE RATE CONTROL

The AIF RX inputs may be selected as input to the digital mixers or signal processing functions within the CS47L24 digital core. The AIF TX outputs are derived from the respective output mixers.

The sample rate for each digital audio interface AIFn is configured using the respective AIFn_RATE register - see Table 21 within the "Digital Core" section.

Note that sample rate conversion is required when routing the AIF paths to any signal chain that is asynchronous and/or configured for a different sample rate.

AIF MASTER / SLAVE CONTROL

The digital audio interfaces can operate in Master or Slave modes and also in mixed master/slave configurations. In Master mode, the BCLK and LRCLK signals are generated by the CS47L24 when any of the respective digital audio interface channels is enabled. In Slave mode, these outputs are disabled by default to allow another device to drive these pins.

Master mode is selected on the AIFnBCLK pin using the AIFn_BCLK_MSTR register bit. In Master mode, the AIFnBCLK signal is generated by the CS47L24 when one or more AIFn channels is enabled.

When the AIFn_BCLK_FRC bit is set in BCLK master mode, the AIFnBCLK signal is output at all times, including when none of the AIFn channels is enabled.

The AIFnBCLK signal can be inverted in Master or Slave modes using the AIFn_BCLK_INV register.

Master mode is selected on the AIFnLRCLK pin using the AIFn_LRCLK_MSTR register bit. In Master mode, the AIFnLRCLK signal is generated by the CS47L24 when one or more AIFn channels is enabled.

When the AIFn_LRCLK_FRC bit is set in LRCLK master mode, the AIFnLRCLK signal is output at all times, including when none of the AIFn channels is enabled. Note that AIFnLRCLK is derived from AIFnBCLK, and an internal or external AIFnBCLK signal must be present to generate AIFnLRCLK.

The AIFnLRCLK signal can be inverted in Master or Slave modes using the AIFn_LRCLK_INV register.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1280 (0500h) AIF1 BCLK Ctrl	7	AIF1_BCLK_INV	0	AIF1 Audio Interface BCLK Invert 0 = AIF1BCLK not inverted 1 = AIF1BCLK inverted This bit is locked when AIF1 channels are enabled; it can only be changed when all AIF1 channels are disabled.
	6	AIF1_BCLK_FRC	0	AIF1 Audio Interface BCLK Output Control 0 = Normal 1 = AIF1BCLK always enabled in Master mode
	5	AIF1_BCLK_MSTR	0	AIF1 Audio Interface BCLK Master Select 0 = AIF1BCLK Slave mode 1 = AIF1BCLK Master mode This bit is locked when AIF1 channels are enabled; it can only be changed when all AIF1 channels are disabled.
R1282 (0502h) AIF1 Rx Pin Ctrl	2	AIF1_LRCLK_INV	0	AIF1 Audio Interface LRCLK Invert 0 = AIF1LRCLK not inverted 1 = AIF1LRCLK inverted This bit is locked when AIF1 channels are enabled; it can only be changed when all AIF1 channels are disabled.
	1	AIF1_LRCLK_FRC	0	AIF1 Audio Interface LRCLK Output Control 0 = Normal 1 = AIF1LRCLK always enabled in Master mode
	0	AIF1_LRCLK_MSTR	0	AIF1 Audio Interface LRCLK Master Select 0 = AIF1LRCLK Slave mode 1 = AIF1LRCLK Master mode This bit is locked when AIF1 channels are enabled; it can only be changed when all AIF1 channels are disabled.

Table 29 AIF1 Master / Slave Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1344 (0540h) AIF2 BCLK Ctrl	7	AIF2_BCLK_INV	0	AIF2 Audio Interface BCLK Invert 0 = AIF2BCLK not inverted 1 = AIF2BCLK inverted This bit is locked when AIF2 channels are enabled; it can only be changed when all AIF2 channels are disabled.
	6	AIF2_BCLK_FRC	0	AIF2 Audio Interface BCLK Output Control 0 = Normal 1 = AIF2BCLK always enabled in Master mode
	5	AIF2_BCLK_MSTR	0	AIF2 Audio Interface BCLK Master Select 0 = AIF2BCLK Slave mode 1 = AIF2BCLK Master mode This bit is locked when AIF2 channels are enabled; it can only be changed when all AIF2 channels are disabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1346 (0542h) AIF2 Px Pin Ctrl	2	AIF2_LRCLK_INV	0	AIF2 Audio Interface LRCLK Invert 0 = AIF2LRCLK not inverted 1 = AIF2LRCLK inverted This bit is locked when AIF2 channels are enabled; it can only be changed when all AIF2 channels are disabled.
	1	AIF2_LRCLK_FRC	0	AIF2 Audio Interface LRCLK Output Control 0 = Normal 1 = AIF2LRCLK always enabled in Master mode
	0	AIF2_LRCLK_MSTR	0	AIF2 Audio Interface LRCLK Master Select 0 = AIF2LRCLK Slave mode 1 = AIF2LRCLK Master mode This bit is locked when AIF2 channels are enabled; it can only be changed when all AIF2 channels are disabled.

Table 30 AIF2 Master / Slave Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1408 (0580h) AIF3 BCLK Ctrl	7	AIF3_BCLK_INV	0	AIF3 Audio Interface BCLK Invert 0 = AIF3BCLK not inverted 1 = AIF3BCLK inverted This bit is locked when AIF3 channels are enabled; it can only be changed when all AIF3 channels are disabled.
	6	AIF3_BCLK_FRC	0	AIF3 Audio Interface BCLK Output Control 0 = Normal 1 = AIF3BCLK always enabled in Master mode
	5	AIF3_BCLK_MSTR	0	AIF3 Audio Interface BCLK Master Select 0 = AIF3BCLK Slave mode 1 = AIF3BCLK Master mode This bit is locked when AIF3 channels are enabled; it can only be changed when all AIF3 channels are disabled.
R1410 (0582h) AIF3 Rx Pin Ctrl	2	AIF3_LRCLK_INV	0	AIF3 Audio Interface LRCLK Invert 0 = AIF3LRCLK not inverted 1 = AIF3LRCLK inverted This bit is locked when AIF3 channels are enabled; it can only be changed when all AIF3 channels are disabled.
	1	AIF3_LRCLK_FRC	0	AIF3 Audio Interface LRCLK Output Control 0 = Normal 1 = AIF3LRCLK always enabled in Master mode
	0	AIF3_LRCLK_MSTR	0	AIF3 Audio Interface LRCLK Master Select 0 = AIF3LRCLK Slave mode 1 = AIF3LRCLK Master mode This bit is locked when AIF3 channels are enabled; it can only be changed when all AIF3 channels are disabled.

Table 31 AIF3 Master / Slave Control

AIF SIGNAL PATH ENABLE

The AIF1 interface supports up to 8 input (RX) channels and up to 8 output (TX) channels. Each of these channels can be enabled or disabled using the register bits defined in Table 32.

The AIF2 interface supports up to 6 input (RX) channels and up to 6 output (TX) channels. Each of these channels can be enabled or disabled using the register bits defined in Table 33.

The AIF3 interface supports up to 2 input (RX) channels and up to 2 output (TX) channels. Each of these channels can be enabled or disabled using the register bits defined in Table 34.

The system clock, SYSCLK, must be configured and enabled before any audio path is enabled. The ASYNCCLK may also be required, depending on the path configuration. See “Clocking and Sample Rates” for details of the system clocks.

The audio interfaces can be re-configured whilst enabled, including changes to the LRCLK frame length and the channel timeslot configurations. Care is required to ensure that this ‘on-the-fly’ re-configuration does not cause corruption to the active signal paths. Wherever possible, it is recommended to disable all channels before changing the AIF configuration.

As noted in the applicable register descriptions, some of the AIF control fields are locked and cannot be updated whilst AIF channels are enabled; this is to ensure continuity of the respective BCLK and LRCLK signals.

The CS47L24 performs automatic checks to confirm that the SYSCLK and ASYNCCLK frequencies are high enough to support the commanded signal paths and processing functions. If an attempt is made to enable an AIF signal path, and there are insufficient SYSCLK or ASYNCCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error conditions can be monitored using the GPIO and/or Interrupt functions. See “General Purpose Input / Output” and “Interrupts” for further details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1305 (0519h) AIF1 Tx Enables	7	AIF1TX8_ENA	0	AIF1 Audio Interface TX Channel 8 Enable 0 = Disabled 1 = Enabled
	6	AIF1TX7_ENA	0	AIF1 Audio Interface TX Channel 7 Enable 0 = Disabled 1 = Enabled
	5	AIF1TX6_ENA	0	AIF1 Audio Interface TX Channel 6 Enable 0 = Disabled 1 = Enabled
	4	AIF1TX5_ENA	0	AIF1 Audio Interface TX Channel 5 Enable 0 = Disabled 1 = Enabled
	3	AIF1TX4_ENA	0	AIF1 Audio Interface TX Channel 4 Enable 0 = Disabled 1 = Enabled
	2	AIF1TX3_ENA	0	AIF1 Audio Interface TX Channel 3 Enable 0 = Disabled 1 = Enabled
	1	AIF1TX2_ENA	0	AIF1 Audio Interface TX Channel 2 Enable 0 = Disabled 1 = Enabled
	0	AIF1TX1_ENA	0	AIF1 Audio Interface TX Channel 1 Enable 0 = Disabled 1 = Enabled
R1306 (051Ah) AIF1 Rx Enables	7	AIF1RX8_ENA	0	AIF1 Audio Interface RX Channel 8 Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	6	AIF1RX7_ENA	0	AIF1 Audio Interface RX Channel 7 Enable 0 = Disabled 1 = Enabled
	5	AIF1RX6_ENA	0	AIF1 Audio Interface RX Channel 6 Enable 0 = Disabled 1 = Enabled
	4	AIF1RX5_ENA	0	AIF1 Audio Interface RX Channel 5 Enable 0 = Disabled 1 = Enabled
	3	AIF1RX4_ENA	0	AIF1 Audio Interface RX Channel 4 Enable 0 = Disabled 1 = Enabled
	2	AIF1RX3_ENA	0	AIF1 Audio Interface RX Channel 3 Enable 0 = Disabled 1 = Enabled
	1	AIF1RX2_ENA	0	AIF1 Audio Interface RX Channel 2 Enable 0 = Disabled 1 = Enabled
	0	AIF1RX1_ENA	0	AIF1 Audio Interface RX Channel 1 Enable 0 = Disabled 1 = Enabled

Table 32 AIF1 Signal Path Enable

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1369 (0559h) AIF2 TX Enables	5	AIF2TX6_ENA	0	AIF2 Audio Interface TX Channel 6 Enable 0 = Disabled 1 = Enabled
	4	AIF2TX5_ENA	0	AIF2 Audio Interface TX Channel 5 Enable 0 = Disabled 1 = Enabled
	3	AIF2TX4_ENA	0	AIF2 Audio Interface TX Channel 4 Enable 0 = Disabled 1 = Enabled
	2	AIF2TX3_ENA	0	AIF2 Audio Interface TX Channel 3 Enable 0 = Disabled 1 = Enabled
	1	AIF2TX2_ENA	0	AIF2 Audio Interface TX Channel 2 Enable 0 = Disabled 1 = Enabled
	0	AIF2TX1_ENA	0	AIF2 Audio Interface TX Channel 1 Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1370 (055Ah) AIF2 RX Enables	5	AIF2RX6_ENA	0	AIF2 Audio Interface RX Channel 6 Enable 0 = Disabled 1 = Enabled
	4	AIF2RX5_ENA	0	AIF2 Audio Interface RX Channel 5 Enable 0 = Disabled 1 = Enabled
	3	AIF2RX4_ENA	0	AIF2 Audio Interface RX Channel 4 Enable 0 = Disabled 1 = Enabled
	2	AIF2RX3_ENA	0	AIF2 Audio Interface RX Channel 3 Enable 0 = Disabled 1 = Enabled
	1	AIF2RX2_ENA	0	AIF2 Audio Interface RX Channel 2 Enable 0 = Disabled 1 = Enabled
	0	AIF2RX1_ENA	0	AIF2 Audio Interface RX Channel 1 Enable 0 = Disabled 1 = Enabled

Table 33 AIF2 Signal Path Enable

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1433 (0599h) AIF3 TX Enables	1	AIF3TX2_ENA	0	AIF3 Audio Interface TX Channel 2 Enable 0 = Disabled 1 = Enabled
	0	AIF3TX1_ENA	0	AIF3 Audio Interface TX Channel 1 Enable 0 = Disabled 1 = Enabled
R1434 (059Ah) AIF3 RX Enables	1	AIF3RX2_ENA	0	AIF3 Audio Interface RX Channel 2 Enable 0 = Disabled 1 = Enabled
	0	AIF3RX1_ENA	0	AIF3 Audio Interface RX Channel 1 Enable 0 = Disabled 1 = Enabled

Table 34 AIF3 Signal Path Enable

AIF BCLK AND LRCLK CONTROL

The AIFnBCLK frequency is selected by the AIFn_BCLK_FREQ register. For each value of this register, the actual frequency depends upon whether AIFn is configured for a 48kHz-related sample rate or a 44.1kHz-related sample rate, as described below.

If AIFn_RATE<1000 (see Table 21), then AIFn is referenced to the SYSCLK clocking domain and the applicable frequency depends upon the SAMPLE_RATE_1, SAMPLE_RATE_2 or SAMPLE_RATE_3 registers.

If AIFn_RATE≥1000, then AIFn is referenced to the ASYNCCLK clocking domain and the applicable frequency depends upon the ASYNC_SAMPLE_RATE_1 or ASYNC_SAMPLE_RATE_2 registers.

The selected AIFnBCLK rate must be less than or equal to SYSCLK/2, or ASYNCCLK/2, as applicable. See “Clocking and Sample Rates” for details of SYSCLK and ASYNCCLK domains, and the associated control registers.

The AIFnLRCLK frequency is controlled relative to AIFnBCLK by the AIFn_BCPF divider.

Note that the BCLK rate must be configured in Master or Slave modes, using the AIFn_BCLK_FREQ registers. The LRCLK rate(s) only require to be configured in Master mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1280 (0500h) AIF1 BCLK Ctrl	4:0	AIF1_BCLK_FREQ [4:0]	01100	AIF1BCLK Rate 00000 = Reserved 00001 = Reserved 00010 = 64kHz (58.8kHz) 00011 = 96kHz (88.2kHz) 00100 = 128kHz (117.6kHz) 00101 = 192kHz (176.4kHz) 00110 = 256kHz (235.2kHz) 00111 = 384kHz (352.8kHz) 01000 = 512kHz (470.4kHz) 01001 = 768kHz (705.6kHz) 01010 = 1.024MHz (940.8kHz) 01011 = 1.536MHz (1.4112MHz) 01100 = 2.048MHz (1.8816MHz) 01101 = 3.072MHz (2.8824MHz) 01110 = 4.096MHz (3.7632MHz) 01111 = 6.144MHz (5.6448MHz) 10000 = 8.192MHz (7.5264MHz) 10001 = 12.288MHz (11.2896MHz) 10010 = 24.576MHz (22.5792MHz) The frequencies in brackets apply for 44.1kHz-related sample rates only. If AIF1_RATE<1000, then AIF1 is referenced to SYSCLK and the 44.1kHz-related frequencies apply if SAMPLE_RATE_n = 01XXX. If AIF1_RATE>=1000, then AIF1 is referenced to ASYNCCLK and the 44.1kHz-related frequencies apply if ASYNC_SAMPLE_RATE_n = 01XXX. The AIF1BCLK rate must be less than or equal to SYSCLK/2, or ASYNCCLK/2, as applicable. This field is locked when AIF1 channels are enabled; it can only be changed when all AIF1 channels are disabled.
R1286 (0506h) AIF1 Tx BCLK Rate	12:0	AIF1_BCPF [12:0]	0040h	AIF1LRCLK Rate This register selects the number of BCLK cycles per AIF1LRCLK frame. AIF1LRCLK clock = AIF1BCLK / AIF1_BCPF Integer (LSB = 1), Valid from 8..8191

Table 35 AIF1 BCLK and LRCLK Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1344 (0540h) AIF2 BCLK Ctrl	4:0	AIF2_BCLK_FREQ [4:0]	01100	AIF2BCLK Rate 00000 = Reserved 00001 = Reserved 00010 = 64kHz (58.8kHz) 00011 = 96kHz (88.2kHz) 00100 = 128kHz (117.6kHz) 00101 = 192kHz (176.4kHz) 00110 = 256kHz (235.2kHz) 00111 = 384kHz (352.8kHz) 01000 = 512kHz (470.4kHz) 01001 = 768kHz (705.6kHz) 01010 = 1.024MHz (940.8kHz) 01011 = 1.536MHz (1.4112MHz) 01100 = 2.048MHz (1.8816MHz) 01101 = 3.072MHz (2.8824MHz) 01110 = 4.096MHz (3.7632MHz) 01111 = 6.144MHz (5.6448MHz) 10000 = 8.192MHz (7.5264MHz) 10001 = 12.288MHz (11.2896MHz) 10010 = 24.576MHz (22.5792MHz) The frequencies in brackets apply for 44.1kHz-related sample rates only. If AIF2_RATE<1000, then AIF2 is referenced to SYSCLK and the 44.1kHz-related frequencies apply if SAMPLE_RATE_n = 01XXX. If AIF2_RATE>=1000, then AIF2 is referenced to ASYNCCLK and the 44.1kHz-related frequencies apply if ASYNC_SAMPLE_RATE_n = 01XXX. The AIF2BCLK rate must be less than or equal to SYSCLK/2, or ASYNCCLK/2, as applicable. This field is locked when AIF2 channels are enabled; it can only be changed when all AIF2 channels are disabled.
R1350 (0546h) AIF2 Rx BCLK Rate	12:0	AIF2_BCPF [12:0]	0040h	AIF2LRCLK Rate This register selects the number of BCLK cycles per AIF2LRCLK frame. AIF2LRCLK clock = AIF2BCLK / AIF2_BCPF Integer (LSB = 1), Valid from 8..8191

Table 36 AIF2 BCLK and LRCLK Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1408 (0580h) AIF3 BCLK Ctrl	4:0	AIF3_BCLK_FREQ [4:0]	01100	AIF3BCLK Rate 00000 = Reserved 00001 = Reserved 00010 = 64kHz (58.8kHz) 00011 = 96kHz (88.2kHz) 00100 = 128kHz (117.6kHz) 00101 = 192kHz (176.4kHz) 00110 = 256kHz (235.2kHz) 00111 = 384kHz (352.8kHz) 01000 = 512kHz (470.4kHz) 01001 = 768kHz (705.6kHz) 01010 = 1.024MHz (940.8kHz) 01011 = 1.536MHz (1.4112MHz) 01100 = 2.048MHz (1.8816MHz) 01101 = 3.072MHz (2.8824MHz) 01110 = 4.096MHz (3.7632MHz) 01111 = 6.144MHz (5.6448MHz) 10000 = 8.192MHz (7.5264MHz) 10001 = 12.288MHz (11.2896MHz) 10010 = 24.576MHz (22.5792MHz) The frequencies in brackets apply for 44.1kHz-related sample rates only. If AIF3_RATE<1000, then AIF3 is referenced to SYSCLK and the 44.1kHz-related frequencies apply if SAMPLE_RATE_n = 01XXX. If AIF3_RATE>=1000, then AIF3 is referenced to ASYNCCLK and the 44.1kHz-related frequencies apply if ASYNC_SAMPLE_RATE_n = 01XXX. The AIF3BCLK rate must be less than or equal to SYSCLK/2, or ASYNCCLK/2, as applicable. This field is locked when AIF3 channels are enabled; it can only be changed when all AIF3 channels are disabled.
R1414 (0586h) AIF3 Rx BCLK Rate	12:0	AIF3_BCPF [12:0]	0040h	AIF3LRCLK Rate This register selects the number of BCLK cycles per AIF3LRCLK frame. AIF3LRCLK clock = AIF3BCLK / AIF3_BCPF Integer (LSB = 1), Valid from 8..8191

Table 37 AIF3 BCLK and LRCLK Control

AIF DIGITAL AUDIO DATA CONTROL

The register bits controlling the audio data format, word lengths and slot configurations for AIF1, AIF2 and AIF3 are described in Table 38, Table 39 and Table 40 respectively.

Note that Left-Justified and DSP-B modes are valid in Master mode only (i.e., BCLK and LRCLK are outputs from the CS47L24).

The AIFn Slot Length is the number of BCLK cycles in one timeslot within the overall LRCLK frame. The Word Length is the number of valid data bits within each timeslot. (If the word length is less than the slot length, then there will be unused BCLK cycles at the end of each timeslot.) The AIFn word length and slot length is independently selectable for the input (RX) and output (TX) paths.

For each AIF input (RX) and AIF output (TX) channel, the position of the audio data sample within the LRCLK frame is configurable. The _SLOT registers define the timeslot position of the audio sample for the associated audio channel. Valid selections are Slot 0 upwards. The timeslots are numbered as illustrated in Figure 37 through to Figure 40.

Note that, in DSP modes, the timeslots are ordered consecutively from the start of the LRCLK frame. In I2S and Left-Justified modes, the even-numbered timeslots are arranged in the first half of the LRCLK frame, and the odd-numbered timeslots are arranged in the second half of the frame.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1284 (0504h) AIF1 Format	2:0	AIF1_FMT [2:0]	000	AIF1 Audio Interface Format 000 = DSP Mode A 001 = DSP Mode B 010 = I^2S mode 011 = Left Justified mode Other codes are Reserved This field is locked when AIF1 channels are enabled; it can only be changed when all AIF1 channels are disabled.
R1287 (0507h) AIF1 Frame Ctrl 1	13:8	AIF1TX_WL [5:0]	18h	AIF1 TX Word Length (Number of valid data bits per slot) Integer (LSB = 1); Valid from 16 to 32
	7:0	AIF1TX_SLOT_LEN [7:0]	18h	AIF1 TX Slot Length (Number of BCLK cycles per slot) Integer (LSB = 1); Valid from 16 to 128
R1288 (0508h) AIF1 Frame Ctrl 2	13:8	AIF1RX_WL [5:0]	18h	AIF1 RX Word Length (Number of valid data bits per slot) Integer (LSB = 1); Valid from 16 to 32
	7:0	AIF1RX_SLOT_LEN [7:0]	18h	AIF1 RX Slot Length (Number of BCLK cycles per slot) Integer (LSB = 1); Valid from 16 to 128
R1289 (0509h) to R1296 (0510h)	5:0	AIF1TX1_SLOT [5:0]	0h	AIF1 TX Channel n Slot position Defines the TX timeslot position of the Channel n audio sample Integer (LSB=1); Valid from 0 to 63
	5:0	AIF1TX2_SLOT [5:0]	1h	
	5:0	AIF1TX3_SLOT [5:0]	2h	
	5:0	AIF1TX4_SLOT [5:0]	3h	
	5:0	AIF1TX5_SLOT [5:0]	4h	
	5:0	AIF1TX6_SLOT [5:0]	5h	
	5:0	AIF1TX7_SLOT [5:0]	6h	
	5:0	AIF1TX8_SLOT [5:0]	7h	
R1297 (0511h) to	5:0	AIF1RX1_SLOT [5:0]	0h	AIF1 RX Channel n Slot position Defines the RX timeslot position of the Channel n audio sample Integer (LSB=1); Valid from 0 to 63
	5:0	AIF1RX2_SLOT [5:0]	1h	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1304 (0518h)	5:0	AIF1RX3_SLOT [5:0]	2h	
	5:0	AIF1RX4_SLOT [5:0]	3h	
	5:0	AIF1RX5_SLOT [5:0]	4h	
	5:0	AIF1RX6_SLOT [5:0]	5h	
	5:0	AIF1RX7_SLOT [5:0]	6h	
	5:0	AIF1RX8_SLOT [5:0]	7h	

Table 38 AIF1 Digital Audio Data Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1348 (0544h) AIF2 Format	2:0	AIF2_FMT [2:0]	000	AIF2 Audio Interface Format 000 = DSP Mode A 001 = DSP Mode B 010 = I^2S mode 011 = Left Justified mode Other codes are Reserved This field is locked when AIF2 channels are enabled; it can only be changed when all AIF2 channels are disabled.
R1351 (0547h) AIF2 Frame Ctrl 1	13:8	AIF2TX_WL [5:0]	18h	AIF2 TX Word Length (Number of valid data bits per slot) Integer (LSB = 1); Valid from 16 to 32
	7:0	AIF2TX_SLOT_LEN [7:0]	18h	AIF2 TX Slot Length (Number of BCLK cycles per slot) Integer (LSB = 1); Valid from 16 to 128
R1352 (0548h) AIF2 Frame Ctrl 2	13:8	AIF2RX_WL [5:0]	18h	AIF2 RX Word Length (Number of valid data bits per slot) Integer (LSB = 1); Valid from 16 to 32
	7:0	AIF2RX_SLOT_LEN [7:0]	18h	AIF2 RX Slot Length (Number of BCLK cycles per slot) Integer (LSB = 1); Valid from 16 to 128
R1353 (0549h) to R1358 (054Eh)	5:0	AIF2TX1_SLOT [5:0]	0h	AIF2 TX Channel n Slot position Defines the TX timeslot position of the Channel n audio sample Integer (LSB=1); Valid from 0 to 63
	5:0	AIF2TX2_SLOT [5:0]	1h	
	5:0	AIF2TX3_SLOT [5:0]	2h	
	5:0	AIF2TX4_SLOT [5:0]	3h	
	5:0	AIF2TX5_SLOT [5:0]	4h	
	5:0	AIF2TX6_SLOT [5:0]	5h	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1361 (0551h) to R1366 (0556h)	5:0	AIF2RX1_SLOT [5:0]	0h	AIF2 RX Channel n Slot position Defines the RX timeslot position of the Channel n audio sample Integer (LSB=1); Valid from 0 to 63
	5:0	AIF2RX2_SLOT [5:0]	1h	
	5:0	AIF2RX3_SLOT [5:0]	2h	
	5:0	AIF2RX4_SLOT [5:0]	3h	
	5:0	AIF2RX5_SLOT [5:0]	4h	
	5:0	AIF2RX6_SLOT [5:0]	5h	

Table 39 AIF2 Digital Audio Data Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1412 (0584h) AIF3 Format	2:0	AIF3_FMT [2:0]	000	AIF3 Audio Interface Format 000 = DSP Mode A 001 = DSP Mode B 010 = I^2S mode 011 = Left Justified mode Other codes are Reserved This field is locked when AIF3 channels are enabled; it can only be changed when all AIF3 channels are disabled.
R1415 (0587h) AIF3 Frame Ctrl 1	13:8	AIF3TX_WL [5:0]	18h	AIF3 TX Word Length (Number of valid data bits per slot) Integer (LSB = 1); Valid from 16 to 32
	7:0	AIF3TX_SLOT_LEN [7:0]	18h	AIF3 TX Slot Length (Number of BCLK cycles per slot) Integer (LSB = 1); Valid from 16 to 128
R1416 (0588h) AIF3 Frame Ctrl 2	13:8	AIF3RX_WL [5:0]	18h	AIF3 RX Word Length (Number of valid data bits per slot) Integer (LSB = 1); Valid from 16 to 32
	7:0	AIF3RX_SLOT_LEN [7:0]	18h	AIF3 RX Slot Length (Number of BCLK cycles per slot) Integer (LSB = 1); Valid from 16 to 128
R1417 (0589h) AIF3 Frame Ctrl 3	5:0	AIF3TX1_SLOT [5:0]	0h	AIF3 TX Channel 1 Slot position Defines the TX timeslot position of the Channel 1 audio sample Integer (LSB=1); Valid from 0 to 63
R1418 (058Ah) AIF3 Frame Ctrl 4	5:0	AIF3TX2_SLOT [5:0]	1h	AIF3 TX Channel 2 Slot position Defines the TX timeslot position of the Channel 2 audio sample Integer (LSB=1); Valid from 0 to 63
R1425 (0591h) AIF3 Frame Ctrl 11	5:0	AIF3RX1_SLOT [5:0]	0h	AIF3 RX Channel 1 Slot position Defines the RX timeslot position of the Channel 1 audio sample Integer (LSB=1); Valid from 0 to 63

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1426 (0592h) AIF3 Frame Ctrl 12	5:0	AIF3RX2_SLOT [5:0]	1h	AIF3 RX Channel 2 Slot position Defines the RX timeslot position of the Channel 2 audio sample Integer (LSB=1); Valid from 0 to 63

Table 40 AIF3 Digital Audio Data Control

AIF TDM AND TRI-STATE CONTROL

The AIFn output pins are tri-stated when the AIFn_TRI register is set.

Under default conditions, the AIFnTXDAT output is held at logic 0 when the CS47L24 is not transmitting data (i.e., during timeslots that are not enabled for output by the CS47L24). When the AIFnTX_DAT_TRI register is set, the CS47L24 tri-states the respective AIFnTXDAT pin when not transmitting data, allowing other devices to drive the AIFnTXDAT connection.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1281 (0501h) AIF1 Tx Pin Ctrl	5	AIF1TX_DAT_TRI	0	AIF1TXDAT Tri-State Control 0 = Logic 0 during unused timeslots 1 = Tri-stated during unused timeslots
R1283 (0503h) AIF1 Rate Ctrl	6	AIF1_TRI	0	AIF1 Audio Interface Tri-State Control 0 = Normal 1 = AIF1 Outputs are tri-stated

Table 41 AIF1 TDM and Tri-State Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1345 (0541h) AIF2 Tx Pin Ctrl	5	AIF2TX_DAT_TRI	0	AIF2TXDAT Tri-State Control 0 = Logic 0 during unused timeslots 1 = Tri-stated during unused timeslots
R1347 (0543h) AIF2 Rate Ctrl	6	AIF2_TRI	0	AIF2 Audio Interface Tri-State Control 0 = Normal 1 = AIF2 Outputs are tri-stated

Table 42 AIF2 TDM and Tri-State Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1409 (0581h) AIF3 Tx Pin Ctrl	5	AIF3TX_DAT_TRI	0	AIF3TXDAT Tri-State Control 0 = Logic 0 during unused timeslots 1 = Tri-stated during unused timeslots
R1411 (0583h) AIF3 Rate Ctrl	6	AIF3_TRI	0	AIF3 Audio Interface Tri-State Control 0 = Normal 1 = AIF3 Outputs are tri-stated

Table 43 AIF3 TDM and Tri-State Control

AIF DIGITAL PULL-UP AND PULL-DOWN

The CS47L24 provides integrated pull-up and pull-down resistors on each of the AIFnLRCLK, AIFnBCLK and AIFnRXDAT pins. This provides a flexible capability for interfacing with other devices.

Each of the pull-up and pull-down resistors can be configured independently using the register bits described in Table 44, Table 45 and Table 46. When the pull-up and pull-down resistors are both enabled, the CS47L24 provides a 'bus keeper' function on the respective pin. The bus keeper function holds the logic level unchanged whenever the pin is undriven (e.g., if the signal is tri-stated).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3107 (0C23h) Misc Pad Ctrl 4	5	AIF1LRCLK_PU	0	AIF1LRCLK Pull-Up Control 0 = Disabled 1 = Enabled Note - when AIF1LRCLK_PD and AIF1LRCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF1LRCLK pin.
	4	AIF1LRCLK_PD	0	AIF1LRCLK Pull-Down Control 0 = Disabled 1 = Enabled Note - when AIF1LRCLK_PD and AIF1LRCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF1LRCLK pin.
	3	AIF1BCLK_PU	0	AIF1BCLK Pull-Up Control 0 = Disabled 1 = Enabled Note - when AIF1BCLK_PD and AIF1BCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF1BCLK pin.
	2	AIF1BCLK_PD	0	AIF1BCLK Pull-Down Control 0 = Disabled 1 = Enabled Note - when AIF1BCLK_PD and AIF1BCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF1BCLK pin.
	1	AIF1RXDAT_PU	0	AIF1RXDAT Pull-Up Control 0 = Disabled 1 = Enabled Note - when AIF1RXDAT_PD and AIF1RXDAT_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF1RXDAT pin.
	0	AIF1RXDAT_PD	0	AIF1RXDAT Pull-Down Control 0 = Disabled 1 = Enabled Note - when AIF1RXDAT_PD and AIF1RXDAT_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF1RXDAT pin.

Table 44 AIF1 Digital Pull-Up and Pull-Down Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3108 (0C24h) Misc Pad Ctrl 5	5	AIF2LRCLK_PU	0	AIF2LRCLK Pull-Up Control 0 = Disabled 1 = Enabled Note - when AIF2LRCLK_PD and AIF2LRCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF2LRCLK pin.
	4	AIF2LRCLK_PD	0	AIF2LRCLK Pull-Down Control 0 = Disabled 1 = Enabled Note - when AIF2LRCLK_PD and AIF2LRCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF2LRCLK pin.
	3	AIF2BCLK_PU	0	AIF2BCLK Pull-Up Control 0 = Disabled 1 = Enabled Note - when AIF2BCLK_PD and AIF2BCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF2BCLK pin.
	2	AIF2BCLK_PD	0	AIF2BCLK Pull-Down Control 0 = Disabled 1 = Enabled Note - when AIF2BCLK_PD and AIF2BCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF2BCLK pin.
	1	AIF2RXDAT_PU	0	AIF2RXDAT Pull-Up Control 0 = Disabled 1 = Enabled Note - when AIF2RXDAT_PD and AIF2RXDAT_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF2RXDAT pin.
	0	AIF2RXDAT_PD	0	AIF2RXDAT Pull-Down Control 0 = Disabled 1 = Enabled Note - when AIF2RXDAT_PD and AIF2RXDAT_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF2RXDAT pin.

Table 45 AIF2 Digital Pull-Up and Pull-Down Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3109 (0C25h) Misc Pad Ctrl 6	5	AIF3LRCLK_PU	0	AIF3LRCLK Pull-Up Control 0 = Disabled 1 = Enabled Note - when AIF3LRCLK_PD and AIF3LRCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF3LRCLK pin.
	4	AIF3LRCLK_PD	0	AIF3LRCLK Pull-Down Control 0 = Disabled 1 = Enabled Note - when AIF3LRCLK_PD and AIF3LRCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF3LRCLK pin.
	3	AIF3BCLK_PU	0	AIF3BCLK Pull-Up Control 0 = Disabled 1 = Enabled Note - when AIF3BCLK_PD and AIF3BCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF3BCLK pin.
	2	AIF3BCLK_PD	0	AIF3BCLK Pull-Down Control 0 = Disabled 1 = Enabled Note - when AIF3BCLK_PD and AIF3BCLK_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF3BCLK pin.
	1	AIF3RXDAT_PU	0	AIF3RXDAT Pull-Up Control 0 = Disabled 1 = Enabled Note - when AIF3RXDAT_PD and AIF3RXDAT_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF3RXDAT pin.
	0	AIF3RXDAT_PD	0	AIF3RXDAT Pull-Down Control 0 = Disabled 1 = Enabled Note - when AIF3RXDAT_PD and AIF3RXDAT_PU are both set to '1', then a 'bus keeper' function is enabled on the AIF3RXDAT pin.

Table 46 AIF3 Digital Pull-Up and Pull-Down Control

OUTPUT SIGNAL PATH

The CS47L24 provides two audio output signal paths. These outputs comprise a ground-referenced headphone driver and a differential speaker driver, as summarised in Table 47.

SIGNAL PATH	DESCRIPTIONS	OUTPUT PINS
OUT1L, OUT1R	Ground-referenced headphone output	HPOUTL, HPOUTR
OUT4L	Differential speaker output	SPKOUTN, SPKOUTP

Table 47 Output Signal Path Summary

The analogue output paths incorporate high performance 24-bit sigma-delta DACs.

Under default conditions, the headphone drivers provide a stereo, single-ended output. A mono mode is also available, providing a differential (BTL) output. The ground-referenced headphone output paths incorporate a common mode feedback path for rejection of system-related noise. These outputs support direct connection to headphone loads, with no requirement for AC coupling capacitors.

The speaker output path is configured to drive a differential (BTL) output. The Class D design offers high efficiency at large signal levels. With a suitable choice of external speaker, the Class D output can drive a loudspeaker directly, without any additional filter components.

Digital volume control is available on all outputs, with programmable ramp control for smooth, glitch-free operation. A configurable noise gate function is available on each of the output signal paths. Any of the output signal paths may be selected as input to the Acoustic Echo Cancellation (AEC) loopback path.

The CS47L24 incorporates thermal protection functions, and also provides short-circuit detection on the Class D speaker and headphone output paths. For further details, refer to the “Thermal Shutdown and Short Circuit Protection” section.

The CS47L24 output signal paths are illustrated in Figure 44. Note that a phase inversion is present in the Class D output (OUT4L) path, as shown below.

The OUT2, OUT3, and OUT4R paths are not implemented on this device.

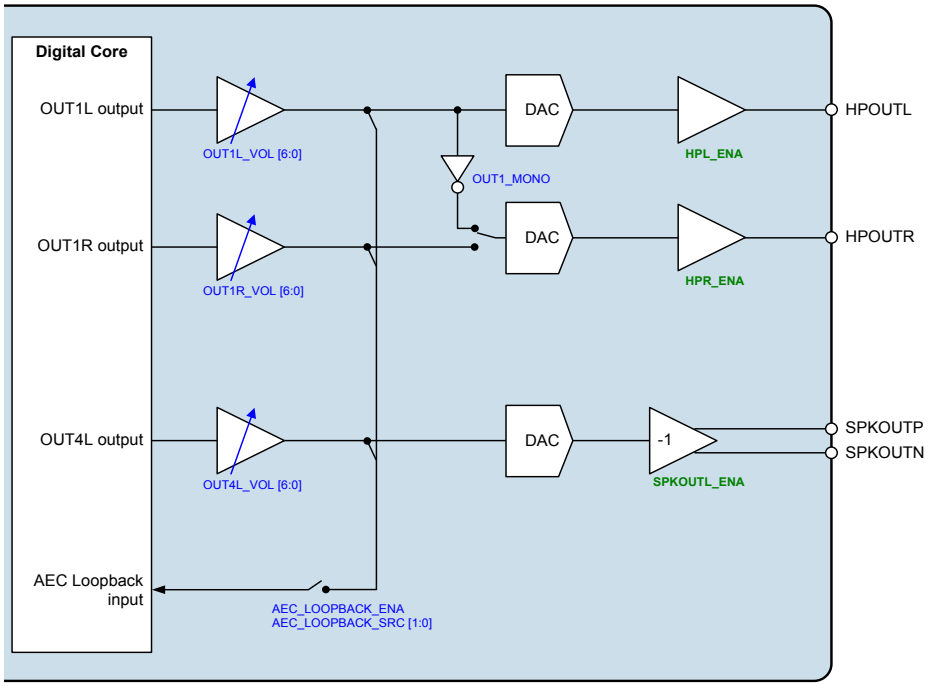


Figure 44 Output Signal Paths

OUTPUT SIGNAL PATH ENABLE

The output signal paths are enabled using the register bits described in Table 48. The respective bit(s) must be enabled for analogue output on the respective output path(s).

The output signal paths are muted by default. It is recommended that de-selecting the mute should be the final step of the path enable control sequence. Similarly, the mute should be selected as the first step of the path disable control sequence. The output signal path mute functions are controlled using the register bits described in Table 49.

The supply rails for the OUT1 outputs (HPOUTL and HPOUTR) are generated using an integrated dual-mode Charge Pump. The Charge Pump is enabled automatically by the CS47L24 when required by the output drivers. See the “Charge Pump, Regulators and Voltage Reference” section for further details.

The CS47L24 schedules a pop-suppressed control sequence to enable or disable the OUT1 and OUT4L signal paths. This is automatically managed in response to setting the respective HPx_ENA or SPKOUTL_ENA register bits. See “Control Write Sequencer” for further details.

The headphone output (OUT1) enable control sequences are inputs to the Interrupt circuit, and can be used to trigger an Interrupt event when a sequence completes. See “Interrupts” for further details.

The headphone output (OUT1) enable control sequences can also generate a GPIO output, providing an external indication of the sequence status. See “General Purpose Input / Output” to configure a GPIO pin for this function.

The system clock, SYSCLK, must be configured and enabled before any audio path is enabled. The ASYNCCLK may also be required, depending on the path configuration. See “Clocking and Sample Rates” for details of the system clocks.

The CS47L24 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the output signal paths and associated DACs. If an attempt is made to enable an output signal path, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error condition can be monitored using the GPIO and/or Interrupt functions. See “General Purpose Input / Output” and “Interrupts” for further details.

The status bits in Register R1025 and R1030 indicate the status of each of the output signal paths. If an Underclocked Error condition occurs, then these bits provide readback of which signal path(s) have been successfully enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1024 (0400h) Output Enables 1	7	SPKOUTL_ENA	0	Output Path 4 (Left) Enable 0 = Disabled 1 = Enabled
	1	HPL_ENA	0	Output Path 1 (Left) Enable 0 = Disabled 1 = Enabled
	0	HPR_ENA	0	Output Path 1 (Right) Enable 0 = Disabled 1 = Enabled
R1025 (0401h) Output Status 1	7	OUT4L_ENA_STS	0	Output Path 4 (Left) Enable Status 0 = Disabled 1 = Enabled
R1030 (0406h) Raw Output Status 1	1	OUT1L_ENA_STS	0	Output Path 1 (Left) Enable Status 0 = Disabled 1 = Enabled
	0	OUT1R_ENA_STS	0	Output Path 1 (Right) Enable Status 0 = Disabled 1 = Enabled

Table 48 Output Signal Path Enable

OUTPUT SIGNAL PATH SAMPLE RATE CONTROL

The output signal paths are derived from the respective output mixers within the CS47L24 digital core. The sample rate for the output signal paths is configured using the OUT_RATE register - see Table 21 within the “Digital Core” section.

Note that sample rate conversion is required when routing the output signal paths to any signal chain that is asynchronous and/or configured for a different sample rate.

OUTPUT SIGNAL PATH DIGITAL VOLUME CONTROL

A digital volume control is provided on each of the output signal paths, providing -64dB to +31.5dB gain control in 0.5dB steps. An independent mute control is also provided for each output signal path.

Whenever the gain or mute setting is changed, the signal path gain is ramped up or down to the new settings at a programmable rate. For increasing gain (or un-mute), the rate is controlled by the OUT_VI_RAMP register. For decreasing gain (or mute), the rate is controlled by the OUT_VD_RAMP register. Note that the OUT_VI_RAMP and OUT_VD_RAMP registers should not be changed while a volume ramp is in progress.

The OUT_VU bits control the loading of the output signal path digital volume and mute controls. When OUT_VU is set to 0, the digital volume and mute settings will be loaded into the respective control register, but will not actually change the signal path gain. The digital volume and mute settings on all of the output signal paths are updated when a 1 is written to OUT_VU. This makes it possible to update the gain of multiple signal paths simultaneously.

Note that, although the digital volume control registers provide 0.5dB steps, the internal circuits provide signal gain adjustment in 0.125dB steps. This allows a very high degree of gain control, and smooth volume ramping under all operating conditions.

The 0dBFS level of the OUT5 digital output path is not equal to the 0dBFS level of the CS47L24 digital core. The maximum digital output level is -6dBFS (see “Electrical Characteristics”). Under 0dBFS gain conditions, a 0dBFS output from the digital core corresponds to a -6dBFS level in the PDM output.

The digital volume control register fields are described in Table 49 and Table 50.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1033 (0409h) Output Volume Ramp	6:4	OUT_VD_RAMP [2:0]	010	Output Volume Decreasing Ramp Rate (seconds/6dB) 000 = 0ms 001 = 0.5ms 010 = 1ms 011 = 2ms 100 = 4ms 101 = 8ms 110 = 15ms 111 = 30ms This register should not be changed while a volume ramp is in progress.
	2:0	OUT_VI_RAMP [2:0]	010	Output Volume Increasing Ramp Rate (seconds/6dB) 000 = 0ms 001 = 0.5ms 010 = 1ms 011 = 2ms 100 = 4ms 101 = 8ms 110 = 15ms 111 = 30ms This register should not be changed while a volume ramp is in progress.
R1041 (0411h) DAC Digital Volume 1L	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT1L_MUTE	1	Output Path 1 (Left) Digital Mute 0 = Un-mute 1 = Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:0	OUT1L_VOL [7:0]	80h	Output Path 1 (Left) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 50 for volume range)
R1045 (0415h) DAC Digital Volume 1R	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT1R_MUTE	1	Output Path 1 (Right) Digital Mute 0 = Un-mute 1 = Mute
	7:0	OUT1R_VOL [7:0]	80h	Output Path 1 (Right) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 50 for volume range)
R1065 (0429h) DAC Digital Volume 4L	9	OUT_VU		Output Signal Paths Volume Update Writing a 1 to this bit will cause the Output Signal Paths Volume and Mute settings to be updated simultaneously
	8	OUT4L_MUTE	1	Output Path 4 (Left) Digital Mute 0 = Un-mute 1 = Mute
	7:0	OUT4L_VOL [7:0]	80h	Output Path 4 (Left) Digital Volume -64dB to +31.5dB in 0.5dB steps 00h = -64dB 01h = -63.5dB … (0.5dB steps) 80h = 0dB … (0.5dB steps) BFh = +31.5dB C0h to FFh = Reserved (See Table 50 for volume range)

Table 49 Output Signal Path Digital Volume Control

Output Volume Register	Volume (dB)	Output Volume Register	Volume (dB)	Output Volume Register	Volume (dB)	Output Volume Register	Volume (dB)
00h	-64.0	40h	-32.0	80h	0.0	C0h	Reserved
01h	-63.5	41h	-31.5	81h	0.5	C1h	Reserved
02h	-63.0	42h	-31.0	82h	1.0	C2h	Reserved
03h	-62.5	43h	-30.5	83h	1.5	C3h	Reserved
04h	-62.0	44h	-30.0	84h	2.0	C4h	Reserved
05h	-61.5	45h	-29.5	85h	2.5	C5h	Reserved
06h	-61.0	46h	-29.0	86h	3.0	C6h	Reserved
07h	-60.5	47h	-28.5	87h	3.5	C7h	Reserved
08h	-60.0	48h	-28.0	88h	4.0	C8h	Reserved
09h	-59.5	49h	-27.5	89h	4.5	C9h	Reserved
0Ah	-59.0	4Ah	-27.0	8Ah	5.0	CAh	Reserved
0Bh	-58.5	4Bh	-26.5	8Bh	5.5	CBh	Reserved
0Ch	-58.0	4Ch	-26.0	8Ch	6.0	CCh	Reserved
0Dh	-57.5	4Dh	-25.5	8Dh	6.5	CDh	Reserved
0Eh	-57.0	4Eh	-25.0	8Eh	7.0	CEh	Reserved
0Fh	-56.5	4Fh	-24.5	8Fh	7.5	CFh	Reserved
10h	-56.0	50h	-24.0	90h	8.0	D0h	Reserved
11h	-55.5	51h	-23.5	91h	8.5	D1h	Reserved
12h	-55.0	52h	-23.0	92h	9.0	D2h	Reserved
13h	-54.5	53h	-22.5	93h	9.5	D3h	Reserved
14h	-54.0	54h	-22.0	94h	10.0	D4h	Reserved
15h	-53.5	55h	-21.5	95h	10.5	D5h	Reserved
16h	-53.0	56h	-21.0	96h	11.0	D6h	Reserved
17h	-52.5	57h	-20.5	97h	11.5	D7h	Reserved
18h	-52.0	58h	-20.0	98h	12.0	D8h	Reserved
19h	-51.5	59h	-19.5	99h	12.5	D9h	Reserved
1Ah	-51.0	5Ah	-19.0	9Ah	13.0	DAh	Reserved
1Bh	-50.5	5Bh	-18.5	9Bh	13.5	DBh	Reserved
1Ch	-50.0	5Ch	-18.0	9Ch	14.0	DCh	Reserved
1Dh	-49.5	5Dh	-17.5	9Dh	14.5	DDh	Reserved
1Eh	-49.0	5Eh	-17.0	9Eh	15.0	DEh	Reserved
1Fh	-48.5	5Fh	-16.5	9Fh	15.5	DFh	Reserved
20h	-48.0	60h	-16.0	A0h	16.0	E0h	Reserved
21h	-47.5	61h	-15.5	A1h	16.5	E1h	Reserved
22h	-47.0	62h	-15.0	A2h	17.0	E2h	Reserved
23h	-46.5	63h	-14.5	A3h	17.5	E3h	Reserved
24h	-46.0	64h	-14.0	A4h	18.0	E4h	Reserved
25h	-45.5	65h	-13.5	A5h	18.5	E5h	Reserved
26h	-45.0	66h	-13.0	A6h	19.0	E6h	Reserved
27h	-44.5	67h	-12.5	A7h	19.5	E7h	Reserved
28h	-44.0	68h	-12.0	A8h	20.0	E8h	Reserved
29h	-43.5	69h	-11.5	A9h	20.5	E9h	Reserved
2Ah	-43.0	6Ah	-11.0	AAh	21.0	EAh	Reserved
2Bh	-42.5	6Bh	-10.5	ABh	21.5	EBh	Reserved
2Ch	-42.0	6Ch	-10.0	ACh	22.0	ECh	Reserved
2Dh	-41.5	6Dh	-9.5	ADh	22.5	EDh	Reserved
2Eh	-41.0	6Eh	-9.0	AEh	23.0	EEh	Reserved
2Fh	-40.5	6Fh	-8.5	AFh	23.5	EFh	Reserved
30h	-40.0	70h	-8.0	B0h	24.0	F0h	Reserved
31h	-39.5	71h	-7.5	B1h	24.5	F1h	Reserved
32h	-39.0	72h	-7.0	B2h	25.0	F2h	Reserved
33h	-38.5	73h	-6.5	B3h	25.5	F3h	Reserved
34h	-38.0	74h	-6.0	B4h	26.0	F4h	Reserved
35h	-37.5	75h	-5.5	B5h	26.5	F5h	Reserved
36h	-37.0	76h	-5.0	B6h	27.0	F6h	Reserved
37h	-36.5	77h	-4.5	B7h	27.5	F7h	Reserved
38h	-36.0	78h	-4.0	B8h	28.0	F8h	Reserved
39h	-35.5	79h	-3.5	B9h	28.5	F9h	Reserved
3Ah	-35.0	7Ah	-3.0	BAh	29.0	FAh	Reserved
3Bh	-34.5	7Bh	-2.5	BBh	29.5	FBh	Reserved
3Ch	-34.0	7Ch	-2.0	BCh	30.0	FCh	Reserved
3Dh	-33.5	7Dh	-1.5	BDh	30.5	FDh	Reserved
3Eh	-33.0	7Eh	-1.0	BEh	31.0	FEh	Reserved
3Fh	-32.5	7Fh	-0.5	BFh	31.5	FFh	Reserved

Table 50 Output Signal Path Digital Volume Range

OUTPUT SIGNAL PATH DIGITAL VOLUME LIMIT

A digital limit control is provided on each of the output signal paths. Any signal which exceeds the applicable limit will be clipped at that level. The limit control is implemented in the digital domain, before the output path DACs.

For typical applications, a limit of 0dBFS is recommended. Caution is advised when selecting other limits, as the output signal may clip in the digital and/or analogue stages of the respective signal path(s)

The digital limit register fields are described in Table 51 and Table 52.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1042 (0412h DAC Volume Limit 1L	7:0	OUT1L_VOL_LIM [7:0]	81h	Output Path 1 (Left) Digital Limit -6dBFS to +6dBFS in 0.5dB steps 00h to 73h = Reserved 74h = -6.0dBFS 75h = -5.5dBFS … (0.5dB steps) 80h = 0.0dBFS … (0.5dB steps) 8Bh = +5.5dBFS 8Ch = +6.0dBFS 8Dh to FFh = Reserved (see Table 52 for limit range)
R1046 (0416h DAC Volume Limit 1R	7:0	OUT1R_VOL_LIM [7:0]	81h	Output Path 1 (Right) Digital Limit -6dBFS to +6dBFS in 0.5dB steps 00h to 73h = Reserved 74h = -6.0dBFS 75h = -5.5dBFS … (0.5dB steps) 80h = 0.0dBFS … (0.5dB steps) 8Bh = +5.5dBFS 8Ch = +6.0dBFS 8Dh to FFh = Reserved (see Table 52 for limit range)
R1066 (042Ah DAC Volume Limit 4L	7:0	OUT4L_VOL_LIM [7:0]	81h	Output Path 4 (Left) Digital Limit -6dBFS to +6dBFS in 0.5dB steps 00h to 73h = Reserved 74h = -6.0dBFS 75h = -5.5dBFS … (0.5dB steps) 80h = 0.0dBFS … (0.5dB steps) 8Bh = +5.5dBFS 8Ch = +6.0dBFS 8Dh to FFh = Reserved (see Table 52 for limit range)

Table 51 Output Signal Path Digital Limit Control

OUTnL_VOL_LIM[7:0], OUTnR_VOL_LIM[7:0]	LIMIT (dBFS)
00h to 73h	Reserved
74h	-6.0
75h	-5.5
76h	-5.0
77h	-4.5
78h	-4.0
79h	-3.5
7Ah	-3.0
7Bh	-2.5
7Ch	-2.0
7Dh	-1.5
7Eh	-1.0
7Fh	-0.5
80h	0.0
81h	+0.5
82h	+1.0
83h	+1.5
84h	+2.0
85h	+2.5
86h	+3.0
87h	+3.5
88h	+4.0
89h	+4.5
8Ah	+5.0
8Bh	+5.5
8Ch	+6.0
8Dh to FFh	Reserved

Table 52 Output Signal Path Digital Limit Range

OUTPUT SIGNAL PATH NOISE GATE CONTROL

The CS47L24 provides a digital noise gate function for each of the output signal paths. The noise gate ensures best noise performance when the signal path is idle. When the noise gate is enabled, and the applicable signal level is below the noise gate threshold, then the noise gate is activated, causing the signal path to be muted.

The noise gate function is enabled using the NGATE_ENA register, as described in Table 53.

For each output path, the noise gate may be associated with one or more of the signal path threshold detection functions using the _NGATE_SRC register fields. When more than one signal threshold is selected, then the output path noise gate is only activated (i.e., muted) when all of the respective signal thresholds are satisfied.

For example, if the OUT1L noise gate is associated with the OUT1L and OUT1R signal paths, then the OUT1L signal path will only be muted if both the OUT1L and OUT1R signal levels are below the respective thresholds.

The noise gate threshold (the signal level below which the noise gate is activated) is set using NGATE_THR. Note that, for each output path, the noise gate threshold represents the signal level at the respective output pin(s) - the threshold is therefore independent of the digital volume register settings.

Note that, although there is only one noise gate threshold level (NGATE_THR), each of the output path noise gates may be activated independently, according to the respective signal content and the associated threshold configuration(s).

To prevent erroneous triggering, a time delay is applied before the gate is activated; the noise gate is only activated (i.e., muted) when the output levels are below the applicable signal level threshold(s) for longer than the noise gate 'hold time'. The 'hold time' is set using the NGATE_HOLD register.

When the noise gate is activated, the CS47L24 gradually attenuates the respective signal path at the rate set by the OUT_VD_RAMP register (see Table 49). When the noise gate is de-activated, the output volume increases at the rate

set by the OUT_VI_RAMP register.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1043 (0413h) Noise Gate Select 1L	11:0	OUT1L_NGATE_ SRC [11:0]	001h	Output Signal Path Noise Gate Source Enables one of more signal paths as inputs to the respective noise gate. If more than one signal path is enabled as an input, the noise gate is only activated (i.e., muted) when all of the respective signal thresholds are satisfied. [11] = Reserved [10] = Reserved [9] = Reserved [8] = Reserved [7] = Reserved [6] = OUT4L [5] = Reserved [4] = Reserved [3] = Reserved [2] = Reserved [1] = OUT1R [0] = OUT1L Each bit is coded as: 0 = Disabled 1 = Enabled
R1047 (0417h) Noise Gate Select 1R	11:0	OUT1R_NGATE_ SRC [11:0]	002h	
R1067 (042Bh) Noise Gate Select 4L	11:0	OUT4L_NGATE_ SRC [11:0]	040h	
R1112 (0458h) Noise Gate Control	5:4	NGATE_HOLD [1:0]	00	Output Signal Path Noise Gate Hold Time (delay before noise gate is activated) 00 = 30ms 01 = 120ms 10 = 250ms 11 = 500ms
	3:1	NGATE_THR [2:0]	000	Output Signal Path Noise Gate Threshold 000 = -60dB 001 = -66dB 010 = -72dB 011 = -78dB 100 = -84dB 101 = -90dB 110 = -96dB 111 = -102dB
	0	NGATE_ENA	0	Output Signal Path Noise Gate Enable 0 = Disabled 1 = Enabled

Table 53 Output Signal Path Noise Gate Control

OUTPUT SIGNAL PATH AEC LOOPBACK

The CS47L24 incorporates loopback signal path, which is ideally suited as a reference for Acoustic Echo Cancellation (AEC) processing. Any of the output signal paths may be selected as the AEC loopback source.

When configured with suitable DSP firmware, the CS47L24 can provide an integrated AEC capability. The AEC loopback feature also enables convenient hook-up to an external device for implementing the required signal processing algorithms.

The AEC Loopback source is connected after the respective digital volume controls, as illustrated in Figure 44. The AEC Loopback signal can be selected as input to any of the digital mixers within the CS47L24 digital core. The sample rate for the AEC Loopback path is configured using the OUT_RATE register - see Table 21 within the “Digital Core” section.

The AEC loopback function is enabled using the AEC_LOOPBACK_ENA register. The source signal for the Transmit Path AEC function is selected using the AEC_LOOPBACK_SRC register.

The CS47L24 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the AEC Loopback function. If an attempt is made to enable this function, and there are insufficient SYSCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

The Underclocked Error condition can be monitored using the GPIO and/or Interrupt functions. See “General Purpose Input / Output” and “Interrupts” for further details.

The AEC_ENA_STS register indicates the status of the AEC Loopback function. If an Underclocked Error condition occurs, then this bit can provide indication of whether the AEC Loopback function has been successfully enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1104 (0450h) DAC AEC Control 1	5:2	AEC_LOOPBACK_SRC [3:0]	0000	Input source for Tx AEC function 0000 = OUT1L 0001 = OUT1R 0110 = OUT4L All other codes are Reserved
	1	AEC_ENA_STS	0	Transmit (Tx) Path AEC Control Status 0 = Disabled 1 = Enabled
	0	AEC_LOOPBACK_ENA	0	Transmit (Tx) Path AEC Control 0 = Disabled 1 = Enabled

Table 54 Output Signal Path AEC Loopback Control

ANALOGUE OUTPUTS

The headphone drivers can provide a mono differential (BTL) output; this is ideal for driving an earpiece or hearing aid coil. The mono differential (BTL) configuration is selected using the OUT1_MONO register bit.

When the OUT1_MONO bit is set, then the Right channel output is an inverted copy of the Left channel output signal; this creates a differential output between the OUT1L and OUT1R signal paths. The Left and Right channel output drivers must both be enabled in Mono mode; both channels should be enabled simultaneously using the register bits described in Table 48.

The mono (BTL) signal paths are illustrated in Figure 44. Note that, in mono configuration, the effective gain of the signal path is increased by 6dB.

The OUT1L and OUT1R output signal paths are associated with the analogue outputs HPOUTL and HPOUTR respectively.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1040 (0410h) Output Path Config 1L	12	OUT1_MONO	0	Output Path 1 Mono Mode (Configures HPOUTL and HPOUTR as a mono differential output.) 0 = Disabled 1 = Enabled The gain of the signal path is increased by 6dB in differential (mono) mode.

Table 55 Headphone Driver Mono Mode Control

The headphone driver outputs HPOUTL and HPOUTR are suitable for direct connection to external headphones and earpieces. The outputs are ground-referenced, eliminating any requirement for AC coupling capacitors.

The headphone outputs incorporate a common mode, or ground loop, feedback path which provides rejection of system-related ground noise. The feedback pin must be connected to ground for normal operation of the headphone outputs.

Note that the feedback pin should be connected to GND close to the respective headphone jack, as illustrated in Figure 45. In mono (differential) mode, the feedback pin should be connected to the ground plane that is physically closest to the respective output PCB tracks.

The ground feedback path for HPOUTL and HPOUTR is provided via the HPOUTFB pin.

The speaker driver outputs SPKOUTP and SPKOUTN provide differential (BTL) outputs suitable for direct connection to an external loudspeaker. The integrated Class D speaker driver provides high efficiency at large signal levels.

The speaker driver signal paths incorporate a boost function which shifts the signal levels between the AVDD and SPKVDD voltage domains. The boost is pre-configured (+12dB) for the recommended AVDD and SPKVDD operating voltages (see “Recommended Operating Conditions”).

Ultra-low leakage and high PSRR allow the speaker supply SPKVDD to be connected directly to a lithium battery.

Note that SYSCLK must be present and enabled when using the Class D speaker output; see “Clocking and Sample Rates” for details of SYSCLK and the associated register control fields.

The OUT4L output signal path is associated with the analogue outputs SPKOUTP and SPKOUTN.

The Class D speaker output is a pulse width modulated signal, and requires external filtering in order to recreate the audio signal. With a suitable choice of external speakers, the speakers themselves can provide the necessary filtering. See “Applications Information” for further information on Class D speaker connections.

The external headphone and speaker connections are illustrated in Figure 45. Note that it is assumed that suitable speakers are chosen to provide the PWM filtering.

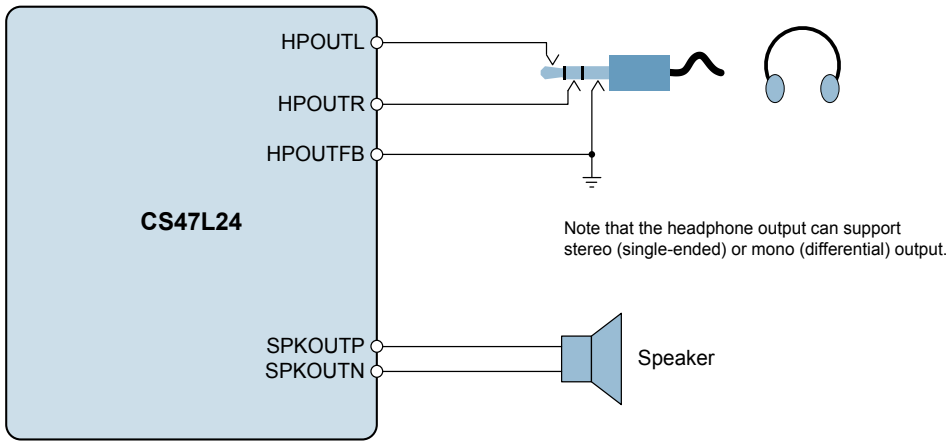


Figure 45 Headphone and Speaker Connections

GENERAL PURPOSE INPUT / OUTPUT

The CS47L24 provides a number of GPIO functions to enable interfacing and detection of external hardware and to provide logic outputs to other devices. The GPIO input functions can be used to generate an Interrupt (IRQ) event. The GPIO and Interrupt circuits support the following functions:

- Logic input / Button detect / Write Sequencer trigger (GPIO input)
- Logic '1' and logic '0' output (GPIO output)
- Interrupt (IRQ) status output
- DSP Status Flag (DSP IRQn) and RAM status output
- Clock output
- Frequency Locked Loop (FLL) status output
- Frequency Locked Loop (FLL) Clock output
- Pulse Width Modulation (PWM) Signal output
- Headphone Enable status output
- Boot Sequence status output
- Asynchronous Sample Rate Converter (ASRC) Lock status and Configuration Error output
- Isochronous Sample Rate Converter (ISRC) Configuration Error output
- Over-Temperature, Short Circuit Protection, and Speaker Shutdown status output
- Dynamic Range Control (DRC) status output
- Control Write Sequencer status output
- Control Interface Error status output
- Clocking Error status output

GPIO CONTROL

For each GPIO, the selected function is determined by the GP*n*_FN field, where n identifies the GPIO pin (1 or 2). The pin direction, set by GP*n*_DIR, must be set according to function selected by GP*n*_FN.

When a pin is configured as a GPIO input (GP*n*_DIR = 1, GP*n*_FN = 01h), the logic level at the pin can be read from the respective GP*n*_LVL bit. Note that GP*n*_LVL is not affected by the GP*n*_POL bit.

A de-bounce circuit can be enabled on any GPIO input, to avoid false event triggers. This is enabled on each pin by setting the respective GP*n*_DB bit. The de-bounce circuit uses the 32kHz clock, which must be enabled whenever input de-bounce functions are required. The de-bounce time is configurable using the GP_DBTIME register. See “Clocking and Sample Rates” for further details of the CS47L24 clocking configuration.

Each of the GPIO pins is an input to the Interrupt control circuit and can be used to trigger an Interrupt event. An interrupt event is triggered on the rising and falling edges of the GPIO input. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

Integrated pull-up and pull-down resistors are provided on each of the GPIO pins; these can be configured independently using the GP*n*_PU and GP*n*_PD fields. Note that, if GP*n*_PU and GP*n*_PD are both set for any GPIO pin, then the pull-up and pull-down will be disabled.

When a pin is configured as a GPIO output (GP*n*_DIR = 0, GP*n*_FN = 01h), its level can be set to logic 0 or logic 1 using the GP*n*_LVL field. Note that the GP*n*_LVL registers are ‘write only’ when the respective GPIO pin is configured as an output.

When a pin is configured as an output (GP*n*_DIR = 0), the polarity can be inverted using the GP*n*_POL bit. When GP*n*_POL = 1, then the selected output function is inverted. In the case of Logic Level output (GP*n*_FN = 01h), the external output will be the opposite logic level to GP*n*_LVL when GP*n*_POL = 1.

A GPIO output can be either CMOS driven or Open Drain. This is selected on each pin using the respective GP*n*_OP_CFG bit.

The register fields that control the GPIO pins are described in Table 56.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3072 (0C00h) GPIO1 CTRL R3073 (0C01h) GPIO2 CTRL	15	GPn_DIR	1	GPIOn Pin Direction 0 = Output 1 = Input
	14	GPn_PU	0	GPIOn Pull-Up Enable 0 = Disabled 1 = Enabled
	13	GPn_PD	1	GPIOn Pull-Down Enable 0 = Disabled 1 = Enabled
	11	GPn_LVL	0	GPIOn level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. For output functions only, when GPn_POL is set, the register is the opposite logic level to the external pin. Note that the GP*n*_LVL register is 'write only' when GP*n*_DIR=0.
	10	GPn_POL	0	GPIOn Output Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)
	9	GPn_OP_CFG	0	GPIOn Output Configuration 0 = CMOS 1 = Open Drain
	8	GPn_DB	1	GPIOn Input De-bounce 0 = Disabled 1 = Enabled
	6:0	GPn_FN [6:0]	01h	GPIOn Pin Function (see Table 57 for details)
R3088 (0C10h) GPIO Debounce Config	15:12	GP_DBTIME [3:0]	0001	GPIO Input de-bounce time 0h = 100us 1h = 1.5ms 2h = 3ms 3h = 6ms 4h = 12ms 5h = 24ms 6h = 48ms 7h = 96ms 8h = 192ms 9h = 384ms Ah = 768ms Bh to Fh = Reserved
Note: *n* is a number (1 or 2) that identifies the individual GPIO.				

Table 56 GPIO Control

GPIO FUNCTION SELECT

The available GPIO functions for GPIO pins 1 and 2 are described in Table 57.

The function of each GPIO is set using the GP*n*_FN register, where n identifies the GPIO pin (1 or 2). Note that the respective GP*n*_DIR must also be set according to whether the function is an input or output.

GPn_FN	DESCRIPTION	COMMENTS
00h		No function
01h	Button detect input / Logic level output	GPn_DIR = 0: GPIO pin logic level is set by GPn_LVL. GPn_DIR = 1: Button detect or logic level input.
02h	IRQ1 Output	Interrupt (IRQ1) output 0 = IRQ1 not asserted 1 = IRQ1 asserted
03h	IRQ2 Output	Interrupt (IRQ2) output 0 = IRQ2 not asserted 1 = IRQ2 asserted
04h	OPCLK Clock Output	Configurable clock output derived from SYSCLK
05h	FLL1 Clock	Clock output from FLL1
06h	FLL2 Clock	Clock output from FLL2
08h	PWM1 Output	Configurable Pulse Width Modulation output PWM1
09h	PWM2 Output	Configurable Pulse Width Modulation output PWM2
0Ah	SYSCLK Underclocked Error	Indicates that an unsupported clocking configuration has been attempted 0 = Normal 1 = SYSCLK underclocking error
0Bh	ASYNCCLK Underclocked Error	Indicates that an unsupported clocking configuration has been attempted 0 = Normal 1 = ASYNCCLK underclocking error
0Ch	FLL1 Lock	Indicates FLL1 Lock status 0 = Not locked 1 = Locked
0Dh	FLL2 Lock	Indicates FLL2 Lock status 0 = Not locked 1 = Locked
0Fh	FLL1 Clock OK	Indicates FLL1 Clock OK status 0 = FLL1 Clock output is not active 1 = FLL1 Clock output is active
10h	FLL2 Clock OK	Indicates FLL2 Clock OK status 0 = FLL2 Clock output is not active 1 = FLL2 Clock output is active
15h	Write Sequencer status	Indicates Write Sequencer status A short pulse is output when the Write Sequencer has completed all scheduled sequences.
16h	Control Interface Address Error	Indicates Control Interface Address error 0 = Normal 1 = Control Interface Address error
1Ah	ASRC1 Lock	Indicates ASRC1 Lock status 0 = Not locked 1 = Locked
1Bh	ASRC2 Lock	Indicates ASRC2 Lock status 0 = Not locked 1 = Locked

GPn_FN	DESCRIPTION	COMMENTS
1Ch	ASRC Configuration Error	Indicates ASRC configuration error 0 = ASRC configuration OK 1 = ASRC configuration error
1Dh	DRC1 Signal Detect	Indicates DRC1 Signal Detect status 0 = Signal threshold not exceeded 1 = Signal threshold exceeded
1Eh	DRC1 Anti-Clip Active	Indicates DRC1 Anti-Clip status 0 = Anti-Clip is not active 1 = Anti-Clip is active
1Fh	DRC1 Decay Active	Indicates DRC1 Decay status 0 = Decay is not active 1 = Decay is active
20h	DRC1 Noise Gate Active	Indicates DRC1 Noise Gate status 0 = Noise Gate is not active 1 = Noise Gate is active
21h	DRC1 Quick Release Active	Indicates DRC1 Quick Release status 0 = Quick Release is not active 1 = Quick Release is active
22h	DRC2 Signal Detect	Indicates DRC2 Signal Detect status 0 = Signal threshold not exceeded 1 = Signal threshold exceeded
23h	DRC2 Anti-Clip Active	Indicates DRC2 Anti-Clip status 0 = Anti-Clip is not active 1 = Anti-Clip is active
24h	DRC2 Decaying	Indicates DRC2 Decay status 0 = Decay is not active 1 = Decay is active
25h	DRC2 Noise Gate Active	Indicates DRC2 Noise Gate status 0 = Noise Gate is not active 1 = Noise Gate is active
26h	DRC2 Quick Release Active	Indicates DRC2 Quick Release status 0 = Quick Release is not active 1 = Quick Release is active
27h	Mixer Dropped Sample Error	Indicates a dropped sample in the digital core mixers 0 = Normal 1 = Mixer dropped sample error
2Bh	Speaker Overheat Shutdown	Indicates Shutdown Temperature status 0 = Temperature is below shutdown level 1 = Temperature is above shutdown level
2Ch	Speaker Overheat Warning	Indicates Warning Temperature status 0 = Temperature is below warning level 1 = Temperature is above warning level
2Dh	Underclocked Error	Indicates insufficient SYSCLK or ASYNCCLK cycles for one or more of the selected signal paths or signal processing functions. Increasing the SYSCLK or ASYNCCLK frequency (as applicable) should allow the selected configuration to be supported. 0 = Normal 1 = Underclocked error
2Eh	Overclocked Error	Indicates that an unsupported device configuration has been attempted, as the clocking requirements of the requested configuration exceed the device limits. 0 = Normal 1 = Overclocked error
2Fh	HPL Status	HPOUTL Enable Status A short pulse is output when the HPOUTL Enable control sequence has completed.

GPn_FN	DESCRIPTION	COMMENTS
30h	HPR Status	HPOUTR Enable Status A short pulse is output when the HPOUTR Enable control sequence has completed.
35h	DSP IRQ1 Flag	DSP Status flag (DSP_IRQ1) output 0 = DSP_IRQ1 not asserted 1 = DSP_IRQ1 asserted
36h	DSP IRQ2 Flag	DSP Status flag (DSP_IRQ2) output 0 = DSP_IRQ2 not asserted 1 = DSP_IRQ2 asserted
37h	DSP IRQ3 Flag	DSP Status flag (DSP_IRQ3) output 0 = DSP_IRQ3 not asserted 1 = DSP_IRQ3 asserted
38h	DSP IRQ4 Flag	DSP Status flag (DSP_IRQ4) output 0 = DSP_IRQ4 not asserted 1 = DSP_IRQ4 asserted
39h	DSP IRQ5 Flag	DSP Status flag (DSP_IRQ5) output 0 = DSP_IRQ5 not asserted 1 = DSP_IRQ5 asserted
3Ah	DSP IRQ6 Flag	DSP Status flag (DSP_IRQ6) output 0 = DSP_IRQ6 not asserted 1 = DSP_IRQ6 asserted
3Bh	DSP IRQ7 Flag	DSP Status flag (DSP_IRQ7) output 0 = DSP_IRQ6 not asserted 1 = DSP_IRQ6 asserted
3Ch	DSP IRQ8 Flag	DSP Status flag (DSP_IRQ8) output 0 = DSP_IRQ6 not asserted 1 = DSP_IRQ6 asserted
3Dh	OPCLK Async Clock Output	Configurable clock output derived from ASYNCCLK
44h	Boot Done	Boot Status A short pulse is output when the Boot Sequence has completed.
46h	DSP2 RAM Ready	DSP2 RAM Status 0 = Not ready 1 = Ready
47h	DSP3 RAM Ready	DSP3 RAM Status 0 = Not ready 1 = Ready
4Bh	SYSCLK_ENA Status	SYSCLK_ENA Status 0 = SYSCLK_ENA is enabled 1 = SYSCLK_ENA is disabled
4Ch	ASYNC_CLK_ENA Status	ASYNC_CLK_ENA Status 0 = ASYNC_CLK_ENA is enabled 1 = ASYNC_CLK_ENA is disabled
4Dh	ISRC1 Configuration Error	Indicates ISRC1 configuration error 0 = ISRC configuration OK 1 = ISRC configuration error
4Eh	ISRC2 Configuration Error	Indicates ISRC2 configuration error 0 = ISRC configuration OK 1 = ISRC configuration error
4Fh	ISRC3 Configuration Error	Indicates ISRC3 configuration error 0 = ISRC configuration OK 1 = ISRC configuration error
53h	HPOUTL Short Circuit Status (Negative side)	HPOUTL Short Circuit status 0 = Normal 1 = Short Circuit detected
54h	HPOUTR Short Circuit Status (Negative side)	HPOUTR Short Circuit status 0 = Normal

GPn_FN	DESCRIPTION	COMMENTS
		1 = Short Circuit detected
55h	HPOUTL Short Circuit Status (Positive side)	HPOUTL Short Circuit status 0 = Normal 1 = Short Circuit detected
56h	HPOUTR Short Circuit Status (Positive side)	HPOUTR Short Circuit status 0 = Normal 1 = Short Circuit detected
5Fh	SPKOUT Short Circuit Status	SPKOUT Short Circuit status 0 = Normal 1 = Short Circuit detected
61h	Speaker Shutdown Status	Speaker Shutdown Status 0 = Normal 1 = Speaker Shutdown completed (due to Overheat Temperature or Short Circuit condition)

Table 57 GPIO Function Select (GPIO1, GPIO2)

BUTTON DETECT / WRITE SEQUENCER TRIGGER (GPIO INPUT)

GP*n*_FN = 01h.

Button detect functionality can be selected on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. The same functionality can be used to support a Jack Detect input function.

It is recommended to enable the GPIO input de-bounce feature when using GPIOs as button input or Jack Detect input.

The GP*n*_LVL fields may be read to determine the logic levels on a GPIO input, after the selectable de-bounce controls. Note that GP*n*_LVL is not affected by the GP*n*_POL bit.

The de-bounced GPIO signals can also be used to trigger the Control Write Sequencer; user-defined control sequences may be associated with either the rising or falling edges of a GPIO input. See “Control Write Sequencer” for further details.

The de-bounced GPIO signals are also inputs to the Interrupt control circuit. An interrupt event is triggered on the rising and falling edges of the GPIO input. The associated interrupt bits are latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

LOGIC ‘1’ AND LOGIC ‘0’ OUTPUT (GPIO OUTPUT)

GP*n*_FN = 01h.

The CS47L24 can be programmed to drive a logic high or logic low level on a GPIO pin by selecting the “GPIO Output” function as described in “GPIO Control”.

The output logic level is selected using the respective GP*n*_LVL bit. Note that the GP*n*_LVL registers are ‘write only’ when the respective GPIO pin is configured as an output.

The polarity of the GPIO output can be inverted using the GP*n*_POL registers. If GP*n*_POL=1, then the external output will be the opposite logic level to GP*n*_LVL.

INTERRUPT (IRQ) STATUS OUTPUT

GP*n*_FN = 02h, 03h.

The CS47L24 has an Interrupt Controller which can be used to indicate when any selected Interrupt events occur. An interrupt can be generated by any of the events described throughout the GPIO function definition above. Individual interrupts may be masked in order to configure the Interrupt as required. See “Interrupts” for further details.

The Interrupt Controller supports two separate Interrupt Request (IRQ) outputs. The IRQ1 or IRQ2 status may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

Note that the IRQ1 status is output on the $\overline{\text{IRQ}}$ pin at all times.

DSP STATUS FLAG (DSP IRQN) OUTPUT

GP*n*_FN = 35h, 36h, 37h, 38h, 39h, 3A, 3Bh, 3Ch, 46h, 47h.

The CS47L24 supports up to eight DSP Status flags as outputs from the DSP blocks. These are configurable within the DSP to provide external indication of the required function(s). Status flags indicating the DSPn RAM status (where ‘n’ is 1 or 2) are also supported. See “Digital Core” for more details of the DSP blocks.

The DSP Status and DSP RAM Ready flags may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. The DSP Status and DSP RAM Ready outputs are described in Table 58.

The DSP Status flags are inputs to the Interrupt Controller circuit. An interrupt event is triggered on the rising edge of the DSP Status (DSP_IRQn) flags or DSP RAM Ready flags. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

GPN_FN	DESCRIPTION	COMMENTS
35h	DSP Status (DSP_IRQ1)	External indication of DSP_IRQ1_STS
36h	DSP Status (DSP_IRQ2)	External indication of DSP_IRQ2_STS
37h	DSP Status (DSP_IRQ3)	External indication of DSP_IRQ3_STS
38h	DSP Status (DSP_IRQ4)	External indication of DSP_IRQ4_STS
39h	DSP Status (DSP_IRQ5)	External indication of DSP_IRQ5_STS
3Ah	DSP Status (DSP_IRQ6)	External indication of DSP_IRQ6_STS
3Bh	DSP Status (DSP_IRQ7)	External indication of DSP_IRQ7_STS
3Ch	DSP Status (DSP_IRQ8)	External indication of DSP_IRQ8_STS
46h	DSP2 RAM Ready	Indicates DSP2 RAM Ready status
47h	DSP3 RAM Ready	Indicates DSP3 RAM Ready status

Table 58 DSP Status and RAM Ready Indications

OPCLK AND OPCLK_ASYNC CLOCK OUTPUT

GP*n*_FN = 04h, 3Dh.

A clock output (OPCLK) derived from SYSCLK can be output on a GPIO pin. The OPCLK frequency is controlled by OPCLK_DIV and OPCLK_SEL. The OPCLK output is enabled using the OPCLK_ENA register, as described in Table 59.

A clock output (OPCLK_ASYNC) derived from ASYNCCLK can be output on a GPIO pin. The OPCLK_ASYNC frequency is controlled by OPCLK_ASYNC_DIV and OPCLK_ASYNC_SEL. The OPCLK_ASYNC output is enabled using the OPCLK_ASYNC_ENA register

It is recommended to disable the clock output (OPCLK_ENA=0 or OPCLK_ASYNC_ENA=0) before making any change to the respective OPCLK_DIV, OPCLK_SEL, OPCLK_ASYNC_DIV or OPCLK_ASYNC_SEL registers.

The OPCLK or OPCLK_ASYNC Clock outputs can be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

Note that the OPCLK source frequency cannot be higher than the SYSCLK frequency. The OPCLK_ASYNC source frequency cannot be higher than the ASYNCCLK frequency. The maximum output frequency supported for GPIO output is noted in the “Electrical Characteristics”.

See “Clocking and Sample Rates” for more details of the system clocks (SYSCLK and ASYNCCLK).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R329 (0149h) Output system clock	15	OPCLK_ENA	0	OPCLK Enable 0 = Disabled 1 = Enabled
	7:3	OPCLK_DIV [4:0]	00h	OPCLK Divider 00h = Divide by 1 01h = Divide by 1 02h = Divide by 2 03h = Divide by 3 … 1Fh = Divide by 31
	2:0	OPCLK_SEL [2:0]	000	OPCLK Source Frequency 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) All other codes are Reserved The frequencies in brackets apply for 44.1kHz-related SYSCLK rates only (i.e., SAMPLE_RATE_n = 01XXX). The OPCLK Source Frequency must be less than or equal to the SYSCLK frequency.
R330 (014Ah) Output async clock	15	OPCLK_ASYNC_ ENA	0	OPCLK_ASYNC Enable 0 = Disabled 1 = Enabled
	7:3	OPCLK_ASYNC_ DIV [4:0]	00h	OPCLK_ASYNC Divider 00h = Divide by 1 01h = Divide by 1 02h = Divide by 2 03h = Divide by 3 … 1Fh = Divide by 31
	2:0	OPCLK_ASYNC_ SEL [2:0]	000	OPCLK_ASYNC Source Frequency 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) All other codes are Reserved The frequencies in brackets apply for 44.1kHz-related ASYNCCLK rates only (i.e., ASYNC_SAMPLE_RATE_n = 01XXX). The OPCLK_ASYNC Source Frequency must be less than or equal to the ASYNCCLK frequency.

Table 59 OPCLK and OPCLK_ASYNC Control

FREQUENCY LOCKED LOOP (FLL) STATUS OUTPUT

GP*n*_FN = 0Ch, 0Dh, 0Fh, 10h.

The CS47L24 supports FLL status flags, which may be used to control other events. See “Clocking and Sample Rates” for more details of the FLL.

The ‘FLL Clock OK’ signals indicate that the respective FLL has started up and is providing an output clock. The ‘FLL Lock’ signals indicate whether FLL Lock has been achieved.

The FLL Clock OK and FLL Lock signals may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

The FLL Clock OK and FLL Lock signals are inputs to the Interrupt Controller circuit. An interrupt event is triggered on the rising and falling edges of these signals. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

FREQUENCY LOCKED LOOP (FLL) CLOCK OUTPUT

GP*n*_FN = 05h, 06h.

Clock outputs derived from the FLLs may be output on a GPIO pin. The GPIO output from each FLLn (where ‘n’ is 1 or 2) is controlled by the respective FLLn_GPCLK_DIV and FLLn_GPCLK_ENA registers, as described in Table 60.

It is recommended to disable the clock output (FLLn_GPCLK_ENA=0) before making any change to the respective FLLn_GPCLK_DIV register.

Note that the FLLn_GPCLK_DIV and FLLn_GPCLK_ENA registers affect the GPIO outputs only; they do not affect the FLL frequency. The maximum output frequency supported for GPIO output is noted in the “Electrical Characteristics”.

The Frequency Locked Loop (FLL) Clock outputs may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

See “Clocking and Sample Rates” for more details of the CS47L24 system clocking and for details of how to configure the FLLs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R394 (018Ah) FLL1 GPIO Clock	7:1	FLL1_GPCLK_DIV [6:0]	06h	FLL1 GPIO Clock Divider 00h to 06h= Divide by 6 07h = Divide by 7 08h = Divide by 8 09h = Divide by 9 … 7Fh = Divide by 127 (F_{GPIO} = F_{VCO} / FLL1_GPCLK_DIV)
	0	FLL1_GPCLK_ENA	0	FLL1 GPIO Clock Enable 0 = Disabled 1 = Enabled
R426 (01AAh) FLL2 GPIO Clock	7:1	FLL2_GPCLK_DIV [6:0]	06h	FLL2 GPIO Clock Divider 00h to 06h= Divide by 6 07h = Divide by 7 08h = Divide by 8 09h = Divide by 9 … 7Fh = Divide by 127 (F_{GPIO} = F_{VCO} / FLL2_GPCLK_DIV)
	0	FLL2_GPCLK_ENA	0	FLL2 GPIO Clock Enable 0 = Disabled 1 = Enabled

Table 60 FLL Clock Output Control

PULSE WIDTH MODULATION (PWM) SIGNAL OUTPUT

GP*n*_FN = 08h, 09h.

The CS47L24 incorporates two Pulse Width Modulation (PWM) signal generators which can be enabled as GPIO outputs. The duty cycle of each PWM signal can be modulated by an audio source, or can be set to a fixed value using a control register setting.

The Pulse Width Modulation (PWM) outputs may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

See “Digital Core” for details of how to configure the PWM signal generators.

Note that the PWM output should always be disabled (PWMn_ENA=0, as described in Table 20) whenever the system clock, SYSCLK, is disabled. Failure to do this may result in a persistent logic ‘1’ DC output from the PWM generator. See “Clocking and Sample Rates” for details of system clocking and the associated control requirements.

HEADPHONE ENABLE STATUS OUTPUT

GP*n*_FN = 2Fh, 30h.

Whenever a headphone output path is enabled or disabled, a pop-suppression control sequence is triggered. Status outputs indicating the progress of these sequences are provided. Note that this provides See “Output Signal Path” for details of the Output Enable functions.

A logic signal from the Headphone Enable control functions may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. This logic signal is set high for a short pulse duration (approx. 100ns) whenever the respective control sequence has completed. The headphone control sequence status outputs are described in Table 61.

The Headphone Enable control sequences also provide inputs to the Interrupt control circuit. An interrupt event is triggered on completion of the respective control sequence. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

GPN_FN	DESCRIPTION	COMMENTS
2Fh	HPOUTL Enable Status	A short pulse is output when the respective control sequence has completed.
30h	HPOUTR Enable Status	

Table 61 Headphone Enable Status Indications

BOOT DONE STATUS OUTPUT

GP*n*_FN = 44h.

The CS47L24 executes a user-configurable Boot Sequence following Power-On Reset (POR), Hardware Reset, or Software Reset. Control register writes should not be attempted while the Boot Sequence is running.

For details of the Boot Sequence, see “Control Write Sequencer”.

The BOOT_DONE_STS register bit (see Table 92) indicates the status of the Boot Sequence. (When BOOT_DONE_STS=1, then the Boot Sequence is complete.)

A logic signal from the Boot Sequence function may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. This logic signal is set high for a short pulse duration (approx. 100ns) when the Boot Sequence has completed. To output this signal, the Boot Sequence must be programmed to configure a GPIO pin for this function. Note that, under default register conditions, completion of the Boot Sequence is indicated via the Interrupt circuit.

The BOOT_DONE_STS signal is also an input to the Interrupt Controller circuit. An interrupt event is triggered on the rising edge of this signal. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

ASYNCHRONOUS SAMPLE RATE CONVERTER (ASRC) LOCK STATUS OUTPUT

GP*n*_FN = 1Ah, 1Bh.

The CS47L24 maintains a flag indicating the lock status of the Asynchronous Sample Rate Converters (ASRCs), which may be used to control other events if required. See “Digital Core” for more details of the ASRCs.

The ASRC Lock signals may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

The ASRC Lock signals are inputs to the Interrupt control circuit. An interrupt event is triggered on the rising and falling edges of the ASRC Lock signals. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

ASYNCHRONOUS SAMPLE RATE CONVERTER (ASRC) CONFIGURATION ERROR STATUS OUTPUT

GPn_FN = 1Ch.

The CS47L24 performs automatic checks to confirm that the ASRCs are configured with valid settings. Invalid settings include conditions where one of the associated sample rates is higher than 48kHz. If an invalid ASRC configuration is detected, this can be indicated using the GPIO and/or Interrupt functions.

The ASRC Configuration Error signal may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

The ASRC Configuration Error signal is an input to the Interrupt Controller circuit. An interrupt event is triggered on the rising edge of the ASRC Configuration Error signal. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

ISOCHRONOUS SAMPLE RATE CONVERTER (ISRC) CONFIGURATION ERROR STATUS OUTPUT

GPn_FN = 4Dh, 4Eh, 4Fh.

The CS47L24 performs automatic checks to confirm that the ISRCs are configured with valid settings. Invalid settings include conditions where an invalid combination of sample rates is configured. If an invalid ISRC configuration is detected, this can be indicated using the GPIO and/or Interrupt functions.

The ISRC Configuration Error signal may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

The ISRC Configuration Error signals are inputs to the Interrupt Controller circuit. An interrupt event is triggered on the rising edge of the ISRC Configuration Error signals. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

OVER-TEMPERATURE, SHORT CIRCUIT PROTECTION, AND SPEAKER SHUTDOWN STATUS OUTPUT

GP*n*_FN = 2Bh, 2Ch, 53h, 54h, 55h, 56h, 5Fh, 61h.

The CS47L24 incorporates a temperature sensor which detects when the device temperature is within normal limits or if the device is approaching a hazardous temperature condition.

The temperature status may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. A GPIO pin can be used to indicate either an Overheat Warning Temperature event or an Overheat Shutdown Temperature event.

The CS47L24 provides short circuit protection on the Class D speaker outputs, and on each of the headphone output paths.

The status of each of the short circuit detection circuits may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”.

Note that two short circuit indications are implemented for each headphone output channel (relating to detection in the positive and negative output voltage regions respectively); if either of these indications is asserted, then a short circuit condition exists in the respective output path.

If the Overheat Shutdown Temperature is exceeded, or if a short circuit is detected on the Class D speaker outputs, then the Class D speaker outputs will automatically be disabled in order to protect the device. When the speaker driver shutdown is complete, the Speaker Shutdown signal will be asserted. The speaker driver shutdown status can also be output directly on a GPIO pin.

The Overtemperature, Short Circuit protection, and Speaker Shutdown status flags are inputs to the Interrupt control

circuit. An interrupt event may be triggered on the applicable edges of these signals. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

DYNAMIC RANGE CONTROL (DRC) STATUS OUTPUT

GP*n*_FN = 1Dh, 1Eh, 1Fh, 20h, 21h, 22h, 23h, 24h, 25h, 26h.

The Dynamic Range Control (DRC) circuits provide status outputs, which may be used to control other events if required.

The DRC status flags may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. The DRC status outputs are described in Table 62.

See “Digital Core” for more details of the DRC.

GPN_FN	DESCRIPTION	COMMENTS
1Dh	DRC1 Signal Detect	Indicates a signal is present on the respective DRC path. The threshold level is configurable (see Table 13).
1Eh	DRC1 Anti-Clip Active	Indicates the DRC anti-clip function has been triggered; the DRC gain is decreasing in response to a rising signal level.
1Fh	DRC1 Decay Active	Indicates that the DRC gain is increasing in response to a low-level signal input.
20h	DRC1 Noise Gate Active	Indicates that the DRC noise gate has been triggered; an idle signal condition has been detected.
21h	DRC1 Quick Release Active	Indicates that the DRC quick-release function has been triggered; the DRC gain is increasing rapidly following detection of a short transient peak.
22h	DRC2 Signal Detect	Description as above.
23h	DRC2 Anti-Clip Active	Description as above.
24h	DRC2 Decay Active	Description as above.
25h	DRC2 Noise Gate Active	Description as above.
26h	DRC2 Quick Release Active	Description as above.

Table 62 Dynamic Range Control (DRC) Status Indications

CONTROL WRITE SEQUENCER STATUS OUTPUT

GP*n*_FN = 15h.

The CS47L24 Control Write Sequencer (WSEQ) can be used to execute a sequence of register write operations in response to a simple trigger event. See “Control Write Sequencer” for details of the Control Write Sequencer.

The WSEQ_BUSY register bit (see Table 86) indicates the status of the Control Write Sequencer. When WSEQ_BUSY=1, this indicates that one or more Write Sequence operations are in progress or are queued for sequential execution.

A logic signal from the Write Sequencer function may be output directly on a GPIO pin by setting the respective GPIO registers as described in “GPIO Control”. This logic signal is set high for a short pulse duration (approx. 100ns) whenever the Write Sequencer has completed all scheduled sequences, and there are no more pending operations

The Write Sequencer status is an input to the Interrupt control circuit. An interrupt event is triggered on completion of a Control Sequence. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See “Interrupts” for more details of the Interrupt event handling.

CONTROL INTERFACE ERROR STATUS OUTPUT

GP*n*_FN = 16h.

The CS47L24 is controlled by writing to registers through a 4-wire (SPI) serial control interface, as described in the "Control Interface" section.

The CS47L24 performs automatic checks to confirm if a register access is successful. Register access will be unsuccessful if an invalid register address is selected. Read/write access to the DSP firmware memory will be unsuccessful if the associated clocking is not enabled. If an invalid or unsuccessful register operation is attempted, this can be indicated using the GPIO and/or Interrupt functions.

The Control Interface Error signal may be output directly on a GPIO pin by setting the respective GPIO registers as described in "GPIO Control".

The Control Interface Error signal is an input to the Interrupt Controller circuit. An interrupt event is triggered on the rising edge of the Control Interface Error signal. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See "Interrupts" for more details of the Interrupt event handling.

SYSTEM CLOCKS ENABLE STATUS OUTPUT

GP*n*_FN = 4Bh, 4Ch.

The CS47L24 requires a system clock (SYSCLK) for its internal functions and to support the input/output signal paths. The CS47L24 can support two independent clock domains, with selected functions referenced to the ASYNCCLK clock domain. See "Clocking and Sample Rates" for details of these clocks.

The SYSCLK_ENA and ASYNC_CLK_ENA registers (see Table 69) control the SYSCLK and ASYNCCLK signals respectively. When '0' is written to these registers, the host processor must wait until the CS47L24 has shut down the associated functions before issuing any other register write commands.

The SYSCLK Enable and ASYNCCLK Enable status may be output directly on a GPIO pin by setting the respective GPIO registers as described in "GPIO Control".

The SYSCLK Enable and ASYNCCLK Enable signals are inputs to the Interrupt Controller circuit. An interrupt event is triggered when the respective clock functions have been shut down. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See "Interrupts" for more details of the Interrupt event handling.

CLOCKING ERROR STATUS OUTPUT

GP*n*_FN = 0Ah, 0Bh, 27h, 2Dh, 2Eh.

The CS47L24 performs automatic checks to confirm that the system clocks are correctly configured according to the commanded functionality. An invalid configuration is one where there are insufficient clock cycles to support the digital processing required by the commanded signal paths.

An Underclocked Error condition is where there are insufficient clock cycles for the requested functionality, and increasing the SYSCLK or ASYNCCLK frequency (as applicable) should allow the selected configuration to be supported.

An Overclocked Error condition is where the requested functionality cannot be supported, as the clocking requirements of the requested configuration exceed the device limits.

The system clocks (SYSCLK and, where applicable, ASYNCCLK) must be enabled before any signal path is enabled. If an attempt is made to enable a signal path, and there are insufficient clock cycles to support that path, then the attempt will be unsuccessful. Note that any signal paths that are already active will not be affected under these circumstances.

The Clocking Error signals may be output directly on a GPIO pin by setting the respective GPIO registers as described in "GPIO Control". The Clocking Error conditions are described in Table 63.

The Clocking Error signals are inputs to the Interrupt Controller circuit. An interrupt event is triggered on the rising and falling edges of the Clocking Error signals. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See "Interrupts" for more details of the Interrupt event handling.

GPN_FN	DESCRIPTION	COMMENTS
0Ah	SYSCLK Underclocked	Indicates insufficient SYSCLK cycles for the commanded functionality.
0Bh	ASYNCCLK Underclocked	Indicates insufficient ASYNCCLK cycles for the commanded functionality.
27h	Mixer Dropped Sample Error	Indicates a dropped sample in the digital core mixer function.
2Dh	Underclocked Error	Indicates insufficient SYSCLK or ASYNCCLK cycles for one or more of the selected signal paths or signal processing functions. Increasing the SYSCLK or ASYNCCLK frequency (as applicable) should allow the selected configuration to be supported. Status bits associated with specific sub-systems provide further de-bug capability. The INnx_ENA_STS bits in register R769 indicate the status of each of the input (digital microphone) signal paths. The OUTnx_ENA_STS bits in registers R1025 and R1030 indicate the status of each of the output (Headphone or Speaker) signal paths. The ASRCnx_ENA_STS bits in register R3809 indicate the status of each of the ASRC signal paths. The FX_STS field in register R3585 indicates the status of each of the Effects (EQ, DRC or LHPF) signal paths. The *MIX_STSn fields in registers R1600 to R3000 indicate the status of each of the Digital Core mixer signal paths. The ISRCn and AIFn functions are also inputs to the Underclocked Error status indication, but there are no specific _STS register bits associated with these.
2Eh	Overclocked Error	Indicates that an unsupported device configuration has been attempted, as the clocking requirements of the requested configuration exceed the device limits.

Table 63 Clocking Error Status Indications

INTERRUPTS

The Interrupt Controller has multiple inputs. These include the GPIO input pins, DSP_IRQn flags, FLL / ASRC Lock detection, and Clocking configuration error indications. (See Table 64, Table 65 and Table 66 for a full definition of the Interrupt Controller inputs.) Any combination of these inputs can be used to trigger an Interrupt Request (IRQ) event.

The Interrupt Controller supports two sets of interrupt registers. This allows two separate Interrupt Request (IRQ) outputs to be generated, and for each IRQ to report a different set of input or status conditions.

For each Interrupt Request (IRQ1 and IRQ2) output, there is an Interrupt register field associated with each of the interrupt inputs. These fields are asserted whenever a logic edge is detected on the respective input. Some inputs are triggered on rising edges only; some are triggered on both edges. The Interrupt register fields for IRQ1 are described in Table 64. The Interrupt register fields for IRQ2 are described in Table 65. The Interrupt flags can be polled at any time, or else in response to the Interrupt Request (IRQ) output being signalled via the IRQ pin or a GPIO pin.

All of the Interrupts are edge-triggered, as noted above. Many of these are triggered on both the rising and falling edges and, therefore, the Interrupt registers cannot indicate which edge has been detected. The “Raw Status” fields described in Table 66 provide readback of the current value of the corresponding inputs to the Interrupt Controller. Note that the status of any GPIO inputs can be read using the GPn_LVL registers, as described in Table 56.

The UNDERCLOCKED_STS and OVERCLOCKED_STS registers represent the logical ‘OR’ of status flags from multiple sub-systems. The status bits in registers R3364 to R3366 (see Table 66) provide readback of these lower-level signals. See “Clocking and Sample Rates” for a description of the Underclocked and Overclocked Error conditions.

Individual mask bits can enable or disable different functions from the Interrupt controller. The mask bits are described in Table 64 (for IRQ1) and Table 65 (for IRQ2). Note that a masked interrupt input will not assert the corresponding interrupt register field, and will not cause the associated Interrupt Request (IRQ) output to be asserted.

The Interrupt Request (IRQ) outputs represent the logical ‘OR’ of the associated interrupt registers. (IRQ1 is derived from the _EINT1 registers; IRQ2 is derived from the _EINT2 registers). The Interrupt register fields are latching fields and, once they are set, they are not reset until a ‘1’ is written to the respective register bit(s). The Interrupt Request (IRQ) outputs are not reset until each of the associated interrupts has been reset.

A de-bounce circuit can be enabled on any GPIO input, to avoid false event triggers. This is enabled on each pin using the register bits described in Table 56. The GPIO de-bounce circuit uses the 32kHz clock, which must be enabled whenever the GPIO de-bounce function is required.

A de-bounce circuit is always enabled on the FLL status inputs; either the 32kHz clock, or the SYSCLK signal, must be enabled to trigger an Interrupt from the FLL status inputs. Note that the “Raw Status” fields (described in Table 66), are valid without clocking, and can be used to provide FLL status readback when system clocks are not available.

The IRQ outputs can be globally masked using the IM_IRQ1 and IM_IRQ2 register bits. When not masked, the IRQ status can be read from IRQ1_STS and IRQ2_STS for the respective IRQ outputs.

The IRQ1 output is provided externally on the IRQ pin. Under default conditions, this output is ‘Active Low’. The polarity can be inverted using the IRQ_POL register. The IRQ output can be either CMOS driven or Open Drain; this is selected using the IRQ_OP_CFG register.

The IRQ2 status can be used to trigger DSP firmware execution - see “DSP Firmware Control”. This allows the DSP firmware execution to be linked to external events (e.g., GPIO input), or to any of the status conditions flagged by the Interrupt registers.

The IRQ1 and IRQ2 signals may be output on a GPIO pin - see “General Purpose Input / Output”.

The CS47L24 Interrupt Controller circuit is illustrated in Figure 46. (Note that not all interrupt inputs are shown.) The associated control fields are described in Table 64, Table 65 and Table 66.

Note that, under default register conditions, the ‘Boot Done’ status is the only un-masked interrupt source; a falling edge on the IRQ pin will indicate completion of the Boot Sequence.

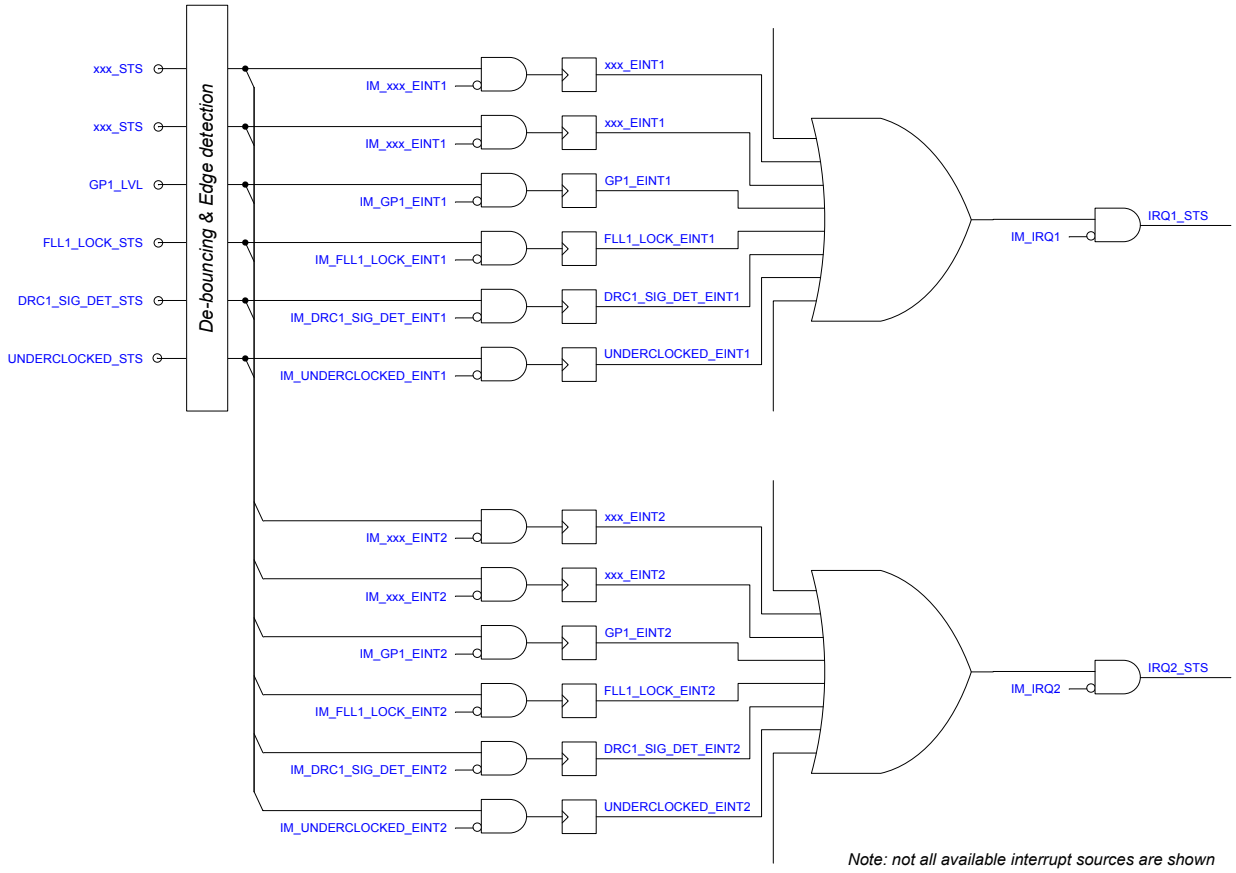


Figure 46 Interrupt Controller

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3087 (0C0Fh) IRQ CTRL 1	10	IRQ_POL	1	IRQ Output Polarity Select 0 = Non-inverted (Active High) 1 = Inverted (Active Low)
	9	IRQ_OP_CFG	0	IRQ Output Configuration 0 = CMOS 1 = Open Drain
R3328 (0D00h) Interrupt Status 1	1	GP2_EINT1	0	GPIO2 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	0	GP1_EINT1	0	GPIO1 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R3329 (0D01h) Interrupt Status 2	10	DSP3_RAM_RDY_EINT1	0	DSP3 RAM Ready Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	9	DSP2_RAM_RDY_EINT1	0	DSP2 RAM Ready Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	7	DSP_IRQ8_EINT1	0	DSP IRQ8 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	6	DSP_IRQ7_EINT1	0	DSP IRQ7 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	5	DSP_IRQ6_EINT1	0	DSP IRQ6 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	4	DSP_IRQ5_EINT1	0	DSP IRQ5 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	3	DSP_IRQ4_EINT1	0	DSP IRQ4 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	2	DSP_IRQ3_EINT1	0	DSP IRQ3 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	1	DSP_IRQ2_EINT1	0	DSP IRQ2 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	0	DSP_IRQ1_EINT1	0	DSP IRQ1 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R3330 (0D02h) Interrupt Status 3	15	SPK_OVERHEAT_WARN_EINT1	0	Speaker Overheat Warning Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	14	SPK_OVERHEAT_EINT1	0	Speaker Overheat Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	11	WSEQ_DONE_EINT1	0	Write Sequencer Done Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	10	DRC2_SIG_DET_EINT1	0	DRC2 Signal Detect Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	9	DRC1_SIG_DET_EINT1	0	DRC1 Signal Detect Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	8	ASRC2_LOCK_EINT1	0	ASRC2 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	7	ASRC1_LOCK_EINT1	0	ASRC1 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	6	UNDERCLOCKED_EINT1	0	Underclocked Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	OVERCLOCKED_EINT1	0	Overclocked Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	FLL2_LOCK_EINT1	0	FLL2 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	2	FLL1_LOCK_EINT1	0	FLL1 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	1	CLKGEN_ERR_EINT1	0	SYSCLK Underclocked Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	CLKGEN_ERR_ASYNC_EINT1	0	ASYNCCLK Underclocked Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3331 (0D03h) Interrupt Status 4	12	CTRLIF_ERR_EINT1	0	Control Interface Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	11	MIXER_DROPPED_SAMPLE_EINT1		Mixer Dropped Sample Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	10	ASYNC_CLK_ENA_LOW_EINT1	0	ASYNC_CLK_ENA Interrupt (Triggered on ASYNCCLK shut-down) Note: Cleared when a '1' is written.
	9	SYSCLK_ENA_LOW_EINT1	0	SYSCLK_ENA Interrupt (Triggered on SYSCLK shut-down) Note: Cleared when a '1' is written.
	8	ISRC1_CFG_ERR_EINT1	0	ISRC1 Configuration Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	7	ISRC2_CFG_ERR_EINT1	0	ISRC2 Configuration Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	6	ISRC3_CFG_ERR_EINT1	0	ISRC3 Configuration Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	HPR_ENABLE_DONE_EINT1	0	HPOUTR Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	HPL_ENABLE_DONE_EINT1	0	HPOUTL Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R3332 (0D04h) Interrupt Status 5	8	BOOT_DONE_EINT1	0	Boot Done Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	ASRC_CFG_ERR_EINT1	0	ASRC Configuration Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	FLL2_CLOCK_OK_EINT1	0	FLL2 Clock OK Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	0	FLL1_CLOCK_OK_EINT1	0	FLL1 Clock OK Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R3333 (0D05h) Interrupt Status 6	15	DSP_SHARED_WR_COLL_EINT1	0	DSP Shared Memory Collision Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	14	SPK_SHUTDOWN_EINT1	0	Speaker Shutdown Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	12	SPKOUTL_SHORT_EINT1	0	SPKOUT Short Circuit Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	2	HPR_SC_EINT1	0	HPOUTR Short Circuit Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	HPL_SC_EINT1	0	HPOUTL Short Circuit Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3336 (0D08h) to R3341 (0D0Dh)		IM_*	(see note)	For each *_EINT1 interrupt register in R3328 to R3333, a corresponding mask bit (IM_*) is provided in R3336 to R3341. The mask bits are coded as: 0 = Do not mask interrupt 1 = Mask interrupt
		Note : The BOOT_DONE_EINT1 interrupt is '0' (un-masked) by default; all other interrupts are '1' (masked) by default.		
R3343 (0D0Fh) Interrupt Control	0	IM_IRQ1	0	IRQ1 Output Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt.

Table 64 Interrupt 1 Control Registers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3344 (0D10h) IRQ2 Status 1	1	GP2_EINT2	0	GPIO2 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	0	GP1_EINT2	0	GPIO1 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R3345 (0D11h) IRQ2 Status 2	10	DSP3_RAM_RDY_EINT2	0	DSP3 RAM Ready Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	9	DSP2_RAM_RDY_EINT2	0	DSP2 RAM Ready Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	7	DSP_IRQ8_EINT2	0	DSP IRQ8 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	6	DSP_IRQ7_EINT2	0	DSP IRQ7 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	5	DSP_IRQ6_EINT2	0	DSP IRQ6 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	4	DSP_IRQ5_EINT2	0	DSP IRQ5 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	3	DSP_IRQ4_EINT2	0	DSP IRQ4 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	2	DSP_IRQ3_EINT2	0	DSP IRQ3 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	1	DSP_IRQ2_EINT2	0	DSP IRQ2 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	0	DSP_IRQ1_EINT2	0	DSP IRQ1 Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R3346 (0D12h) IRQ2	15	SPK_OVERHEAT_WARN_EINT2	0	Speaker Overheat Warning Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
Status 3	14	SPK_OVERHEAT_EINT2	0	Speaker Overheat Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	11	WSEQ_DONE_EINT2	0	Write Sequencer Done Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	10	DRC2_SIG_DET_EINT2	0	DRC2 Signal Detect Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	9	DRC1_SIG_DET_EINT2	0	DRC1 Signal Detect Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	8	ASRC2_LOCK_EINT2	0	ASRC2 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	7	ASRC1_LOCK_EINT2	0	ASRC1 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	6	UNDERCLOCKED_EINT2	0	Underclocked Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	5	OVERCLOCKED_EINT2	0	Overclocked Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	FLL2_LOCK_EINT2	0	FLL2 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	2	FLL1_LOCK_EINT2	0	FLL1 Lock Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	1	CLKGEN_ERR_EINT2	0	SYSCLK Underclocked Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	CLKGEN_ERR_ASYNC_EINT2	0	ASYNCCLK Underclocked Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R3347 (0D13h) IRQ2 Status 4	12	CTRLIF_ERR_EINT2	0	Control Interface Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	11	MIXER_DROPPED_SAMPLE_EINT2		Mixer Dropped Sample Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	10	ASYNC_CLK_ENA_LOW_EINT2	0	ASYNC_CLK_ENA Interrupt (Triggered on ASYNCCLK shut-down) Note: Cleared when a '1' is written.
	9	SYSCLK_ENA_LOW_EINT2	0	SYSCLK_ENA Interrupt (Triggered on SYSCLK shut-down) Note: Cleared when a '1' is written.
	8	ISRC1_CFG_ERR_EINT2	0	ISRC1 Configuration Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	7	ISRC2_CFG_ERR_EINT2	0	ISRC2 Configuration Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	6	ISRC3_CFG_ERR_EINT2	0	ISRC3 Configuration Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1	HPR_ENABLE_DONE_EINT2	0	HPOUTR Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	HPL_ENABLE_DONE_EINT2	0	HPOUTL Enable Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R3348 (0D14h) IRQ2 Status 5	8	BOOT_DONE_EINT2	0	Boot Done Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	3	ASRC_CFG_ERR_EINT2	0	ASRC Configuration Error Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	1	FLL2_CLOCK_OK_EINT2	0	FLL2 Clock OK Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	0	FLL1_CLOCK_OK_EINT2	0	FLL1 Clock OK Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
R3349 (0D15h) IRQ2 Status 6	15	DSP_SHARED_WR_COLL_EINT2	0	DSP Shared Memory Collision Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	14	SPK_SHUTDOWN_EINT2	0	Speaker Shutdown Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	12	SPKOUTL_SHORT_EINT2	0	SPKOUT Short Circuit Interrupt (Rising and falling edge triggered) Note: Cleared when a '1' is written.
	2	HPR_SC_EINT2	0	HPOUTR Short Circuit Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
	0	HPL_SC_EINT2	0	HPOUTL Short Circuit Interrupt (Rising edge triggered) Note: Cleared when a '1' is written.
R3352 (0D18h) to R3357 (0D1Dh)		IM_*	(see note)	For each *_EINT2 interrupt register in R3344 to R3349, a corresponding mask bit (IM_*) is provided in R3352 to R3357. The mask bits are coded as: 0 = Do not mask interrupt 1 = Mask interrupt
		Note : The BOOT_DONE_EINT2 interrupt is '0' (un-masked) by default; all other interrupts are '1' (masked) by default.		
R3359 (0D1Fh) IRQ2 Control	0	IM_IRQ2	0	IRQ2 Output Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt.

Table 65 Interrupt 2 Control Registers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3360 (0D20h) Interrupt Raw Status 1	10	DSP3_RAM_RDY_STS	0	DSP3 RAM Status 0 = Not ready 1 = Ready
	9	DSP2_RAM_RDY_STS	0	DSP2 RAM Status 0 = Not ready 1 = Ready

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7	DSP_IRQ8_STS	0	DSP IRQ8 Status 0 = Not asserted 1 = Asserted
	6	DSP_IRQ7_STS	0	DSP IRQ7 Status 0 = Not asserted 1 = Asserted
	5	DSP_IRQ6_STS	0	DSP IRQ6 Status 0 = Not asserted 1 = Asserted
	4	DSP_IRQ5_STS	0	DSP IRQ5 Status 0 = Not asserted 1 = Asserted
	3	DSP_IRQ4_STS	0	DSP IRQ4 Status 0 = Not asserted 1 = Asserted
	2	DSP_IRQ3_STS	0	DSP IRQ3 Status 0 = Not asserted 1 = Asserted
	1	DSP_IRQ2_STS	0	DSP IRQ2 Status 0 = Not asserted 1 = Asserted
	0	DSP_IRQ1_STS	0	DSP IRQ1 Status 0 = Not asserted 1 = Asserted
R3361 (0D21h) Interrupt Raw Status 2	15	SPK_OVERHEAT_WARN_STS	0	Speaker Overheat Warning Status 0 = Normal 1 = Warning temperature exceeded
	14	SPK_OVERHEAT_STS	0	Speaker Overheat Status 0 = Normal 1 = Shutdown temperature exceeded
	11	WSEQ_DONE_STS	0	Write Sequencer Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	10	DRC2_SIG_DET_STS	0	DRC2 Signal Detect Status 0 = Normal 1 = Signal detected
	9	DRC1_SIG_DET_STS	0	DRC1 Signal Detect Status 0 = Normal 1 = Signal detected
	8	ASRC2_LOCK_STS	0	ASRC2 Lock Status 0 = Not locked 1 = Locked
	7	ASRC1_LOCK_STS	0	ASRC1 Lock Status 0 = Not locked 1 = Locked
	6	UNDERCLOCKED_STS	0	Underclocked Error Status 0 = Normal 1 = Underclocked Error
	5	OVERCLOCKED_STS	0	Overclocked Error Status 0 = Normal 1 = Overclocked Error
	3	FLL2_LOCK_STS	0	FLL2 Lock Status 0 = Not locked 1 = Locked
	2	FLL1_LOCK_STS	0	FLL1 Lock Status 0 = Not locked 1 = Locked

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1	CLKGEN_ERR_STS	0	SYSCLK Underclocked Error Status 0 = Normal 1 = Underclocked Error
	0	CLKGEN_ERR_ASYNC_STS	0	ASYNCCLK Underclocked Error Status 0 = Normal 1 = Underclocked Error
R3362 (0D22h) Interrupt Raw Status 3	12	CTRLIF_ERR_STS	0	Control Interface Error Status 0 = Normal 1 = Control Interface Error
	11	MIXER_DROPPED_SAMPLE_STS		Mixer Dropped Sample Status 0 = Normal 1 = Dropped Sample Error
	10	ASYNC_CLK_ENA_LOW_STS	0	ASYNC_CLK_ENA Status 0 = ASYNC_CLK_ENA is enabled 1 = ASYNC_CLK_ENA is disabled When a '0' is written to ASYNCCLK_ENA, then no other control register writes should be attempted until ASYNC_CLK_ENA_LOW_STS=1.
	9	SYSCLK_ENA_LOW_STS	0	SYSCLK_ENA Status 0 = SYSCLK_ENA is enabled 1 = SYSCLK_ENA is disabled When a '0' is written to SYSCLK_ENA, then no other control register writes should be attempted until SYSCLK_ENA_LOW_STS=1.
	8	ISRC1_CFG_ERR_STS	0	ISRC1 Configuration Error Interrupt 0 = Normal 1 = Configuration Error
	7	ISRC2_CFG_ERR_STS	0	ISRC2 Configuration Error Interrupt 0 = Normal 1 = Configuration Error
	6	ISRC3_CFG_ERR_STS	0	ISRC3 Configuration Error Interrupt 0 = Normal 1 = Configuration Error
	1	HPR_ENABLE_DONE_STS	0	HPOUTR Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
	0	HPL_ENABLE_DONE_STS	0	HPOUTL Enable Status 0 = Busy (sequence in progress) 1 = Idle (sequence completed)
R3363 (0D23h) Interrupt Raw Status 4	8	BOOT_DONE_STS	0	Boot Status 0 = Busy (boot sequence in progress) 1 = Idle (boot sequence completed) Control register writes should not be attempted until Boot Sequence has completed.
	3	ASRC_CFG_ERR_STS	0	ASRC Configuration Error Interrupt 0 = Normal 1 = Configuration Error
	1	FLL2_CLOCK_OK_STS	0	FLL2 Clock OK Interrupt 0 = FLL2 Clock is not OK 1 = FLL2 Clock is OK
	0	FLL1_CLOCK_OK_STS	0	FLL1 Clock OK Interrupt 0 = FLL1 Clock is not OK 1 = FLL1 Clock is OK
R3364 (0D24h)	13	PWM_OVERCLOCKED_STS	0	Indicates an Overclocked Error condition for each respective sub-system.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
Interrupt Raw Status 5	12	FX_CORE_OVERCLOCKED_STS	0	The bits are coded as: 0 = Normal 1 = Overclocked The OVERCLOCKED_STS bit will be asserted whenever any of these register bits is asserted.
	10	DAC_SYS_OVERCLOCKED_STS	0	
	9	DAC_WARP_OVERCLOCKED_STS	0	
	7	MIXER_OVERCLOCKED_STS	0	
	6	AIF3_ASYNC_OVERCLOCKED_STS	0	
	5	AIF2_ASYNC_OVERCLOCKED_STS	0	
	4	AIF1_ASYNC_OVERCLOCKED_STS	0	
	3	AIF3_SYNC_OVERCLOCKED_STS	0	
	2	AIF2_SYNC_OVERCLOCKED_STS	0	
	1	AIF1_SYNC_OVERCLOCKED_STS	0	
	0	PAD_CTRL_OVERCLOCKED_STS	0	
R3365 (0D25h) Interrupt Raw Status 6	12	ASRC_ASYNC_SYS_OVERCLOCKED_STS	0	Indicates an Overclocked Error condition for each respective sub-system. The bits are coded as: 0 = Normal 1 = Overclocked The OVERCLOCKED_STS bit will be asserted whenever any of these register bits is asserted.
	11	ASRC_ASYNC_WARP_OVERCLOCKED_STS	0	
	10	ASRC_SYNC_SYS_OVERCLOCKED_STS	0	
	9	ASRC_SYNC_WARP_OVERCLOCKED_STS	0	
	7	DSP3_OVERCLOCKED_STS	0	
	5	DSP2_OVERCLOCKED_STS	0	
	2	ISRC3_OVERCLOCKED_STS	0	
	1	ISRC2_OVERCLOCKED_STS	0	
	0	ISRC1_OVERCLOCKED_STS	0	
R3366 (0D26h) Interrupt Raw Status 7	10	AIF3_UNDERCLOCKED_STS	0	Indicates an Underclocked Error condition for each respective sub-system. The bits are coded as: 0 = Normal 1 = Overclocked
	9	AIF2_UNDERCLOCKED_STS	0	
	8	AIF1_UNDERCLOCKED_STS	0	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7	ISRC3_UNDERCLOCKED_STS	0	The UNDERCLOCKED_STS bit will be asserted whenever any of these register bits is asserted.
	6	ISRC2_UNDERCLOCKED_STS	0	
	5	ISRC1_UNDERCLOCKED_STS	0	
	4	FX_UNDERCLOCKED_STS	0	
	3	ASRC_UNDERCLOCKED_STS	0	
	2	DAC_UNDERCLOCKED_STS	0	
	0	MIXER_UNDERCLOCKED_STS	0	
R3368 (0D28h) Interrupt Raw Status 8	14	SPK_SHUTDOWN_STS	0	Speaker Shutdown Status 0 = Normal 1 = Speaker Shutdown completed (due to Overheat Temperature or Short Circuit condition)
	12	SPKOUTL_SHORT_STS	0	SPKOUT Short Circuit Status 0 = Normal 1 = Short Circuit detected
	2	HPR_SC_STS	0	HPOUTR Short Circuit Status 0 = Normal 1 = Short Circuit detected
	0	HPL_SC_STS	0	HPOUTL Short Circuit Status 0 = Normal 1 = Short Circuit detected
R3392 (0D40h) Interrupt Pin Status	1	IRQ2_STS	0	IRQ2 Status IRQ2_STS is the logical 'OR' of all unmasked _EINT2 interrupts. 0 = Not asserted 1 = Asserted
	0	IRQ1_STS	0	IRQ1 Status IRQ1_STS is the logical 'OR' of all unmasked _EINT1 interrupts. 0 = Not asserted 1 = Asserted

Table 66 Interrupt Status

CLOCKING AND SAMPLE RATES

The CS47L24 requires a clock reference for its internal functions and also for the input (DMIC) paths, output (DAC) paths and digital audio interfaces. Under typical clocking configurations, all commonly-used audio sample rates can be derived directly from the external reference; for additional flexibility, the CS47L24 incorporates two Frequency Locked Loop (FLL) circuits to perform frequency conversion and filtering.

External clock signals may be connected via MCLK1 and MCLK2. In AIF Slave modes, the BCLK signals may be used as a reference for the system clocks. To avoid audible glitches, all clock configurations must be set up before enabling playback.

SYSTEM CLOCKING

The CS47L24 supports two independent clock domains, referenced to the SYSCLK and ASYNCCLK system clocks respectively.

Up to five different sample rates may be independently selected for specific audio interfaces and other input/output signal paths. Each selected sample rate must be synchronised either to SYSCLK or to ASYNCCLK, as described later.

The two system clocks are independent (i.e., not synchronised). Stereo full-duplex sample rate conversion is supported, allowing asynchronous audio data to be mixed and to be routed between independent interfaces. See “Digital Core” for further details.

Each subsystem within the CS47L24 digital core is clocked at a dynamically-controlled rate, limited by the SYSCLK (or ASYNCCLK) frequency, as applicable. For maximum signal mixing and processing capacity, it is recommended that the highest possible SYSCLK and ASYNCCLK frequencies are configured.

SAMPLE RATE CONTROL

The CS47L24 supports two independent clock domains, referenced to SYSCLK and ASYNCCLK respectively.

Different sample rates may be selected for each of the audio interfaces (AIF1, AIF2, AIF3), and for the input (DMIC) and output (DAC) paths. Each of these must be referenced either to SYSCLK or to ASYNCCLK.

The CS47L24 can support a maximum of five different sample rates at any time. The supported sample rates range from 8kHz to 192kHz.

Up to three different sample rates can be selected using the SAMPLE_RATE_1, SAMPLE_RATE_2 and SAMPLE_RATE_3 registers. These must each be numerically related to each other and to the SYSCLK frequency (further details of these requirements are provided in Table 67 and the accompanying text).

The remaining two sample rates can be selected using the ASYNC_SAMPLE_RATE_1 and ASYNC_SAMPLE_RATE_2 registers. These sample rates must be numerically related to each other and to the ASYNCCLK frequency (further details of these requirements are provided in Table 68 and the accompanying text),

Each of the audio interfaces, input paths and output paths is associated with one of the sample rates selected by the SAMPLE_RATE_n or ASYNC_SAMPLE_RATE_n registers.

Note that if any two interfaces are operating at the same sample rate, but are not synchronised, then one of these must be referenced to the ASYNCCLK domain, and the other to the SYSCLK domain.

Note that, when any of the SAMPLE_RATE_n or ASYNC_SAMPLE_RATE_n registers is written to, the activation of the new setting is automatically synchronised by the CS47L24 to ensure continuity of all active signal paths. The SAMPLE_RATE_n_STS and ASYNC_SAMPLE_RATE_n_STS registers provide readback of the sample rate selections that have been implemented.

There are some restrictions to be observed regarding the sample rate control configuration, as noted below:

- The input (Digital Microphone) and output (DAC) signal paths must always be associated with the SYSCLK clocking domain.
- All external clock references (MCLK input or Slave mode AIF input) must be within 1% of the applicable register setting(s).
- The input (Digital Microphone) sample rate is valid from 8kHz to 192kHz. If 768kHz DMIC clock rate is selected, then the supported sample rate is valid from 8kHz to 16kHz only.
- The Effects (EQ, DRC, LHPF) sample rate is valid from 8kHz to 192kHz. When the DRC is enabled, the maximum sample rate for these functions is 96kHz.
- The Asynchronous Sample Rate Converter (ASRC) supports sample rates 8kHz to 48kHz. The associated SYSCLK and ASYNCLK sample rates must both be 8kHz to 48kHz.
- The Isochronous Sample Rate Converters (ISRCs) support sample rates 8kHz to 192kHz. For each ISRC, the higher sample rate must be an integer multiple of the lower rate.

AUTOMATIC SAMPLE RATE DETECTION

The CS47L24 supports automatic sample rate detection on the digital audio interfaces (AIF1, AIF2 and AIF3). Note that this is only possible when the respective interface is operating in Slave mode (i.e., when LRCLK and BCLK are inputs to the CS47L24).

Automatic sample rate detection is enabled using the RATE_EST_ENA register bit. The LRCLK input pin selected for sample rate detection is set using the LRCLK_SRC register.

Up to four audio sample rates can be configured for automatic detection; these sample rates are selected using the SAMPLE_RATE_DETECT_n registers. Note that the function will only detect sample rates that match one of the SAMPLE_RATE_DETECT_n registers.

If one of the selected audio sample rates is detected on the selected LRCLK input, then a Control Write Sequence will be triggered. A unique sequence of actions may be programmed for each of the detected sample rates. Note that the applicable control sequences must be programmed by the user for each detection outcome. See “Control Write Sequencer” for further details.

The TRIG_ON_STARTUP register controls whether the sample rate detection circuit responds to the initial detection of the applicable interface (i.e., when the AIFn interface starts up).

When TRIG_ON_STARTUP=0, then the detection circuit will only respond (i.e., trigger the Control Write Sequencer) to a change in the detected sample rate - the initial sample rate detection will be ignored. (Note that the ‘initial sample rate detection’ is the first detection of a sample rate that matches one of the SAMPLE_RATE_DETECT_n registers.)

When TRIG_ON_STARTUP=1, then the detection circuit will trigger the Control Write Sequencer whenever a selected sample rate is detected, including when the AIF interface starts up, or when the sample rate detection is first enabled.

As described above, setting TRIG_ON_STARTUP=0 is designed to inhibit any response to the initial detection of a sample rate that matches one of the SAMPLE_RATE_DETECT_n registers. Note that, if the LRCLK_SRC setting is changed, or if the detection function is disabled and re-enabled, then a subsequent detection of a matching sample rate may trigger the Control Write Sequencer, regardless of the TRIG_ON_STARTUP setting.

There are some restrictions to be observed regarding the automatic sample rate detection, as noted below:

- The same sample rate must not be selected on more than one of the SAMPLE_RATE_DETECT_n registers.
- Sample rates 192kHz and 176.4kHz must not be selected concurrently.
- Sample rates 96kHz and 88.2kHz must not be selected concurrently.

The control registers associated with the automatic sample rate detection function are described in Table 69.

SYSCLK AND ASYNCCLK CONTROL

The SYSCLK and ASYNCCLK clocks may be provided directly from external inputs (MCLK, or slave mode BCLK inputs). Alternatively, the SYSCLK and ASYNCCLK clocks can be derived using the integrated FLL(s), with MCLK, BCLK or LRCLK as a reference.

The required SYSCLK frequency is dependent on the SAMPLE_RATE_n registers. Table 67 illustrates the valid SYSCLK frequencies for every supported sample rate.

The SYSCLK_FREQ and SYSCLK_FRAC registers are used to identify the applicable SYSCLK frequency. It is recommended that the highest possible SYSCLK frequency is selected.

The chosen SYSCLK frequency must be valid for all of the SAMPLE_RATE_n registers. It follows that all of the SAMPLE_RATE_n registers must select numerically-related values, i.e., all from the same cell as represented in Table 67.

Sample Rate	SAMPLE_RATE_n	SYSCLK Frequency	SYSCLK_FREQ	SYSCLK_FRAC
12kHz 24kHz 48kHz 96kHz 192kHz 8kHz 16kHz 32kHz	01h 02h 03h 04h 05h 11h 12h 13h	6.144MHz, 12.288MHz, 24.576MHz, 49.152MHz, 73.728MHz, 98.304MHz, or 147.456MHz	000, 001, 010, 011, 100, 101, or 110	0
11.025kHz 22.05kHz 44.1kHz 88.2kHz 176.4kHz	09h 0Ah 0Bh 0Ch 0Dh	5.6448MHz, 11.2896MHz, 22.5792MHz, 45.1584MHz, 67.7376MHz, 90.3168MHz, or 135.4752MHz	000, 001, 010, 011, 100, 101, or 110	1
Note that each of the SAMPLE_RATE_n registers must select a sample rate value from the same group in the two lists above.				

Table 67 SYSCLK Frequency Selection

The required ASYNCCLK frequency is dependent on the ASYNC_SAMPLE_RATE_n registers. Table 68 illustrates the valid ASYNCCLK frequencies for every supported sample rate.

The ASYNC_CLK_FREQ register is used to identify the applicable ASYNCCLK frequency. It is recommended that the highest possible ASYNCCLK frequency is selected.

Note that, if all the sample rates in the system are synchronised to SYSCLK, then the ASYNCCLK may not be required at all. In this case, the ASYNCCLK should be disabled (see Table 69), and the associated register values are not important.

Sample Rate	ASYNC_SAMPLE_RATE_n	ASYNCCLK Frequency	ASYNC_CLK_FREQ
12kHz 24kHz 48kHz 96kHz 192kHz 8kHz 16kHz 32kHz	01h 02h 03h 04h 05h 11h 12h 13h	6.144MHz, 12.288MHz, 24.576MHz, or 49.152MHz	000, 001, 010, or 011
11.025kHz 22.05kHz 44.1kHz 88.2kHz 176.4kHz	09h 0Ah 0Bh 0Ch 0Dh	5.6448MHz, 11.2896MHz, 22.5792MHz or 45.1584MHz	000, 001, 010, or 011
Note that each of the ASYNC_SAMPLE_RATE_n registers must select a sample rate value from the same group in the two lists above.			

Table 68 ASYNCCLK Frequency Selection

The CS47L24 supports automatic clocking configuration. The programmable dividers associated with the DMICs, DACs and DSP functions are configured automatically, with values determined from the SYSCLK_FREQ, SAMPLE_RATE_n, ASYNC_CLK_FREQ and ASYNC_SAMPLE_RATE_n fields.

Note that the digital audio interface (AIF) clocking rates must be configured separately.

The sample rates of each AIF, the input (DMIC) paths, output (DAC) paths and DSP functions are selected as described in the respective sections. Stereo full-duplex sample rate conversion is supported in multiple configurations to allow digital audio to be routed between interfaces and for asynchronous audio data to be mixed. See “Digital Core” for further details.

The SYSCLK_SRC register is used to select the SYSCLK source, as described in Table 69. The source may be MCLKn, AIFnBCLK or FLLn. If one of the Frequency Locked Loop (FLL) circuits is selected as the source, then the relevant FLL must be enabled and configured, as described later.

The SYSCLK_FREQ and SYSCLK_FRAC registers are set according to the frequency of the selected SYSCLK source.

The SYSCLK-referenced circuits within the digital core are clocked at a dynamically-controlled rate, limited by the SYSCLK frequency itself. For maximum signal mixing and processing capacity, it is recommended that the highest possible SYSCLK frequency is configured.

The SAMPLE_RATE_n registers are set according to the sample rate(s) that are required by one or more of the CS47L24 audio interfaces. The CS47L24 supports sample rates ranging from 4kHz to 192kHz.

The SYSCLK signal is enabled by the register bit SYSCLK_ENA. The applicable clock source (MCLKn, AIFnBCLK or FLLn) must be enabled before setting SYSCLK_ENA=1. This bit should be set to 0 when reconfiguring the clock sources (see below for additional requirements when setting SYSCLK_ENA=0).

When disabling SYSCLK, note that all of the input, output or digital core functions associated with the SYSCLK clock domain must be disabled before setting SYSCLK_ENA=0.

When ‘0’ is written to SYSCLK_ENA, the host processor must wait until the CS47L24 has shut down the associated functions before issuing any other register write commands. The SYSCLK Enable status can be polled via the SYSCLK_ENA_LOW_STS bit (see Table 66), or else monitored using the Interrupt or GPIO functions.

The SYSCLK Enable status is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see “Interrupts”. The corresponding Interrupt event indicates that the CS47L24 has shut down the SYSCLK functions and is ready to accept register write commands.

The SYSCLK Enable status can be output directly on a GPIO pin as an external indication of the SYSCLK status. See “General Purpose Input / Output” to configure a GPIO pin for this function.

The required control sequence for disabling SYSCLK is summarised below:

- Disable all SYSCLK-associated functions (inputs, outputs, digital core)
- Set SYSCLK_ENA = 0
- Wait until SYSCLK_ENA_LOW = 1 (or wait for the corresponding IRQ/GPIO event)

The ASYNC_CLK_SRC register is used to select the ASYNCCLK source, as described in Table 69. The source may be MCLKn, AIFnBCLK or FLLn. If one of the Frequency Locked Loop (FLL) circuits is selected as the source, then the relevant FLL must be enabled and configured, as described later.

The ASYNC_CLK_FREQ register is set according to the frequency of the selected ASYNCCLK source.

The ASYNCCLK-referenced circuits within the digital core are clocked at a dynamically-controlled rate, limited by the ASYNCCLK frequency itself. For maximum signal mixing and processing capacity, it is recommended that the highest possible ASYNCCLK frequency is configured.

The ASYNC_SAMPLE_RATE_n registers are set according to the sample rate(s) of any audio interface that is not synchronised to the SYSCLK clock domain.

The ASYNCCLK signal is enabled by the register bit ASYNC_CLK_ENA. The applicable clock source (MCLKn, AIFnBCLK or FLLn) must be enabled before setting ASYNC_CLK_ENA=1. This bit should be set to 0 when reconfiguring the clock sources (see below for additional requirements when setting ASYNC_CLK_ENA=0).

When disabling ASYNCCLK, note that all of the input, output or digital core functions associated with the ASYNCCLK clock domain must be disabled before setting ASYNC_CLK_ENA=0.

When ‘0’ is written to ASYNC_CLK_ENA, the host processor must wait until the CS47L24 has shut down the associated functions before issuing any other register write commands. The ASYNCCLK Enable status can be polled via the ASYNC_CLK_ENA_LOW_STS bit (see Table 66), or else monitored using the Interrupt or GPIO functions.

The ASYNCCLK Enable status is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see “Interrupts”. The corresponding Interrupt event indicates that the CS47L24 has shut down the ASYNCCLK functions and is ready to accept register write commands.

The ASYNCCLK Enable status can be output directly on a GPIO pin as an external indication of the ASYNCCLK status. See “General Purpose Input / Output” to configure a GPIO pin for this function.

The required control sequence for disabling ASYNCCLK is summarised below:

- Disable all ASYNCCLK-associated functions (inputs, outputs, digital core)
- Set ASYNCCLK_ENA = 0
- Wait until ASYNCCLK_ENA_LOW = 1 (or wait for the corresponding IRQ/GPIO event)

The SYSCLK (and ASYNCCLK, when applicable) clocks must be configured and enabled before any audio path is enabled.

The CS47L24 performs automatic checks to confirm that the SYSCLK and ASYNCCLK frequencies are high enough to support the commanded signal paths and processing functions. If an attempt is made to enable a signal path or processing function, and there are insufficient SYSCLK or ASYNCCLK cycles to support it, then the attempt will be unsuccessful. (Note that any signal paths that are already active will not be affected under these circumstances.)

An Underclocked Error condition is where there are insufficient clock cycles for the requested functionality, and increasing the SYSCLK or ASYNCCLK frequency (as applicable) should allow the selected configuration to be supported.

An Overclocked Error condition is where the requested functionality cannot be supported, as the clocking requirements of the requested configuration exceed the device limits.

The SYSCLK Underclocked condition, ASYNCCLK Underclocked condition, and other Clocking Error conditions can be monitored using the GPIO and/or Interrupt functions. See “General Purpose Input / Output” and “Interrupts” for further details.

MISCELLANEOUS CLOCK CONTROLS

The CS47L24 requires a 32kHz clock for miscellaneous de-bounce functions. This can be generated automatically from SYSCLK, or may be input directly as MCLK1 or MCLK2. The 32kHz clock source is selected using the CLK_32K_SRC register. The 32kHz clock is enabled using the CLK_32K_ENA register.

A clock output (OPCLK) derived from SYSCLK can be output on a GPIO pin. See “General Purpose Input / Output” to configure a GPIO pin for this function.

A clock output (OPCLK_ASYNC) derived from ASYNCCLK can be output on a GPIO pin. See “General Purpose Input / Output” to configure a GPIO pin for this function.

The CS47L24 provides integrated pull-down resistors on the MCLK1 and MCLK2 pins. This provides a flexible capability for interfacing with other devices.

The clocking scheme for the CS47L24 is illustrated in Figure 47.

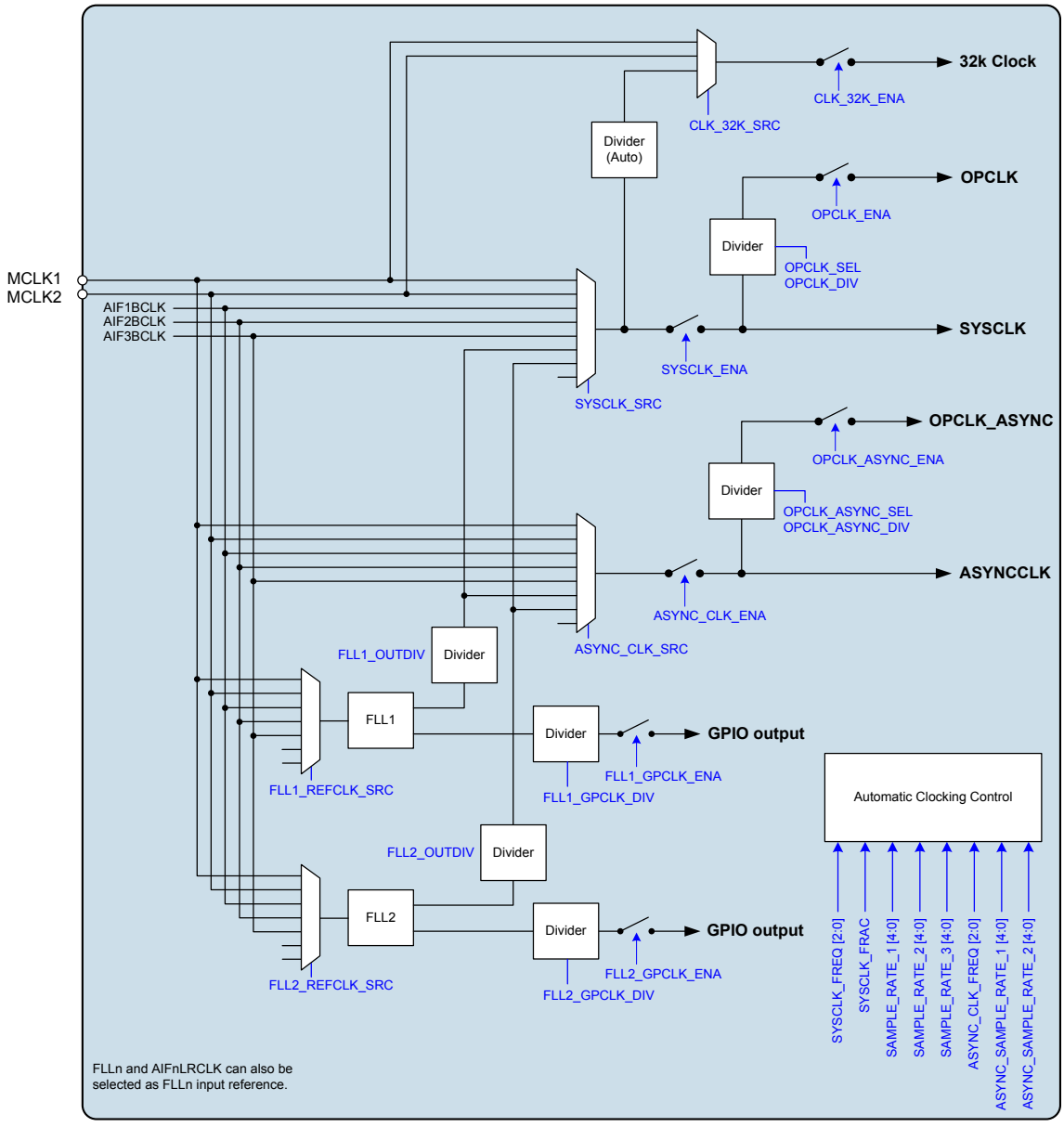


Figure 47 System Clocking

The CS47L24 clocking control registers are described in Table 69.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R256 (0100h) Clock 32k 1	6	CLK_32K_ENA	0	32kHz Clock Enable 0 = Disabled 1 = Enabled
	1:0	CLK_32K_SRC [1:0]	10	32kHz Clock Source 00 = MCLK1 (direct) 01 = MCLK2 (direct) 10 = SYSCLK (automatically divided) 11 = Reserved
R257 (0101h) System Clock 1	15	SYSCLK_FRAC	0	SYSCLK Frequency 0 = SYSCLK is a multiple of 6.144MHz 1 = SYSCLK is a multiple of 5.6448MHz
	10:8	SYSCLK_FREQ [2:0]	101	SYSCLK Frequency 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) 100 = 73.728MHz (67.7376MHz) 101 = 98.304MHz (90.3168MHz) 110 = 147.456MHz (135.4752MHz) 111 = Reserved The frequencies in brackets apply for 44.1kHz-related sample rates only (i.e., SAMPLE_RATE_n = 01XXX).
	6	SYSCLK_ENA	0	SYSCLK Control 0 = Disabled 1 = Enabled SYSCLK should only be enabled after the applicable clock source has been configured and enabled. Set this bit to 0 when reconfiguring the clock sources.
	3:0	SYSCLK_SRC [3:0]	0100	SYSCLK Source 0000 = MCLK1 0001 = MCLK2 0100 = FLL1 0101 = FLL2 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK All other codes are Reserved
R258 (0102h) Sample rate 1	4:0	SAMPLE_RATE_1 [4:0]	10001	Sample Rate 1 Select 00h = None 01h = 12kHz 02h = 24kHz 03h = 48kHz 04h = 96kHz 05h = 192kHz 09h = 11.025kHz 0Ah = 22.05kHz 0Bh = 44.1kHz 0Ch = 88.2kHz 0Dh = 176.4kHz 10h = 4kHz 11h = 8kHz 12h = 16kHz 13h = 32kHz All other codes are Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R259 (0103h) Sample rate 2	4:0	SAMPLE_RATE_2 [4:0]	10001	Sample Rate 2 Select *Register coding is same as SAMPLE_RATE_1.*
R260 (0104h) Sample rate 3	4:0	SAMPLE_RATE_3 [4:0]	10001	Sample Rate 3 Select *Register coding is same as SAMPLE_RATE_1.*
R266 (010Ah) Sample rate 1 status	4:0	SAMPLE_RATE_1_STS [4:0]	00000	Sample Rate 1 Status (Read only) *Register coding is same as SAMPLE_RATE_1.*
R267 (010Bh) Sample rate 2 status	4:0	SAMPLE_RATE_2_STS [4:0]	00000	Sample Rate 2 Status (Read only) *Register coding is same as SAMPLE_RATE_1.*
R268 (010Ch) Sample rate 3 status	4:0	SAMPLE_RATE_3_STS [4:0]	00000	Sample Rate 3 Status (Read only) *Register coding is same as SAMPLE_RATE_1.*
R274 (0112h) Async clock 1	10:8	ASYNC_CLK_FREQ [2:0]	011	ASYNCCLK Frequency 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) All other codes are Reserved The frequencies in brackets apply for 44.1kHz-related sample rates only (i.e., ASYNC_SAMPLE_RATE_n = 01XXX).
	6	ASYNC_CLK_ENA	0	ASYNCCLK Control 0 = Disabled 1 = Enabled ASYNCCLK should only be enabled after the applicable clock source has been configured and enabled. Set this bit to 0 when reconfiguring the clock sources.
	3:0	ASYNC_CLK_SRC [3:0]	0101	ASYNCCLK Source 0000 = MCLK1 0001 = MCLK2 0100 = FLL1 0101 = FLL2 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK 1011 to 1111 = Reserved All other codes are Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R275 (0113h) Async sample rate 1	4:0	ASYNC_SAMPLE_RATE_1 [4:0]	10001	ASYNC Sample Rate 1 Select 00h = None 01h = 12kHz 02h = 24kHz 03h = 48kHz 04h = 96kHz 05h = 192kHz 09h = 11.025kHz 0Ah = 22.05kHz 0Bh = 44.1kHz 0Ch = 88.2kHz 0Dh = 176.4kHz 10h = 4kHz 11h = 8kHz 12h = 16kHz 13h = 32kHz All other codes are Reserved
R276 (0114h) Async sample rate 2	4:0	ASYNC_SAMPLE_RATE_2 [4:0]	10001	ASYNC Sample Rate 2 Select *Register coding is same as ASYNC_SAMPLE_RATE_1.*
R283 (011Bh) Async sample rate 1 status	4:0	ASYNC_SAMPLE_RATE_1_STS [4:0]	00000	ASYNC Sample Rate 1 Status (Read only) *Register coding is same as ASYNC_SAMPLE_RATE_1.*
R284 (011Ch) Async sample rate 2 status	4:0	ASYNC_SAMPLE_RATE_2_STS [4:0]	00000	ASYNC Sample Rate 2 Status (Read only) *Register coding is same as ASYNC_SAMPLE_RATE_1.*
R329 (0149h) Output system clock	15	OPCLK_ENA	0	OPCLK Enable 0 = Disabled 1 = Enabled
	7:3	OPCLK_DIV [4:0]	00h	OPCLK Divider 00h = Divide by 1 01h = Divide by 1 02h = Divide by 2 03h = Divide by 3 … 1Fh = Divide by 31
	2:0	OPCLK_SEL [2:0]	000	OPCLK Source Frequency 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) All other codes are Reserved The frequencies in brackets apply for 44.1kHz-related SYSCLK rates only (i.e., SAMPLE_RATE_n = 01XXX). The OPCLK Source Frequency must be less than or equal to the SYSCLK frequency.
R330 (014Ah) Output	15	OPCLK_ASYNC_ENA	0	OPCLK_ASYNC Enable 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
async clock	7:3	OPCLK_ASYNC_DIV [4:0]	00h	OPCLK_ASYNC Divider 00h = Divide by 1 01h = Divide by 1 02h = Divide by 2 03h = Divide by 3 … 1Fh = Divide by 31
	2:0	OPCLK_ASYNC_SEL [2:0]	000	OPCLK_ASYNC Source Frequency 000 = 6.144MHz (5.6448MHz) 001 = 12.288MHz (11.2896MHz) 010 = 24.576MHz (22.5792MHz) 011 = 49.152MHz (45.1584MHz) All other codes are Reserved The frequencies in brackets apply for 44.1kHz-related ASYNCCLK rates only (i.e., ASYNC_SAMPLE_RATE_n = 01XXX). The OPCLK_ASYNC Source Frequency must be less than or equal to the ASYNCCLK frequency.
R338 (0152h) Rate Estimator 1	4	TRIG_ON_STARTUP	0	Automatic Sample Rate Detection Start-Up select 0 = Do not trigger Write Sequence on initial detection 1 = Always trigger the Write Sequencer on sample rate detection
	3:1	LRCLK_SRC [2:0]	000	Automatic Sample Rate Detection source 000 = AIF1LRCLK 010 = AIF2LRCLK 100 = AIF3LRCLK All other codes are Reserved
	0	RATE_EST_ENA	0	Automatic Sample Rate Detection control 0 = Disabled 1 = Enabled
R339 (0153h) Rate Estimator 2	4:0	SAMPLE_RATE_DETECT_A [4:0]	00h	Automatic Detection Sample Rate A (Up to four different sample rates can be configured for automatic detection.) *Register coding is same as SAMPLE_RATE_n.*
R340 (0154h) Rate Estimator 3	4:0	SAMPLE_RATE_DETECT_B [4:0]	00h	Automatic Detection Sample Rate B (Up to four different sample rates can be configured for automatic detection.) *Register coding is same as SAMPLE_RATE_n.*
R341 (0155h) Rate Estimator 4	4:0	SAMPLE_RATE_DETECT_C [4:0]	00h	Automatic Detection Sample Rate C (Up to four different sample rates can be configured for automatic detection.) *Register coding is same as SAMPLE_RATE_n.*
R342 (0156h) Rate Estimator 5	4:0	SAMPLE_RATE_DETECT_D [4:0]	00h	Automatic Detection Sample Rate D (Up to four different sample rates can be configured for automatic detection.) *Register coding is same as SAMPLE_RATE_n.*
R3104 (0C20h) Misc Pad Ctrl 1	13	MCLK2_PD	0	MCLK2 Pull-Down Control 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3105 (0C21h) Misc Pad Ctrl 2	12	MCLK1_PD	0	MCLK1 Pull-Down Control 0 = Disabled 1 = Enabled

Table 69 Clocking Control

In AIF Slave modes, it is important to ensure the applicable clock domain (SYSCLK or ASYNCCLK) is synchronised with the associated external LRCLK. This can be achieved by selecting an MCLK input that is derived from the same reference as the LRCLK, or can be achieved by selecting the external BCLK or LRCLK signal as a reference input to one of the FLLs, as a source for SYSCLK or ASYNCCLK.

If the AIF clock domain is not synchronised with the LRCLK, then clicks arising from dropped or repeated audio samples will occur, due to the inherent tolerances of multiple, asynchronous, system clocks. See “Applications Information” for further details on valid clocking configurations.

BCLK AND LRCLK CONTROL

The digital audio interfaces (AIF1, AIF2 and AIF3) use BCLK and LRCLK signals for synchronisation. In master mode, these are output signals, generated by the CS47L24. In slave mode, these are input signals to the CS47L24. It is also possible to support mixed master/slave operation.

The BCLK and LRCLK signals are controlled as illustrated in Figure 48. See the “Digital Audio Interface Control” section for further details of the relevant control registers.

Note that the BCLK and LRCLK signals are synchronised to SYSCLK or ASYNCLK, depending upon the applicable clocking domain for the respective interface. See “Digital Core” for further details.

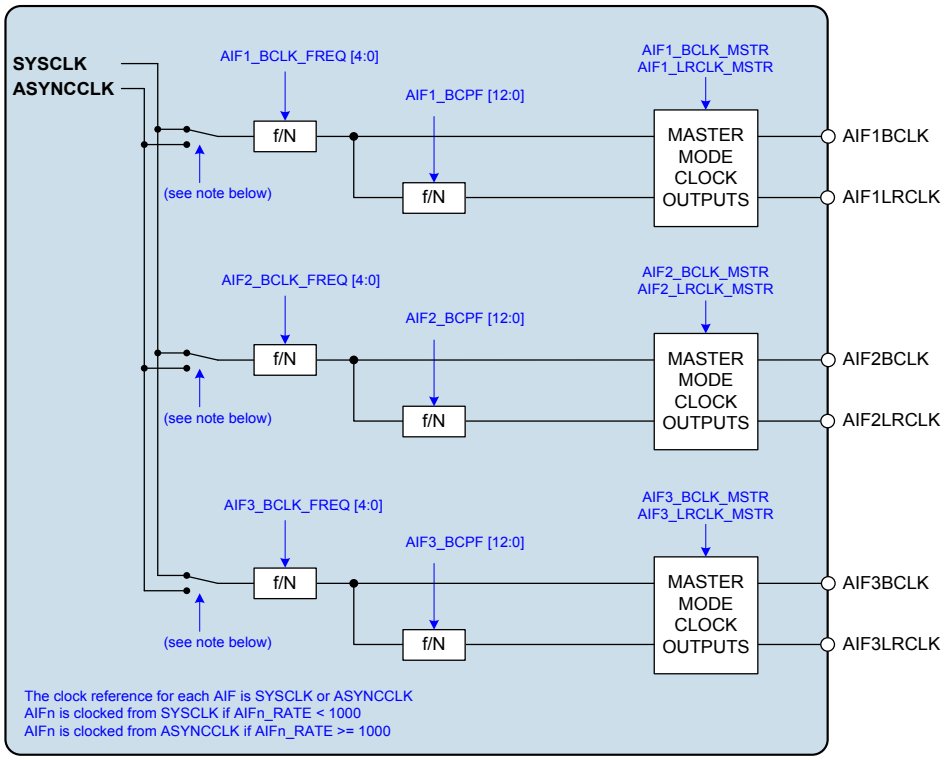


Figure 48 BCLK and LRCLK Control

CONTROL INTERFACE CLOCKING

Register map access is possible with or without a system clock. Clocking is provided from SYSCLK, when available; the SYSCLK_SRC register selects the applicable SYSCLK source.

See “Control Interface” for further details of control register access.

FREQUENCY LOCKED LOOP (FLL)

Two integrated FLLs are provided to support the clocking requirements of the CS47L24. These can be enabled and configured independently according to the available reference clocks and the application requirements. The reference clock may be a high frequency (e.g., 12.288MHz) or low frequency (e.g., 32.768kHz).

The FLL is tolerant of jitter and may be used to generate a stable output clock from a less stable input reference. The FLL characteristics are summarised in “Electrical Characteristics”. Note that the FLL can be used to generate a free-running clock in the absence of an external reference source. This is described in the “Free-Running FLL Mode” section below. Configurable spread-spectrum modulation can be applied to the FLL outputs, to control EMI effects.

Each of the FLLs comprises two sub-systems - the ‘main’ loop and the ‘synchroniser’ loop; these can be used together to maintain best frequency accuracy and noise (jitter) performance across multiple use-cases. The two-loop design enables the FLL to synchronise effectively to an input clock that may be intermittent or noisy, whilst also achieving the performance benefits of a stable clock reference that may be asynchronous to the audio data.

The main loop takes a constant and stable clock reference as its input. For best performance, a high frequency (e.g., 12.288MHz) reference is recommended. The main FLL loop will free-run without any clock reference if the input signal is removed; it can also be configured to initiate an output in the absence of any reference signal.

The synchroniser loop takes a separate clock reference as its input. The synchroniser input may be intermittent (e.g., during voice calls only). The FLL uses the synchroniser input, when available, as the frequency reference. To achieve the designed performance advantage, the synchroniser input must be synchronous with the audio data.

Note that, if only a single clock input reference is used, this must be configured as the main FLL input reference. The synchroniser should be disabled in this case.

The synchroniser loop should only be used when the main loop clock reference is present. If the input reference to the main FLL is intermittent, or may be interrupted unexpectedly, then the synchroniser should be disabled.

The FLL is enabled using the FLL*n*_ENA register bit (where *n* = 1 or 2 for the corresponding FLL). The FLL Synchroniser is enabled using the FLL*n*_SYNC_ENA register bit.

Note that the other FLL registers should be configured before enabling the FLL; the FLL*n*_ENA bit should be set as the final step of the FLL*n* enable sequence.

The FLL_SYNC_ENA bit should not be changed if FLL*n*_ENA = 1; the FLLn_ENA bit should be cleared before changing FLL*n*_SYNC_ENA.

The FLL supports configurable free-running operation, using the FLL*n*_FREERUN register bits described in the next section. Note that, once the FLL output has been established, the FLL will always free-run when the input reference clock is stopped, regardless of the FLL*n*_FREERUN bits.

To disable the FLL while the input reference clock has stopped, the respective FLL*n*_FREERUN bit must be set to ‘1’, before setting the FLL*n*_ENA bit to ‘0’.

When changing any of the FLL configuration fields, it is recommended that the digital circuit be disabled via FLL*n*_ENA and then re-enabled after the other register settings have been updated. If the FLL configuration is changed while the FLL is enabled, the respective FLL*n*_FREERUN bit should be set before updating any other FLL fields. A minimum delay of 32µs should be allowed between setting FLL*n*_FREERUN and writing to the required FLL register fields. The FLL*n*_FREERUN bit should remain set until after the FLL has been reconfigured.

Note that, if the FLL*n*_N or FLL*n*_THETA fields are changed while the FLL is enabled, the FLL*n*_CTRL_UPD bit must also be written, as described below. As a general rule, however, it is recommended to configure the FLL (and FLL Synchroniser, if applicable), before setting the corresponding _ENA register bit(s).

The FLL configuration requirements are illustrated in Figure 49.

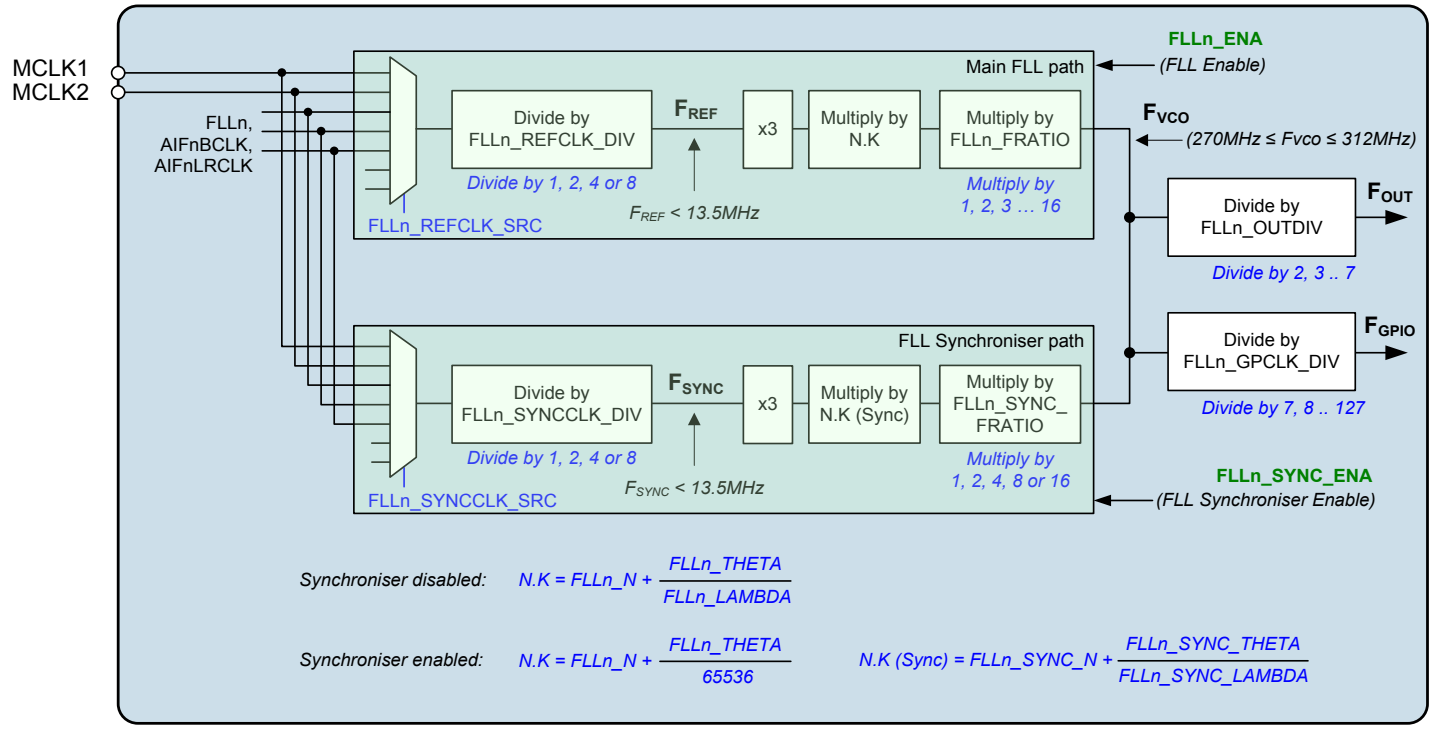


Figure 49 FLL Configuration

The procedure for configuring the FLL is described below. Note that the configuration of the main FLL path and the FLL Synchroniser path are very similar. One or both paths must be configured, depending on the application requirements:

- If a single clock input reference is used, then only the main FLL path should be used.
- If the input reference to the main FLL is intermittent, or may be interrupted unexpectedly, then only the main FLL path should be used.
- If two clock input references are used, then the constant or low-noise clock is configured on the main FLL path, and the high-accuracy clock is configured on the FLL synchroniser path. Note that the synchroniser input must be synchronous with the audio data.

The following description is applicable to FLL1 and FLL2. The associated register control fields are described in Table 74 and Table 75 respectively.

The main input reference is selected using FLLn_REFCLK_SRC. The synchroniser input reference is selected using FLLn_SYNCCLK_SRC. The available options in each case comprise MCLK1, MCLK2, AIFnBCLK, AIFnLRCLK, or the output from another FLL.

The FLL*n*_REFCLK_DIV field controls a programmable divider on the main input reference. The FLL*n*_SYNCCLK_DIV field controls a programmable divider on the synchroniser input reference. Each input can be divided by 1, 2, 4 or 8. These registers should be set to bring each reference down to 13.5MHz or below. For best performance, it is recommended that the highest possible frequency - within the 13.5MHz limit - should be selected. (Note that additional guidelines also apply, as described below.)

The FLL output frequency, relative to the main input reference F_{REF}, is directly determined from FLL*n*_FRATIO, FLL*n*_OUTDIV and the real number represented by N.K.

The integer value, N, is held in the FLL*n*_N register field. The fractional portion, K, is determined by the FLL*n*_THETA and FLL*n*_LAMBDA fields.

The FLL output frequency is generated according to the following equation:

$F_{OUT} = (F_{VCO} / FLLn\_OUTDIV)$

The FLL operating frequency, F_{VCO} is set according to the following equation:

$F_{VCO} = (F_{REF} \times 3 \times N.K \times FLLn\_FRATIO)$

F_{REF} is the input frequency, as determined by FLL*n*_REFCLK_DIV.

When the FLL output is selected as the SYSCLK or ASYNCCLK source, then F_{VCO} must be exactly 294.912MHz (for 48kHz-related sample rates) or 270.9504MHz (for 44.1kHz-related sample rates).

Note that the output frequencies that do not lie on or between the frequencies quoted above cannot be guaranteed across the full range of device operating conditions.

In order to follow the above requirements for F_{VCO}, the value of FLL*n*_OUTDIV should be selected according to the desired output F_{OUT}. The divider, FLL*n*_OUTDIV, must be set so that F_{VCO} is in the range 270MHz to 295MHz. The available divisions are integers from 2 to 7. Some typical settings of FLL*n*_OUTDIV are noted in Table 70.

OUTPUT FREQUENCY F_{OUT}	FLL*n*_OUTDIV
45 MHz to 52 MHz	110 (divide by 6)
67.5 MHz to 78 MHz	100 (divide by 4)
90 MHz to 104 MHz	011 (divide by 3)
135 MHz to 150 MHz	010 (divide by 2)

Table 70 Selection of FLL*n*_OUTDIV

The FLL*n*_FRATIO field selects the frequency division ratio of the FLL input. The FLL*n*_GAIN field is used to optimise the FLL, according to the input frequency. As a general guide, these fields should be selected as described in Table 71. (Note that additional guidelines also apply, as described below.)

REFERENCE FREQUENCY F_{REF}	FLL*n*_FRATIO	FLL*n*_GAIN
1MHz - 13.5MHz	0h (divide by 1)	4h (16x gain)
256kHz - 1MHz	1h (divide by 2)	2h (4x gain)
128kHz - 256kHz	3h (divide by 4)	0h (1x gain)
64kHz - 128kHz	7h (divide by 8)	0h (1x gain)
Less than 64kHz	Fh (divide by 16)	0h (1x gain)

Table 71 Selection of FLL*n*_FRATIO and FLL*n*_GAIN

In order to determine the remaining FLL parameters, the FLL operating frequency, F_{VCO}, must be calculated, as given by the following equation:

$F_{VCO} = (F_{OUT} \times FLLn\_OUTDIV)$

The value of N.K can then be determined as follows:

$N.K = F_{VCO} / (FLLn\_FRATIO \times 3 \times F_{REF})$

Note that, in the above equations:

FLL*n*_OUTDIV is the F_{OUT} clock ratio.

F_{REF} is the input frequency, after division by FLL*n*_REFCLK_DIV, where applicable.

FLL*n*_FRATIO is the F_{VCO} clock ratio (1, 2, 3 … 16).

If the above equations produce an integer value for N.K, then the value of FLL*n*_FRATIO should be adjusted to a different, odd-number division (e.g., divide by 3), and the value of N.K re-calculated. A non-integer value of N.K is recommended for best performance of the FLL. (If possible, the FLL*n*_FRATIO value should be decreased to the nearest alternative odd-number division. If a suitable lower value does not exist, FLL*n*_FRATIO should be increased to the nearest odd-number division instead.)

After the value of FLL*n*_FRATIO has been determined, the input frequency, F_{REF}, must be compared with the maximum frequency limit noted in Table 72. If the input frequency (after division by FLL*n*_REFCLK_DIV) is higher than the applicable limit, then the FLL*n*_REFCLK_DIV division ratio should be increased, and the value of N.K re-calculated. (Note that the same value of FLL*n*_FRATIO as already calculated should be used, when deriving the new value of N.K.)

FLL*n*_FRATIO	REFERENCE FREQUENCY F_{REF} - MAXIMUM VALUE
0h (divide by 1)	13.5 MHz
1h (divide by 2)	6.144 MHz
2h (divide by 3)	
3h (divide by 4)	3.072 MHz
4h (divide by 5)	
5h (divide by 6)	2.8224 MHz
6h (divide by 7)	
7h (divide by 8)	1.536 MHz
8h (divide by 9)	
9h (divide by 10)	
Ah (divide by 11)	
Bh (divide by 12)	
Ch (divide by 13)	
Dh (divide by 14)	
Eh (divide by 15)	
Fh (divide by 16)	768 kHz

Table 72 Maximum FLL input frequency (function of FLLn_FRATIO)

The value of N is held in the FLL*n*_N register field.

The value of K is determined by the FLL*n*_THETA and FLL*n*_LAMBDA fields, as described later.

The FLL*n*_N, FLL*n*_THETA and FLL*n*_LAMBDA fields are all coded as integers (LSB = 1).

If the FLL*n*_N or FLL*n*_THETA registers are updated while the FLL is enabled (FLL*n*_ENA=1), then the new values will only be effective when a '1' is written to the FLL*n*_CTRL_UPD bit. This makes it possible to update the two registers simultaneously, without disabling the FLL.

Note that, when the FLL is disabled (FLL*n*_ENA=0), then the FLL*n*_N and FLL*n*_THETA registers can be updated without writing to the FLL*n*_CTRL_UPD bit.

The values of FLL*n*_THETA and FLL*n*_LAMBDA can be calculated as described later.

A similar procedure applies for the deriviation of the FLL Synchroniser parameters - assuming that this function is used.

The FLL*n*_SYNC_FRATIO field selects the frequency division ratio of the FLL synchroniser input. The FLL*n*_GAIN and FLL*n*_SYNC_DFSAT fields are used to optimise the FLL, according to the input frequency. These fields should be set as described in Table 73.

Note that the FLL*n*_SYNC_FRATIO register coding is not the same as the FLL*n*_FRATIO register.

SYNCHRONISER FREQUENCY F_{SYNC}	FLL*n*_SYNC_FRATIO	FLLn_SYNC_GAIN	FLLn_SYNC_DFSAT
1MHz - 13.5MHz	0h (divide by 1)	4h (16x gain)	0 (wide bandwidth)
256kHz - 1MHz	1h (divide by 2)	2h (4x gain)	0 (wide bandwidth)
128kHz - 256kHz	2h (divide by 4)	0h (1x gain)	0 (wide bandwidth)
64kHz - 128kHz	3h (divide by 8)	0h (1x gain)	1 (narrow bandwidth)
Less than 64kHz	4h (divide by 16)	0h (1x gain)	1 (narrow bandwidth)

Table 73 Selection of FLL*n*_SYNC_FRATIO, FLL*n*_SYNC_GAIN, FLL*n*_SYNC_DFSAT

The FLL operating frequency, F_{VCO}, is the same frequency calculated as described above.

The value of N.K (Sync) can then be determined as follows:

N.K (Sync) = F_{VCO} / (FLL*n*_SYNC_FRATIO x 3 x F_{SYNC})

Note that, in the above equations:

F_{SYNC} is the synchroniser input frequency, after division by FLL*n*_SYNCCLK_DIV, where applicable.

FLL*n*_SYNC_FRATIO is the F_{VCO} clock ratio (1, 2, 4, 8 or 16).

The value of N (Sync) is held in the FLL*n*_SYNC_N register field.

The value of K (Sync) is determined by the FLL*n*_SYNC_THETA and FLL*n*_SYNC_LAMBDA fields.

The FLL*n*_SYNC_N, FLL*n*_SYNC_THETA and FLL*n*_SYNC_LAMBDA fields are all coded as integers (LSB = 1).

In Fractional Mode, with the synchroniser disabled (K > 0, and FLL*n*_SYNC_ENA = 0), the register fields FLL*n*_THETA and FLL*n*_LAMBDA can be calculated as described below.

The equivalent procedure is also used to derive the FLL*n*_SYNC_THETA and FLL*n*_SYNC_LAMBDA register values from the corresponding synchroniser parameters. (This is only required if the synchroniser is enabled.)

Calculate GCD(FLL) using the 'Greatest Common Denominator' function:

GCD(FLL) = GCD(FLL*n*_FRATIO x F_{REF}, F_{VCO} / 3)

where GCD(x, y) is the greatest common denominator of x and y

F_{REF} is the input frequency, after division by FLL*n*_REFCLK_DIV, where applicable.

Next, calculate FLL*n*_THETA and FLL*n*_LAMBDA using the following equations:

FLL*n*_THETA = ((F_{VCO} / 3) - (FLL_N x FLL*n*_FRATIO x F_{REF})) / GCD(FLL)

FLL*n*_LAMBDA = (FLL*n*_FRATIO x F_{REF}) / GCD(FLL)

Note that, in the operating conditions described above, the values of FLL*n*_THETA and FLL*n*_LAMBDA must be co-prime (i.e., not divisible by any common integer). The calculation above ensures that the values will be co-prime. The value of K must be a fraction less than 1 (i.e., FLL*n*_THETA must be less than FLL*n*_LAMBDA).

In Fractional Mode, with the synchroniser enabled (K > 0, and FLLn_SYNC_ENA = 1), the value of FLL*n*_THETA is calculated as described below. The value of FLLn_LAMBDA is ignored in this case.

FLLn_THETA = K x 65536

The FLL control registers are described in Table 74 and Table 75. Example settings for a variety of reference frequencies and output frequencies are shown in Table 78.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R369 (0171h) FLL1 Control 1	0	FLL1_ENA	0	FLL1 Enable 0 = Disabled 1 = Enabled This should be set as the final step of the FLL1 enable sequence, i.e., after the other FLL registers have been configured.
R370 (0172h) FLL1 Control 2	15	FLL1_CTRL_UPD	0	FLL1 Control Update Write '1' to apply the FLL1_N and FLL1_THETA register settings. (Only valid when FLL1_ENA=1)
	9:0	FLL1_N [9:0]	008h	FLL1 Integer multiply for F_{REF} (LSB = 1) If updated while the FLL is enabled, the new value is only effective when a '1' is written to FLL1_CTRL_UPD.
R371 (0173h) FLL1 Control 3	15:0	FLL1_THETA [15:0]	0018h	FLL1 Fractional multiply for F_{REF} This field sets the numerator (multiply) part of the FLL1_THETA / FLL1_LAMBDA ratio. Coded as LSB = 1. If updated while the FLL is enabled, the new value is only effective when a '1' is written to FLL1_CTRL_UPD.
R372 (0174h) FLL1 Control 4	15:0	FLL1_LAMBDA [15:0]	007Dh	FLL1 Fractional multiply for F_{REF} This field sets the denominator (dividing) part of the FLL1_THETA / FLL1_LAMBDA ratio. Coded as LSB = 1.
R373 (0175h) FLL1 Control 5	11:8	FLL1_FRATIO [3:0]	0h	FLL1 F_{VCO} clock divider 0h = 1 1h = 2 2h = 3 3h = 4 … Fh = 16
	3:1	FLL1_OUTDIV [2:0]	011	FLL1 F_{OUT} clock divider 000 = Reserved 001 = Reserved 010 = Divide by 2 011 = Divide by 3 100 = Divide by 4 101 = Divide by 5 110 = Divide by 6 111 = Divide by 7 (F_{OUT} = F_{VCO} / FLL1_OUTDIV)
R374 (0176h) FLL1 Control 6	7:6	FLL1_REFCLK_DIV [1:0]	00	FLL1 Clock Reference Divider 00 = 1 01 = 2 10 = 4 11 = 8 MCLK (or other input reference) must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:0	FLL1_REFCLK_SRC	0000	FLL1 Clock source 0000 = MCLK1 0001 = MCLK2 0100 = FLL1 0101 = FLL2 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK 1100 = AIF1LRCLK 1101 = AIF2LRCLK 1110 = AIF3LRCLK All other codes are Reserved
R377 (0179h) FLL1 Control 7	5:2	FLL1_GAIN [3:0]	0000	FLL1 Gain 0000 = 1 0001 = 2 0010 = 4 0011 = 8 0100 = 16 0101 = 32 0110 = 64 0111 = 128 1000 to 1111 = 256
R385 (0181h) FLL1 Synchroniser 1	0	FLL1_SYNC_ENA	0	FLL1 Synchroniser Enable 0 = Disabled 1 = Enabled This should be set as the final step of the FLL1 synchroniser enable sequence, i.e., after the other synchroniser registers have been configured.
R386 (0182h) FLL1 Synchroniser 2	9:0	FLL1_SYNC_N [9:0]	000h	FLL1 Integer multiply for F_{SYNC} (LSB = 1)
R387 (0183h) FLL1 Synchroniser 3	15:0	FLL1_SYNC_THETA [15:0]	0000h	FLL1 Fractional multiply for F_{SYNC} This field sets the numerator (multiply) part of the FLL1_SYNC_THETA / FLL1_SYNC_LAMBDA ratio. Coded as LSB = 1.
R388 (0184h) FLL1 Synchroniser 4	15:0	FLL1_SYNC_LAMBDA [15:0]	0000h	FLL1 Fractional multiply for F_{SYNC} This field sets the denominator (dividing) part of the FLL1_SYNC_THETA / FLL1_SYNC_LAMBDA ratio. Coded as LSB = 1.
R389 (0185h) FLL1 Synchroniser 5	10:8	FLL1_SYNC_FRATIO [2:0]	000	FLL1 Synchroniser F_{VCO} clock divider 000 = 1 001 = 2 010 = 4 011 = 8 1XX = 16

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R390 (0186h) FLL1 Synchroniser 6	7:6	FLL1_SYNCCLK_DIV [1:0]	00	FLL1 Synchroniser Clock Reference Divider 00 = 1 01 = 2 10 = 4 11 = 8 MCLK (or other input reference) must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.
	3:0	FLL1_SYNCCLK_SRC	0000	FLL1 Synchroniser Clock source 0000 = MCLK1 0001 = MCLK2 0100 = FLL1 0101 = FLL2 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK 1100 = AIF1LRCLK 1101 = AIF2LRCLK 1110 = AIF3LRCLK All other codes are Reserved
R391 (0187h) FLL1 Synchroniser 7	5:2	FLL1_SYNC_GAIN [3:0]	0000	FLL1 Synchroniser Gain 0000 = 1 0001 = 2 0010 = 4 0011 = 8 0100 = 16 0101 = 32 0110 = 64 0111 = 128 1000 to 1111 = 256
	0	FLL1_SYNC_DFSAT	1	FLL1 Synchroniser Bandwidth 0 = Wide bandwidth 1 = Narrow bandwidth

Table 74 FLL1 Register Map

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R401 (0191h) FLL2 Control 1	0	FLL2_ENA	0	FLL2 Enable 0 = Disabled 1 = Enabled This should be set as the final step of the FLL2 enable sequence, i.e., after the other FLL registers have been configured.
R402 (0192h) FLL2 Control 2	15	FLL2_CTRL_UPD	0	FLL2 Control Update Write '1' to apply the FLL2_N and FLL2_THETA register settings. (Only valid when FLL2_ENA=1)
	9:0	FLL2_N [9:0]	008h	FLL2 Integer multiply for F_{REF} (LSB = 1) If updated while the FLL is enabled, the new value is only effective when a '1' is written to FLL2_CTRL_UPD.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R403 (0193h) FLL2 Control 3	15:0	FLL2_THETA [15:0]	0018h	FLL2 Fractional multiply for F_{REF} This field sets the numerator (multiply) part of the FLL2_THETA / FLL2_LAMBDA ratio. Coded as LSB = 1. If updated while the FLL is enabled, the new value is only effective when a '1' is written to FLL2_CTRL_UPD.
R404 (0194h) FLL2 Control 4	15:0	FLL2_LAMBDA [15:0]	007Dh	FLL2 Fractional multiply for F_{REF} This field sets the denominator (dividing) part of the FLL2_THETA / FLL2_LAMBDA ratio. Coded as LSB = 1.
R405 (0195h) FLL2 Control 5	11:8	FLL2_FRATIO [3:0]	0h	FLL2 F_{VCO} clock divider 0h = 1 1h = 2 2h = 3 3h = 4 … Fh = 16
	3:1	FLL2_OUTDIV [2:0]	110	FLL2 F_{OUT} clock divider 000 = Reserved 001 = Reserved 010 = Divide by 2 011 = Divide by 3 100 = Divide by 4 101 = Divide by 5 110 = Divide by 6 111 = Divide by 7 (F_{OUT} = F_{VCO} / FLL2_OUTDIV)
R406 (0196h) FLL2 Control 6	7:6	FLL2_REFCLK_ DIV [1:0]	00	FLL2 Clock Reference Divider 00 = 1 01 = 2 10 = 4 11 = 8 MCLK (or other input reference) must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.
	3:0	FLL2_REFCLK_S RC	0000	FLL2 Clock source 0000 = MCLK1 0001 = MCLK2 0100 = FLL1 0101 = FLL2 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK 1100 = AIF1LRCLK 1101 = AIF2LRCLK 1110 = AIF3LRCLK All other codes are Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R409 (0199h) FLL2 Control 7	5:2	FLL2_GAIN [3:0]	0000	FLL2 Gain 0000 = 1 0001 = 2 0010 = 4 0011 = 8 0100 = 16 0101 = 32 0110 = 64 0111 = 128 1000 to 1111 = 256
R417 (01A1h) FLL2 Synchroniser 1	0	FLL2_SYNC_ENA	0	FLL2 Synchroniser Enable 0 = Disabled 1 = Enabled This should be set as the final step of the FLL2 synchroniser enable sequence, i.e., after the other synchroniser registers have been configured.
R418 (01A2h) FLL2 Synchroniser 2	9:0	FLL2_SYNC_N [9:0]	000h	FLL2 Integer multiply for F_{SYNC} (LSB = 1)
R419 (01A3h) FLL2 Synchroniser 3	15:0	FLL2_SYNC_THETA [15:0]	0000h	FLL2 Fractional multiply for F_{SYNC} This field sets the numerator (multiply) part of the FLL2_SYNC_THETA / FLL2_SYNC_LAMBDA ratio. Coded as LSB = 1.
R420 (01A4h) FLL2 Synchroniser 4	15:0	FLL2_SYNC_LAMBDA [15:0]	0000h	FLL2 Fractional multiply for F_{SYNC} This field sets the denominator (dividing) part of the FLL2_SYNC_THETA / FLL2_SYNC_LAMBDA ratio. Coded as LSB = 1.
R421 (01A5h) FLL2 Synchroniser 5	10:8	FLL2_SYNC_FRATIO [2:0]	000	FLL2 Synchroniser F_{VCO} clock divider 000 = 1 001 = 2 010 = 4 011 = 8 1XX = 16
R422 (01A6h) FLL2 Synchroniser 6	7:6	FLL2_SYNCCLK_DIV [1:0]	00	FLL2 Synchroniser Clock Reference Divider 00 = 1 01 = 2 10 = 4 11 = 8 MCLK (or other input reference) must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:0	FLL2_SYNCCLK_SRC	0000	FLL2 Synchroniser Clock source 0000 = MCLK1 0001 = MCLK2 0100 = FLL1 0101 = FLL2 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK 1100 = AIF1LRCLK 1101 = AIF2LRCLK 1110 = AIF3LRCLK All other codes are Reserved
R423 (01A7h) FLL2 Synchroniser 7	5:2	FLL2_SYNC_GAIN [3:0]	0000	FLL2 Synchroniser Gain 0000 = 1 0001 = 2 0010 = 4 0011 = 8 0100 = 16 0101 = 32 0110 = 64 0111 = 128 1000 to 1111 = 256
	0	FLL2_SYNC_DFSAT	1	FLL2 Synchroniser Bandwidth 0 = Wide bandwidth 1 = Narrow bandwidth

Table 75 FLL2 Register Map

FREE-RUNNING FLL MODE

The FLL can generate a clock signal even when no external reference is available. This may be because the normal input reference has been interrupted, or may be during a standby or start-up period when no initial reference clock is available.

Free-running FLL mode is enabled using the FLLn_FREERUN register. (Note that FLLn_ENA must also be enabled in Free-running FLL mode.)

In Free-running FLL mode, the normal feedback mechanism of the FLL is halted, and the FLL oscillates independently of the external input reference(s).

If the FLL was previously operating normally, (with an input reference clock), then the FLL output frequency will remain unchanged when Free-running FLL mode is enabled. The FLL output will be independent of the input reference while operating in free-running mode with FLLn_FREERUN=1.

The main FLL loop will always continue to free-run if the input reference clock is stopped (regardless of the FLLn_FREERUN setting). If FLLn_FREERUN=0, the FLL will re-lock to the input reference whenever it is available.

In free-running mode, (with FLLn_FREERUN=1), the FLL integrator value (part of the feedback mechanism) can be commanded directly using the FLLn_FRC_INTEG_VAL register. The integrator value in this register is applied to the FLL when a '1' is written to the FLLn_FRC_INTEG_UPD bit.

If the FLL is started up in free-running mode, (i.e., it was not previously running), then the default value of FLLn_FRC_INTEG_VAL will be applied.

The FLL integrator value (part of the feedback mechanism) can be read from the FLLn_INTEG register; the value of this field may be stored for later use. Note that the readback value of the FLLn_INTEG register is only valid when FLLn_FREERUN=1, and the FLLn_INTEG_VALID bit is set.

The FLL integrator setting does not ensure a specific output frequency for the FLL across all devices and operating conditions; some level of variation will apply.

The free-running FLL clock may be selected as the SYSCLK source or ASYNCCLK source as shown Figure 47.

The control registers applicable to Free-running FLL mode are described in Table 76.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R369 (0171h) FLL1 Control 1	1	FLL1_FREERUN	1	FLL1 Free-Running Mode Enable 0 = Disabled 1 = Enabled The FLL feedback mechanism is halted in Free-Running mode, and the latest integrator setting is maintained
R375 (0177h) FLL1 Loop Filter Test 1	15	FLL1_FRC_INTEG_UPD	0	Write '1' to apply the FLL1_FRC_INTEG_VAL setting. (Only valid when FLL1_FREERUN=1)
	11:0	FLL1_FRC_INTEG_VAL [11:0]	281h	FLL1 Forced Integrator Value
R376 (0178h) FLL1 NCO Test 0	15	FLL1_INTEG_VALID	0	FLL1 Integrator Valid Indicates if the FLL1_INTEG register is valid 0 = Not valid 1 = Valid
	11:0	FLL1_INTEG [11:0]	000h	FLL1 Integrator Value (Read-only) Indicates the current FLL1 integrator setting. Only valid when FLL1_INTEG_VALID = 1.
R401 (0191h) FLL2 Control 1	1	FLL2_FREERUN	1	FLL2 Free-Running Mode Enable 0 = Disabled 1 = Enabled The FLL feedback mechanism is halted in Free-Running mode, and the latest integrator setting is maintained
R407 (0197h) FLL2 Loop Filter Test 1	15	FLL2_FRC_INTEG_UPD	0	Write '1' to apply the FLL2_FRC_INTEG_VAL setting. (Only valid when FLL2_FREERUN=1)
	11:0	FLL2_FRC_INTEG_VAL [11:0]	000h	FLL2 Forced Integrator Value
R408 (0198h) FLL2 NCO Test 0	15	FLL2_INTEG_VALID	0	FLL2 Integrator Valid Indicates if the FLL2_INTEG register is valid 0 = Not valid 1 = Valid
	11:0	FLL2_INTEG [11:0]	000h	FLL2 Integrator Value (Read-only) Indicates the current FLL2 integrator setting. Only valid when FLL2_INTEG_VALID = 1.

Table 76 Free-Running FLL Mode Control

SPREAD SPECTRUM FLL CONTROL

The CS47L24 can apply modulation to the FLL outputs, using spread spectrum techniques. This can be used to control the EMI characteristics of the circuits that are clocked via the FLLs.

Each of the FLLs can be individually configured for Triangle modulation, Zero Mean Frequency Modulation (ZMFM) or Dither. The amplitude and frequency parameters of the spread spectrum functions is also programmable, using the registers described in Table 77.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R393 (0189h) FLL1 Spread Spectrum	5:4	FLL1_SS_AMPL [1:0]	00	FLL1 Spread Spectrum Amplitude Controls the extent of the spread-spectrum modulation. 00 = 0.7% (triangle), 0.7% (ZMFM, dither) 01 = 1.1% (triangle), 1.3% (ZMFM, dither) 10 = 2.3% (triangle), 2.6% (ZMFM, dither) 11 = 4.6% (triangle), 5.2% (ZMFM, dither)
	3:2	FLL1_SS_FREQ [1:0]	00	FLL1 Spread Spectrum Frequency Controls the spread spectrum modulation frequency in Triangle mode. 00 = 439kHz 01 = 878kHz 10 = 1.17MHz 11 = 1.76MHz
	1:0	FLL1_SS_SEL [1:0]	00	FLL1 Spread Spectrum Select 00 = Disabled 01 = Zero Mean Frequency (ZMFM) 10 = Triangle 11 = Dither
R425 (01A9h) FLL2 Spread Spectrum	5:4	FLL2_SS_AMPL [1:0]	00	FLL2 Spread Spectrum Amplitude Controls the extent of the spread-spectrum modulation. 00 = 0.7% (triangle), 0.7% (ZMFM, dither) 01 = 1.1% (triangle), 1.3% (ZMFM, dither) 10 = 2.3% (triangle), 2.6% (ZMFM, dither) 11 = 4.6% (triangle), 5.2% (ZMFM, dither)
	3:2	FLL2_SS_FREQ [1:0]	00	FLL2 Spread Spectrum Frequency Controls the spread spectrum modulation frequency in Triangle mode. 00 = 439kHz 01 = 878kHz 10 = 1.17MHz 11 = 1.76MHz
	1:0	FLL2_SS_SEL [1:0]	00	FLL2 Spread Spectrum Select 00 = Disabled 01 = Zero Mean Frequency (ZMFM) 10 = Triangle 11 = Dither

Table 77 FLL Spread Spectrum Control

FLL INTERRUPTS AND GPIO OUTPUT

For each FLL, the CS47L24 supports an 'FLL Clock OK' signal which, when asserted, indicates that the FLL has started up and is providing an output clock. Each FLL also supports an 'FLL Lock' signal which indicates whether FLL Lock has been achieved.

The FLL Clock OK status and FLL Lock status are inputs to the Interrupt control circuit and can be used to trigger an Interrupt event - see "Interrupts". Note that these Interrupt signals are de-bounced, and require clocking to be present in order to assert the respective Interrupt; either the 32kHz clock, or the SYSCLK signal, must be enabled to trigger an Interrupt from the FLL signals.

The FLL Clock OK and FLL Lock signals can be output directly on a GPIO pin as an external indication of the FLL status. See "General Purpose Input / Output" to configure a GPIO pin for these functions. (These GPIO outputs are not de-bounced, and do not require clocking to be present.)

Clock output signals derived from the FLL can be output on a GPIO pin. See "General Purpose Input / Output" to configure a GPIO pin for this function.

The FLL clocking configuration is illustrated in Figure 49.

EXAMPLE FLL CALCULATION

The following example illustrates how to derive the FLL1 registers to generate 147.456 MHz output (F_{OUT}) from a 12.000 MHz reference clock (F_{REF}). Note that, for this calculation, it is assumed that the synchroniser is disabled.

- Set FLL1_REFCLK_DIV in order to generate F_{REF} <=13.5MHz:
  FLL1_REFCLK_DIV = 00 (divide by 1)
- Set FLL1_OUTDIV for the required output frequency as shown in Table 70:-
  F_{OUT} = 147.456 MHz, therefore FLL1_OUTDIV = 2h (divide by 2)
- Set FLL1_FRATIO for the given reference frequency as shown in Table 71:
  F_{REF} = 12MHz, therefore FLL1_FRATIO = 0h (divide by 1)
- Calculate F_{VCO} as given by $F_{VCO} = F_{OUT}$ x FLL1_OUTDIV:-
  F_{VCO} = 147.456 x 2 = 294.912 MHz
- Calculate N.K as given by N.K = F_{VCO} / (FLL1_FRATIO x 3 x F_{REF}):
  N.K = 294.912 / (1 x 3 x 12) = 8.192
- Confirm that a non-integer value has been calculated for N.K.
- Confirm that the input frequency, F_{REF}, is less than the applicable limit shown in Table 72.
- Determine FLL1_N from the integer portion of N.K:-
  FLL1_N = 8 (008h)
- Determine GCD(FLL), as given by GCD(FLL) = GCD(FLL1_FRATIO x F_{REF}, F_{VCO} / 3):
  GCD(FLL) = GCD(1 x 12000000, 294912000 / 3) = 96000
- Determine FLL1_THETA, as given by
  FLL1_THETA = ((F_{VCO} / 3) - (FLL1_N x FLL1_FRATIO x F_{REF})) / GCD(FLL):
  FLL1_THETA = ((294912000 / 3) - (8 x 1 x 12000000)) / 96000
  FLL1_THETA = 24 (0018h)
- Determine FLL_LAMBDA, as given by
  FLL1_LAMBDA = (FLL1_FRATIO x F_{REF}) / GCD(FLL):
  FLL1_LAMBDA = (1 x 12000000) / 96000
  FLL1_LAMBDA = 125 (007Dh)

EXAMPLE FLL SETTINGS

Table 78 provides example FLL settings for generating an oscillator frequency (F_{VCO}) of 294.912MHz from a variety of low and high frequency reference inputs. This is suitable for generating SYSCLK at 147.456MHz. Note that, in these examples, it is assumed that the synchroniser is disabled.

FLL (Main Loop) Settings							
F_{SOURCE}	F_{VCO} (MHz)	F_{REF} Divider	FRATIO	N.K	FLLn_N	FLLn_ THETA	FLLn_ LAMBDA
32.000 kHz	294.912	1	15	204.8	0CCh	0004h	0005h
32.768 kHz	294.912	1	16	187.5	0BBh	0001h	0002h
48 kHz	294.912	1	15	136.5333	088h	0008h	000Fh
128 kHz	294.912	1	7	109.4173	06Dh	0005h	0007h
512 kHz	294.912	1	5	38.4	026h	0002h	0005h
1.536 MHz	294.912	1	3	21.3333	015h	0001h	0003h
3.072 MHz	294.912	1	3	10.6667	00Ah	0002h	0003h
11.2896 MHz	294.912	1	1	8.7075	008h	0068h	0093h
12.000 MHz	294.912	1	1	8.192	008h	0018h	007Dh
12.288 MHz	294.912	2	3	5.3333	005h	0001h	0003h
13.000 MHz	294.912	1	1	7.5618	007h	0391h	0659h
19.200 MHz	294.912	2	1	10.24	00Ah	0006h	0019h
24 MHz	294.912	2	1	8.192	008h	0018h	007Dh
26 MHz	294.912	2	1	7.5618	007h	0391h	0659h
27 MHz	294.912	2	1	7.2818	007h	013Dh	0465h

F_{OUT} = (F_{SOURCE} / F_{REF} Divider) * 3 * N.K * FRATIO / OUTDIV
The values of N and K are contained in the FLLn_N, FLLn_THETA and FLLn_LAMBDA registers as shown above.
See Table 74 and Table 75 for the coding of the FLLn_REFCLK_DIV, FLLn_FRATIO and FLLn_OUTDIV registers.

Table 78 Example FLL Settings – Synchroniser Disabled

Table 79 provides example FLL settings for generating SYSCLK at 147.456MHz, with the synchroniser enabled. The main loop and the synchroniser loop must each be configured according to the respective input source.

FLL (Main Loop) Settings							
F_{SOURCE}	F_{VCO} (MHz)	F_{REF} Divider	FRATIO	N.K	FLLn_N	FLLn_ THETA	FLLn_ LAMBDA
32.000 kHz	294.912	1	15	204.8	0CCh	CCCCh	0000h
32.768 kHz	294.912	1	16	187.5	0BBh	8000h	0000h
48 kHz	294.912	1	15	136.5333	088h	8888h	0000h
128 kHz	294.912	1	7	109.7143	06Dh	B6DBh	0000h
512 kHz	294.912	1	5	38.4	026h	6666h	0000h
1.536 MHz	294.912	1	3	21.3333	015h	5555h	0000h
3.072 MHz	294.912	1	3	10.6667	00Ah	AAAAh	0000h
11.2896 MHz	294.912	1	1	8.7075	008h	B51Dh	0000h
12.000 MHz	294.912	1	1	8.192	008h	3126h	0000h
12.288 MHz	294.912	2	3	5.3333	005h	5555h	0000h
13.000 MHz	294.912	1	1	7.5618	007h	8FD5h	0000h
19.200 MHz	294.912	2	1	10.24	00Ah	3D70h	0000h
24 MHz	294.912	2	1	8.192	008h	3126h	0000h
26 MHz	294.912	2	1	7.5618	007h	8FD5h	0000h
27 MHz	294.912	2	1	7.2818	007h	4822h	0000h
FLL (Synchroniser Loop) Settings							
F_{SOURCE}	F_{VCO} (MHz)	F_{SYNC} Divider	FRATIO (SYNC)	N.K (SYNC)	FLLn_ SYNC_N	FLLn_ SYNC_ THETA	FLLn_ SYNC_ LAMBDA
32.000 kHz	294.912	1	16	192	0C0h	0000h	0000h
32.768 kHz	294.912	1	16	187.5	0BBh	0001h	0002h
48 kHz	294.912	1	16	128	080h	0000h	0000h
128 kHz	294.912	1	8	96	060h	0000h	0000h
512 kHz	294.912	1	2	96	060h	0000h	0000h
1.536 MHz	294.912	1	1	64	040h	0000h	0000h
3.072 MHz	294.912	1	1	32	020h	0000h	0000h
11.2896 MHz	294.912	1	1	8.7075	008h	0068h	0093h
12.000 MHz	294.912	1	1	8.192	008h	0018h	007Dh
12.288 MHz	294.912	1	1	8	008h	0000h	0000h
13.000 MHz	294.912	1	1	7.5618	007h	0391h	0659h
19.200 MHz	294.912	2	1	10.24	00Ah	0006h	0019h
24 MHz	294.912	2	1	8.192	008h	0018h	007Dh
26 MHz	294.912	2	1	7.5618	007h	0391h	0659h
27 MHz	294.912	2	1	7.2818	007h	013Dh	0465h

F_{OUT} = (F_{SOURCE} / F_{REF} Divider) * 3 * N.K * FRATIO / OUTDIV
The values of N and K are contained in the FLLn_N, FLLn_THETA and FLLn_LAMBDA registers.
See Table 74 and Table 75 for the coding of the FLL configuration registers.
Note that the register coding of FLLn_FRATIO is different to FLLn_SYNC_FRATIO.

Table 79 Example FLL Settings – Synchroniser Enabled

CONTROL INTERFACE

The CS47L24 is controlled by writing to its control registers. Readback is available for all registers.

Note that the Control Interface function can be supported with or without system clocking. Where applicable, the register map access is synchronised with SYSCLK in order to ensure predictable operation of cross-domain functions. See “Clocking and Sample Rates” for further details of Control Interface clocking.

The CS47L24 executes a Boot Sequence following Power-On Reset (POR), Hardware Reset or Software Reset. Note that Control Register writes should not be attempted until the Boot Sequence has completed. See “Power-On Reset (POR)” for further details.

The CS47L24 performs automatic checks to confirm that the control interface does not attempt a Read or Write operation to an invalid register address. The Control Interface Address Error condition can be monitored using the GPIO and/or Interrupt functions. See “General Purpose Input / Output” and “Interrupts” for further details.

The Control Interface is a 4-wire (SPI) interface, comprising the following pins:

- CIFSCLK - serial interface clock input
- CIFMOSI - serial data input
- CIFMISO - serial data output
- $\overline{\text{CIF1SS}}$ - ‘slave select’ input

The Control Interface configuration registers are described in Table 80.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h) Ctrl IF SPI CFG 1	4	SPI_CFG	1	CIFMISO pin configuration 0 = CMOS 1 = Wired ‘OR’.
	3	SPI_4WIRE	1	Reserved - Do not change from default ‘1’.

Table 80 Control Interface Configuration

Note that, when writing to register R8, it is important that bit [3] is always maintained at logic ‘1’. This bit relates to a feature option that is not supported on CS47L24.

The MISO output pin can be configured as CMOS or 'Wired OR', as described in Table 80. In CMOS mode, MISO is driven low when not outputting register data bits. In 'Wired OR' mode, MISO is undriven (high impedance) when not outputting register data bits.

In Write operations (R/W=0), all MOSI bits are driven by the controlling device.

In Read operations (R/W=1), the MOSI pin is ignored following receipt of the valid register address. MISO is driven by the CS47L24.

Continuous read and write modes enable multiple register operations to be scheduled faster than is possible with single register operations. The register address auto-increments (by 1) for each successive register access.

The CS47L24 will increment the register address at the end of the sequences illustrated below, and every 16 clock cycles thereafter, for as long as SS is held low and SCLK is toggled. Successive data words can be input/output every 16 clock cycles.

The 4-wire (SPI) protocol is illustrated in Figure 50 and Figure 51.

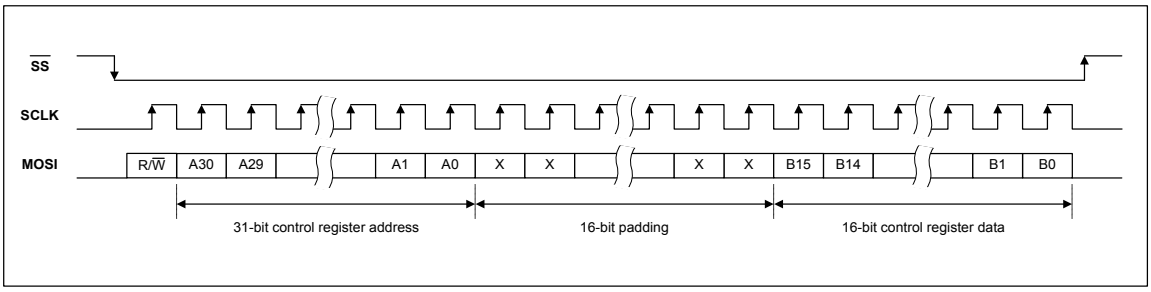


Figure 50 Control Interface 4-wire (SPI) Register Write

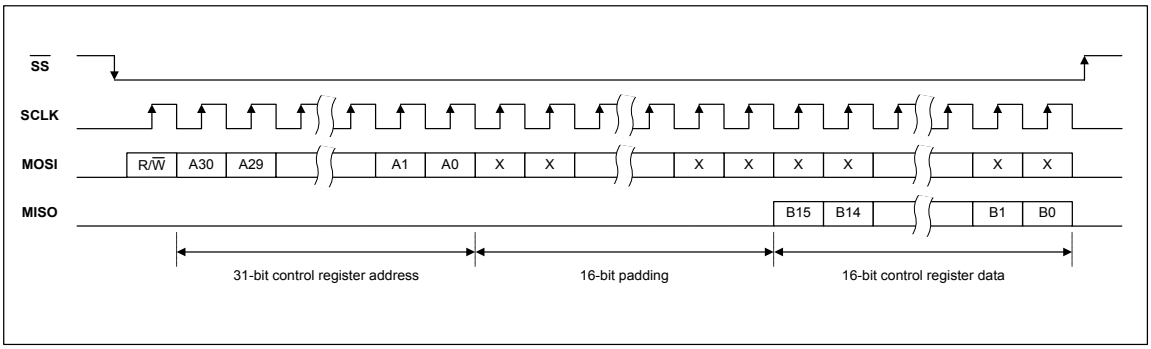


Figure 51 Control Interface 4-wire (SPI) Register Read

CONTROL WRITE SEQUENCER

The Control Write Sequencer is a programmable unit that forms part of the CS47L24 control interface logic. It provides the ability to perform a sequence of register write operations with the minimum of demands on the host processor - the sequence may be initiated by a single operation from the host processor and then left to execute independently.

Default sequences for pop-suppressed start-up and shut-down of each headphone/earpiece output driver are provided (these are scheduled automatically when the respective output paths are enabled or disabled). Other control sequences can be programmed, and may be associated with DRC (signal detect) or Sample Rate Detection functions - these sequences are automatically scheduled whenever a corresponding event is detected.

When a sequence is initiated, the sequencer performs a series of pre-defined register writes. The 'start index' of a control sequence within the sequencer's memory may be commanded directly by the host processor. The applicable 'start index' for each of the sequences associated with DRC (signal detect) or Sample Rate Detection is held in a user-programmed control register.

The Control Write Sequencer may be triggered in a number of ways, as described above. Multiple sequences will be queued if necessary, and each is scheduled in turn. When all of the queued sequences have completed, the sequencer stops, and an Interrupt status flag is asserted.

A valid clock (SYSCLK) must be enabled whenever a Control Write Sequence is scheduled. See "Clocking and Sample Rates" for further details.

INITIATING A SEQUENCE

The Register fields associated with running the Control Write Sequencer are described in Table 81.

The Write Sequencer is enabled using the WSEQ_ENA bit. The index location of the first command in the selected sequence is held in the WSEQ_START_INDEX register.

Writing a '1' to the WSEQ_START bit commands the sequencer to execute a control sequence, starting at the given index. Note that, if the sequencer is already running, then the WSEQ_START command will be queued, and will be executed later when the sequencer becomes available.

Note that the mechanism for queuing multiple sequence requests has some limitations, when using the WSEQ_START bit to trigger the write sequencer. If a sequence is initiated using the WSEQ_START bit, no other control sequences should be triggered until the sequence completes. The WSEQ_BUSY bit (described in Table 86) provides an indication of the sequencer status, and can be used to confirm that sequence has completed. Control sequences triggered by another other method are queued if necessary, and scheduled in turn.

The Write Sequencer can be interrupted by writing a '1' to the WSEQ_ABORT bit. Note that this command will only abort a sequence that is currently running; if other sequence commands are pending and not yet started, these sequences will not be aborted by writing to the WSEQ_ABORT bit.

The Write Sequencer stores up to 510 register write commands. These are defined in Registers R12288 (3000h) to R13307 (33FBh). Each of the 510 possible commands is defined in 2 control registers - see Table 87 for a description of these registers.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R22 (0016h) Write Sequencer Ctrl 0	11	WSEQ_ABORT	0	Writing a 1 to this bit aborts the current sequence.
	10	WSEQ_START	0	Writing a 1 to this bit starts the write sequencer at the index location selected by WSEQ_START_INDEX. At the end of the sequence, this bit will be reset by the Write Sequencer.
	9	WSEQ_ENA	0	Write Sequencer Enable 0 = Disabled 1 = Enabled Only applies to sequences triggered using the WSEQ_START bit.
	8:0	WSEQ_START_INDEX [8:0]	000h	Sequence Start Index This field contains the index location in the sequencer memory of the first command in the selected sequence. Only applies to sequences triggered using the WSEQ_START bit. Valid from 0 to 509 (1FDh).

Table 81 Write Sequencer Control - Initiating a Sequence

AUTOMATIC SAMPLE RATE DETECTION SEQUENCES

The CS47L24 supports automatic sample rate detection on the digital audio interfaces (AIF1, AIF2 and AIF3), when operating in AIF Slave mode. Automatic sample rate detection is enabled using the RATE_EST_ENA register bit (see Table 69).

Up to four audio sample rates can be configured for automatic detection; these sample rates are selected using the SAMPLE_RATE_DETECT_n registers. If one of the selected audio sample rates is detected, then the Control Write Sequencer will be triggered. The applicable start index location within the sequencer memory is separately configurable for each detected sample rate.

The WSEQ_SAMPLE_RATE_DETECT_A_INDEX register defines the sequencer start index corresponding to the SAMPLE_RATE_DETECT_A sample rate. Equivalent start index values are defined for the other sample rates, as described in Table 82.

Note that a sequencer start index of 1FFh will cause the respective sequence to be aborted.

The automatic sample rate detection control sequences are undefined following Power-On Reset (POR), but can be user-programmed after power-up. Note that all control sequences are maintained in the sequencer memory through Hardware Reset and Software Reset.

See “Clocking and Sample Rates” for further details of the automatic sample rate detection function.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R97 (0061h) Sample Rate Sequence Select 1	8:0	WSEQ_SAMPLE_RATE_DETECT_A_INDEX [8:0]	1FFh	Sample Rate A Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with Sample Rate A detection. Valid from 0 to 509 (1FDh)
R98 (0062h) Sample Rate Sequence Select 2	8:0	WSEQ_SAMPLE_RATE_DETECT_B_INDEX [8:0]	1FFh	Sample Rate B Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with Sample Rate B detection. Valid from 0 to 509 (1FDh)
R99 (0063h) Sample Rate Sequence Select 3	8:0	WSEQ_SAMPLE_RATE_DETECT_C_INDEX [8:0]	1FFh	Sample Rate C Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with Sample Rate C detection. Valid from 0 to 509 (1FDh)
R100 (0064h) Sample Rate Sequence Select 4	8:0	WSEQ_SAMPLE_RATE_DETECT_D_INDEX [8:0]	1FFh	Sample Rate D Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with Sample Rate D detection. Valid from 0 to 509 (1FDh)

Table 82 Write Sequencer Control - Automatic Sample Rate Detection

GENERAL PURPOSE (GPIO) CONTROL SEQUENCES

The CS47L24 supports two General Purpose (GPIO) pins, which provide flexible functionality for interfacing to external circuits. The GPIO pins can also be used as inputs to the Control Write Sequencer.

A Control Write Sequence can be associated with a rising edge and/or a falling edge of the GPIO inputs. This is enabled using the GPn_WSEQ_ENA register bits, as described in Table 83.

When the GPIO control sequences are enabled, the Control Write Sequencer will be triggered whenever a rising or falling edge is detected on the associated GPIO input pin. The applicable start index location within the sequencer memory is separately configurable for each logic condition.

The WSEQ_GP1_RISE_INDEX register defines the sequencer start index corresponding to the rising edge condition of the GPIO1 input. Equivalent start index registers are provided for the rising and falling edge conditions of each GPIO, as described in Table 83.

Note that a sequencer start index of 1FFh will cause the respective sequence to be aborted.

The GPIO control sequences cannot be independently enabled for rising and falling edges. Instead, a start index of 1FFh can be used to disable the sequence for either edge, if required.

The GPIO control sequences are undefined following Power-On Reset (POR), but can be user-programmed after power-up. Note that all control sequences are maintained in the sequencer memory through Hardware Reset and Software Reset.

See “General Purpose Input / Output” for further details of the GPIO functions.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R65 (0041h) Sequence control	1	GP2_WSEQ_ENA	0	GPIO2 Write Sequencer Trigger Enable 0 = Disabled 1 = Enabled When enabled, a rising or falling edge on GPIO2 will trigger the Write Sequencer, starting at the respective memory index.
	0	GP1_WSEQ_ENA	0	Enables WSEQ control on GPIO1 pin 0 = Disabled 1 = Enabled When enabled, a rising or falling edge on GPIO1 will trigger the Write Sequencer, starting at the respective memory index.
R104 (0068h) GPIO Triggers Sequence Select 1	8:0	WSEQ_GP1_RISE_INDEX [8:0]	1FFh	Sequence GPIO1 (Rising) start index This field contains the index location in the sequencer memory of the first command in the sequence associated with the GPIO1 (Rising) trigger. Valid from 0 to 509 (1FDh).
R105 (0069h) GPIO Triggers Sequence Select 2	8:0	WSEQ_GP1_FALL_INDEX [8:0]	1FFh	Sequence GPIO1 (Falling) start index This field contains the index location in the sequencer memory of the first command in the sequence associated with the GPIO1 (Falling) trigger. Valid from 0 to 509 (1FDh).
R106 (006Ah) GPIO Triggers Sequence Select 3	8:0	WSEQ_GP2_RISE_INDEX [8:0]	1FFh	Sequence GPIO2 (Rising) start index This field contains the index location in the sequencer memory of the first command in the sequence associated with the GPIO2 (Rising) trigger. Valid from 0 to 509 (1FDh).
R107 (006Bh) GPIO Triggers Sequence Select 4	8:0	WSEQ_GP2_FALL_INDEX [8:0]	1FFh	Sequence GPIO2 (Falling) start index This field contains the index location in the sequencer memory of the first command in the sequence associated with the GPIO2 (Falling) trigger. Valid from 0 to 509 (1FDh).

Table 83 Write Sequencer Control - GPIO

DRC SIGNAL DETECT SEQUENCES

The Dynamic Range Control (DRC) function within the CS47L24 Digital Core provides a configurable signal detect function. This allows the signal level at the DRC input to be monitored and used to trigger other events.

The DRC Signal Detect functions are enabled and configured using the register fields described in Table 13 and Table 14 for DRC1 and DRC2 respectively.

A Control Write Sequence can be associated with a rising edge and/or a falling edge of the DRC1 Signal Detect output. This is enabled using the DRC1_WSEQ_SIG_DET_ENA register bit.

Note that signal detection is supported on DRC1 and DRC2, but the triggering of the Control Write Sequencer is available on DRC1 only.

When the DRC Signal Detect sequence is enabled, the Control Write Sequencer will be triggered whenever the DRC1 Signal Detect output transitions (high or low). The applicable start index location within the sequencer memory is separately configurable for each logic condition.

The WSEQ_DRC1_SIG_DET_RISE_SEQ_INDEX register defines the sequencer start index corresponding to a DRC1 Signal Detect Rising Edge event, as described in Table 84. The WSEQ_DRC1_SIG_DET_FALL_SEQ_INDEX register defines the sequencer start index corresponding to a DRC1 Signal Detect Falling Edge event.

Note that a sequencer start index of 1FFh will cause the respective sequence to be aborted.

The DRC Signal Detect sequences cannot be independently enabled for rising and falling edges. Instead, a start index of 1FFh can be used to disable the sequence for either edge, if required.

The DRC Signal Detect control sequences are undefined following Power-On Reset (POR), but can be user-programmed after power-up. Note that all control sequences are maintained in the sequencer memory through Hardware Reset and Software Reset.

See “Digital Core” for further details of the Dynamic Range Control (DRC) function.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R110 (006Eh) Trigger Sequence Select 32	8:0	WSEQ_DRC1_SIG_DET_RISE_INDEX [8:0]	1FFh	DRC1 Signal Detect (Rising) Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with DRC1 Signal Detect (Rising) detection. Valid from 0 to 509 (1FDh).
R111 (006Fh) Trigger Sequence Select 33	8:0	WSEQ_DRC1_SIG_DET_FALL_INDEX [8:0]	1FFh	DRC1 Signal Detect (Falling) Write Sequence start index This field contains the index location in the sequencer memory of the first command in the sequence associated with DRC1 Signal Detect (Falling) detection. Valid from 0 to 509 (1FDh).

Table 84 Write Sequencer Control - DRC Signal Detect

BOOT SEQUENCE

The CS47L24 executes a Boot Sequence following Power-On Reset (POR), Hardware Reset, or Software Reset.

See “Power-On Reset (POR)” and “Hardware Reset, Software Reset, and Device ID” for further details.

The Boot Sequence configures the CS47L24 with factory-set trim (calibration) data. Space is allocated within the Boot Sequence memory to allow user-configurable register operations to be added (e.g., to automatically enable SYSCLK as part of the Boot Sequence). Further details of the sequencer memory are provided later in this section. Note that all control sequences are maintained in the sequencer memory through Hardware Reset and Software Reset.

If the Boot Sequence is programmed to enable SYSCLK, note that the default SYSCLK frequency must be used. If a different SYSCLK frequency is required, this must be configured after the Boot Sequence has completed.

The start index location of the the Boot Sequence is 384 (180h). Index locations 384 (180h) to 393 (189h) are available for any user-configured Boot Sequence requirements.

The Boot Sequence can be commanded at any time by writing ‘1’ to the WSEQ_BOOT_START bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (0018h) Write Sequencer Ctrl 2	1	WSEQ_BOOT_START	0	Writing a 1 to this bit starts the write sequencer at the index location configured for the Boot Sequence. The Boot Sequence start index is 384 (180h).

Table 85 Write Sequencer Control - Boot Sequence

SEQUENCER OUTPUTS AND READBACK

The status of the Write Sequencer can be read using the WSEQ_BUSY and WSEQ_CURRENT_INDEX registers, as described in Table 86.

When the WSEQ_BUSY bit is asserted, this indicates that the Write Sequencer is busy.

The index address of the most recent Write Sequencer command can be read from the WSEQ_CURRENT_INDEX field. This can be used to provide a precise indication of the Write Sequencer progress.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (0017h) Write Sequencer Ctrl 1	9	WSEQ_BUSY (read only)	0	Sequencer Busy flag (Read Only). 0 = Sequencer idle 1 = Sequencer busy
	8:0	WSEQ_CURRENT_INDEX [8:0] (read only)	000h	Sequence Current Index. This indicates the memory location of the most recently accessed command in the write sequencer memory. Coding is the same as WSEQ_START_INDEX.

Table 86 Write Sequencer Control - Status Readback

The Write Sequencer status is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see “Interrupts”.

The Write Sequencer status can be output directly on a GPIO pin as an external indication of the Write Sequencer. See “General Purpose Input / Output” to configure a GPIO pin for this function.

PROGRAMMING A SEQUENCE

A Control Write Sequence comprises a series of write operations to data bits (or groups of bits) within the control register map. Each write operation is defined by a block of 2 registers, each containing 5 fields, as described below.

The block of 2 registers is replicated 510 times, defining each of the sequencer's 510 possible index addresses. Many sequences can be stored in the sequencer memory at the same time, with each assigned a unique range of index addresses.

The WSEQ_DELAYn register is used to identify the 'end of sequence' position, as described below.

Note that, in the following descriptions, the term '*n*' denotes the sequencer index address (valid from 0 to 509).

WSEQ_DATA_WIDTH*n* is a 3-bit field which identifies the width of the data block to be written. Note that the maximum value of this field selects a width of 8-bits; writing to register fields greater than 8 bits wide must be performed using two separate operations of the Write Sequencer.

WSEQ_ADDR*n* is a 13-bit field containing the register address in which the data should be written.

WSEQ_DELAY*n* is a 4-bit field which controls the waiting time between the current step and the next step in the sequence (i.e., the delay occurs after the write in which it was called). The total delay time per step (including execution) is defined below, giving a useful range of execution/delay times from 3.3µs up to 1s per step. Setting this field to 0xF identifies the step as the last in the sequence.

If WSEQ_DELAYn = 0h or Fh, the step execution time is 3.3µs

For all other values, the step execution time is 61.44µs x ((2 $^{WSEQ\_DELAY}$) - 1)

WSEQ_DATA_START*n* is a 4-bit field which identifies the LSB position within the selected control register to which the data should be written. For example, setting WSEQ_DATA_START*n* = 0100 will select bit 4 as the LSB position of the data to be written.

WSEQ_DATA*n* is an 8-bit field which contains the data to be written to the selected control register. The WSEQ_DATA_WIDTH*n* field determines how many of these bits are written to the selected control register; the most significant bits (above the number indicated by WSEQ_DATA_WIDTH*n*) are ignored.

The register definitions for Step 0 are described in Table 87. The equivalent definitions also apply to Step 1 through to Step 509, in the subsequent register address locations.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12288 (3000h) WSEQ Sequence 1	15:13	WSEQ_DATA_ WIDTH0 [2:0]	000	Width of the data block written in this sequence step. 000 = 1 bit 001 = 2 bits 010 = 3 bits 011 = 4 bits 100 = 5 bits 101 = 6 bits 110 = 7 bits 111 = 8 bits
	12:0	WSEQ_ADDR0 [12:0]	0000h	Control Register Address to be written to in this sequence step.
R12289 (3001h) WSEQ Sequence 2	15:12	WSEQ_DELAY0 [3:0]	0000	Time delay after executing this step. 00h = 3.3us 01h to 0Eh = 61.44us x ((2^WSEQ_DELAY)-1) 0Fh = End of sequence marker
	11:8	WSEQ_DATA_S TART0 [3:0]	0000	Bit position of the LSB of the data block written in this sequence step. 0000 = Bit 0 … 1111 = Bit 15

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7:0	WSEQ_DATA0 [7:0]	00h	Data to be written in this sequence step. When the data width is less than 8 bits, then one or more of the MSBs of WSEQ_DATA*n* are ignored. It is recommended that unused bits be set to 0.

Table 87 Write Sequencer Control - Programming a Sequence

SEQUENCER MEMORY DEFINITION

The Write Sequencer memory defines up to 510 write operations; these are indexed as 0 to 509 in the sequencer memory map.

Following Power-On Reset (POR), the sequence memory will contain the Boot Sequence, and the OUT1, OUT4L signal path enable/disable sequences. The remainder of the sequence memory will be undefined on power-up. See the "Applications Information" section for a summary of the CS47L24 memory reset conditions.

User-defined sequences can be programmed after power-up. Note that all control sequences are maintained in the sequencer memory through Hardware Reset and Software Reset.

The default control sequences can be overwritten in the sequencer memory, if required. Note that the headphone and earpiece output path enable registers (HPx_ENA, SPKOUTL_ENA) will always trigger the Write Sequencer (at the pre-determined start index addresses).

Writing '1' to the WSEQ_LOAD_MEM bit will clear the sequencer memory to the POR state.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (0018h) Write Sequencer Ctrl 2	0	WSEQ_LOAD_ MEM	0	Writing a 1 to this bit resets the sequencer memory to the POR state.

Table 88 Write Sequencer Control - Load Memory Control

The sequencer memory is summarised in Table 89. User-defined sequences should be assigned space within the allocated portion ('user space') of the Write Sequencer memory.

The start index for the user-defined sequences is configured using the registers described in Table 82, Table 83, and and Table 84.

The start index location of the the Boot Sequence is 384 (180h), as shown in Table 85. Index locations 384 (180h) to 393 (189h) are available for any user-configured Boot Sequence requirements. The remainder of the Boot Sequence memory should not be written to.

DESCRIPTION	SEQUENCE INDEX RANGE
Default Sequences	0 to 89
User Space	90 to 383
Boot Sequence (User Space)	384 to 393
Boot Sequence (Reserved)	394 to 412
User Space	413 to 507

Table 89 Write Sequencer Memory Allocation

CHARGE PUMP, REGULATORS AND VOLTAGE REFERENCE

The CS47L24 incorporates a Charge Pump circuit to support the ground-referenced headphone output driver. It also provides two MICBIAS generators, suitable for powering digital microphones.

Refer to the “Applications Information” section for recommended external components.

CHARGE PUMP (CP) CONTROL

The Charge Pump (CP) is used to generate the positive and negative supply rails for the stereo headphone output drivers. This circuit is enabled automatically by the CS47L24 when required.

Note that decoupling capacitors and flyback capacitors are required for this circuit. Refer to the “Applications Information” section for recommended external components.

MICROPHONE BIAS (MICBIAS) CONTROL

There are two MICBIAS generators which provide low noise reference voltages suitable for powering digital microphones. Refer to the “Applications Information” section for recommended external components.

The MICBIAS generators are powered from the MICVDD supply, as illustrated in Figure 52.

The MICBIAS outputs can be independently enabled using the MICB*n*_ENA register bits (where *n* = 1 or 2 for MICBIAS1 or 2 respectively).

When a MICBIAS output is disabled, the output pin can be configured to be floating or to be actively discharged. This is selected using the MICB*n*_DISCH register bits.

The MICBIAS generators can each operate as a voltage regulator or in bypass mode. The applicable mode is selected using the MICB*n*_BYPASS registers.

In Regulator mode, the output voltage is selected using the MICB*n*_LVL register bits. In this mode, MICVDD must be at least 200mV greater than the required MICBIAS output voltages. The MICBIAS outputs are powered from the MICVDD pin, and use the internal bandgap circuit as a reference.

In Regulator mode, the MICBIAS regulators are designed to operate without external decoupling capacitors. The regulators can be configured to support a capacitive load if required, using the MICBn_EXT_CAP register bits. It is important that the external capacitance is compatible with the applicable MICBn_EXT_CAP setting. The compatible load conditions are detailed in the “Electrical Characteristics” section.

In Bypass mode, the output pin (MICBIAS1 or MICBIAS2) is connected directly to MICVDD. This enables a low power operating state. Note that the MICBn_EXT_CAP register settings are not applicable in Bypass mode; there are no restrictions on the external MICBIAS capacitance in Bypass mode.

The MICBIAS generators incorporate a pop-free control circuit to ensure smooth transitions when the MICBIAS outputs are enabled or disabled in Bypass mode; this feature is enabled using the MICB*n*_RATE registers.

The MICBIAS generators are illustrated in Figure 52. The MICBIAS control register bits are descrbed in Table 90.

The maximum output current for each MICBIAS*n* pin is noted in the “Electrical Characteristics”. This limit must be observed on each MICBIAS output, especially if more than one microphone is connected to a single MICBIAS pin. Note that the maximum output current differs between Regulator mode and Bypass mode.

VOLTAGE REFERENCE CIRCUIT

The CS47L24 incorporates a voltage reference circuit, powered by AVDD. This circuit ensures the accuracy of the MICBIAS voltage settings.

BLOCK DIAGRAM AND CONTROL REGISTERS

The Charge Pump and Regulator circuits are illustrated in Figure 52. Note that decoupling capacitors and flyback capacitors are required for these circuits. Refer to the “Applications Information” section for recommended external components.

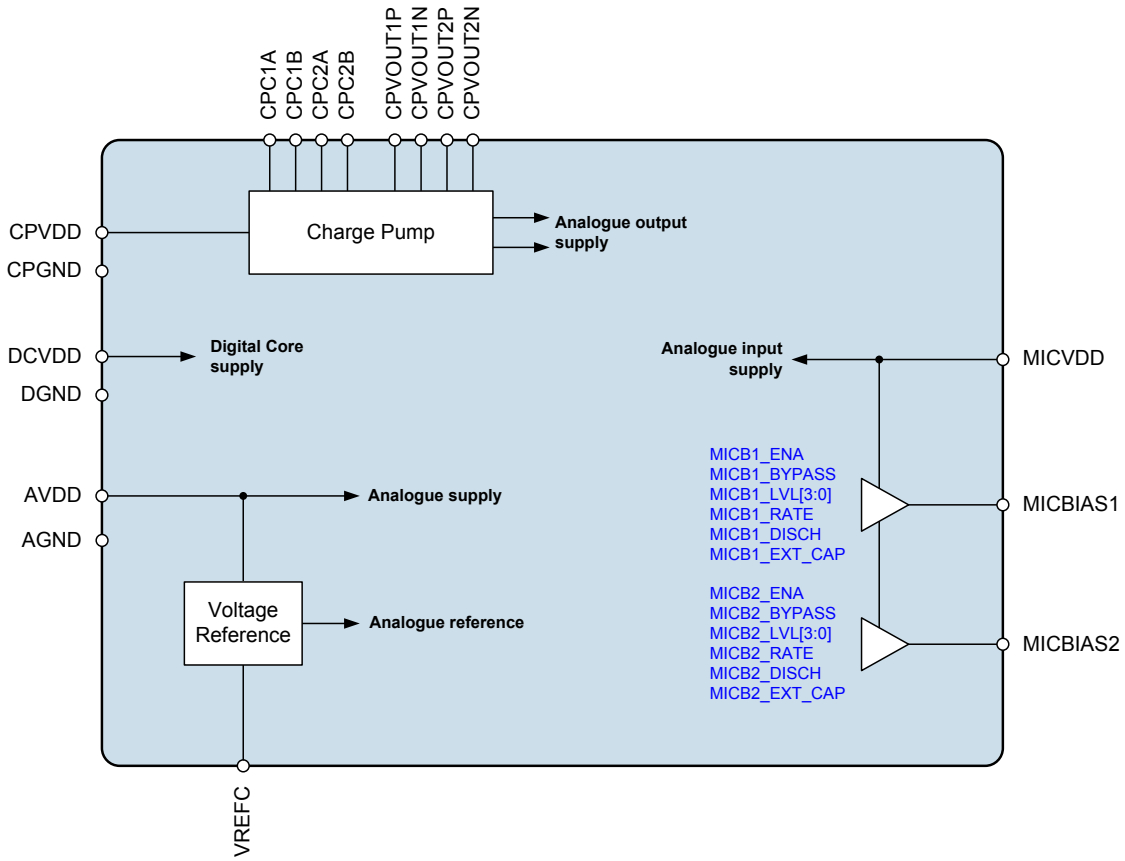


Figure 52 Charge Pump and MICBIAS Regulators

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R536 (218h) Mic Bias Ctrl 1	15	MICB1_EXT_CAP	0	Microphone Bias 1 External Capacitor (when MICB1_BYPASS = 0). Configures the MICBIAS1 regulator according to the specified capacitance connected to the MICBIAS1 output. 0 = No external capacitor 1 = External capacitor connected
	8:5	MICB1_LVL [3:0]	7h	Microphone Bias 1 Voltage Control (when MICB1_BYPASS = 0) 0h = 1.5V 1h = 1.6V … (0.1V steps) Ch = 2.7V Dh = 2.8V Eh = Reserved Fh = Reserved
	3	MICB1_RATE	0	Microphone Bias 1 Rate (Bypass mode) 0 = Fast start-up / shut-down 1 = Pop-free start-up / shut-down

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	2	MICB1_DISCH	1	Microphone Bias 1 Discharge 0 = MICBIAS1 floating when disabled 1 = MICBIAS1 discharged when disabled
	1	MICB1_BYPASS	1	Microphone Bias 1 Mode 0 = Regulator mode 1 = Bypass mode
	0	MICB1_ENA	0	Microphone Bias 1 Enable 0 = Disabled 1 = Enabled
R537 (219h) Mic Bias Ctrl 2	15	MICB2_EXT_CAP	0	Microphone Bias 2 External Capacitor (when MICB2_BYPASS = 0). Configures the MICBIAS2 regulator according to the specified capacitance connected to the MICBIAS2 output. 0 = No external capacitor 1 = External capacitor connected
	8:5	MICB2_LVL [3:0]	7h	Microphone Bias 2 Voltage Control (when MICB2_BYPASS = 0) 0h = 1.5V 1h = 1.6V … (0.1V steps) Ch = 2.7V Dh = 2.8V Eh = Reserved Fh = Reserved
	3	MICB2_RATE	0	Microphone Bias 2 Rate (Bypass mode) 0 = Fast start-up / shut-down 1 = Pop-free start-up / shut-down
	2	MICB2_DISCH	1	Microphone Bias 2 Discharge 0 = MICBIAS2 floating when disabled 1 = MICBIAS2 discharged when disabled
	1	MICB2_BYPASS	1	Microphone Bias 2 Mode 0 = Regulator mode 1 = Bypass mode
	0	MICB2_ENA	0	Microphone Bias 2 Enable 0 = Disabled 1 = Enabled

Table 90 Charge Pump and MICBIAS Control Registers

JTAG INTERFACE

The JTAG interface provides test and debug access to the CS47L24 DSP core. The interface comprises 5 pins, as detailed below.

- TCK: Clock input
- TDI: Data input
- TDO: Data output
- TMS: Mode select input
- TRST: Test Access Port reset input (active low)

For normal operation (test and debug access disabled), the JTAG interface should be held in reset (i.e., TRST should be at logic 0). An internal pull-down resistor holds the TRST pin low when not actively driven.

The other JTAG input pins (TCK, TDI, TMS) should also be held at logic 0 for normal operation. An internal pull-down resistor holds these pins low when not actively driven.

If the JTAG interface is enabled (TRST de-asserted, and TCK active) at the time of Power-On Reset, or any other Reset, then a Software Reset must be scheduled, with the TCK input stopped or TRST asserted (logic '0'), before using the JTAG interface.

As a general rule, it is recommended to always schedule a Software Reset before starting the JTAG clock, or de-asserting the JTAG reset. In this event, the JTAG interface should be held in its reset state until the Software Reset has completed, and the BOOT_DONE_STS bit has been set.

See "Hardware Reset, Software Reset, and Device ID" for further details of the CS47L24 Software Reset.

THERMAL SHUTDOWN AND SHORT CIRCUIT PROTECTION

The CS47L24 incorporates thermal protection functions, and also provides short-circuit detection on the Class D speaker and headphone output paths, as described below.

The temperature sensor detects when the device temperature is within normal limits or if the device is approaching a hazardous temperature condition.

The temperature sensor is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see "Interrupts". A two-stage indication is provided, via the SPK_OVERHEAT_WARN_EINTn and SPK_OVERHEAT_EINTn interrupts.

If the upper temperature threshold (SPK_OVERHEAT_EINTn) is exceeded, then the Class D speaker outputs will automatically be disabled in order to protect the device. When the speaker driver shutdown is complete, a further interrupt, SPK_SHUTDOWN_EINTn, will be asserted.

The short circuit detection function for the Class D speaker outputs is triggered when the respective output drivers are enabled (using the register bits described in Table 48). If a short circuit is detected at this time, then the enable will be unsuccessful, and the respective output driver will not be enabled.

The Class D speaker short circuit detection provides inputs to the Interrupt control circuit and can be used to trigger an Interrupt event - see "Interrupts".

If the Class D speaker short circuit condition is detected, then the respective driver(s) will automatically be disabled in order to protect the device. When the speaker driver shutdown is complete, a further interrupt, SPK_SHUTDOWN_EINTn, will be asserted.

To enable the Class D speaker outputs following a short circuit detection, the host processor must disable and re-enable the output driver(s) twice over (i.e., disable, enable, disable, enable). Note that the short circuit status bits will always be cleared when the drivers are disabled.

The short circuit detection function for the headphone output paths operates continuously whilst the respective output driver is enabled. If a short circuit is detected on any headphone output, then current limiting is applied, in order to protect the output driver. Note that the respective output driver will continue to operate, but the output is current-limited.

The short circuit detection function for the headphone outputs is designed to operate under a range of typical load conditions. However, it is not compatible with highly reactive loads (either inductive or capacitive), as found on some multi-driver headphones, due to phase shifting that arises under these conditions. The headphone short circuit detection function must be disabled if these load conditions may be applicable.

The short circuit detection function for the headphone output paths is enabled by default, but can be disabled using the HP1_SC_ENA register bit, described in Table 91. The output path performance (THD, THD+N) is improved when the short circuit function is disabled.

Note that, when writing to the HP1_SC_ENA bit, care is required not to change the value of other bits in the same register, which may have changed from the default setting. Accordingly, a 'read-modify-write' sequence is required to implement this.

The headphone output short circuit detection provides inputs to the Interrupt control circuit and can be used to trigger an Interrupt event - see "Interrupts". Note that two short circuit indications are implemented for each headphone output channel (relating to detection in the positive and negative output voltage regions respectively); if either of these indications is asserted, then a short circuit condition exists in the respective output path.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1184 (04A0h) HP1 Short Circuit Ctrl	12	HP1_SC_ENA	1	HPOUT Short Circuit Detect Enable 0 = Disabled 1 = Enabled

Table 91 Headphone Short Circuit Detection Control

The Thermal Shutdown and Short Circuit protection status flags can be output directly on a GPIO pin as an external indication of the associated events. See "General Purpose Input / Output" to configure a GPIO pin for this function.

POWER-ON RESET (POR)

The CS47L24 will remain in the reset state until AVDD, DBVDD and DCVDD are all above their respective reset thresholds. Note that specified device performance is not assured outside the voltage ranges defined in the "Recommended Operating Conditions" section.

Refer to "Recommended Operating Conditions" for the CS47L24 power-up sequencing requirements.

After the initial power-up, the Power-On Reset will be re-scheduled following an interruption to the DCVDD, DBVDD or AVDD supplies. Note that the AVDD supply must always be maintained whenever the DCVDD supply is present.

Following Power-On Reset (POR), a Boot Sequence is executed. The BOOT_DONE_STS register is asserted on completion of the Boot Sequence, as described in Table 92. Control register writes should not be attempted until the BOOT_DONE_STS register has been asserted.

The BOOT_DONE_STS signal is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see "Interrupts". Under default register conditions, a falling edge on the IRQ pin will indicate completion of the Boot Sequence.

The BOOT_DONE_STS signal can also generate a GPIO output, providing an external indication of the Boot Sequence. See "General Purpose Input / Output" to configure a GPIO pin for this function.

For details of the Boot Sequence, see "Control Write Sequencer".

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3363 (0D23h) Interrupt Raw Status 5	8	BOOT_DONE_STS	0	Boot Status 0 = Busy (boot sequence in progress) 1 = Idle (boot sequence completed) Control register writes should not be attempted until Boot Sequence has completed.

Table 92 Device Boot-Up Status

Table 93 describes the default status of the CS47L24 digital I/O pins on completion of Power-On Reset, prior to any register writes. The same default conditions are also applicable on completion of a Hardware Reset or Software Reset (see "Hardware Reset, Software Reset, and Device ID").

Note that the default conditions described in Table 93 will not be valid if modified by the Boot Sequence. See "Control Write Sequencer" for details of the Boot Sequence function.

PIN NO	NAME	TYPE	RESET STATUS
MICVDD power domain			
H5	DMICCLK1	Digital Output	Digital output
F3	DMICCLK2	Digital Output	Digital output
G4	DMICDAT1	Digital Input	Digital input
H3	DMICDAT2	Digital Input	Digital input
DBVDD power domain			
M7	AIF1BCLK	Digital Input / Output	Digital input
N8	AIF1LRCLK	Digital Input / Output	Digital input
L8	AIF1RXDAT	Digital Input	Digital input
K7	AIF1TXDAT	Digital Output	Digital output
L4	AIF2BCLK	Digital Input / Output	Digital input
N4	AIF2LRCLK	Digital Input / Output	Digital input
P3	AIF2RXDAT	Digital Input	Digital input
M5	AIF2TXDAT	Digital Output	Digital output
M1	AIF3BCLK	Digital Input / Output	Digital input
N2	AIF3LRCLK	Digital Input / Output	Digital input
M3	AIF3RXDAT	Digital Input	Digital input
L2	AIF3TXDAT	Digital Output	Digital output
J4	CIFMISO	Digital Output	Digital output
N6	CIFMOSI	Digital Input	Digital input
L6	CIFSCLK	Digital Input	Digital input
K5	CIFSS	Digital Input	Digital input
F9	GPIO1	Digital Input / Output	Digital input, Pull-down to DGND
H9	GPIO2	Digital Input / Output	Digital input, Pull-down to DGND
J8	IRQ	Digital Output	Digital output
P5	MCLK1	Digital Input	Digital input
K9	MCLK2	Digital Input	Digital input
E8	RESET	Digital Input	Digital input, Pull-up to DBVDD
G8	TCK	Digital Input	Digital input, Pull-down to DGND
H7	TDI	Digital Input	Digital input, Pull-down to DGND
J6	TDO	Digital Output	Digital output
G6	TMS	Digital Input	Digital input, Pull-down to DGND
K3	TRST	Digital Input	Digital input, Pull-down to DGND

Table 93 CS47L24 Digital I/O Status in Reset

HARDWARE RESET, SOFTWARE RESET, AND DEVICE ID

The CS47L24 provides a Hardware Reset function, which is executed whenever the $\overline{\text{RESET}}$ input is asserted (logic 0). The $\overline{\text{RESET}}$ input is active low and is referenced to the DBVDD power domain.

A Hardware Reset causes most of the CS47L24 control registers to be reset to their default states. Note that the Control Write Sequencer memory and DSP firmware memory contents are retained during Hardware Reset (assuming the conditions noted below).

An internal pull-up resistor is enabled by default on the $\overline{\text{RESET}}$ pin; this can be configured using the RESET_PU register bit. A pull-down resistor is also available, as described in Table 94. When the pull-up and pull-down resistors are both enabled, the CS47L24 provides a 'bus keeper' function on the $\overline{\text{RESET}}$ pin. The bus keeper function holds the input logic level unchanged whenever the external circuit removes the drive (e.g., if the signal is tri-stated).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3104 (0C20h) Misc Pad Ctrl 1	1	RESET_PU	1	RESET Pull-up enable 0 = Disabled 1 = Enabled Note - when RESET_PD and RESET_PU are both set to '1', then a 'bus keeper' function is enabled on the RESET pin.
	0	RESET_PD	0	RESET Pull-down enable 0 = Disabled 1 = Enabled Note - when RESET_PD and RESET_PU are both set to '1', then a 'bus keeper' function is enabled on the RESET pin.

Table 94 Reset Pull-Up Configuration

A Software Reset is executed by writing any value to register R0. A Software Reset causes most of the CS47L24 control registers to be reset to their default states. Note that the Control Write Sequencer memory and DSP firmware memory contents are retained during Software Reset (assuming the conditions noted below).

The Control Write Sequencer memory contents are retained during Hardware Reset or Software Reset; these registers are only reset following a Power-On Reset (POR).

The DSP firmware memory contents are also retained during Hardware Reset and Software Reset, provided DCVDD is held above its reset threshold, and the DSPn_MEM_ENA bits are set to '1' (default).

See the "Applications Information" section for a summary of the CS47L24 memory reset conditions. The DSPn_MEM_ENA register bits are described in Table 25.

Following Hardware Reset or Software Reset, a Boot Sequence is executed. The BOOT_DONE_STS register (see Table 92) is de-asserted during Hardware Reset and Software Reset. The BOOT_DONE_STS register is asserted on completion of the boot-up sequence. Control register writes should not be attempted until the BOOT_DONE_STS register has been asserted.

The BOOT_DONE_STS signal is an input to the Interrupt control circuit and can be used to trigger an Interrupt event - see "Interrupts".

The BOOT_DONE_STS signal can also generate a GPIO output, providing an external indication of the Boot Sequence. See "General Purpose Input / Output" to configure a GPIO pin for this function.

For details of the Boot Sequence, see "Control Write Sequencer".

The status of the CS47L24 digital I/O pins following Hardware Reset or Software Reset is described in the “Power-On Reset (POR)” section.

The Device ID can be read back from Register R0. The Hardware Revision can be read back from Register R1.

The Software Revision can be read back from Register R2. The Software Revision code is incremented if software driver compatibility or software feature support is changed.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (0000h) Software Reset	15:0	SW_RST_DEV_ID [15:0]	6363h	Writing to this register resets all registers to their default state. Reading from this register will indicate Device ID 6363h.
R1 (0001h) Hardware Revision	7:0	HW_REVISION [7:0]		Hardware Device revision. (incremented for every new revision of the device)
R2 (0002h) Software Revision	6:0	SW_REVISION [6:0]		Software Device revision. (incremented if software driver compatibility or software feature support is changed)

Table 95 Device Reset and ID

REGISTER MAP

The CS47L24 control registers are listed below. Note that only the register addresses described here should be accessed; writing to other addresses may result in undefined behaviour. Register bits that are not documented should not be changed from the default values.

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R0 (0h)	Software Reset	SW_RST_DEV_ID [15:0]																6363h
R1 (1h)	Hardware Revision	0	0	0	0	0	0	0	0	HW_REVISION [7:0]								0000h
R2 (2h)	Software Revision	0	0	0	0	0	0	0	0	SW_REVISION [6:0]							0	0000h
R8 (8h)	Ctrl IF SPI CFG 1	0	0	0	0	0	0	0	0	0	0	0	SPI_CFG	SPI_4WIRE	0	0	1	0019h
R22 (16h)	Write Sequencer Ctrl 0	0	0	0	0	WSEQ_ABORT	WSEQ_START	WSEQ_ENA	WSEQ_START_INDEX [8:0]									0000h
R23 (17h)	Write Sequencer Ctrl 1	0	0	0	0	0	0	WSEQ_BUSY	WSEQ_CURRENT_INDEX [8:0]									0000h
R24 (18h)	Write Sequencer Ctrl 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	WSEQ_BOOT_START	WSEQ_LOAD_MEM	0000h
R32 (20h)	Tone Generator 1	0	TONE_RATE [3:0]				0	TONE_OFFSET [1:0]		0	0	TONE2_OVD	TONE1_OVD	0	0	TONE2_ENA	TONE1_ENA	0000h
R33 (21h)	Tone Generator 2	TONE1_LVL [15:0]																1000h
R34 (22h)	Tone Generator 3	0	0	0	0	0	0	0	0	TONE1_LVL [7:0]								0000h
R35 (23h)	Tone Generator 4	TONE2_LVL [15:0]																1000h
R36 (24h)	Tone Generator 5	0	0	0	0	0	0	0	0	TONE2_LVL [7:0]								0000h
R48 (30h)	PWM Drive 1	0	PWM_RATE [3:0]				PWM_CLK_SEL [2:0]			0	0	PWM2_OVD	PWM1_OVD	0	0	PWM2_ENA	PWM1_ENA	0000h
R49 (31h)	PWM Drive 2	0	0	0	0	0	0	PWM1_LVL [9:0]										0100h
R50 (32h)	PWM Drive 3	0	0	0	0	0	0	PWM2_LVL [9:0]										0100h
R65 (41h)	Sequence control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GP2_WSEQ_ENA	GP1_WSEQ_ENA	0000h
R97 (61h)	Sample Rate Sequence Select 1	0	0	0	0	0	0	0	WSEQ_SAMPLE_RATE_DETECT_A_INDEX [8:0]									01FFh
R98 (62h)	Sample Rate Sequence Select 2	0	0	0	0	0	0	0	WSEQ_SAMPLE_RATE_DETECT_B_INDEX [8:0]									01FFh
R99 (63h)	Sample Rate Sequence Select 3	0	0	0	0	0	0	0	WSEQ_SAMPLE_RATE_DETECT_C_INDEX [8:0]									01FFh
R100 (64h)	Sample Rate Sequence Select 4	0	0	0	0	0	0	0	WSEQ_SAMPLE_RATE_DETECT_D_INDEX [8:0]									01FFh
R104 (68h)	GPIO Triggers Sequence Select 1	0	0	0	0	0	0	0	WSEQ_GP1_RISE_INDEX [8:0]									01FFh
R105 (69h)	GPIO Triggers Sequence Select 2	0	0	0	0	0	0	0	WSEQ_GP1_FALL_INDEX [8:0]									01FFh
R106 (6Ah)	GPIO Triggers Sequence Select 3	0	0	0	0	0	0	0	WSEQ_GP2_RISE_INDEX [8:0]									01FFh
R107 (6Bh)	GPIO Triggers Sequence Select 4	0	0	0	0	0	0	0	WSEQ_GP2_FALL_INDEX [8:0]									01FFh
R110 (6Eh)	Trigger Sequence Select 32	0	0	0	0	0	0	0	WSEQ_DRC1_SIG_DET_RISE_INDEX [8:0]									01FFh
R111 (6Fh)	Trigger Sequence Select 33	0	0	0	0	0	0	0	WSEQ_DRC1_SIG_DET_FALL_INDEX [8:0]									01FFh
R112 (70h)	Comfort Noise Generator	0	NOISE_GEN_RATE [3:0]				0	0	0	0	0	NOISE_GEN_ENA	NOISE_GEN_GAIN [4:0]					0000h
R144 (90h)	Haptics Control 1	0	HAP_RATE [3:0]				0	0	0	0	0	0	ONESHOT_TRIG	HAP_CTRL [1:0]		HAP_ACT	0	0000h
R145 (91h)	Haptics Control 2	0	LRA_FREQ [14:0]															7FFFh

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R146 (92h)	Haptics phase 1 intensity	0	0	0	0	0	0	0	0	PHASE1_INTENSITY [7:0]								0000h
R147 (93h)	Haptics phase 1 duration	0	0	0	0	0	0	0	PHASE1_DURATION [8:0]									0000h
R148 (94h)	Haptics phase 2 intensity	0	0	0	0	0	0	0	0	PHASE2_INTENSITY [7:0]								0000h
R149 (95h)	Haptics phase 2 duration	0	0	0	0	0	PHASE2_DURATION [10:0]											0000h
R150 (96h)	Haptics phase 3 intensity	0	0	0	0	0	0	0	0	PHASE3_INTENSITY [7:0]								0000h
R151 (97h)	Haptics phase 3 duration	0	0	0	0	0	0	0	PHASE3_DURATION [8:0]									0000h
R152 (98h)	Haptics Status	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ONESHOT_STS	0000h
R256 (100h)	Clock 32k 1	0	0	0	0	0	0	0	0	0	CLK_32K_ENA	0	0	0	0	CLK_32K_SRC [1:0]		0002h
R257 (101h)	System Clock 1	SYSCLK_FRAC	0	0	0	0	SYSCLK_FREQ [2:0]			0	SYSCLK_ENA	0	0	SYSCLK_SRC [3:0]				0504h
R258 (102h)	Sample rate 1	0	0	0	0	0	0	0	0	0	0	0	SAMPLE_RATE_1 [4:0]					0011h
R259 (103h)	Sample rate 2	0	0	0	0	0	0	0	0	0	0	0	SAMPLE_RATE_2 [4:0]					0011h
R260 (104h)	Sample rate 3	0	0	0	0	0	0	0	0	0	0	0	SAMPLE_RATE_3 [4:0]					0011h
R266 (10Ah)	Sample rate 1 status	0	0	0	0	0	0	0	0	0	0	0	SAMPLE_RATE_1_STS [4:0]					0000h
R267 (10Bh)	Sample rate 2 status	0	0	0	0	0	0	0	0	0	0	0	SAMPLE_RATE_2_STS [4:0]					0000h
R268 (10Ch)	Sample rate 3 status	0	0	0	0	0	0	0	0	0	0	0	SAMPLE_RATE_3_STS [4:0]					0000h
R274 (112h)	Async clock 1	0	0	0	0	0	ASYNC_CLK_FREQ [2:0]			0	ASYNC_CLK_ENA	0	0	ASYNC_CLK_SRC [3:0]				0305h
R275 (113h)	Async sample rate 1	0	0	0	0	0	0	0	0	0	0	0	ASYNC_SAMPLE_RATE_1 [4:0]					0011h
R276 (114h)	Async sample rate 2	0	0	0	0	0	0	0	0	0	0	0	ASYNC_SAMPLE_RATE_2 [4:0]					0011h
R283 (11Bh)	Async sample rate 1 status	0	0	0	0	0	0	0	0	0	0	0	ASYNC_SAMPLE_RATE_1_STS [4:0]					0000h
R284 (11Ch)	Async sample rate 2 status	0	0	0	0	0	0	0	0	0	0	0	ASYNC_SAMPLE_RATE_2_STS [4:0]					0000h
R329 (149h)	Output system clock	OPCLK_ENA	0	0	0	0	0	0	0	OPCLK_DIV [4:0]					OPCLK_SEL [2:0]			0000h
R330 (14Ah)	Output async clock	OPCLK_ASYNC_ENA	0	0	0	0	0	0	0	OPCLK_ASYNC_DIV [4:0]					OPCLK_ASYNC_SEL [2:0]			0000h
R338 (152h)	Rate Estimator 1	0	0	0	0	0	0	0	0	0	0	0	TRIG_ON_STARTUP	LRCLK_SRC [2:0]			RATE_EST_ENA	0000h
R339 (153h)	Rate Estimator 2	0	0	0	0	0	0	0	0	0	0	0	SAMPLE_RATE_DETECT_A [4:0]					0000h
R340 (154h)	Rate Estimator 3	0	0	0	0	0	0	0	0	0	0	0	SAMPLE_RATE_DETECT_B [4:0]					0000h
R341 (155h)	Rate Estimator 4	0	0	0	0	0	0	0	0	0	0	0	SAMPLE_RATE_DETECT_C [4:0]					0000h
R342 (156h)	Rate Estimator 5	0	0	0	0	0	0	0	0	0	0	0	SAMPLE_RATE_DETECT_D [4:0]					0000h
R369 (171h)	FLL1 Control 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FLL1_FREERUN	FLL1_ENA	0002h
R370 (172h)	FLL1 Control 2	FLL1_CTRL_UPD	0	0	0	0	0	FLL1_N [9:0]										0008h
R371 (173h)	FLL1 Control 3	FLL1_THETA [15:0]																0018h
R372 (174h)	FLL1 Control 4	FLL1_LAMBDA [15:0]																007Dh
R373 (175h)	FLL1 Control 5	0	0	0	0	FLL1_FRATIO [3:0]				0	0	0	0	FLL1_OUTDIV [2:0]			0	0006h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R374 (176h)	FLL1 Control 6	0	0	0	0	0	0	0	0	FLL1_REFCLK_DIV [1:0]		0	0	FLL1_REFCLK_SRC [3:0]				0000h
R375 (177h)	FLL1 Loop Filter Test 1	FLL1_FRC_INTEG_UPD	0	0	0	FLL1_FRC_INTEG_VAL [11:0]												0281h
R376 (178h)	FLL1 NCO Test 0	FLL1_INTEG_VALID	0	0	0	FLL1_INTEG [11:0]												0000h
R377 (179h)	FLL1 Control 7	0	0	0	0	0	0	0	0	0	0	FLL1_GAIN [3:0]				0	0	0000h
R385 (181h)	FLL1 Synchroniser 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FLL1_SYNC_ENA	0000h
R386 (182h)	FLL1 Synchroniser 2	0	0	0	0	0	0	FLL1_SYNC_N [9:0]										0000h
R387 (183h)	FLL1 Synchroniser 3	FLL1_SYNC_THETA [15:0]																0000h
R388 (184h)	FLL1 Synchroniser 4	FLL1_SYNC_LAMBDA [15:0]																0000h
R389 (185h)	FLL1 Synchroniser 5	0	0	0	0	0	FLL1_SYNC_FRATIO [2:0]			0	0	0	0	0	0	0	0	0000h
R390 (186h)	FLL1 Synchroniser 6	0	0	0	0	0	0	0	0	FLL1_SYNCCLK_DIV [1:0]		0	0	FLL1_SYNCCLK_SRC [3:0]				0000h
R391 (187h)	FLL1 Synchroniser 7	0	0	0	0	0	0	0	0	0	0	FLL1_SYNC_GAIN [3:0]				0	FLL1_SYNC_DFSAT	0001h
R393 (189h)	FLL1 Spread Spectrum	0	0	0	0	0	0	0	0	0	0	FLL1_SS_AMPL [1:0]		FLL1_SS_FREQ [1:0]		FLL1_SS_SEL [1:0]		0000h
R394 (18Ah)	FLL1 GPIO Clock	0	0	0	0	0	0	0	0	FLL1_GPCLK_DIV [6:0]							FLL1_GPCLK_ENA	000Ch
R401 (191h)	FLL2 Control 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FLL2_FREERUN	FLL2_ENA	0002h
R402 (192h)	FLL2 Control 2	FLL2_CTRL_UPD	0	0	0	0	0	FLL2_N [9:0]										0008h
R403 (193h)	FLL2 Control 3	FLL2_THETA [15:0]																0018h
R404 (194h)	FLL2 Control 4	FLL2_LAMBDA [15:0]																007Dh
R405 (195h)	FLL2 Control 5	0	0	0	0	FLL2_FRATIO [3:0]				0	0	0	0	FLL2_OUTDIV [2:0]			0	000Ch
R406 (196h)	FLL2 Control 6	0	0	0	0	0	0	0	0	FLL2_REFCLK_DIV [1:0]		0	0	FLL2_REFCLK_SRC [3:0]				0000h
R407 (197h)	FLL2 Loop Filter Test 1	FLL2_FRC_INTEG_UPD	0	0	0	FLL2_FRC_INTEG_VAL [11:0]												0000h
R408 (198h)	FLL2 NCO Test 0	FLL2_INTEG_VALID	0	0	0	FLL2_INTEG [11:0]												0000h
R409 (199h)	FLL2 Control 7	0	0	0	0	0	0	0	0	0	0	FLL2_GAIN [3:0]				0	0	0000h
R417 (1A1h)	FLL2 Synchroniser 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FLL2_SYNC_ENA	0000h
R418 (1A2h)	FLL2 Synchroniser 2	0	0	0	0	0	0	FLL2_SYNC_N [9:0]										0000h
R419 (1A3h)	FLL2 Synchroniser 3	FLL2_SYNC_THETA [15:0]																0000h
R420 (1A4h)	FLL2 Synchroniser 4	FLL2_SYNC_LAMBDA [15:0]																0000h
R421 (1A5h)	FLL2 Synchroniser 5	0	0	0	0	0	FLL2_SYNC_FRATIO [2:0]			0	0	0	0	0	0	0	0	0000h
R422 (1A6h)	FLL2 Synchroniser 6	0	0	0	0	0	0	0	0	FLL2_SYNCCLK_DIV [1:0]		0	0	FLL2_SYNCCLK_SRC [3:0]				0000h
R423 (1A7h)	FLL2 Synchroniser 7	0	0	0	0	0	0	0	0	0	0	FLL2_SYNC_GAIN [3:0]				0	FLL2_SYNC_DFSAT	0001h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R425 (1A9h)	FLL2 Spread Spectrum	0	0	0	0	0	0	0	0	0	0	FLL2_SS_AMPL [1:0]		FLL2_SS_FREQ [1:0]		FLL2_SS_SEL [1:0]		0000h
R426 (1AAh)	FLL2 GPIO Clock	0	0	0	0	0	0	0	0	FLL2_GPCLK_DIV [6:0]							FLL2_GPCLK_ENA	000Ch
R536 (218h)	Mic Bias Ctrl 1	MICB1_EXT_CAP	0	0	0	0	0	0	MICB1_LVL [3:0]				0	MICB1_RATE	MICB1_DISCH	MICB1_BYPASS	MICB1_ENA	00E6h
R537 (219h)	Mic Bias Ctrl 2	MICB2_EXT_CAP	0	0	0	0	0	0	MICB2_LVL [3:0]				0	MICB2_RATE	MICB2_DISCH	MICB2_BYPASS	MICB2_ENA	00E6h
R768 (300h)	Input Enables	0	0	0	0	0	0	0	0	0	0	0	0	IN2L_ENA	IN2R_ENA	IN1L_ENA	IN1R_ENA	0000h
R769 (301h)	Input Enables Status	0	0	0	0	0	0	0	0	0	0	0	0	IN2L_ENA_STS	IN2R_ENA_STS	IN1L_ENA_STS	IN1R_ENA_STS	0000h
R776 (308h)	Input Rate	0	IN_RATE [3:0]				0	0	0	0	0	0	0	0	0	0	0	0000h
R777 (309h)	Input Volume Ramp	0	0	0	0	0	0	0	0	0	IN_VD_RAMP [2:0]			0	IN_VI_RAMP [2:0]			0022h
R780 (30Ch)	HPF Control	0	0	0	0	0	0	0	0	0	0	0	0	0	IN_HPF_CUT [2:0]			0002h
R784 (310h)	IN1L Control	IN1L_HPF	IN1_OSR [1:0]		IN1_DMIC_SUP [1:0]		0	0	0	0	0	0	0	0	0	0	0	2000h
R785 (311h)	ADC Digital Volume 1L	0	0	0	0	0	0	IN_VU	IN1L_MUTE	IN1L_VOL [7:0]								0180h
R786 (312h)	DMIC1L Control	0	0	0	0	0	0	0	0	0	0	IN1L_DMIC_DLY [5:0]						0000h
R788 (314h)	IN1R Control	IN1R_HPF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
R789 (315h)	ADC Digital Volume 1R	0	0	0	0	0	0	IN_VU	IN1R_MUTE	IN1R_VOL [7:0]								0180h
R790 (316h)	DMIC1R Control	0	0	0	0	0	0	0	0	0	0	IN1R_DMIC_DLY [5:0]						0000h
R792 (318h)	IN2L Control	IN2L_HPF	IN2_OSR [1:0]		IN2_DMIC_SUP [1:0]		0	0	0	0	0	0	0	0	0	0	0	2000h
R793 (319h)	ADC Digital Volume 2L	0	0	0	0	0	0	IN_VU	IN2L_MUTE	IN2L_VOL [7:0]								0180h
R794 (31Ah)	DMIC2L Control	0	0	0	0	0	0	0	0	0	0	IN2L_DMIC_DLY [5:0]						0000h
R796 (31Ch)	IN2R Control	IN2R_HPF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
R797 (31Dh)	ADC Digital Volume 2R	0	0	0	0	0	0	IN_VU	IN2R_MUTE	IN2R_VOL [7:0]								0180h
R798 (31Eh)	DMIC2R Control	0	0	0	0	0	0	0	0	0	0	IN2R_DMIC_DLY [5:0]						0000h
R1024 (400h)	Output Enables 1	0	0	0	0	0	0	0	0	SPKOUTL_ENA	0	0	0	0	0	HPL_ENA	HPR_ENA	0000h
R1025 (401h)	Output Status 1	0	0	0	0	0	0	0	0	OUT4L_ENA_STS	0	0	0	0	0	0	0	0000h
R1030 (406h)	Raw Output Status 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OUT1L_ENA_STS	OUT1R_ENA_STS	0000h
R1032 (408h)	Output Rate 1	0	OUT_RATE [3:0]				0	0	0	0	0	0	0	0	0	0	0	0000h
R1033 (409h)	Output Volume Ramp	0	0	0	0	0	0	0	0	0	OUT_VD_RAMP [2:0]			0	OUT_VI_RAMP [2:0]			0022h
R1040 (410h)	Output Path Config 1L	0	0	0	OUT1_MONO	0	0	0	0	1	0	0	0	0	0	0	0	0080h
R1041 (411h)	DAC Digital Volume 1L	0	0	0	0	0	0	OUT_VU	OUT1L_MUTE	OUT1L_VOL [7:0]								0180h
R1042 (412h)	DAC Volume Limit 1L	0	0	0	0	0	0	0	0	OUT1L_VOL_LIM [7:0]								0081h
R1043 (413h)	Noise Gate Select 1L	0	0	0	0	OUT1L_NGATE_SRC [11:0]												0001h
R1045 (415h)	DAC Digital Volume 1R	0	0	0	0	0	0	OUT_VU	OUT1R_MUTE	OUT1R_VOL [7:0]								0180h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1046 (416h)	DAC Volume Limit 1R	0	0	0	0	0	0	0	0	OUT1R_VOL_LIM [7:0]								0081h
R1047 (417h)	Noise Gate Select 1R	0	0	0	0	OUT1R_NGATE_SRC [11:0]												0002h
R1065 (429h)	DAC Digital Volume 4L	0	0	0	0	0	0	OUT_VU	OUT4L_MUTE	OUT4L_VOL [7:0]								0180h
R1066 (42Ah)	Out Volume 4L	0	0	0	0	0	0	0	0	OUT4L_VOL_LIM [7:0]								0081h
R1067 (42Bh)	Noise Gate Select 4L	0	0	0	0	OUT4L_NGATE_SRC [11:0]												0040h
R1104 (450h)	DAC AEC Control 1	0	0	0	0	0	0	0	0	0	0	AEC_LOOPBACK_SRC [3:0]				AEC_ENA_STS	AEC_LOOPBACK_ENA	0000h
R1112 (458h)	Noise Gate Control	0	0	0	0	0	0	0	0	0	0	NGATE_HOLD [1:0]		NGATE_THR [2:0]			NGATE_ENA	0000h
R1184 (4A0h)	HP1 Short Circuit Ctrl	0	0	1	HP1_SC_ENA	0	1	0	0	1	0	0	0	0	0	0	0	3480h
R1280 (500h)	AIF1 BCLK Ctrl	0	0	0	0	0	0	0	0	AIF1_BCLK_INV	AIF1_BCLK_FRC	AIF1_BCLK_MSTR	AIF1_BCLK_FREQ [4:0]					000Ch
R1281 (501h)	AIF1 Tx Pin Ctrl	0	0	0	0	0	0	0	0	0	0	AIF1TX_DAT_TRI	0	1	0	0	0	0008h
R1282 (502h)	AIF1 Rx Pin Ctrl	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF1_LRCLK_INV	AIF1_LRCLK_FRC	AIF1_LRCLK_MSTR	0000h
R1283 (503h)	AIF1 Rate Ctrl	0	AIF1_RATE [3:0]				0	0	0	0	AIF1_TRI	0	0	0	0	0	0	0000h
R1284 (504h)	AIF1 Format	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF1_FMT [2:0]			0000h
R1286 (506h)	AIF1 Rx BCLK Rate	0	0	0	AIF1_BCPF [12:0]													0040h
R1287 (507h)	AIF1 Frame Ctrl 1	0	0	AIF1TX_WL [5:0]						AIF1TX_SLOT_LEN [7:0]								1818h
R1288 (508h)	AIF1 Frame Ctrl 2	0	0	AIF1RX_WL [5:0]						AIF1RX_SLOT_LEN [7:0]								1818h
R1289 (509h)	AIF1 Frame Ctrl 3	0	0	0	0	0	0	0	0	0	0	AIF1TX1_SLOT [5:0]						0000h
R1290 (50Ah)	AIF1 Frame Ctrl 4	0	0	0	0	0	0	0	0	0	0	AIF1TX2_SLOT [5:0]						0001h
R1291 (50Bh)	AIF1 Frame Ctrl 5	0	0	0	0	0	0	0	0	0	0	AIF1TX3_SLOT [5:0]						0002h
R1292 (50Ch)	AIF1 Frame Ctrl 6	0	0	0	0	0	0	0	0	0	0	AIF1TX4_SLOT [5:0]						0003h
R1293 (50Dh)	AIF1 Frame Ctrl 7	0	0	0	0	0	0	0	0	0	0	AIF1TX5_SLOT [5:0]						0004h
R1294 (50Eh)	AIF1 Frame Ctrl 8	0	0	0	0	0	0	0	0	0	0	AIF1TX6_SLOT [5:0]						0005h
R1295 (50Fh)	AIF1 Frame Ctrl 9	0	0	0	0	0	0	0	0	0	0	AIF1TX7_SLOT [5:0]						0006h
R1296 (510h)	AIF1 Frame Ctrl 10	0	0	0	0	0	0	0	0	0	0	AIF1TX8_SLOT [5:0]						0007h
R1297 (511h)	AIF1 Frame Ctrl 11	0	0	0	0	0	0	0	0	0	0	AIF1RX1_SLOT [5:0]						0000h
R1298 (512h)	AIF1 Frame Ctrl 12	0	0	0	0	0	0	0	0	0	0	AIF1RX2_SLOT [5:0]						0001h
R1299 (513h)	AIF1 Frame Ctrl 13	0	0	0	0	0	0	0	0	0	0	AIF1RX3_SLOT [5:0]						0002h
R1300 (514h)	AIF1 Frame Ctrl 14	0	0	0	0	0	0	0	0	0	0	AIF1RX4_SLOT [5:0]						0003h
R1301 (515h)	AIF1 Frame Ctrl 15	0	0	0	0	0	0	0	0	0	0	AIF1RX5_SLOT [5:0]						0004h
R1302 (516h)	AIF1 Frame Ctrl 16	0	0	0	0	0	0	0	0	0	0	AIF1RX6_SLOT [5:0]						0005h
R1303 (517h)	AIF1 Frame Ctrl 17	0	0	0	0	0	0	0	0	0	0	AIF1RX7_SLOT [5:0]						0006h
R1304 (518h)	AIF1 Frame Ctrl 18	0	0	0	0	0	0	0	0	0	0	AIF1RX8_SLOT [5:0]						0007h
R1305 (519h)	AIF1 Tx Enables	0	0	0	0	0	0	0	0	AIF1TX8_ENA	AIF1TX7_ENA	AIF1TX6_ENA	AIF1TX5_ENA	AIF1TX4_ENA	AIF1TX3_ENA	AIF1TX2_ENA	AIF1TX1_ENA	0000h
R1306 (51Ah)	AIF1 Rx Enables	0	0	0	0	0	0	0	0	AIF1RX8_ENA	AIF1RX7_ENA	AIF1RX6_ENA	AIF1RX5_ENA	AIF1RX4_ENA	AIF1RX3_ENA	AIF1RX2_ENA	AIF1RX1_ENA	0000h
R1344 (540h)	AIF2 BCLK Ctrl	0	0	0	0	0	0	0	0	AIF2_BCLK_INV	AIF2_BCLK_FRC	AIF2_BCLK_MSTR	AIF2_BCLK_FREQ [4:0]					000Ch
R1345 (541h)	AIF2 Tx Pin Ctrl	0	0	0	0	0	0	0	0	0	0	AIF2TX_DAT_TRI	0	1	0	0	0	0008h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1346 (542h)	AIF2 Rx Pin Ctrl	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF2_LRCLK_INV	AIF2_LRCLK_FRC	AIF2_LRCLK_MSTR	0000h
R1347 (543h)	AIF2 Rate Ctrl	0	AIF2_RATE [3:0]			0	0	0	0	AIF2_TRI	0	0	0	0	0	0	0	0000h
R1348 (544h)	AIF2 Format	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF2_FMT [2:0]			0000h
R1350 (546h)	AIF2 Rx BCLK Rate	0	0	0	AIF2_BCPF [12:0]													0040h
R1351 (547h)	AIF2 Frame Ctrl 1	0	0	AIF2TX_WL [5:0]						AIF2TX_SLOT_LEN [7:0]								1818h
R1352 (548h)	AIF2 Frame Ctrl 2	0	0	AIF2RX_WL [5:0]						AIF2RX_SLOT_LEN [7:0]								1818h
R1353 (549h)	AIF2 Frame Ctrl 3	0	0	0	0	0	0	0	0	0	0	AIF2TX1_SLOT [5:0]						0000h
R1354 (54Ah)	AIF2 Frame Ctrl 4	0	0	0	0	0	0	0	0	0	0	AIF2TX2_SLOT [5:0]						0001h
R1355 (54Bh)	AIF2 Frame Ctrl 5	0	0	0	0	0	0	0	0	0	0	AIF2TX3_SLOT [5:0]						0002h
R1356 (54Ch)	AIF2 Frame Ctrl 6	0	0	0	0	0	0	0	0	0	0	AIF2TX4_SLOT [5:0]						0003h
R1357 (54Dh)	AIF2 Frame Ctrl 7	0	0	0	0	0	0	0	0	0	0	AIF2TX5_SLOT [5:0]						0004h
R1358 (54Eh)	AIF2 Frame Ctrl 8	0	0	0	0	0	0	0	0	0	0	AIF2TX6_SLOT [5:0]						0005h
R1361 (551h)	AIF2 Frame Ctrl 11	0	0	0	0	0	0	0	0	0	0	AIF2RX1_SLOT [5:0]						0000h
R1362 (552h)	AIF2 Frame Ctrl 12	0	0	0	0	0	0	0	0	0	0	AIF2RX2_SLOT [5:0]						0001h
R1363 (553h)	AIF2 Frame Ctrl 13	0	0	0	0	0	0	0	0	0	0	AIF2RX3_SLOT [5:0]						0002h
R1364 (554h)	AIF2 Frame Ctrl 14	0	0	0	0	0	0	0	0	0	0	AIF2RX4_SLOT [5:0]						0003h
R1365 (555h)	AIF2 Frame Ctrl 15	0	0	0	0	0	0	0	0	0	0	AIF2RX5_SLOT [5:0]						0004h
R1366 (556h)	AIF2 Frame Ctrl 16	0	0	0	0	0	0	0	0	0	0	AIF2RX6_SLOT [5:0]						0005h
R1369 (559h)	AIF2 Tx Enables	0	0	0	0	0	0	0	0	0	0	AIF2TX6_ENA	AIF2TX5_ENA	AIF2TX4_ENA	AIF2TX3_ENA	AIF2TX2_ENA	AIF2TX1_ENA	0000h
R1370 (55Ah)	AIF2 Rx Enables	0	0	0	0	0	0	0	0	0	0	AIF2RX6_ENA	AIF2RX5_ENA	AIF2RX4_ENA	AIF2RX3_ENA	AIF2RX2_ENA	AIF2RX1_ENA	0000h
R1408 (580h)	AIF3 BCLK Ctrl	0	0	0	0	0	0	0	0	AIF3_BCLK_INV	AIF3_BCLK_FRC	AIF3_BCLK_MSTR	AIF3_BCLK_FREQ [4:0]					000Ch
R1409 (581h)	AIF3 Tx Pin Ctrl	0	0	0	0	0	0	0	0	0	0	AIF3TX_DAT_TRI	0	1	0	0	0	0008h
R1410 (582h)	AIF3 Rx Pin Ctrl	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF3_LRCLK_INV	AIF3_LRCLK_FRC	AIF3_LRCLK_MSTR	0000h
R1411 (583h)	AIF3 Rate Ctrl	0	AIF3_RATE [3:0]			0	0	0	0	AIF3_TRI	0	0	0	0	0	0	0	0000h
R1412 (584h)	AIF3 Format	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF3_FMT [2:0]			0000h
R1414 (586h)	AIF3 Rx BCLK Rate	0	0	0	AIF3_BCPF [12:0]													0040h
R1415 (587h)	AIF3 Frame Ctrl 1	0	0	AIF3TX_WL [5:0]						AIF3TX_SLOT_LEN [7:0]								1818h
R1416 (588h)	AIF3 Frame Ctrl 2	0	0	AIF3RX_WL [5:0]						AIF3RX_SLOT_LEN [7:0]								1818h
R1417 (589h)	AIF3 Frame Ctrl 3	0	0	0	0	0	0	0	0	0	0	AIF3TX1_SLOT [5:0]						0000h
R1418 (58Ah)	AIF3 Frame Ctrl 4	0	0	0	0	0	0	0	0	0	0	AIF3TX2_SLOT [5:0]						0001h
R1425 (591h)	AIF3 Frame Ctrl 11	0	0	0	0	0	0	0	0	0	0	AIF3RX1_SLOT [5:0]						0000h
R1426 (592h)	AIF3 Frame Ctrl 12	0	0	0	0	0	0	0	0	0	0	AIF3RX2_SLOT [5:0]						0001h
R1433 (599h)	AIF3 Tx Enables	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF3TX2_ENA	AIF3TX1_ENA	0000h
R1434 (59Ah)	AIF3 Rx Enables	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AIF3RX2_ENA	AIF3RX1_ENA	0000h
R1600 (640h)	PWM1MIX Input 1 Source	PWM1MIX_STS1	0	0	0	0	0	0	0	PWM1MIX_SRC1 [7:0]								0000h
R1601 (641h)	PWM1MIX Input 1 Volume	0	0	0	0	0	0	0	0	PWM1MIX_VOL1 [6:0]							0	0080h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1602 (642h)	PWM1MIX Input 2 Source	PWM1MIX_STS2	0	0	0	0	0	0	0	PWM1MIX_SRC2 [7:0]								0000h
R1603 (643h)	PWM1MIX Input 2 Volume	0	0	0	0	0	0	0	0	PWM1MIX_VOL2 [6:0]							0	0080h
R1604 (644h)	PWM1MIX Input 3 Source	PWM1MIX_STS3	0	0	0	0	0	0	0	PWM1MIX_SRC3 [7:0]								0000h
R1605 (645h)	PWM1MIX Input 3 Volume	0	0	0	0	0	0	0	0	PWM1MIX_VOL3 [6:0]							0	0080h
R1606 (646h)	PWM1MIX Input 4 Source	PWM1MIX_STS4	0	0	0	0	0	0	0	PWM1MIX_SRC4 [7:0]								0000h
R1607 (647h)	PWM1MIX Input 4 Volume	0	0	0	0	0	0	0	0	PWM1MIX_VOL4 [6:0]							0	0080h
R1608 (648h)	PWM2MIX Input 1 Source	PWM2MIX_STS1	0	0	0	0	0	0	0	PWM2MIX_SRC1 [7:0]								0000h
R1609 (649h)	PWM2MIX Input 1 Volume	0	0	0	0	0	0	0	0	PWM2MIX_VOL1 [6:0]							0	0080h
R1610 (64Ah)	PWM2MIX Input 2 Source	PWM2MIX_STS2	0	0	0	0	0	0	0	PWM2MIX_SRC2 [7:0]								0000h
R1611 (64Bh)	PWM2MIX Input 2 Volume	0	0	0	0	0	0	0	0	PWM2MIX_VOL2 [6:0]							0	0080h
R1612 (64Ch)	PWM2MIX Input 3 Source	PWM2MIX_STS3	0	0	0	0	0	0	0	PWM2MIX_SRC3 [7:0]								0000h
R1613 (64Dh)	PWM2MIX Input 3 Volume	0	0	0	0	0	0	0	0	PWM2MIX_VOL3 [6:0]							0	0080h
R1614 (64Eh)	PWM2MIX Input 4 Source	PWM2MIX_STS4	0	0	0	0	0	0	0	PWM2MIX_SRC4 [7:0]								0000h
R1615 (64Fh)	PWM2MIX Input 4 Volume	0	0	0	0	0	0	0	0	PWM2MIX_VOL4 [6:0]							0	0080h
R1664 (680h)	OUT1LMIX Input 1 Source	OUT1LMIX_STS1	0	0	0	0	0	0	0	OUT1LMIX_SRC1 [7:0]								0000h
R1665 (681h)	OUT1LMIX Input 1 Volume	0	0	0	0	0	0	0	0	OUT1LMIX_VOL1 [6:0]							0	0080h
R1666 (682h)	OUT1LMIX Input 2 Source	OUT1LMIX_STS2	0	0	0	0	0	0	0	OUT1LMIX_SRC2 [7:0]								0000h
R1667 (683h)	OUT1LMIX Input 2 Volume	0	0	0	0	0	0	0	0	OUT1LMIX_VOL2 [6:0]							0	0080h
R1668 (684h)	OUT1LMIX Input 3 Source	OUT1LMIX_STS3	0	0	0	0	0	0	0	OUT1LMIX_SRC3 [7:0]								0000h
R1669 (685h)	OUT1LMIX Input 3 Volume	0	0	0	0	0	0	0	0	OUT1LMIX_VOL3 [6:0]							0	0080h
R1670 (686h)	OUT1LMIX Input 4 Source	OUT1LMIX_STS4	0	0	0	0	0	0	0	OUT1LMIX_SRC4 [7:0]								0000h
R1671 (687h)	OUT1LMIX Input 4 Volume	0	0	0	0	0	0	0	0	OUT1LMIX_VOL4 [6:0]							0	0080h
R1672 (688h)	OUT1RMIX Input 1 Source	OUT1RMIX_STS1	0	0	0	0	0	0	0	OUT1RMIX_SRC1 [7:0]								0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1673 (689h)	OUT1RMIX Input 1 Volume	0	0	0	0	0	0	0	0	OUT1RMIX_VOL1 [6:0]							0	0080h
R1674 (68Ah)	OUT1RMIX Input 2 Source	OUT1RMIX_STS2	0	0	0	0	0	0	0	OUT1RMIX_SRC2 [7:0]								0000h
R1675 (68Bh)	OUT1RMIX Input 2 Volume	0	0	0	0	0	0	0	0	OUT1RMIX_VOL2 [6:0]							0	0080h
R1676 (68Ch)	OUT1RMIX Input 3 Source	OUT1RMIX_STS3	0	0	0	0	0	0	0	OUT1RMIX_SRC3 [7:0]								0000h
R1677 (68Dh)	OUT1RMIX Input 3 Volume	0	0	0	0	0	0	0	0	OUT1RMIX_VOL3 [6:0]							0	0080h
R1678 (68Eh)	OUT1RMIX Input 4 Source	OUT1RMIX_STS4	0	0	0	0	0	0	0	OUT1RMIX_SRC4 [7:0]								0000h
R1679 (68Fh)	OUT1RMIX Input 4 Volume	0	0	0	0	0	0	0	0	OUT1RMIX_VOL4 [6:0]							0	0080h
R1712 (6B0h)	OUT4LMIX Input 1 Source	OUT4LMIX_STS1	0	0	0	0	0	0	0	OUT4LMIX_SRC1 [7:0]								0000h
R1713 (6B1h)	OUT4LMIX Input 1 Volume	0	0	0	0	0	0	0	0	OUT4LMIX_VOL1 [6:0]							0	0080h
R1714 (6B2h)	OUT4LMIX Input 2 Source	OUT4LMIX_STS2	0	0	0	0	0	0	0	OUT4LMIX_SRC2 [7:0]								0000h
R1715 (6B3h)	OUT4LMIX Input 2 Volume	0	0	0	0	0	0	0	0	OUT4LMIX_VOL2 [6:0]							0	0080h
R1716 (6B4h)	OUT4LMIX Input 3 Source	OUT4LMIX_STS3	0	0	0	0	0	0	0	OUT4LMIX_SRC3 [7:0]								0000h
R1717 (6B5h)	OUT4LMIX Input 3 Volume	0	0	0	0	0	0	0	0	OUT4LMIX_VOL3 [6:0]							0	0080h
R1718 (6B6h)	OUT4LMIX Input 4 Source	OUT4LMIX_STS4	0	0	0	0	0	0	0	OUT4LMIX_SRC4 [7:0]								0000h
R1719 (6B7h)	OUT4LMIX Input 4 Volume	0	0	0	0	0	0	0	0	OUT4LMIX_VOL4 [6:0]							0	0080h
R1792 (700h)	AIF1TX1MIX Input 1 Source	AIF1TX1MIX_STS1	0	0	0	0	0	0	0	AIF1TX1MIX_SRC1 [7:0]								0000h
R1793 (701h)	AIF1TX1MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF1TX1MIX_VOL1 [6:0]							0	0080h
R1794 (702h)	AIF1TX1MIX Input 2 Source	AIF1TX1MIX_STS2	0	0	0	0	0	0	0	AIF1TX1MIX_SRC2 [7:0]								0000h
R1795 (703h)	AIF1TX1MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF1TX1MIX_VOL2 [6:0]							0	0080h
R1796 (704h)	AIF1TX1MIX Input 3 Source	AIF1TX1MIX_STS3	0	0	0	0	0	0	0	AIF1TX1MIX_SRC3 [7:0]								0000h
R1797 (705h)	AIF1TX1MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF1TX1MIX_VOL3 [6:0]							0	0080h
R1798 (706h)	AIF1TX1MIX Input 4 Source	AIF1TX1MIX_STS4	0	0	0	0	0	0	0	AIF1TX1MIX_SRC4 [7:0]								0000h
R1799 (707h)	AIF1TX1MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF1TX1MIX_VOL4 [6:0]							0	0080h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1800 (708h)	AIF1TX2MIX Input 1 Source	AIF1TX2MIX_STS1	0	0	0	0	0	0	0	AIF1TX2MIX_SRC1 [7:0]								0000h
R1801 (709h)	AIF1TX2MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF1TX2MIX_VOL1 [6:0]							0	0080h
R1802 (70Ah)	AIF1TX2MIX Input 2 Source	AIF1TX2MIX_STS2	0	0	0	0	0	0	0	AIF1TX2MIX_SRC2 [7:0]								0000h
R1803 (70Bh)	AIF1TX2MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF1TX2MIX_VOL2 [6:0]							0	0080h
R1804 (70Ch)	AIF1TX2MIX Input 3 Source	AIF1TX2MIX_STS3	0	0	0	0	0	0	0	AIF1TX2MIX_SRC3 [7:0]								0000h
R1805 (70Dh)	AIF1TX2MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF1TX2MIX_VOL3 [6:0]							0	0080h
R1806 (70Eh)	AIF1TX2MIX Input 4 Source	AIF1TX2MIX_STS4	0	0	0	0	0	0	0	AIF1TX2MIX_SRC4 [7:0]								0000h
R1807 (70Fh)	AIF1TX2MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF1TX2MIX_VOL4 [6:0]							0	0080h
R1808 (710h)	AIF1TX3MIX Input 1 Source	AIF1TX3MIX_STS1	0	0	0	0	0	0	0	AIF1TX3MIX_SRC1 [7:0]								0000h
R1809 (711h)	AIF1TX3MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF1TX3MIX_VOL1 [6:0]							0	0080h
R1810 (712h)	AIF1TX3MIX Input 2 Source	AIF1TX3MIX_STS2	0	0	0	0	0	0	0	AIF1TX3MIX_SRC2 [7:0]								0000h
R1811 (713h)	AIF1TX3MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF1TX3MIX_VOL2 [6:0]							0	0080h
R1812 (714h)	AIF1TX3MIX Input 3 Source	AIF1TX3MIX_STS3	0	0	0	0	0	0	0	AIF1TX3MIX_SRC3 [7:0]								0000h
R1813 (715h)	AIF1TX3MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF1TX3MIX_VOL3 [6:0]							0	0080h
R1814 (716h)	AIF1TX3MIX Input 4 Source	AIF1TX3MIX_STS4	0	0	0	0	0	0	0	AIF1TX3MIX_SRC4 [7:0]								0000h
R1815 (717h)	AIF1TX3MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF1TX3MIX_VOL4 [6:0]							0	0080h
R1816 (718h)	AIF1TX4MIX Input 1 Source	AIF1TX4MIX_STS1	0	0	0	0	0	0	0	AIF1TX4MIX_SRC1 [7:0]								0000h
R1817 (719h)	AIF1TX4MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF1TX4MIX_VOL1 [6:0]							0	0080h
R1818 (71Ah)	AIF1TX4MIX Input 2 Source	AIF1TX4MIX_STS2	0	0	0	0	0	0	0	AIF1TX4MIX_SRC2 [7:0]								0000h
R1819 (71Bh)	AIF1TX4MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF1TX4MIX_VOL2 [6:0]							0	0080h
R1820 (71Ch)	AIF1TX4MIX Input 3 Source	AIF1TX4MIX_STS3	0	0	0	0	0	0	0	AIF1TX4MIX_SRC3 [7:0]								0000h
R1821 (71Dh)	AIF1TX4MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF1TX4MIX_VOL3 [6:0]							0	0080h
R1822 (71Eh)	AIF1TX4MIX Input 4 Source	AIF1TX4MIX_STS4	0	0	0	0	0	0	0	AIF1TX4MIX_SRC4 [7:0]								0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1823 (71Fh)	AIF1TX4MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF1TX4MIX_VOL4 [6:0]							0	0080h
R1824 (720h)	AIF1TX5MIX Input 1 Source	AIF1TX5MIX_STS1	0	0	0	0	0	0	0	AIF1TX5MIX_SRC1 [7:0]								0000h
R1825 (721h)	AIF1TX5MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF1TX5MIX_VOL1 [6:0]							0	0080h
R1826 (722h)	AIF1TX5MIX Input 2 Source	AIF1TX5MIX_STS2	0	0	0	0	0	0	0	AIF1TX5MIX_SRC2 [7:0]								0000h
R1827 (723h)	AIF1TX5MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF1TX5MIX_VOL2 [6:0]							0	0080h
R1828 (724h)	AIF1TX5MIX Input 3 Source	AIF1TX5MIX_STS3	0	0	0	0	0	0	0	AIF1TX5MIX_SRC3 [7:0]								0000h
R1829 (725h)	AIF1TX5MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF1TX5MIX_VOL3 [6:0]							0	0080h
R1830 (726h)	AIF1TX5MIX Input 4 Source	AIF1TX5MIX_STS4	0	0	0	0	0	0	0	AIF1TX5MIX_SRC4 [7:0]								0000h
R1831 (727h)	AIF1TX5MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF1TX5MIX_VOL4 [6:0]							0	0080h
R1832 (728h)	AIF1TX6MIX Input 1 Source	AIF1TX6MIX_STS1	0	0	0	0	0	0	0	AIF1TX6MIX_SRC1 [7:0]								0000h
R1833 (729h)	AIF1TX6MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF1TX6MIX_VOL1 [6:0]							0	0080h
R1834 (72Ah)	AIF1TX6MIX Input 2 Source	AIF1TX6MIX_STS2	0	0	0	0	0	0	0	AIF1TX6MIX_SRC2 [7:0]								0000h
R1835 (72Bh)	AIF1TX6MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF1TX6MIX_VOL2 [6:0]							0	0080h
R1836 (72Ch)	AIF1TX6MIX Input 3 Source	AIF1TX6MIX_STS3	0	0	0	0	0	0	0	AIF1TX6MIX_SRC3 [7:0]								0000h
R1837 (72Dh)	AIF1TX6MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF1TX6MIX_VOL3 [6:0]							0	0080h
R1838 (72Eh)	AIF1TX6MIX Input 4 Source	AIF1TX6MIX_STS4	0	0	0	0	0	0	0	AIF1TX6MIX_SRC4 [7:0]								0000h
R1839 (72Fh)	AIF1TX6MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF1TX6MIX_VOL4 [6:0]							0	0080h
R1840 (730h)	AIF1TX7MIX Input 1 Source	AIF1TX7MIX_STS1	0	0	0	0	0	0	0	AIF1TX7MIX_SRC1 [7:0]								0000h
R1841 (731h)	AIF1TX7MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF1TX7MIX_VOL1 [6:0]							0	0080h
R1842 (732h)	AIF1TX7MIX Input 2 Source	AIF1TX7MIX_STS2	0	0	0	0	0	0	0	AIF1TX7MIX_SRC2 [7:0]								0000h
R1843 (733h)	AIF1TX7MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF1TX7MIX_VOL2 [6:0]							0	0080h
R1844 (734h)	AIF1TX7MIX Input 3 Source	AIF1TX7MIX_STS3	0	0	0	0	0	0	0	AIF1TX7MIX_SRC3 [7:0]								0000h
R1845 (735h)	AIF1TX7MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF1TX7MIX_VOL3 [6:0]							0	0080h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1846 (736h)	AIF1TX7MIX Input 4 Source	AIF1TX7MIX_STS4	0	0	0	0	0	0	0	AIF1TX7MIX_SRC4 [7:0]								0000h
R1847 (737h)	AIF1TX7MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF1TX7MIX_VOL4 [6:0]							0	0080h
R1848 (738h)	AIF1TX8MIX Input 1 Source	AIF1TX8MIX_STS1	0	0	0	0	0	0	0	AIF1TX8MIX_SRC1 [7:0]								0000h
R1849 (739h)	AIF1TX8MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF1TX8MIX_VOL1 [6:0]							0	0080h
R1850 (73Ah)	AIF1TX8MIX Input 2 Source	AIF1TX8MIX_STS2	0	0	0	0	0	0	0	AIF1TX8MIX_SRC2 [7:0]								0000h
R1851 (73Bh)	AIF1TX8MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF1TX8MIX_VOL2 [6:0]							0	0080h
R1852 (73Ch)	AIF1TX8MIX Input 3 Source	AIF1TX8MIX_STS3	0	0	0	0	0	0	0	AIF1TX8MIX_SRC3 [7:0]								0000h
R1853 (73Dh)	AIF1TX8MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF1TX8MIX_VOL3 [6:0]							0	0080h
R1854 (73Eh)	AIF1TX8MIX Input 4 Source	AIF1TX8MIX_STS4	0	0	0	0	0	0	0	AIF1TX8MIX_SRC4 [7:0]								0000h
R1855 (73Fh)	AIF1TX8MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF1TX8MIX_VOL4 [6:0]							0	0080h
R1856 (740h)	AIF2TX1MIX Input 1 Source	AIF2TX1MIX_STS1	0	0	0	0	0	0	0	AIF2TX1MIX_SRC1 [7:0]								0000h
R1857 (741h)	AIF2TX1MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF2TX1MIX_VOL1 [6:0]							0	0080h
R1858 (742h)	AIF2TX1MIX Input 2 Source	AIF2TX1MIX_STS2	0	0	0	0	0	0	0	AIF2TX1MIX_SRC2 [7:0]								0000h
R1859 (743h)	AIF2TX1MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF2TX1MIX_VOL2 [6:0]							0	0080h
R1860 (744h)	AIF2TX1MIX Input 3 Source	AIF2TX1MIX_STS3	0	0	0	0	0	0	0	AIF2TX1MIX_SRC3 [7:0]								0000h
R1861 (745h)	AIF2TX1MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF2TX1MIX_VOL3 [6:0]							0	0080h
R1862 (746h)	AIF2TX1MIX Input 4 Source	AIF2TX1MIX_STS4	0	0	0	0	0	0	0	AIF2TX1MIX_SRC4 [7:0]								0000h
R1863 (747h)	AIF2TX1MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF2TX1MIX_VOL4 [6:0]							0	0080h
R1864 (748h)	AIF2TX2MIX Input 1 Source	AIF2TX2MIX_STS1	0	0	0	0	0	0	0	AIF2TX2MIX_SRC1 [7:0]								0000h
R1865 (749h)	AIF2TX2MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF2TX2MIX_VOL1 [6:0]							0	0080h
R1866 (74Ah)	AIF2TX2MIX Input 2 Source	AIF2TX2MIX_STS2	0	0	0	0	0	0	0	AIF2TX2MIX_SRC2 [7:0]								0000h
R1867 (74Bh)	AIF2TX2MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF2TX2MIX_VOL2 [6:0]							0	0080h
R1868 (74Ch)	AIF2TX2MIX Input 3 Source	AIF2TX2MIX_STS3	0	0	0	0	0	0	0	AIF2TX2MIX_SRC3 [7:0]								0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1869 (74Dh)	AIF2TX2MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF2TX2MIX_VOL3 [6:0]							0	0080h
R1870 (74Eh)	AIF2TX2MIX Input 4 Source	AIF2TX2MIX_STS4	0	0	0	0	0	0	0	AIF2TX2MIX_SRC4 [7:0]								0000h
R1871 (74Fh)	AIF2TX2MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF2TX2MIX_VOL4 [6:0]							0	0080h
R1872 (750h)	AIF2TX3MIX Input 1 Source	AIF2TX3MIX_STS1	0	0	0	0	0	0	0	AIF2TX3MIX_SRC1 [7:0]								0000h
R1873 (751h)	AIF2TX3MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF2TX3MIX_VOL1 [6:0]							0	0080h
R1874 (752h)	AIF2TX3MIX Input 2 Source	AIF2TX3MIX_STS2	0	0	0	0	0	0	0	AIF2TX3MIX_SRC2 [7:0]								0000h
R1875 (753h)	AIF2TX3MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF2TX3MIX_VOL2 [6:0]							0	0080h
R1876 (754h)	AIF2TX3MIX Input 3 Source	AIF2TX3MIX_STS3	0	0	0	0	0	0	0	AIF2TX3MIX_SRC3 [7:0]								0000h
R1877 (755h)	AIF2TX3MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF2TX3MIX_VOL3 [6:0]							0	0080h
R1878 (756h)	AIF2TX3MIX Input 4 Source	AIF2TX3MIX_STS4	0	0	0	0	0	0	0	AIF2TX3MIX_SRC4 [7:0]								0000h
R1879 (757h)	AIF2TX3MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF2TX3MIX_VOL4 [6:0]							0	0080h
R1880 (758h)	AIF2TX4MIX Input 1 Source	AIF2TX4MIX_STS1	0	0	0	0	0	0	0	AIF2TX4MIX_SRC1 [7:0]								0000h
R1881 (759h)	AIF2TX4MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF2TX4MIX_VOL1 [6:0]							0	0080h
R1882 (75Ah)	AIF2TX4MIX Input 2 Source	AIF2TX4MIX_STS2	0	0	0	0	0	0	0	AIF2TX4MIX_SRC2 [7:0]								0000h
R1883 (75Bh)	AIF2TX4MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF2TX4MIX_VOL2 [6:0]							0	0080h
R1884 (75Ch)	AIF2TX4MIX Input 3 Source	AIF2TX4MIX_STS3	0	0	0	0	0	0	0	AIF2TX4MIX_SRC3 [7:0]								0000h
R1885 (75Dh)	AIF2TX4MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF2TX4MIX_VOL3 [6:0]							0	0080h
R1886 (75Eh)	AIF2TX4MIX Input 4 Source	AIF2TX4MIX_STS4	0	0	0	0	0	0	0	AIF2TX4MIX_SRC4 [7:0]								0000h
R1887 (75Fh)	AIF2TX4MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF2TX4MIX_VOL4 [6:0]							0	0080h
R1888 (760h)	AIF2TX5MIX Input 1 Source	AIF2TX5MIX_STS1	0	0	0	0	0	0	0	AIF2TX5MIX_SRC1 [7:0]								0000h
R1889 (761h)	AIF2TX5MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF2TX5MIX_VOL1 [6:0]							0	0080h
R1890 (762h)	AIF2TX5MIX Input 2 Source	AIF2TX5MIX_STS2	0	0	0	0	0	0	0	AIF2TX5MIX_SRC2 [7:0]								0000h
R1891 (763h)	AIF2TX5MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF2TX5MIX_VOL2 [6:0]							0	0080h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1892 (764h)	AIF2TX5MIX Input 3 Source	AIF2TX5MIX_STS3	0	0	0	0	0	0	0	AIF2TX5MIX_SRC3 [7:0]								0000h
R1893 (765h)	AIF2TX5MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF2TX5MIX_VOL3 [6:0]							0	0080h
R1894 (766h)	AIF2TX5MIX Input 4 Source	AIF2TX5MIX_STS4	0	0	0	0	0	0	0	AIF2TX5MIX_SRC4 [7:0]								0000h
R1895 (767h)	AIF2TX5MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF2TX5MIX_VOL4 [6:0]							0	0080h
R1896 (768h)	AIF2TX6MIX Input 1 Source	AIF2TX6MIX_STS1	0	0	0	0	0	0	0	AIF2TX6MIX_SRC1 [7:0]								0000h
R1897 (769h)	AIF2TX6MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF2TX6MIX_VOL1 [6:0]							0	0080h
R1898 (76Ah)	AIF2TX6MIX Input 2 Source	AIF2TX6MIX_STS2	0	0	0	0	0	0	0	AIF2TX6MIX_SRC2 [7:0]								0000h
R1899 (76Bh)	AIF2TX6MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF2TX6MIX_VOL2 [6:0]							0	0080h
R1900 (76Ch)	AIF2TX6MIX Input 3 Source	AIF2TX6MIX_STS3	0	0	0	0	0	0	0	AIF2TX6MIX_SRC3 [7:0]								0000h
R1901 (76Dh)	AIF2TX6MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF2TX6MIX_VOL3 [6:0]							0	0080h
R1902 (76Eh)	AIF2TX6MIX Input 4 Source	AIF2TX6MIX_STS4	0	0	0	0	0	0	0	AIF2TX6MIX_SRC4 [7:0]								0000h
R1903 (76Fh)	AIF2TX6MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF2TX6MIX_VOL4 [6:0]							0	0080h
R1920 (780h)	AIF3TX1MIX Input 1 Source	AIF3TX1MIX_STS1	0	0	0	0	0	0	0	AIF3TX1MIX_SRC1 [7:0]								0000h
R1921 (781h)	AIF3TX1MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF3TX1MIX_VOL1 [6:0]							0	0080h
R1922 (782h)	AIF3TX1MIX Input 2 Source	AIF3TX1MIX_STS2	0	0	0	0	0	0	0	AIF3TX1MIX_SRC2 [7:0]								0000h
R1923 (783h)	AIF3TX1MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF3TX1MIX_VOL2 [6:0]							0	0080h
R1924 (784h)	AIF3TX1MIX Input 3 Source	AIF3TX1MIX_STS3	0	0	0	0	0	0	0	AIF3TX1MIX_SRC3 [7:0]								0000h
R1925 (785h)	AIF3TX1MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF3TX1MIX_VOL3 [6:0]							0	0080h
R1926 (786h)	AIF3TX1MIX Input 4 Source	AIF3TX1MIX_STS4	0	0	0	0	0	0	0	AIF3TX1MIX_SRC4 [7:0]								0000h
R1927 (787h)	AIF3TX1MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF3TX1MIX_VOL4 [6:0]							0	0080h
R1928 (788h)	AIF3TX2MIX Input 1 Source	AIF3TX2MIX_STS1	0	0	0	0	0	0	0	AIF3TX2MIX_SRC1 [7:0]								0000h
R1929 (789h)	AIF3TX2MIX Input 1 Volume	0	0	0	0	0	0	0	0	AIF3TX2MIX_VOL1 [6:0]							0	0080h
R1930 (78Ah)	AIF3TX2MIX Input 2 Source	AIF3TX2MIX_STS2	0	0	0	0	0	0	0	AIF3TX2MIX_SRC2 [7:0]								0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R1931 (78Bh)	AIF3TX2MIX Input 2 Volume	0	0	0	0	0	0	0	0	AIF3TX2MIX_VOL2 [6:0]							0	0080h
R1932 (78Ch)	AIF3TX2MIX Input 3 Source	AIF3TX2MIX_STS3	0	0	0	0	0	0	0	AIF3TX2MIX_SRC3 [7:0]								0000h
R1933 (78Dh)	AIF3TX2MIX Input 3 Volume	0	0	0	0	0	0	0	0	AIF3TX2MIX_VOL3 [6:0]							0	0080h
R1934 (78Eh)	AIF3TX2MIX Input 4 Source	AIF3TX2MIX_STS4	0	0	0	0	0	0	0	AIF3TX2MIX_SRC4 [7:0]								0000h
R1935 (78Fh)	AIF3TX2MIX Input 4 Volume	0	0	0	0	0	0	0	0	AIF3TX2MIX_VOL4 [6:0]							0	0080h
R2176 (880h)	EQ1MIX Input 1 Source	EQ1MIX_STS1	0	0	0	0	0	0	0	EQ1MIX_SRC1 [7:0]								0000h
R2177 (881h)	EQ1MIX Input 1 Volume	0	0	0	0	0	0	0	0	EQ1MIX_VOL1 [6:0]							0	0080h
R2178 (882h)	EQ1MIX Input 2 Source	EQ1MIX_STS2	0	0	0	0	0	0	0	EQ1MIX_SRC2 [7:0]								0000h
R2179 (883h)	EQ1MIX Input 2 Volume	0	0	0	0	0	0	0	0	EQ1MIX_VOL2 [6:0]							0	0080h
R2180 (884h)	EQ1MIX Input 3 Source	EQ1MIX_STS3	0	0	0	0	0	0	0	EQ1MIX_SRC3 [7:0]								0000h
R2181 (885h)	EQ1MIX Input 3 Volume	0	0	0	0	0	0	0	0	EQ1MIX_VOL3 [6:0]							0	0080h
R2182 (886h)	EQ1MIX Input 4 Source	EQ1MIX_STS4	0	0	0	0	0	0	0	EQ1MIX_SRC4 [7:0]								0000h
R2183 (887h)	EQ1MIX Input 4 Volume	0	0	0	0	0	0	0	0	EQ1MIX_VOL4 [6:0]							0	0080h
R2184 (888h)	EQ2MIX Input 1 Source	EQ2MIX_STS1	0	0	0	0	0	0	0	EQ2MIX_SRC1 [7:0]								0000h
R2185 (889h)	EQ2MIX Input 1 Volume	0	0	0	0	0	0	0	0	EQ2MIX_VOL1 [6:0]							0	0080h
R2186 (88Ah)	EQ2MIX Input 2 Source	EQ2MIX_STS2	0	0	0	0	0	0	0	EQ2MIX_SRC2 [7:0]								0000h
R2187 (88Bh)	EQ2MIX Input 2 Volume	0	0	0	0	0	0	0	0	EQ2MIX_VOL2 [6:0]							0	0080h
R2188 (88Ch)	EQ2MIX Input 3 Source	EQ2MIX_STS3	0	0	0	0	0	0	0	EQ2MIX_SRC3 [7:0]								0000h
R2189 (88Dh)	EQ2MIX Input 3 Volume	0	0	0	0	0	0	0	0	EQ2MIX_VOL3 [6:0]							0	0080h
R2190 (88Eh)	EQ2MIX Input 4 Source	EQ2MIX_STS4	0	0	0	0	0	0	0	EQ2MIX_SRC4 [7:0]								0000h
R2191 (88Fh)	EQ2MIX Input 4 Volume	0	0	0	0	0	0	0	0	EQ2MIX_VOL4 [6:0]							0	0080h
R2240 (8C0h)	DRC1LMIX Input 1 Source	DRC1LMIX_STS1	0	0	0	0	0	0	0	DRC1LMIX_SRC1 [7:0]								0000h
R2241 (8C1h)	DRC1LMIX Input 1 Volume	0	0	0	0	0	0	0	0	DRC1LMIX_VOL1 [6:0]							0	0080h
R2242 (8C2h)	DRC1LMIX Input 2 Source	DRC1LMIX_STS2	0	0	0	0	0	0	0	DRC1LMIX_SRC2 [7:0]								0000h
R2243 (8C3h)	DRC1LMIX Input 2 Volume	0	0	0	0	0	0	0	0	DRC1LMIX_VOL2 [6:0]							0	0080h
R2244 (8C4h)	DRC1LMIX Input 3 Source	DRC1LMIX_STS3	0	0	0	0	0	0	0	DRC1LMIX_SRC3 [7:0]								0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R2245 (8C5h)	DRC1LMIX Input 3 Volume	0	0	0	0	0	0	0	0	DRC1LMIX_VOL3 [6:0]							0	0080h
R2246 (8C6h)	DRC1LMIX Input 4 Source	DRC1LMIX_STS4	0	0	0	0	0	0	0	DRC1LMIX_SRC4 [7:0]								0000h
R2247 (8C7h)	DRC1LMIX Input 4 Volume	0	0	0	0	0	0	0	0	DRC1LMIX_VOL4 [6:0]							0	0080h
R2248 (8C8h)	DRC1RMIX Input 1 Source	DRC1RMIX_STS1	0	0	0	0	0	0	0	DRC1RMIX_SRC1 [7:0]								0000h
R2249 (8C9h)	DRC1RMIX Input 1 Volume	0	0	0	0	0	0	0	0	DRC1RMIX_VOL1 [6:0]							0	0080h
R2250 (8CAh)	DRC1RMIX Input 2 Source	DRC1RMIX_STS2	0	0	0	0	0	0	0	DRC1RMIX_SRC2 [7:0]								0000h
R2251 (8CBh)	DRC1RMIX Input 2 Volume	0	0	0	0	0	0	0	0	DRC1RMIX_VOL2 [6:0]							0	0080h
R2252 (8CCh)	DRC1RMIX Input 3 Source	DRC1RMIX_STS3	0	0	0	0	0	0	0	DRC1RMIX_SRC3 [7:0]								0000h
R2253 (8CDh)	DRC1RMIX Input 3 Volume	0	0	0	0	0	0	0	0	DRC1RMIX_VOL3 [6:0]							0	0080h
R2254 (8CEh)	DRC1RMIX Input 4 Source	DRC1RMIX_STS4	0	0	0	0	0	0	0	DRC1RMIX_SRC4 [7:0]								0000h
R2255 (8CFh)	DRC1RMIX Input 4 Volume	0	0	0	0	0	0	0	0	DRC1RMIX_VOL4 [6:0]							0	0080h
R2256 (8D0h)	DRC2LMIX Input 1 Source	DRC2LMIX_STS1	0	0	0	0	0	0	0	DRC2LMIX_SRC1 [7:0]								0000h
R2257 (8D1h)	DRC2LMIX Input 1 Volume	0	0	0	0	0	0	0	0	DRC2LMIX_VOL1 [6:0]							0	0080h
R2258 (8D2h)	DRC2LMIX Input 2 Source	DRC2LMIX_STS2	0	0	0	0	0	0	0	DRC2LMIX_SRC2 [7:0]								0000h
R2259 (8D3h)	DRC2LMIX Input 2 Volume	0	0	0	0	0	0	0	0	DRC2LMIX_VOL2 [6:0]							0	0080h
R2260 (8D4h)	DRC2LMIX Input 3 Source	DRC2LMIX_STS3	0	0	0	0	0	0	0	DRC2LMIX_SRC3 [7:0]								0000h
R2261 (8D5h)	DRC2LMIX Input 3 Volume	0	0	0	0	0	0	0	0	DRC2LMIX_VOL3 [6:0]							0	0080h
R2262 (8D6h)	DRC2LMIX Input 4 Source	DRC2LMIX_STS4	0	0	0	0	0	0	0	DRC2LMIX_SRC4 [7:0]								0000h
R2263 (8D7h)	DRC2LMIX Input 4 Volume	0	0	0	0	0	0	0	0	DRC2LMIX_VOL4 [6:0]							0	0080h
R2264 (8D8h)	DRC2RMIX Input 1 Source	DRC2RMIX_STS1	0	0	0	0	0	0	0	DRC2RMIX_SRC1 [7:0]								0000h
R2265 (8D9h)	DRC2RMIX Input 1 Volume	0	0	0	0	0	0	0	0	DRC2RMIX_VOL1 [6:0]							0	0080h
R2266 (8DAh)	DRC2RMIX Input 2 Source	DRC2RMIX_STS2	0	0	0	0	0	0	0	DRC2RMIX_SRC2 [7:0]								0000h
R2267 (8DBh)	DRC2RMIX Input 2 Volume	0	0	0	0	0	0	0	0	DRC2RMIX_VOL2 [6:0]							0	0080h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R2268 (8DCh)	DRC2RMIX Input 3 Source	DRC2RMIX_STS3	0	0	0	0	0	0	0	DRC2RMIX_SRC3 [7:0]								0000h
R2269 (8DDh)	DRC2RMIX Input 3 Volume	0	0	0	0	0	0	0	0	DRC2RMIX_VOL3 [6:0]							0	0080h
R2270 (8DEh)	DRC2RMIX Input 4 Source	DRC2RMIX_STS4	0	0	0	0	0	0	0	DRC2RMIX_SRC4 [7:0]								0000h
R2271 (8DFh)	DRC2RMIX Input 4 Volume	0	0	0	0	0	0	0	0	DRC2RMIX_VOL4 [6:0]							0	0080h
R2304 (900h)	HPLP1MIX Input 1 Source	LHPF1MIX_STS1	0	0	0	0	0	0	0	LHPF1MIX_SRC1 [7:0]								0000h
R2305 (901h)	HPLP1MIX Input 1 Volume	0	0	0	0	0	0	0	0	LHPF1MIX_VOL1 [6:0]							0	0080h
R2306 (902h)	HPLP1MIX Input 2 Source	LHPF1MIX_STS2	0	0	0	0	0	0	0	LHPF1MIX_SRC2 [7:0]								0000h
R2307 (903h)	HPLP1MIX Input 2 Volume	0	0	0	0	0	0	0	0	LHPF1MIX_VOL2 [6:0]							0	0080h
R2308 (904h)	HPLP1MIX Input 3 Source	LHPF1MIX_STS3	0	0	0	0	0	0	0	LHPF1MIX_SRC3 [7:0]								0000h
R2309 (905h)	HPLP1MIX Input 3 Volume	0	0	0	0	0	0	0	0	LHPF1MIX_VOL3 [6:0]							0	0080h
R2310 (906h)	HPLP1MIX Input 4 Source	LHPF1MIX_STS4	0	0	0	0	0	0	0	LHPF1MIX_SRC4 [7:0]								0000h
R2311 (907h)	HPLP1MIX Input 4 Volume	0	0	0	0	0	0	0	0	LHPF1MIX_VOL4 [6:0]							0	0080h
R2312 (908h)	HPLP2MIX Input 1 Source	LHPF2MIX_STS1	0	0	0	0	0	0	0	LHPF2MIX_SRC1 [7:0]								0000h
R2313 (909h)	HPLP2MIX Input 1 Volume	0	0	0	0	0	0	0	0	LHPF2MIX_VOL1 [6:0]							0	0080h
R2314 (90Ah)	HPLP2MIX Input 2 Source	LHPF2MIX_STS2	0	0	0	0	0	0	0	LHPF2MIX_SRC2 [7:0]								0000h
R2315 (90Bh)	HPLP2MIX Input 2 Volume	0	0	0	0	0	0	0	0	LHPF2MIX_VOL2 [6:0]							0	0080h
R2316 (90Ch)	HPLP2MIX Input 3 Source	LHPF2MIX_STS3	0	0	0	0	0	0	0	LHPF2MIX_SRC3 [7:0]								0000h
R2317 (90Dh)	HPLP2MIX Input 3 Volume	0	0	0	0	0	0	0	0	LHPF2MIX_VOL3 [6:0]							0	0080h
R2318 (90Eh)	HPLP2MIX Input 4 Source	LHPF2MIX_STS4	0	0	0	0	0	0	0	LHPF2MIX_SRC4 [7:0]								0000h
R2319 (90Fh)	HPLP2MIX Input 4 Volume	0	0	0	0	0	0	0	0	LHPF2MIX_VOL4 [6:0]							0	0080h
R2320 (910h)	HPLP3MIX Input 1 Source	LHPF3MIX_STS1	0	0	0	0	0	0	0	LHPF3MIX_SRC1 [7:0]								0000h
R2321 (911h)	HPLP3MIX Input 1 Volume	0	0	0	0	0	0	0	0	LHPF3MIX_VOL1 [6:0]							0	0080h
R2322 (912h)	HPLP3MIX Input 2 Source	LHPF3MIX_STS2	0	0	0	0	0	0	0	LHPF3MIX_SRC2 [7:0]								0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R2323 (913h)	HPLP3MIX Input 2 Volume	0	0	0	0	0	0	0	0	LHPF3MIX_VOL2 [6:0]							0	0080h
R2324 (914h)	HPLP3MIX Input 3 Source	LHPF3 MIX_ST S3	0	0	0	0	0	0	0	LHPF3MIX_SRC3 [7:0]								0000h
R2325 (915h)	HPLP3MIX Input 3 Volume	0	0	0	0	0	0	0	0	LHPF3MIX_VOL3 [6:0]							0	0080h
R2326 (916h)	HPLP3MIX Input 4 Source	LHPF3 MIX_ST S4	0	0	0	0	0	0	0	LHPF3MIX_SRC4 [7:0]								0000h
R2327 (917h)	HPLP3MIX Input 4 Volume	0	0	0	0	0	0	0	0	LHPF3MIX_VOL4 [6:0]							0	0080h
R2328 (918h)	HPLP4MIX Input 1 Source	LHPF4 MIX_ST S1	0	0	0	0	0	0	0	LHPF4MIX_SRC1 [7:0]								0000h
R2329 (919h)	HPLP4MIX Input 1 Volume	0	0	0	0	0	0	0	0	LHPF4MIX_VOL1 [6:0]							0	0080h
R2330 (91Ah)	HPLP4MIX Input 2 Source	LHPF4 MIX_ST S2	0	0	0	0	0	0	0	LHPF4MIX_SRC2 [7:0]								0000h
R2331 (91Bh)	HPLP4MIX Input 2 Volume	0	0	0	0	0	0	0	0	LHPF4MIX_VOL2 [6:0]							0	0080h
R2332 (91Ch)	HPLP4MIX Input 3 Source	LHPF4 MIX_ST S3	0	0	0	0	0	0	0	LHPF4MIX_SRC3 [7:0]								0000h
R2333 (91Dh)	HPLP4MIX Input 3 Volume	0	0	0	0	0	0	0	0	LHPF4MIX_VOL3 [6:0]							0	0080h
R2334 (91Eh)	HPLP4MIX Input 4 Source	LHPF4 MIX_ST S4	0	0	0	0	0	0	0	LHPF4MIX_SRC4 [7:0]								0000h
R2335 (91Fh)	HPLP4MIX Input 4 Volume	0	0	0	0	0	0	0	0	LHPF4MIX_VOL4 [6:0]							0	0080h
R2432 (980h)	DSP2LMIX Input 1 Source	DSP2L MIX_ST S1	0	0	0	0	0	0	0	DSP2LMIX_SRC1 [7:0]								0000h
R2433 (981h)	DSP2LMIX Input 1 Volume	0	0	0	0	0	0	0	0	DSP2LMIX_VOL1 [6:0]							0	0080h
R2434 (982h)	DSP2LMIX Input 2 Source	DSP2L MIX_ST S2	0	0	0	0	0	0	0	DSP2LMIX_SRC2 [7:0]								0000h
R2435 (983h)	DSP2LMIX Input 2 Volume	0	0	0	0	0	0	0	0	DSP2LMIX_VOL2 [6:0]							0	0080h
R2436 (984h)	DSP2LMIX Input 3 Source	DSP2L MIX_ST S3	0	0	0	0	0	0	0	DSP2LMIX_SRC3 [7:0]								0000h
R2437 (985h)	DSP2LMIX Input 3 Volume	0	0	0	0	0	0	0	0	DSP2LMIX_VOL3 [6:0]							0	0080h
R2438 (986h)	DSP2LMIX Input 4 Source	DSP2L MIX_ST S4	0	0	0	0	0	0	0	DSP2LMIX_SRC4 [7:0]								0000h
R2439 (987h)	DSP2LMIX Input 4 Volume	0	0	0	0	0	0	0	0	DSP2LMIX_VOL4 [6:0]							0	0080h
R2440 (988h)	DSP2RMIX Input 1 Source	DSP2R MIX_ST S1	0	0	0	0	0	0	0	DSP2RMIX_SRC1 [7:0]								0000h
R2441 (989h)	DSP2RMIX Input 1 Volume	0	0	0	0	0	0	0	0	DSP2RMIX_VOL1 [6:0]							0	0080h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R2442 (98Ah)	DSP2RMIX Input 2 Source	DSP2RMIX_STS2	0	0	0	0	0	0	0	DSP2RMIX_SRC2 [7:0]								0000h
R2443 (98Bh)	DSP2RMIX Input 2 Volume	0	0	0	0	0	0	0	0	DSP2RMIX_VOL2 [6:0]							0	0080h
R2444 (98Ch)	DSP2RMIX Input 3 Source	DSP2RMIX_STS3	0	0	0	0	0	0	0	DSP2RMIX_SRC3 [7:0]								0000h
R2445 (98Dh)	DSP2RMIX Input 3 Volume	0	0	0	0	0	0	0	0	DSP2RMIX_VOL3 [6:0]							0	0080h
R2446 (98Eh)	DSP2RMIX Input 4 Source	DSP2RMIX_STS4	0	0	0	0	0	0	0	DSP2RMIX_SRC4 [7:0]								0000h
R2447 (98Fh)	DSP2RMIX Input 4 Volume	0	0	0	0	0	0	0	0	DSP2RMIX_VOL4 [6:0]							0	0080h
R2448 (990h)	DSP2AUX1MIX Input 1 Source	DSP2AUX1MIX_STS	0	0	0	0	0	0	0	DSP2AUX1_SRC [7:0]								0000h
R2456 (998h)	DSP2AUX2MIX Input 1 Source	DSP2AUX2MIX_STS	0	0	0	0	0	0	0	DSP2AUX2_SRC [7:0]								0000h
R2464 (9A0h)	DSP2AUX3MIX Input 1 Source	DSP2AUX3MIX_STS	0	0	0	0	0	0	0	DSP2AUX3_SRC [7:0]								0000h
R2472 (9A8h)	DSP2AUX4MIX Input 1 Source	DSP2AUX4MIX_STS	0	0	0	0	0	0	0	DSP2AUX4_SRC [7:0]								0000h
R2480 (9B0h)	DSP2AUX5MIX Input 1 Source	DSP2AUX5MIX_STS	0	0	0	0	0	0	0	DSP2AUX5_SRC [7:0]								0000h
R2488 (9B8h)	DSP2AUX6MIX Input 1 Source	DSP2AUX6MIX_STS	0	0	0	0	0	0	0	DSP2AUX6_SRC [7:0]								0000h
R2496 (9C0h)	DSP3LMIX Input 1 Source	DSP3LMIX_STS1	0	0	0	0	0	0	0	DSP3LMIX_SRC1 [7:0]								0000h
R2497 (9C1h)	DSP3LMIX Input 1 Volume	0	0	0	0	0	0	0	0	DSP3LMIX_VOL1 [6:0]							0	0080h
R2498 (9C2h)	DSP3LMIX Input 2 Source	DSP3LMIX_STS2	0	0	0	0	0	0	0	DSP3LMIX_SRC2 [7:0]								0000h
R2499 (9C3h)	DSP3LMIX Input 2 Volume	0	0	0	0	0	0	0	0	DSP3LMIX_VOL2 [6:0]							0	0080h
R2500 (9C4h)	DSP3LMIX Input 3 Source	DSP3LMIX_STS3	0	0	0	0	0	0	0	DSP3LMIX_SRC3 [7:0]								0000h
R2501 (9C5h)	DSP3LMIX Input 3 Volume	0	0	0	0	0	0	0	0	DSP3LMIX_VOL3 [6:0]							0	0080h
R2502 (9C6h)	DSP3LMIX Input 4 Source	DSP3LMIX_STS4	0	0	0	0	0	0	0	DSP3LMIX_SRC4 [7:0]								0000h
R2503 (9C7h)	DSP3LMIX Input 4 Volume	0	0	0	0	0	0	0	0	DSP3LMIX_VOL4 [6:0]							0	0080h
R2504 (9C8h)	DSP3RMIX Input 1 Source	DSP3RMIX_STS1	0	0	0	0	0	0	0	DSP3RMIX_SRC1 [7:0]								0000h
R2505 (9C9h)	DSP3RMIX Input 1 Volume	0	0	0	0	0	0	0	0	DSP3RMIX_VOL1 [6:0]							0	0080h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R2506 (9CAh)	DSP3RMIX Input 2 Source	DSP3RMIX_STS2	0	0	0	0	0	0	0	DSP3RMIX_SRC2 [7:0]								0000h
R2507 (9CBh)	DSP3RMIX Input 2 Volume	0	0	0	0	0	0	0	0	DSP3RMIX_VOL2 [6:0]							0	0080h
R2508 (9CCh)	DSP3RMIX Input 3 Source	DSP3RMIX_STS3	0	0	0	0	0	0	0	DSP3RMIX_SRC3 [7:0]								0000h
R2509 (9CDh)	DSP3RMIX Input 3 Volume	0	0	0	0	0	0	0	0	DSP3RMIX_VOL3 [6:0]							0	0080h
R2510 (9CEh)	DSP3RMIX Input 4 Source	DSP3RMIX_STS4	0	0	0	0	0	0	0	DSP3RMIX_SRC4 [7:0]								0000h
R2511 (9CFh)	DSP3RMIX Input 4 Volume	0	0	0	0	0	0	0	0	DSP3RMIX_VOL4 [6:0]							0	0080h
R2512 (9D0h)	DSP3AUX1MIX Input 1 Source	DSP3AUX1MIX_STS	0	0	0	0	0	0	0	DSP3AUX1_SRC [7:0]								0000h
R2520 (9D8h)	DSP3AUX2MIX Input 1 Source	DSP3AUX2MIX_STS	0	0	0	0	0	0	0	DSP3AUX2_SRC [7:0]								0000h
R2528 (9E0h)	DSP3AUX3MIX Input 1 Source	DSP3AUX3MIX_STS	0	0	0	0	0	0	0	DSP3AUX3_SRC [7:0]								0000h
R2536 (9E8h)	DSP3AUX4MIX Input 1 Source	DSP3AUX4MIX_STS	0	0	0	0	0	0	0	DSP3AUX4_SRC [7:0]								0000h
R2544 (9F0h)	DSP3AUX5MIX Input 1 Source	DSP3AUX5MIX_STS	0	0	0	0	0	0	0	DSP3AUX5_SRC [7:0]								0000h
R2552 (9F8h)	DSP3AUX6MIX Input 1 Source	DSP3AUX6MIX_STS	0	0	0	0	0	0	0	DSP3AUX6_SRC [7:0]								0000h
R2688 (A80h)	ASRC1LMIX Input 1 Source	ASRC1LMIX_STS	0	0	0	0	0	0	0	ASRC1L_SRC [7:0]								0000h
R2696 (A88h)	ASRC1RMIX Input 1 Source	ASRC1RMIX_STS	0	0	0	0	0	0	0	ASRC1R_SRC [7:0]								0000h
R2704 (A90h)	ASRC2LMIX Input 1 Source	ASRC2LMIX_STS	0	0	0	0	0	0	0	ASRC2L_SRC [7:0]								0000h
R2712 (A98h)	ASRC2RMIX Input 1 Source	ASRC2RMIX_STS	0	0	0	0	0	0	0	ASRC2R_SRC [7:0]								0000h
R2816 (B00h)	ISRC1DEC1MIX Input 1 Source	ISRC1DEC1MIX_STS	0	0	0	0	0	0	0	ISRC1DEC1_SRC [7:0]								0000h
R2824 (B08h)	ISRC1DEC2MIX Input 1 Source	ISRC1DEC2MIX_STS	0	0	0	0	0	0	0	ISRC1DEC2_SRC [7:0]								0000h
R2832 (B10h)	ISRC1DEC3MIX Input 1 Source	ISRC1DEC3MIX_STS	0	0	0	0	0	0	0	ISRC1DEC3_SRC [7:0]								0000h
R2840 (B18h)	ISRC1DEC4MIX Input 1 Source	ISRC1DEC4MIX_STS	0	0	0	0	0	0	0	ISRC1DEC4_SRC [7:0]								0000h
R2848 (B20h)	ISRC1INT1MIX Input 1 Source	ISRC1INT1MIX_STS	0	0	0	0	0	0	0	ISRC1INT1_SRC [7:0]								0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R2856 (B28h)	ISRC1INT2MIX Input 1 Source	ISRC1INT2MIX_STS	0	0	0	0	0	0	0	ISRC1INT2_SRC [7:0]								0000h
R2864 (B30h)	ISRC1INT3MIX Input 1 Source	ISRC1INT3MIX_STS	0	0	0	0	0	0	0	ISRC1INT3_SRC [7:0]								0000h
R2872 (B38h)	ISRC1INT4MIX Input 1 Source	ISRC1INT4MIX_STS	0	0	0	0	0	0	0	ISRC1INT4_SRC [7:0]								0000h
R2880 (B40h)	ISRC2DEC1MIX Input 1 Source	ISRC2DEC1MIX_STS	0	0	0	0	0	0	0	ISRC2DEC1_SRC [7:0]								0000h
R2888 (B48h)	ISRC2DEC2MIX Input 1 Source	ISRC2DEC2MIX_STS	0	0	0	0	0	0	0	ISRC2DEC2_SRC [7:0]								0000h
R2896 (B50h)	ISRC2DEC3MIX Input 1 Source	ISRC2DEC3MIX_STS	0	0	0	0	0	0	0	ISRC2DEC3_SRC [7:0]								0000h
R2904 (B58h)	ISRC2DEC4MIX Input 1 Source	ISRC2DEC4MIX_STS	0	0	0	0	0	0	0	ISRC2DEC4_SRC [7:0]								0000h
R2912 (B60h)	ISRC2INT1MIX Input 1 Source	ISRC2INT1MIX_STS	0	0	0	0	0	0	0	ISRC2INT1_SRC [7:0]								0000h
R2920 (B68h)	ISRC2INT2MIX Input 1 Source	ISRC2INT2MIX_STS	0	0	0	0	0	0	0	ISRC2INT2_SRC [7:0]								0000h
R2928 (B70h)	ISRC2INT3MIX Input 1 Source	ISRC2INT3MIX_STS	0	0	0	0	0	0	0	ISRC2INT3_SRC [7:0]								0000h
R2936 (B78h)	ISRC2INT4MIX Input 1 Source	ISRC2INT4MIX_STS	0	0	0	0	0	0	0	ISRC2INT4_SRC [7:0]								0000h
R2944 (B80h)	ISRC3DEC1MIX Input 1 Source	ISRC3DEC1MIX_STS	0	0	0	0	0	0	0	ISRC3DEC1_SRC [7:0]								0000h
R2952 (B88h)	ISRC3DEC2MIX Input 1 Source	ISRC3DEC2MIX_STS	0	0	0	0	0	0	0	ISRC3DEC2_SRC [7:0]								0000h
R2960 (B90h)	ISRC3DEC3MIX Input 1 Source	ISRC3DEC3MIX_STS	0	0	0	0	0	0	0	ISRC3DEC3_SRC [7:0]								0000h
R2968 (B98h)	ISRC3DEC4MIX Input 1 Source	ISRC3DEC4MIX_STS	0	0	0	0	0	0	0	ISRC3DEC4_SRC [7:0]								0000h
R2976 (BA0h)	ISRC3INT1MIX Input 1 Source	ISRC3INT1MIX_STS	0	0	0	0	0	0	0	ISRC3INT1_SRC [7:0]								0000h
R2984 (BA8h)	ISRC3INT2MIX Input 1 Source	ISRC3INT2MIX_STS	0	0	0	0	0	0	0	ISRC3INT2_SRC [7:0]								0000h
R2992 (BB0h)	ISRC3INT3MIX Input 1 Source	ISRC3INT3MIX_STS	0	0	0	0	0	0	0	ISRC3INT3_SRC [7:0]								0000h
R3000 (BB8h)	ISRC3INT4MIX Input 1 Source	ISRC3INT4MIX_STS	0	0	0	0	0	0	0	ISRC3INT4_SRC [7:0]								0000h
R3072 (C00h)	GPIO1 CTRL	GP1_DIR	GP1_PU	GP1_PD	0	GP1_LVL	GP1_POL	GP1_OP_CFG	GP1_DB	0	GP1_FN [6:0]							A101h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R3073 (C01h)	GPIO2 CTRL	GP2_DIR	GP2_PU	GP2_PD	0	GP2_LVL	GP2_POL	GP2_OP_CFG	GP2_DB	0	GP2_FN [6:0]							A101h
R3087 (C0Fh)	IRQ CTRL 1	0	0	0	0	0	IRQ_POL	IRQ_OP_CFG	0	0	0	0	0	0	0	0	0	0400h
R3088 (C10h)	GPIO Debounce Config	GP_DBTIME [3:0]				0	0	0	0	0	0	0	0	0	0	0	0	1000h
R3104 (C20h)	Misc Pad Ctrl 1	0	0	MCLK2_PD	0	0	0	0	0	0	0	0	0	0	0	RESET_PU	RESET_PD	0002h
R3105 (C21h)	Misc Pad Ctrl 2	0	0	0	MCLK1_PD	0	0	0	0	0	0	0	0	0	0	0	0	0000h
R3106 (C22h)	Misc Pad Ctrl 3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DMICDAT2_PD	DMICDAT1_PD	0000h
R3107 (C23h)	Misc Pad Ctrl 4	0	0	0	0	0	0	0	0	0	0	AIF1LRCLK_PU	AIF1LRCLK_PD	AIF1BCLK_PU	AIF1BCLK_PD	AIF1RXDAT_PU	AIF1RXDAT_PD	0000h
R3108 (C24h)	Misc Pad Ctrl 5	0	0	0	0	0	0	0	0	0	0	AIF2LRCLK_PU	AIF2LRCLK_PD	AIF2BCLK_PU	AIF2BCLK_PD	AIF2RXDAT_PU	AIF2RXDAT_PD	0000h
R3109 (C25h)	Misc Pad Ctrl 6	0	0	0	0	0	0	0	0	0	0	AIF3LRCLK_PU	AIF3LRCLK_PD	AIF3BCLK_PU	AIF3BCLK_PD	AIF3RXDAT_PU	AIF3RXDAT_PD	0000h
R3120 (C30h)	Misc Pad Ctrl 7	0	0	0	0	0	CIFMISO_DRV_STR	0	0	0	0	0	0	0	1	0	0	0404h
R3122 (C32h)	Misc Pad Ctrl 9	0	0	0	0	0	AIF1LRCLK_DRV_STR	0	0	0	0	0	0	0	GPIO1_DRV_STR	0	0	0404h
R3123 (C33h)	Misc Pad Ctrl 10	0	0	0	0	0	AIF1BCLK_DRV_STR	0	0	0	0	0	0	0	AIF1TXDAT_DRV_STR	0	0	0404h
R3124 (C34h)	Misc Pad Ctrl 11	0	0	0	0	0	AIF2LRCLK_DRV_STR	0	0	0	0	0	0	0	GPIO2_DRV_STR	0	0	0404h
R3125 (C35h)	Misc Pad Ctrl 12	0	0	0	0	0	AIF2BCLK_DRV_STR	0	0	0	0	0	0	0	AIF2TXDAT_DRV_STR	0	0	0404h
R3126 (C36h)	Misc Pad Ctrl 13	0	0	0	0	0	AIF3LRCLK_DRV_STR	0	0	0	0	0	0	0	0	0	0	0400h
R3127 (C37h)	Misc Pad Ctrl 14	0	0	0	0	0	AIF3BCLK_DRV_STR	0	0	0	0	0	0	0	AIF3TXDAT_DRV_STR	0	0	0404h
R3129 (C39h)	Misc Pad Ctrl 16	0	0	0	0	0	IRQ_DRV_STR	0	0	0	0	0	0	0	0	0	0	0400h
R3328 (D00h)	Interrupt Status 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GP2_EINT1	GP1_EINT1	0000h
R3329 (D01h)	Interrupt Status 2	0	0	0	0	0	DSP3_RAM_RDY_EINT1	DSP2_RAM_RDY_EINT1	0	DSP_IRQ8_EINT1	DSP_IRQ7_EINT1	DSP_IRQ6_EINT1	DSP_IRQ5_EINT1	DSP_IRQ4_EINT1	DSP_IRQ3_EINT1	DSP_IRQ2_EINT1	DSP_IRQ1_EINT1	0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R3330 (D02h)	Interrupt Status 3	SPK_OVERHEAT_WARN_EINT1	SPK_OVERHEAT_EINT1	0	0	WSEQ_DONE_EINT1	DRC2_SIG_DET_EINT1	DRC1_SIG_DET_EINT1	ASRC2_LOCK_EINT1	ASRC1_LOCK_EINT1	UNDERCLOCKED_EINT1	OVERCLOCKED_EINT1	0	FLL2_LOCK_EINT1	FLL1_LOCK_EINT1	CLKGEN_ERR_EINT1	CLKGEN_ERR_ASYNC_EINT1	0000h
R3331 (D03h)	Interrupt Status 4	0	0	0	CTRLIF_ERR_EINT1	MIXER_DROPPED_SAMPLE_EINT1	ASYNC_CLK_ENA_LOW_EINT1	SYSCLK_ENA_LOW_EINT1	ISRC1_CFG_ERR_EINT1	ISRC2_CFG_ERR_EINT1	ISRC3_CFG_ERR_EINT1	0	0	0	0	HPR_ENABLE_DONE_EINT1	HPL_ENABLE_DONE_EINT1	0000h
R3332 (D04h)	Interrupt Status 5	0	0	0	0	0	0	0	BOOT_DONE_EINT1	0	0	0	0	ASRC_CFG_ERR_EINT1	0	FLL2_CLOCK_OK_EINT1	FLL1_CLOCK_OK_EINT1	0000h
R3333 (D05h)	Interrupt Status 6	DSP_SHARED_WR_COLL_EINT1	SPK_SHUTDOWN_EINT1	0	SPKOUTL_SHORT_EINT1	0	0	0	0	0	0	0	0	0	HPR_SC_EINT1	0	HPL_SC_EINT1	0000h
R3336 (D08h)	Interrupt Status 1 Mask	0	0	0	0	0	0	0	0	0	0	0	0	0	1	IM_GP2_EINT1	IM_GP1_EINT1	0007h
R3337 (D09h)	Interrupt Status 2 Mask	0	0	0	0	0	IM_DSP3_RAM_RDY_EINT1	IM_DSP2_RAM_RDY_EINT1	0	IM_DSP_IRQ8_EINT1	IM_DSP_IRQ7_EINT1	IM_DSP_IRQ6_EINT1	IM_DSP_IRQ5_EINT1	IM_DSP_IRQ4_EINT1	IM_DSP_IRQ3_EINT1	IM_DSP_IRQ2_EINT1	IM_DSP_IRQ1_EINT1	06FFh
R3338 (D0Ah)	Interrupt Status 3 Mask	IM_SPK_OVERHEAT_WARN_EINT1	IM_SPK_OVERHEAT_EINT1	0	0	IM_WSEQ_DONE_EINT1	IM_DRC2_SIG_DET_EINT1	IM_DRC1_SIG_DET_EINT1	IM_ASRC2_LOCK_EINT1	IM_ASRC1_LOCK_EINT1	IM_UNDERCLOCKED_EINT1	IM_OVERCLOCKED_EINT1	0	IM_FLL2_LOCK_EINT1	IM_FLL1_LOCK_EINT1	IM_CLKGEN_ERR_EINT1	IM_CLKGEN_ERR_ASYNC_EINT1	CFEFh
R3339 (D0Bh)	Interrupt Status 4 Mask	1	1	1	IM_CTRLIF_ERR_EINT1	IM_MIXER_DROPPED_SAMPLE_EINT1	IM_ASYNC_CLK_ENA_LOW_EINT1	IM_SYSCLK_ENA_LOW_EINT1	IM_ISRC1_CFG_ERR_EINT1	IM_ISRC2_CFG_ERR_EINT1	IM_ISRC3_CFG_ERR_EINT1	0	0	0	0	IM_HPR_ENABLE_DONE_EINT1	IM_HPL_ENABLE_DONE_EINT1	FFC3h
R3340 (D0Ch)	Interrupt Status 5 Mask	0	0	0	0	0	0	0	IM_BOOT_DONE_EINT1	0	0	0	0	IM_ASRC_CFG_ERR_EINT1	0	IM_FLL2_CLOCK_OK_EINT1	IM_FLL1_CLOCK_OK_EINT1	000Bh
R3341 (D0Dh)	Interrupt Status 6 Mask	IM_DSP_SHARED_WR_COLL_EINT1	IM_SPK_SHUTDOWN_EINT1	0	IM_SPKOUTL_SHORT_EINT1	0	0	0	0	0	0	0	0	0	IM_HPR_SC_EINT1	0	IM_HPL_SC_EINT1	D005h
R3343 (D0Fh)	Interrupt Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IM_IRQ1	0000h
R3344 (D10h)	IRQ2 Status 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GP2_EINT2	GP1_EINT2	0000h
R3345 (D11h)	IRQ2 Status 2	0	0	0	0	0	DSP3_RAM_RDY_EINT2	DSP2_RAM_RDY_EINT2	0	DSP_IRQ8_EINT2	DSP_IRQ7_EINT2	DSP_IRQ6_EINT2	DSP_IRQ5_EINT2	DSP_IRQ4_EINT2	DSP_IRQ3_EINT2	DSP_IRQ2_EINT2	DSP_IRQ1_EINT2	0000h
R3346 (D12h)	IRQ2 Status 3	SPK_OVERHEAT_WARN_EINT2	SPK_OVERHEAT_EINT2	0	0	WSEQ_DONE_EINT2	DRC2_SIG_DET_EINT2	DRC1_SIG_DET_EINT2	ASRC2_LOCK_EINT2	ASRC1_LOCK_EINT2	UNDERCLOCKED_EINT2	OVERCLOCKED_EINT2	0	FLL2_LOCK_EINT2	FLL1_LOCK_EINT2	CLKGEN_ERR_EINT2	CLKGEN_ERR_ASYNC_EINT2	0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R3347 (D13h)	IRQ2 Status 4	0	0	0	CTRLIF_ERR_EINT2	MIXER_DROPPED_SAMPLE_EINT2	ASYNC_CLK_ENA_LOW_EINT2	SYSCLK_ENA_LOW_EINT2	ISRC1_CFG_ERR_EINT2	ISRC2_CFG_ERR_EINT2	ISRC3_CFG_ERR_EINT2	0	0	0	0	HPR_ENABLE_DONE_EINT2	HPL_ENABLE_DONE_EINT2	0000h
R3348 (D14h)	IRQ2 Status 5	0	0	0	0	0	0	0	BOOT_DONE_EINT2	0	0	0	0	ASRC_CFG_ERR_EINT2	0	FLL2_CLOCK_OK_EINT2	FLL1_CLOCK_OK_EINT2	0000h
R3349 (D15h)	IRQ2 Status 6	DSP_SHARED_WR_COLL_EINT2	SPK_SHUTDOWN_EINT2	0	SPKOUTL_SHORT_EINT2	0	0	0	0	0	0	0	0	0	HPR_SC_EINT2	0	HPL_SC_EINT2	0000h
R3352 (D18h)	IRQ2 Status 1 Mask	0	0	0	0	0	0	0	0	0	0	0	0	0	1	IM_GP2_EINT2	IM_GP1_EINT2	0007h
R3353 (D19h)	IRQ2 Status 2 Mask	0	0	0	0	0	IM_DSP3_RAM_RDY_EINT2	IM_DSP2_RAM_RDY_EINT2	0	IM_DSP_IRQ8_EINT2	IM_DSP_IRQ7_EINT2	IM_DSP_IRQ6_EINT2	IM_DSP_IRQ5_EINT2	IM_DSP_IRQ4_EINT2	IM_DSP_IRQ3_EINT2	IM_DSP_IRQ2_EINT2	IM_DSP_IRQ1_EINT2	06FFh
R3354 (D1Ah)	IRQ2 Status 3 Mask	IM_SPK_OVERHEAT_WARN_EINT2	IM_SPK_OVERHEAT_EINT2	0	0	IM_WSEQ_DONE_EINT2	IM_DRC2_SIG_DET_EINT2	IM_DRC1_SIG_DET_EINT2	IM_ASRC2_LOCK_EINT2	IM_ASRC1_LOCK_EINT2	IM_UNDERCLOCKED_EINT2	IM_OVERCLOCKED_EINT2	0	IM_FLL2_LOCK_EINT2	IM_FLL1_LOCK_EINT2	IM_CLKGEN_ERR_EINT2	IM_CLKGEN_ERR_ASYNC_EINT2	CFEFh
R3355 (D1Bh)	IRQ2 Status 4 Mask	1	1	1	IM_CTRLIF_ERR_EINT2	IM_MIXER_DROPPED_SAMPLE_EINT2	IM_ASYNC_CLK_ENA_LOW_EINT2	IM_SYSCLK_ENA_LOW_EINT2	IM_ISRC1_CFG_ERR_EINT2	IM_ISRC2_CFG_ERR_EINT2	IM_ISRC3_CFG_ERR_EINT2	0	0	0	0	IM_HPR_ENABLE_DONE_EINT2	IM_HPL_ENABLE_DONE_EINT2	FFC3h
R3356 (D1Ch)	IRQ2 Status 5 Mask	0	0	0	0	0	0	0	IM_BOOT_DONE_EINT2	0	0	0	0	IM_ASRC_CFG_ERR_EINT2	0	IM_FLL2_CLOCK_OK_EINT2	IM_FLL1_CLOCK_OK_EINT2	000Bh
R3357 (D1Dh)	IRQ2 Status 6 Mask	IM_DSP_SHARED_WR_COLL_EINT2	IM_SPK_SHUTDOWN_EINT2	0	IM_SPKOUTL_SHORT_EINT2	0	0	0	0	0	0	0	0	0	IM_HPR_SC_EINT2	0	IM_HPL_SC_EINT2	D005h
R3359 (D1Fh)	IRQ2 Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IM_IRQ2	0000h
R3360 (D20h)	Interrupt Raw Status 1	0	0	0	0	0	DSP3_RAM_RDY_STS	DSP2_RAM_RDY_STS	0	DSP_IRQ8_STS	DSP_IRQ7_STS	DSP_IRQ6_STS	DSP_IRQ5_STS	DSP_IRQ4_STS	DSP_IRQ3_STS	DSP_IRQ2_STS	DSP_IRQ1_STS	0000h
R3361 (D21h)	Interrupt Raw Status 2	SPK_OVERHEAT_WARN_STS	SPK_OVERHEAT_STS	0	0	WSEQ_DONE_STS	DRC2_SIG_DET_STS	DRC1_SIG_DET_STS	ASRC2_LOCK_STS	ASRC1_LOCK_STS	UNDERCLOCKED_STS	OVERCLOCKED_STS	0	FLL2_LOCK_STS	FLL1_LOCK_STS	CLKGEN_ERR_STS	CLKGEN_ERR_ASYNC_STS	0000h
R3362 (D22h)	Interrupt Raw Status 3	0	0	0	CTRLIF_ERR_STS	MIXER_DROPPED_SAMPLE_STS	ASYNC_CLK_ENA_LOW_STS	SYSCLK_ENA_LOW_STS	ISRC1_CFG_ERR_STS	ISRC2_CFG_ERR_STS	ISRC3_CFG_ERR_STS	0	0	0	0	HPR_ENABLE_DONE_STS	HPL_ENABLE_DONE_STS	0000h
R3363 (D23h)	Interrupt Raw Status 4	0	0	0	0	0	0	0	BOOT_DONE_STS	0	0	0	0	ASRC_CFG_ERR_STS	0	FLL2_CLOCK_OK_STS	FLL1_CLOCK_OK_STS	0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R3364 (D24h)	Interrupt Raw Status 5	0	0	PWM_OVERCLOCKED_STS	FX_CORE_OVERCLOCKED_STS	0	DAC_SYS_OVERCLOCKED_STS	DAC_WARP_OVERCLOCKED_STS	ADC_OVERCLOCKED_STS	MIXER_OVERCLOCKED_STS	AIF3_ASYNC_OVERCLOCKED_STS	AIF2_ASYNC_OVERCLOCKED_STS	AIF1_ASYNC_OVERCLOCKED_STS	AIF3_SYNC_OVERCLOCKED_STS	AIF2_SYNC_OVERCLOCKED_STS	AIF1_SYNC_OVERCLOCKED_STS	PAD_CTRL_OVERCLOCKED_STS	0000h
R3365 (D25h)	Interrupt Raw Status 6	0	0	0	ASRC_ASYNC_SYS_OVERCLOCKED_STS	ASRC_ASYNC_WARP_OVERCLOCKED_STS	ASRC_SYNC_SYS_OVERCLOCKED_STS	ASRC_SYNC_WARP_OVERCLOCKED_STS	0	DSP3_OVERCLOCKED_STS	0	DSP2_OVERCLOCKED_STS	0	0	ISRC3_OVERCLOCKED_STS	ISRC2_OVERCLOCKED_STS	ISRC1_OVERCLOCKED_STS	0000h
R3366 (D26h)	Interrupt Raw Status 7	0	0	0	0	0	AIF3_UNDERCLOCKED_STS	AIF2_UNDERCLOCKED_STS	AIF1_UNDERCLOCKED_STS	ISRC3_UNDERCLOCKED_STS	ISRC2_UNDERCLOCKED_STS	ISRC1_UNDERCLOCKED_STS	FX_UNDERCLOCKED_STS	ASRC_UNDERCLOCKED_STS	DAC_UNDERCLOCKED_STS	ADC_UNDERCLOCKED_STS	MIXER_UNDERCLOCKED_STS	0000h
R3368 (D28h)	Interrupt Raw Status 8	0	SPK_SHUTDOWN_STS	0	SPKOUTL_SHORT_STS	0	0	0	0	0	0	0	0	0	HPR_SC_STS	0	HPL_SC_STS	0000h
R3392 (D40h)	IRQ Pin Status	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IRQ2_STS	IRQ1_STS	0000h
R3393 (D41h)	ADSP2 IRQ0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSP_IRQ2	DSP_IRQ1	0000h
R3394 (D42h)	ADSP2 IRQ1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSP_IRQ4	DSP_IRQ3	0000h
R3395 (D43h)	ADSP2 IRQ2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSP_IRQ6	DSP_IRQ5	0000h
R3396 (D44h)	ADSP2 IRQ3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSP_IRQ8	DSP_IRQ7	0000h
R3584 (E00h)	FX_Ctrl1	0	FX_RATE [3:0]				0	0	0	0	0	0	0	0	0	0	0	0000h
R3585 (E01h)	FX_Ctrl2	FX_STS [11:0]												0	0	0	0	0000h
R3600 (E10h)	EQ1_1	EQ1_B1_GAIN [4:0]					EQ1_B2_GAIN [4:0]					EQ1_B3_GAIN [4:0]					EQ1_ENA	6318h
R3601 (E11h)	EQ1_2	EQ1_B4_GAIN [4:0]					EQ1_B5_GAIN [4:0]					0	0	0	0	0	EQ1_B1_MODE	6300h
R3602 (E12h)	EQ1_3	EQ1_B1_A [15:0]																0FC8h
R3603 (E13h)	EQ1_4	EQ1_B1_B [15:0]																03FEh
R3604 (E14h)	EQ1_5	EQ1_B1_PG [15:0]																00E0h
R3605 (E15h)	EQ1_6	EQ1_B2_A [15:0]																1EC4h
R3606 (E16h)	EQ1_7	EQ1_B2_B [15:0]																F136h
R3607 (E17h)	EQ1_8	EQ1_B2_C [15:0]																0409h
R3608 (E18h)	EQ1_9	EQ1_B2_PG [15:0]																04CCh
R3609 (E19h)	EQ1_10	EQ1_B3_A [15:0]																1C9Bh
R3610 (E1Ah)	EQ1_11	EQ1_B3_B [15:0]																F337h
R3611 (E1Bh)	EQ1_12	EQ1_B3_C [15:0]																040Bh
R3612 (E1Ch)	EQ1_13	EQ1_B3_PG [15:0]																0CBBh
R3613 (E1Dh)	EQ1_14	EQ1_B4_A [15:0]																16F8h
R3614 (E1Eh)	EQ1_15	EQ1_B4_B [15:0]																F7D9h
R3615 (E1Fh)	EQ1_16	EQ1_B4_C [15:0]																040Ah
R3616 (E20h)	EQ1_17	EQ1_B4_PG [15:0]																1F14h
R3617 (E21h)	EQ1_18	EQ1_B5_A [15:0]																058Ch
R3618 (E22h)	EQ1_19	EQ1_B5_B [15:0]																0563h
R3619 (E23h)	EQ1_20	EQ1_B5_PG [15:0]																4000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R3620 (E24h)	EQ1_21	EQ1_B1_C [15:0]																0B75h
R3622 (E26h)	EQ2_1	EQ2_B1_GAIN [4:0]					EQ2_B2_GAIN [4:0]					EQ2_B3_GAIN [4:0]					EQ2_ENA	6318h
R3623 (E27h)	EQ2_2	EQ2_B4_GAIN [4:0]					EQ2_B5_GAIN [4:0]					0	0	0	0	0	EQ2_B1_MODE	6300h
R3624 (E28h)	EQ2_3	EQ2_B1_A [15:0]																0FC8h
R3625 (E29h)	EQ2_4	EQ2_B1_B [15:0]																03FEh
R3626 (E2Ah)	EQ2_5	EQ2_B1_PG [15:0]																00E0h
R3627 (E2Bh)	EQ2_6	EQ2_B2_A [15:0]																1EC4h
R3628 (E2Ch)	EQ2_7	EQ2_B2_B [15:0]																F136h
R3629 (E2Dh)	EQ2_8	EQ2_B2_C [15:0]																0409h
R3630 (E2Eh)	EQ2_9	EQ2_B2_PG [15:0]																04CCh
R3631 (E2Fh)	EQ2_10	EQ2_B3_A [15:0]																1C9Bh
R3632 (E30h)	EQ2_11	EQ2_B3_B [15:0]																F337h
R3633 (E31h)	EQ2_12	EQ2_B3_C [15:0]																040Bh
R3634 (E32h)	EQ2_13	EQ2_B3_PG [15:0]																0CBBh
R3635 (E33h)	EQ2_14	EQ2_B4_A [15:0]																16F8h
R3636 (E34h)	EQ2_15	EQ2_B4_B [15:0]																F7D9h
R3637 (E35h)	EQ2_16	EQ2_B4_C [15:0]																040Ah
R3638 (E36h)	EQ2_17	EQ2_B4_PG [15:0]																1F14h
R3639 (E37h)	EQ2_18	EQ2_B5_A [15:0]																058Ch
R3640 (E38h)	EQ2_19	EQ2_B5_B [15:0]																0563h
R3641 (E39h)	EQ2_20	EQ2_B5_PG [15:0]																4000h
R3642 (E3Ah)	EQ2_21	EQ2_B1_C [15:0]																0B75h
R3712 (E80h)	DRC1 ctrl1	DRC1_SIG_DET_RMS [4:0]					DRC1_SIG_DET_PK [1:0]		DRC1_NG_ENA	DRC1_SIG_DET_MODE	DRC1_SIG_DET	DRC1_KNEE2_OP_ENA	DRC1_QR	DRC1_ANTICLIP	DRC1_WSEQ_SIG_DET_ENA	DRC1L_ENA	DRC1R_ENA	0018h
R3713 (E81h)	DRC1 ctrl2	0	0	0	DRC1_ATK [3:0]				DRC1_DCY [3:0]				DRC1_MINGAIN [2:0]			DRC1_MAXGAIN [1:0]		0933h
R3714 (E82h)	DRC1 ctrl3	DRC1_NG_MINGAIN [3:0]				DRC1_NG_EXP [1:0]		DRC1_QR_THR [1:0]		DRC1_QR_DCY [1:0]		DRC1_HI_COMP [2:0]			DRC1_LO_COMP [2:0]			0018h
R3715 (E83h)	DRC1 ctrl4	0	0	0	0	0	DRC1_KNEE_IP [5:0]						DRC1_KNEE_OP [4:0]					0000h
R3716 (E84h)	DRC1 ctrl5	0	0	0	0	0	0	DRC1_KNEE2_IP [4:0]					DRC1_KNEE2_OP [4:0]					0000h
R3721 (E89h)	DRC2 ctrl1	DRC2_SIG_DET_RMS [4:0]					DRC2_SIG_DET_PK [1:0]		DRC2_NG_ENA	DRC2_SIG_DET_MODE	DRC2_SIG_DET	DRC2_KNEE2_OP_ENA	DRC2_QR	DRC2_ANTICLIP	0	DRC2L_ENA	DRC2R_ENA	0018h
R3722 (E8Ah)	DRC2 ctrl2	0	0	0	DRC2_ATK [3:0]				DRC2_DCY [3:0]				DRC2_MINGAIN [2:0]			DRC2_MAXGAIN [1:0]		0933h
R3723 (E8Bh)	DRC2 ctrl3	DRC2_NG_MINGAIN [3:0]				DRC2_NG_EXP [1:0]		DRC2_QR_THR [1:0]		DRC2_QR_DCY [1:0]		DRC2_HI_COMP [2:0]			DRC2_LO_COMP [2:0]			0018h
R3724 (E8Ch)	DRC2 ctrl4	0	0	0	0	0	DRC2_KNEE_IP [5:0]						DRC2_KNEE_OP [4:0]					0000h
R3725 (E8Dh)	DRC2 ctrl5	0	0	0	0	0	0	DRC2_KNEE2_IP [4:0]					DRC2_KNEE2_OP [4:0]					0000h
R3776 (EC0h)	HPLPF1_1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LHPF1_MODE	LHPF1_ENA	0000h
R3777 (EC1h)	HPLPF1_2	LHPF1_COEFF [15:0]																0000h
R3780 (EC4h)	HPLPF2_1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LHPF2_MODE	LHPF2_ENA	0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R3781 (EC5h)	HPLPF2_2	LHPF2_COEFF [15:0]																0000h
R3784 (EC8h)	HPLPF3_1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LHPF3_MODE	LHPF3_ENA	0000h
R3785 (EC9h)	HPLPF3_2	LHPF3_COEFF [15:0]																0000h
R3788 (ECCh)	HPLPF4_1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LHPF4_MODE	LHPF4_ENA	0000h
R3789 (ECDh)	HPLPF4_2	LHPF4_COEFF [15:0]																0000h
R3808 (EE0h)	ASRC_ENABLE	0	0	0	0	0	0	0	0	0	0	0	0	ASRC2L_ENA	ASRC2R_ENA	ASRC1L_ENA	ASRC1R_ENA	0000h
R3809 (EE1h)	ASRC_STATUS	0	0	0	0	0	0	0	0	0	0	0	0	ASRC2L_ENA_STS	ASRC2R_ENA_STS	ASRC1L_ENA_STS	ASRC1R_ENA_STS	0000h
R3810 (EE2h)	ASRC_RATE1	0	ASRC_RATE1 [3:0]				0	0	0	0	0	0	0	0	0	0	0	0000h
R3811 (EE3h)	ASRC_RATE2	0	ASRC_RATE2 [3:0]				0	0	0	0	0	0	0	0	0	0	0	4000h
R3824 (EF0h)	ISRC 1 CTRL 1	0	ISRC1_FSH [3:0]				0	0	0	0	0	0	0	0	0	0	0	0000h
R3825 (EF1h)	ISRC 1 CTRL 2	0	ISRC1_FSL [3:0]				0	0	0	0	0	0	0	0	0	0	0	0000h
R3826 (EF2h)	ISRC 1 CTRL 3	ISRC1_INT1_ENA	ISRC1_INT2_ENA	ISRC1_INT3_ENA	ISRC1_INT4_ENA	0	0	ISRC1_DEC1_ENA	ISRC1_DEC2_ENA	ISRC1_DEC3_ENA	ISRC1_DEC4_ENA	0	0	0	0	0	ISRC1_NOTCH_ENA	0000h
R3827 (EF3h)	ISRC 2 CTRL 1	0	ISRC2_FSH [3:0]				0	0	0	0	0	0	0	0	0	0	0	0000h
R3828 (EF4h)	ISRC 2 CTRL 2	0	ISRC2_FSL [3:0]				0	0	0	0	0	0	0	0	0	0	0	0000h
R3829 (EF5h)	ISRC 2 CTRL 3	ISRC2_INT1_ENA	ISRC2_INT2_ENA	ISRC2_INT3_ENA	ISRC2_INT4_ENA	0	0	ISRC2_DEC1_ENA	ISRC2_DEC2_ENA	ISRC2_DEC3_ENA	ISRC2_DEC4_ENA	0	0	0	0	0	ISRC2_NOTCH_ENA	0000h
R3830 (EF6h)	ISRC 3 CTRL 1	0	ISRC3_FSH [3:0]				0	0	0	0	0	0	0	0	0	0	0	0000h
R3831 (EF7h)	ISRC 3 CTRL 2	0	ISRC3_FSL [3:0]				0	0	0	0	0	0	0	0	0	0	0	0000h
R3832 (EF8h)	ISRC 3 CTRL 3	ISRC3_INT1_ENA	ISRC3_INT2_ENA	ISRC3_INT3_ENA	ISRC3_INT4_ENA	0	0	ISRC3_DEC1_ENA	ISRC3_DEC2_ENA	ISRC3_DEC3_ENA	ISRC3_DEC4_ENA	0	0	0	0	0	ISRC3_NOTCH_ENA	0000h
R4608 (1200h)	DSP2 Control 1	0	DSP2_RATE [3:0]				0	0	0	0	0	0	DSP2_MEM_ENA	DSP2_DBG_CLK_ENA	DSP2_SYS_ENA	DSP2_CORE_ENA	DSP2_START	0010h
R4609 (1201h)	DSP2 Clocking 1	0	0	0	0	0	0	0	0	0	0	0	0	0	DSP2_CLK_SEL [2:0]			0000h
R4612 (1204h)	DSP2 Status 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSP2_RAM_RDY	0000h
R4613 (1205h)	DSP2 Status 2	DSP2_PING_FULL	DSP2_PONG_FULL	0	0	0	0	0	0	DSP2_WDMA_ACTIVE_CHANNELS [7:0]								0000h
R4614 (1206h)	DSP2 Status 3	0	0	0	0	0	0	0	0	0	0	0	0	DSP2_CLK_SEL_STS [2:0]			DSP2_CLK_AVAIL	0000h
R4624 (1210h)	DSP2 WDMA Buffer 1	DSP2_START_ADDRESS_WDMA_BUFFER_0 [15:0]																0000h
R4625 (1211h)	DSP2 WDMA Buffer 2	DSP2_START_ADDRESS_WDMA_BUFFER_1 [15:0]																0000h
R4626 (1212h)	DSP2 WDMA Buffer 3	DSP2_START_ADDRESS_WDMA_BUFFER_2 [15:0]																0000h
R4627 (1213h)	DSP2 WDMA Buffer 4	DSP2_START_ADDRESS_WDMA_BUFFER_3 [15:0]																0000h
R4628 (1214h)	DSP2 WDMA Buffer 5	DSP2_START_ADDRESS_WDMA_BUFFER_4 [15:0]																0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R4629 (1215h)	DSP2 WDMA Buffer 6	DSP2_START_ADDRESS_WDMA_BUFFER_5 [15:0]																0000h
R4630 (1216h)	DSP2 WDMA Buffer 7	DSP2_START_ADDRESS_WDMA_BUFFER_6 [15:0]																0000h
R4631 (1217h)	DSP2 WDMA Buffer 8	DSP2_START_ADDRESS_WDMA_BUFFER_7 [15:0]																0000h
R4640 (1220h)	DSP2 RDMA Buffer 1	DSP2_START_ADDRESS_RDMA_BUFFER_0 [15:0]																0000h
R4641 (1221h)	DSP2 RDMA Buffer 2	DSP2_START_ADDRESS_RDMA_BUFFER_1 [15:0]																0000h
R4642 (1222h)	DSP2 RDMA Buffer 3	DSP2_START_ADDRESS_RDMA_BUFFER_2 [15:0]																0000h
R4643 (1223h)	DSP2 RDMA Buffer 4	DSP2_START_ADDRESS_RDMA_BUFFER_3 [15:0]																0000h
R4644 (1224h)	DSP2 RDMA Buffer 5	DSP2_START_ADDRESS_RDMA_BUFFER_4 [15:0]																0000h
R4645 (1225h)	DSP2 RDMA Buffer 6	DSP2_START_ADDRESS_RDMA_BUFFER_5 [15:0]																0000h
R4656 (1230h)	DSP2 WDMA Config 1	0	0	DSP2_WDMA_BUFFER_LENGTH [13:0]														0000h
R4657 (1231h)	DSP2 WDMA Config 2	0	0	0	0	0	0	0	0	DSP2_WDMA_CHANNEL_ENABLE [7:0]								0000h
R4658 (1232h)	DSP2 WDMA Offset 1	0	0	0	0	0	0	0	0	DSP2_WDMA_CHANNEL_OFFSET [7:0]								0000h
R4660 (1234h)	DSP2 RDMA Config 1	0	0	0	0	0	0	0	0	0	0	DSP2_RDMA_CHANNEL_ENABLE [5:0]						0000h
R4661 (1235h)	DSP2 RDMA Offset 1	0	0	0	0	0	0	0	0	0	0	DSP2_RDMA_CHANNEL_OFFSET [5:0]						0000h
R4664 (1238h)	DSP2 External Start Select 1	0	0	0	0	0	0	0	0	0	0	0	0	DSP2_START_IN_SEL [3:0]				0000h
R4672 (1240h)	DSP2 Scratch 0	DSP2_SCRATCH_0 [15:0]																0000h
R4673 (1241h)	DSP2 Scratch 1	DSP2_SCRATCH_1 [15:0]																0000h
R4674 (1242h)	DSP2 Scratch 2	DSP2_SCRATCH_2 [15:0]																0000h
R4675 (1243h)	DSP2 Scratch 3	DSP2_SCRATCH_3 [15:0]																0000h
R4864 (1300h)	DSP3 Control 1	0	DSP3_RATE [3:0]				0	0	0	0	0	0	DSP3_MEM_ENA	DSP3_DBG_CLK_ENA	DSP3_SYS_ENA	DSP3_CORE_ENA	DSP3_START	0010h
R4865 (1301h)	DSP3 Clocking 1	0	0	0	0	0	0	0	0	0	0	0	0	0	DSP3_CLK_SEL [2:0]			0000h
R4868 (1304h)	DSP3 Status 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSP3_RAM_RDY	0000h
R4869 (1305h)	DSP3 Status 2	DSP3_PING_FULL	DSP3_PONG_FULL	0	0	0	0	0	0	DSP3_WDMA_ACTIVE_CHANNELS [7:0]								0000h
R4870 (1306h)	DSP3 Status 3	0	0	0	0	0	0	0	0	0	0	0	0	DSP3_CLK_SEL_STS [2:0]			DSP3_CLK_AVAIL	0000h
R4871 (1307h)	DSP3 Status 4	DSP3_DUALMEM_COLLISION_ADDR [15:0]																0000h
R4880 (1310h)	DSP3 WDMA Buffer 1	DSP3_START_ADDRESS_WDMA_BUFFER_0 [15:0]																0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R4881 (1311h)	DSP3 WDMA Buffer 2	DSP3_START_ADDRESS_WDMA_BUFFER_1 [15:0]																0000h
R4882 (1312h)	DSP3 WDMA Buffer 3	DSP3_START_ADDRESS_WDMA_BUFFER_2 [15:0]																0000h
R4883 (1313h)	DSP3 WDMA Buffer 4	DSP3_START_ADDRESS_WDMA_BUFFER_3 [15:0]																0000h
R4884 (1314h)	DSP3 WDMA Buffer 5	DSP3_START_ADDRESS_WDMA_BUFFER_4 [15:0]																0000h
R4885 (1315h)	DSP3 WDMA Buffer 6	DSP3_START_ADDRESS_WDMA_BUFFER_5 [15:0]																0000h
R4886 (1316h)	DSP3 WDMA Buffer 7	DSP3_START_ADDRESS_WDMA_BUFFER_6 [15:0]																0000h
R4887 (1317h)	DSP3 WDMA Buffer 8	DSP3_START_ADDRESS_WDMA_BUFFER_7 [15:0]																0000h
R4896 (1320h)	DSP3 RDMA Buffer 1	DSP3_START_ADDRESS_RDMA_BUFFER_0 [15:0]																0000h
R4897 (1321h)	DSP3 RDMA Buffer 2	DSP3_START_ADDRESS_RDMA_BUFFER_1 [15:0]																0000h
R4898 (1322h)	DSP3 RDMA Buffer 3	DSP3_START_ADDRESS_RDMA_BUFFER_2 [15:0]																0000h
R4899 (1323h)	DSP3 RDMA Buffer 4	DSP3_START_ADDRESS_RDMA_BUFFER_3 [15:0]																0000h
R4900 (1324h)	DSP3 RDMA Buffer 5	DSP3_START_ADDRESS_RDMA_BUFFER_4 [15:0]																0000h
R4901 (1325h)	DSP3 RDMA Buffer 6	DSP3_START_ADDRESS_RDMA_BUFFER_5 [15:0]																0000h
R4912 (1330h)	DSP3 WDMA Config 1	0	0	DSP3_WDMA_BUFFER_LENGTH [13:0]														0000h
R4913 (1331h)	DSP3 WDMA Config 2	0	0	0	0	0	0	0	0	DSP3_WDMA_CHANNEL_ENABLE [7:0]								0000h
R4914 (1332h)	DSP3 WDMA Offset 1	0	0	0	0	0	0	0	0	DSP3_WDMA_CHANNEL_OFFSET [7:0]								0000h
R4916 (1334h)	DSP3 RDMA Config 1	0	0	0	0	0	0	0	0	0	0	DSP3_RDMA_CHANNEL_ENABLE [5:0]						0000h
R4917 (1335h)	DSP3 RDMA Offset 1	0	0	0	0	0	0	0	0	0	0	DSP3_RDMA_CHANNEL_OFFSET [5:0]						0000h
R4920 (1338h)	DSP3 External Start Select 1	0	0	0	0	0	0	0	0	0	0	0	0	DSP3_START_IN_SEL [3:0]				0000h
R4928 (1340h)	DSP3 Scratch 0	DSP3_SCRATCH_0 [15:0]																0000h
R4929 (1341h)	DSP3 Scratch 1	DSP3_SCRATCH_1 [15:0]																0000h
R4930 (1342h)	DSP3 Scratch 2	DSP3_SCRATCH_2 [15:0]																0000h
R4931 (1343h)	DSP3 Scratch 3	DSP3_SCRATCH_3 [15:0]																0000h
Control Write Sequencer Memory																		
R12288 (3000h)	WSEQ Sequence 1	WSEQ_DATA_WIDTH0 [2:0]			WSEQ_ADDR0 [12:0]													
R12289 (3001h)	WSEQ Sequence 2	WSEQ_DELAY0 [3:0]				WSEQ_DATA_START0 [3:0]				WSEQ_DATA0 [7:0]								
R12290 (3002h)	WSEQ Sequence 3	WSEQ_DATA_WIDTH1 [2:0]			WSEQ_ADDR1 [12:0]													
R12291 (3003h)	WSEQ Sequence 4	WSEQ_DELAY1 [3:0]				WSEQ_DATA_START1 [3:0]				WSEQ_DATA1 [7:0]								
		(Similar for WSEQ Index 2…508)																

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R13306 (33FAh)	WSEQ Sequence 1019	WSEQ_DATA_WIDTH509 [2:0]			WSEQ_ADDR509 [12:0]													
R13307 (33FBh)	WSEQ Sequence 1020	WSEQ_DELAY509 [3:0]				WSEQ_DATA_START509 [3:0]				WSEQ_DATA509 [7:0]								
DSP2 Firmware Memory																		
R2097152 (20_0000h)	DSP2 PM 0	0	0	0	0	0	0	0	0	DSP2_PM_0 [39:32]								0000h
R2097153 (20_0001h)	DSP2 PM 1	DSP2_PM_0 [31:16]																0000h
R2097154 (20_0002h)	DSP2 PM 2	DSP2_PM_0 [15:0]																0000h
R2097155 (20_0003h)	DSP2 PM 3	0	0	0	0	0	0	0	0	DSP2_PM_1 [39:32]								0000h
R2097156 (20_0004h)	DSP2 PM 4	DSP2_PM_1 [31:16]																0000h
R2097157 (20_0005h)	DSP2 PM 5	DSP2_PM_1 [15:0]																0000h
		(Similar for DSP2 Program Memory 2 … 8190)																
R2121725 (20_5FFDh)	DSP2 PM 24573	0	0	0	0	0	0	0	0	DSP2_PM_8191 [39:32]								0000h
R2121726 (20_5FFEh)	DSP2 PM 24574	DSP2_PM_8191 [31:16]																0000h
R2121727 (20_5FFFh)	DSP2 PM 24575	DSP2_PM_8191 [15:0]																0000h
R2621440 (28_0000h)	DSP2 ZM 0	0	0	0	0	0	0	0	0	DSP2_ZM_0 [23:16]								0000h
R2621441 (28_0001h)	DSP2 ZM 1	DSP2_ZM_0 [15:0]																0000h
R2621442 (28_0002h)	DSP2 ZM 2	0	0	0	0	0	0	0	0	DSP2_ZM_1 [23:16]								0000h
R2621443 (28_0003h)	DSP2 ZM 3	DSP2_ZM_1 [15:0]																0000h
		(Similar for DSP2 Coefficient Memory 2 … 4094)																
R2629630 (28_1FFEh)	DSP2 ZM 8190	0	0	0	0	0	0	0	0	DSP2_ZM_4095 [23:16]								0000h
R2629631 (28_1FFFh)	DSP2 ZM 8191	DSP2_ZM_4095 [15:0]																0000h
R2686976 (29_0000h)	DSP2 XM 0	0	0	0	0	0	0	0	0	DSP2_XM_0 [23:16]								0000h
R2686977 (29_0001h)	DSP2 XM 1	DSP2_XM_0 [15:0]																0000h
R2686978 (29_0002h)	DSP2 XM 2	0	0	0	0	0	0	0	0	DSP2_XM_1 [23:16]								0000h
R2686979 (29_0003h)	DSP2 XM 3	DSP2_XM_1 [15:0]																0000h
		(Similar for DSP2 X Data Memory 2 … 24574)																
R2736126 (29_BFFEh)	DSP2 XM 49150	0	0	0	0	0	0	0	0	DSP2_XM_24575 [23:16]								0000h
R2736127 (29_BFFFh)	DSP2 XM 49151	DSP2_XM_24575 [15:0]																0000h
R2777088 (2A_6000h)	DSP2 XM EXT 0	0	0	0	0	0	0	0	0	DSP2_XM_EXT_0 [23:16]								0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R2777089 (2A_6001h)	DSP2 XM EXT 1	DSP2_XM_EXT_0 [15:0]																0000h
R2777090 (2A_6002h)	DSP2 XM EXT 2	0	0	0	0	0	0	0	0	DSP2_XM_EXT_1 [23:16]								0000h
R2777091 (2A_6003h)	DSP2 XM EXT 3	DSP2_XM_EXT_1 [15:0]																0000h
		(Similar for DSP2 X Data Memory 2 … 4094)																
R2785278 (2A_7FFEh)	DSP2 XM EXT 8190	0	0	0	0	0	0	0	0	DSP2_XM_EXT_4095 [23:16]								0000h
R2785279 (2A_7FFFh)	DSP2 XM EXT 8191	DSP2_XM_EXT_4095 [15:0]																0000h
R2785280 (2A_8000h)	DSP2 YM 0	0	0	0	0	0	0	0	0	DSP2_YM_0 [23:16]								0000h
R2785281 (2A_8001h)	DSP2 YM 1	DSP2_YM_0 [15:0]																0000h
R2785282 (2A_8002h)	DSP2 YM 2	0	0	0	0	0	0	0	0	DSP2_YM_1 [23:16]								0000h
R2785283 (2A_8003h)	DSP2 YM 3	DSP2_YM_1 [15:0]																0000h
		(Similar for DSP2 Y Data Memory 2 … 24574)																
R2834430 (2B_3FFEh)	DSP2 YM 49150	0	0	0	0	0	0	0	0	DSP2_YM_24575 [23:16]								0000h
R2834431 (2B_3FFFh)	DSP2 YM 49151	DSP2_YM_24575 [15:0]																0000h
DSP3 Firmware Memory																		
R3145728 (30_0000h)	DSP3 PM 0	0	0	0	0	0	0	0	0	DSP3_PM_0 [39:32]								0000h
R3145729 (30_0001h)	DSP3 PM 1	DSP3_PM_0 [31:16]																0000h
R3145730 (30_0002h)	DSP3 PM 2	DSP3_PM_0 [15:0]																0000h
R3145731 (30_0003h)	DSP3 PM 3	0	0	0	0	0	0	0	0	DSP3_PM_1 [39:32]								0000h
R3145732 (30_0004h)	DSP3 PM 4	DSP3_PM_1 [31:16]																0000h
R3145733 (30_0005h)	DSP3 PM 5	DSP3_PM_1 [15:0]																0000h
		(Similar for DSP3 Program Memory 2 … 12286)																
R3182589 (30_8FFDh)	DSP3 PM 36861	0	0	0	0	0	0	0	0	DSP3_PM_12287 [39:32]								0000h
R3182590 (30_8FFEh)	DSP3 PM 36862	DSP3_PM_12287 [31:16]																0000h
R3182591 (30_8FFFh)	DSP3 PM 36863	DSP3_PM_12287 [15:0]																0000h
R3670016 (38_0000h)	DSP3 ZM 0	0	0	0	0	0	0	0	0	DSP3_ZM_0 [23:16]								0000h
R3670017 (38_0001h)	DSP3 ZM 1	DSP3_ZM_0 [15:0]																0000h
R3670018 (38_0002h)	DSP3 ZM 2	0	0	0	0	0	0	0	0	DSP3_ZM_1 [23:16]								0000h
R3670019 (38_0003h)	DSP3 ZM 3	DSP3_ZM_1 [15:0]																0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
		(Similar for DSP3 Coefficient Memory 2 … 4094)																
R3678206 (38_1FFEh)	DSP3 ZM 8190	0	0	0	0	0	0	0	0	DSP3_ZM_4095 [23:16]								0000h
R3678207 (38_1FFFh)	DSP3 ZM 8191	DSP3_ZM_4095 [15:0]																0000h
R3735552 (39_0000h)	DSP3 XM 0	0	0	0	0	0	0	0	0	DSP3_XM_0 [23:16]								0000h
R3735553 (39_0001h)	DSP3 XM 1	DSP3_XM_0 [15:0]																0000h
R3735554 (39_0002h)	DSP3 XM 2	0	0	0	0	0	0	0	0	DSP3_XM_1 [23:16]								0000h
R3735555 (39_0003h)	DSP3 XM 3	DSP3_XM_1 [15:0]																0000h
		(Similar for DSP3 X Data Memory 2 … 36864)																
R3809278 (3A_1FEEh)	DSP3 XM 73730	0	0	0	0	0	0	0	0	DSP3_XM_36865 [23:16]								0000h
R3809279 (3A_1FFFh)	DSP3 XM 73731	DSP3_XM_36865 [15:0]																0000h
R3825664 (3A_6000h)	DSP3 XM EXT 0	0	0	0	0	0	0	0	0	DSP3_XM_EXT_0 [23:16]								0000h
R3825665 (3A_6001h)	DSP3 XM EXT 1	DSP3_XM_EXT_0 [15:0]																0000h
R3825666 (3A_6002h)	DSP3 XM EXT 2	0	0	0	0	0	0	0	0	DSP3_XM_EXT_1 [23:16]								0000h
R3825667 (3A_6003h)	DSP3 XM EXT 3	DSP3_XM_EXT_1 [15:0]																0000h
		(Similar for DSP3 X Data Memory 2 … 4094)																
R3833854 (3A_7FFEh)	DSP3 XM EXT 8190	0	0	0	0	0	0	0	0	DSP3_XM_EXT_4095 [23:16]								0000h
R3833855 (3A_7FFFh)	DSP3 XM EXT 8191	DSP3_XM_EXT_4095 [15:0]																0000h
R3833856 (3A_8000h)	DSP3 YM 0	0	0	0	0	0	0	0	0	DSP3_YM_0 [23:16]								0000h
R3833857 (3A_8001h)	DSP3 YM 1	DSP3_YM_0 [15:0]																0000h
R3833858 (3A_8002h)	DSP3 YM 2	0	0	0	0	0	0	0	0	DSP3_YM_1 [23:16]								0000h
R3833859 (3A_8003h)	DSP3 YM 3	DSP3_YM_1 [15:0]																0000h
		(Similar for DSP3 Y Data Memory 2 … 24574)																
R3883006 (3B_3FFEh)	DSP3 YM 49150	0	0	0	0	0	0	0	0	DSP3_YM_24575 [23:16]								0000h
R3883007 (3B_3FFFh)	DSP3 YM 49151	DSP3_YM_24575 [15:0]																0000h

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

DIGITAL MICROPHONE INPUT PATHS

The CS47L24 provides up to 4 digital microphone input paths; two channels of audio data can be multiplexed on each of the DMICDATn pins. Each of these stereo pairs is clocked using the respective DMICCLKn pin.

The external connections for digital microphones, incorporating the CS47L24 microphone bias circuit, are shown later in the “Microphone Bias Circuit” section - see Figure 53.

Ceramic decoupling capacitors for the digital microphones may be required - refer to the specific recommendations for the application microphone(s).

When two microphones are connected to a single DMICDAT pin, the microphones must be configured to ensure that the Left mic transmits a data bit when DMICCLK is high, and the Right mic transmits a data bit when DMICCLK is low. The CS47L24 samples the digital microphone data at the end of each DMICCLK phase. Each microphone must tri-state its data output when the other microphone is transmitting. Integrated pull-down resistors can be enabled on the DMICDAT pins if required.

The voltage reference for each digital microphone interface is selectable. It is important that the selected reference for the CS47L24 interface is compatible with the applicable configuration of the external microphone.

MICROPHONE BIAS CIRCUIT

The CS47L24 is designed to interface easily with up to 4 digital microphones. Each microphone requires a supply voltage, which can be provided by the MICBIAS1 or MICBIAS2 regulators on the CS47L24.

Note that the MICVDD supply can also be used (instead of MICBIASn) as a reference or power supply for external microphones. The MICBIAS outputs are recommended, as these offer better noise performance and independent enable/disable control.

Digital microphone connection to the CS47L24 is illustrated in Figure 53.

Ceramic decoupling capacitors for the digital microphones may be required - refer to the specific recommendations for the application microphone(s).

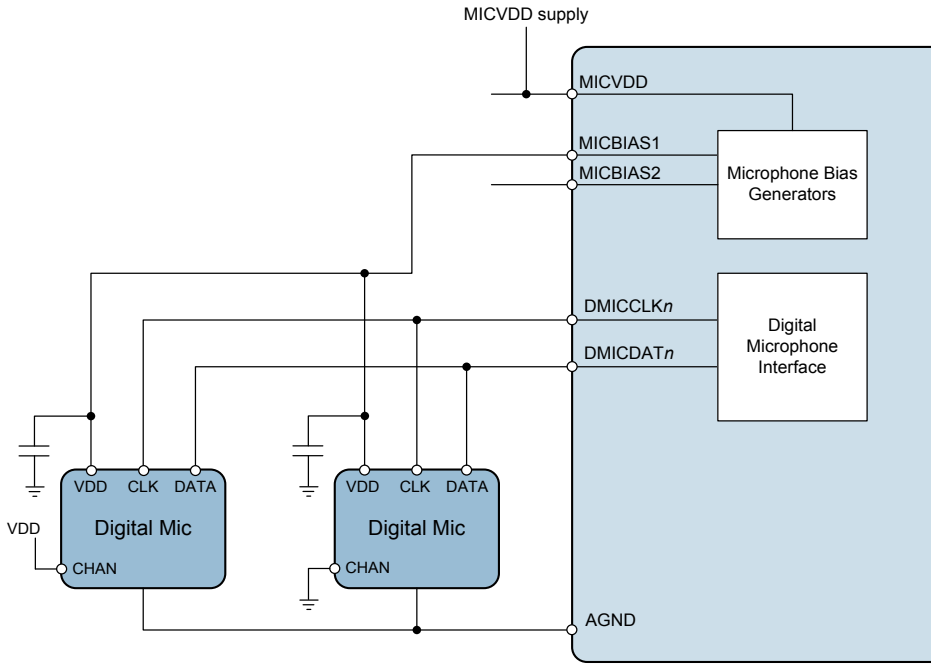


Figure 53 Digital Microphone Connection

The MICBIAS generators can each operate as a voltage regulator or in bypass mode. See “Charge Pump, Regulators and Voltage Reference” for details of the MICBIAS generators.

In Regulator mode, the MICBIAS regulators are designed to operate without external decoupling capacitors. The regulators can be configured to support a capacitive load if required (e.g., for digital microphone supply decoupling). The compatible load conditions are detailed in the “Electrical Characteristics” section.

If the capacitive load on MICBIAS1 or MICBIAS2 exceeds the specified conditions for Regulator mode (e.g., due to a decoupling capacitor or long PCB trace), then the respective generator must be configured in Bypass mode.

The maximum output current for each MICBIAS*n* pin is noted in the “Electrical Characteristics”. This limit must be observed on each MICBIAS output, especially if more than one microphone is connected to a single MICBIAS pin. Note that the maximum output current differs between Regulator mode and Bypass mode. The MICBIAS output voltage can be adjusted using register control in Regulator mode.

HEADPHONE DRIVER OUTPUT PATH

The CS47L24 provides a stereo headphone output driver. The headphone outputs are ground-referenced, allowing direct connection to the external load(s). There is no requirement for DC blocking capacitors.

In single-ended (default) configuration, the headphone output comprises 2 independently controlled output channels, for stereo headphone or line outputs. In mono (BTL) mode, the headphone drivers provide a differential output, suitable for a mono earpiece or hearing coil load.

The headphone outputs incorporate a common mode, or ground loop, feedback path which provides rejection of system-related ground noise. The feedback pin must be connected to ground for normal operation of the headphone outputs.

The feedback pin should be connected to GND close to the respective headphone jack, as illustrated in Figure 54. In mono (differential) mode, the feedback pin should be connected to the ground plane that is physically closest to the respective output PCB tracks.

It is recommended to ensure that the electrical characteristics of the PCB traces for each output pair are closely matched. This is particularly important to matching the two traces of a differential (BTL) output.

Typical headphone connections are illustrated in Figure 54.

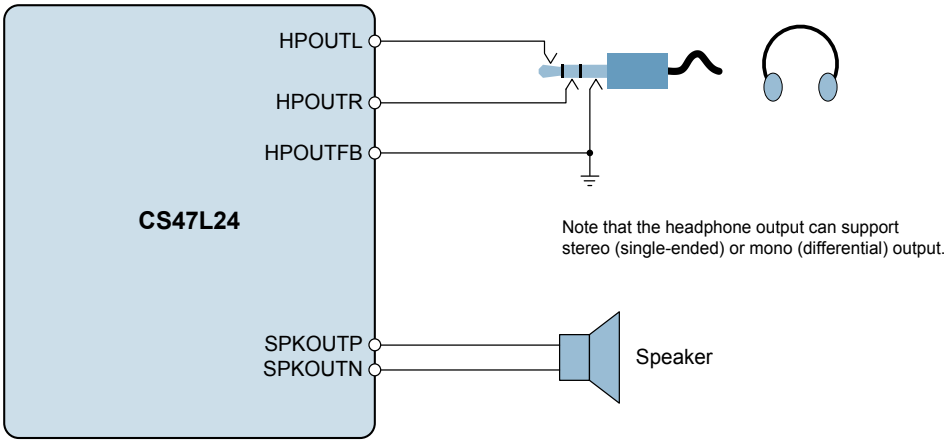


Figure 54 Headphone and Speaker Connections

It is common for ESD diodes to be wired to pins that link to external connectors. This provides protection from potentially harmful ESD effects. In a typical application, ESD diodes would be recommended for the headphone paths (HPOUT), when used as external headphone or line output.

The HPOUT outputs are ground-referenced, and the respective voltages may swing between +1.8V and -1.8V. The ESD diode configuration must be carefully chosen.

The recommended ESD diode configuration for these ground-referenced outputs is illustrated in Figure 55. The ‘back-to-back’ arrangement is necessary in order to prevent clipping and distortion of the output signal.

Note that similar care is required when connecting the CS47L24 outputs to external circuits that provide input path ESD protection - the configuration on those input circuits must be correctly designed to accommodate ground-referenced signals.

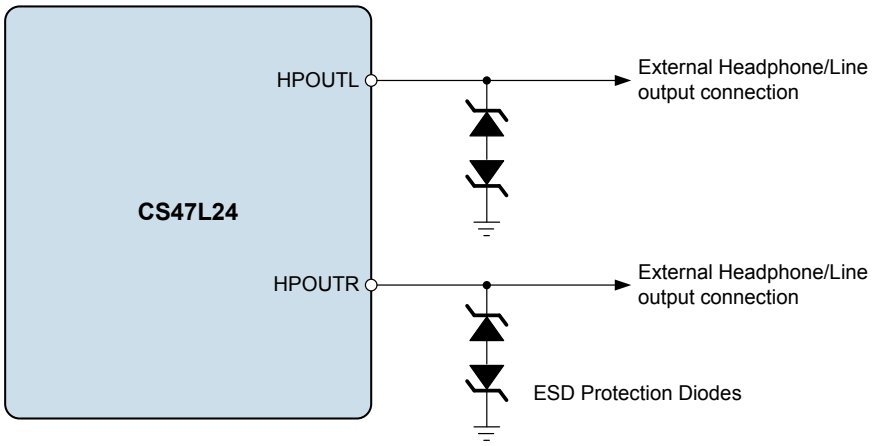


Figure 55 ESD Diode Configuration for External Output Connections

SPEAKER DRIVER OUTPUT PATH

The CS47L24 incorporates a Class D speaker driver, offering high amplifier efficiency at large signal levels. As the Class D output is a pulse width modulated signal, the choice of speakers and tracking of signals is critical for ensuring good performance and reducing EMI in this mode.

The efficiency of the speaker drivers is affected by the series resistance between the CS47L24 and the speaker (e.g. PCB track loss and inductor ESR) as shown in Figure 56. This resistance should be as low as possible to maximise efficiency.

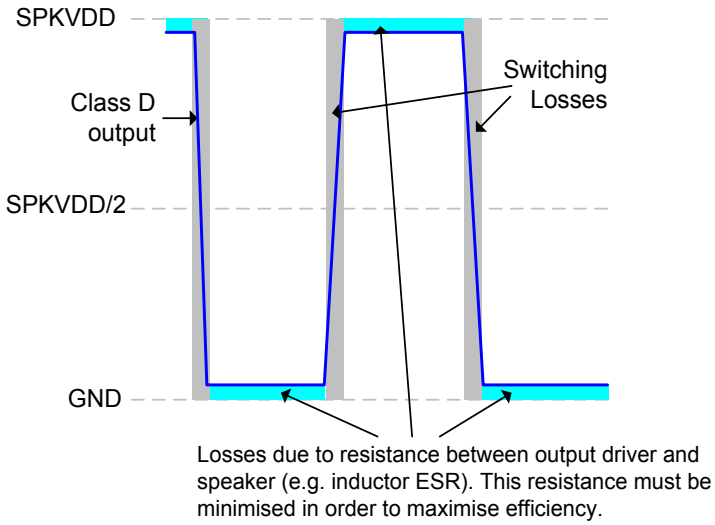


Figure 56 Speaker Connection Losses

The Class D output requires external filtering in order to recreate the audio signal. This may be implemented using a 2nd order LC or 1st order RC filter, or else may be achieved by using a loudspeaker whose internal inductance provides the required filter response. An LC or RC filter should be used if the loudspeaker characteristics are unknown or unsuitable, or if the length of the loudspeaker connection is likely to lead to EMI problems.

In applications where it is necessary to provide Class D filter components, a 2nd order LC filter is the recommended solution as it provides more attenuation at higher frequencies and minimises power dissipated in the filter when compared to a first order RC filter (lower ESR). This maximises both rejection of unwanted switching frequencies and overall speaker efficiency. A suitable implementation is illustrated in Figure 57.

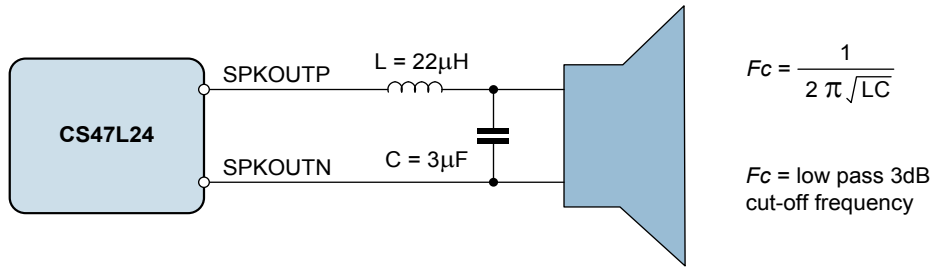


Figure 57 Class D Output Filter Components

A simple equivalent circuit of a loudspeaker consists of a serially connected resistor and inductor, as shown in Figure 58. This circuit provides a low pass filter for the speaker output. If the loudspeaker characteristics are suitable, then the loudspeaker itself can be used in place of the filter components described earlier. This is known as 'filterless' operation.

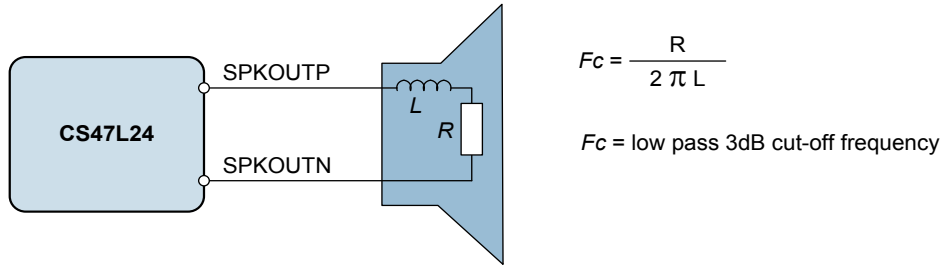


Figure 58 Speaker Equivalent Circuit for Filterless Operation

For filterless Class D operation, it is important to ensure that a speaker with suitable inductance is chosen. For example, if we know the speaker impedance is 8Ω and the desired cut-off frequency is 20kHz, then the optimum speaker inductance may be calculated as:

$$L = \frac{R}{2 \pi Fc} = \frac{8\Omega}{2 \pi * 20kHz} = 64\mu H$$

8Ω loudspeakers typically have an inductance in the range 20µH to 100µH, however, it should be noted that a loudspeaker inductance will not be constant across the relevant frequencies for Class D operation (up to and beyond the Class D switching frequency). Care should be taken to ensure that the cut-off frequency of the loudspeaker's filtering is low enough to suppress the high frequency energy of the Class D switching and, in so doing, to prevent speaker damage. The Class D outputs of the CS47L24 operate at much higher frequencies than is recommended for most speakers and it must be ensured that the cut-off frequency is low enough to protect the speaker.

POWER SUPPLY / REFERENCE DECOUPLING

Electrical coupling exists particularly in digital logic systems where switching in one sub-system causes fluctuations on the power supply. This effect occurs because the inductance of the power supply acts in opposition to the changes in current flow that are caused by the logic switching. The resultant variations ('spikes') in the power supply voltage can cause malfunctions and unintentional behaviour in other components. A decoupling ('bypass') capacitor can be used as an energy storage component which will provide power to the decoupled circuit for the duration of these power supply variations, protecting it from malfunctions that could otherwise arise.

Coupling also occurs in a lower frequency form when ripple is present on the power supply rail caused by changes in the load current or by limitations of the power supply regulation method. In audio components such as the CS47L24, these variations can alter the performance of the signal path, leading to degradation in signal quality. A decoupling capacitor can be used to filter these effects, by presenting the ripple voltage with a low impedance path that does not affect the circuit to be decoupled.

These coupling effects are addressed by placing a capacitor between the supply rail and the corresponding ground reference. In the case of systems comprising multiple power supply rails, decoupling should be provided on each rail.

The recommended power supply decoupling capacitors for CS47L24 are detailed below in Table 96.

POWER SUPPLY	DECOUPLING CAPACITOR
DBVDD	0.1µF ceramic (see Note)
AVDD	1.0µF ceramic
CPVDD	4.7µF ceramic
MICVDD	1.0µF ceramic
DCVDD	4.7µF ceramic
SPKVDD	4.7µF ceramic
VREFC	2.2µF ceramic

Table 96 Power Supply Decoupling Capacitors

Note: 0.1µF is required with 4.7µF a guide to the total required power rail capacitance.

All decoupling capacitors should be placed as close as possible to the CS47L24 device. The connection between AGND, the AVDD decoupling capacitor and the main system ground should be made at a single point as close as possible to the AGND balls of the CS47L24.

Due to the wide tolerance of many types of ceramic capacitors, care must be taken to ensure that the selected components provide the required capacitance across the required temperature and voltage ranges in the intended application. For most application the use of ceramic capacitors with capacitor dielectric X5R is recommended.

CHARGE PUMP COMPONENTS

The CS47L24 incorporates a Charge Pump circuit, which generates the CPVOUTP and CPVOUTN supply rails for the ground-referenced headphone drivers.

Decoupling capacitors are required on each of the Charge Pump outputs. Two fly-back capacitors are also required.

The recommended Charge Pump capacitors for CS47L24 are detailed below in Table 97.

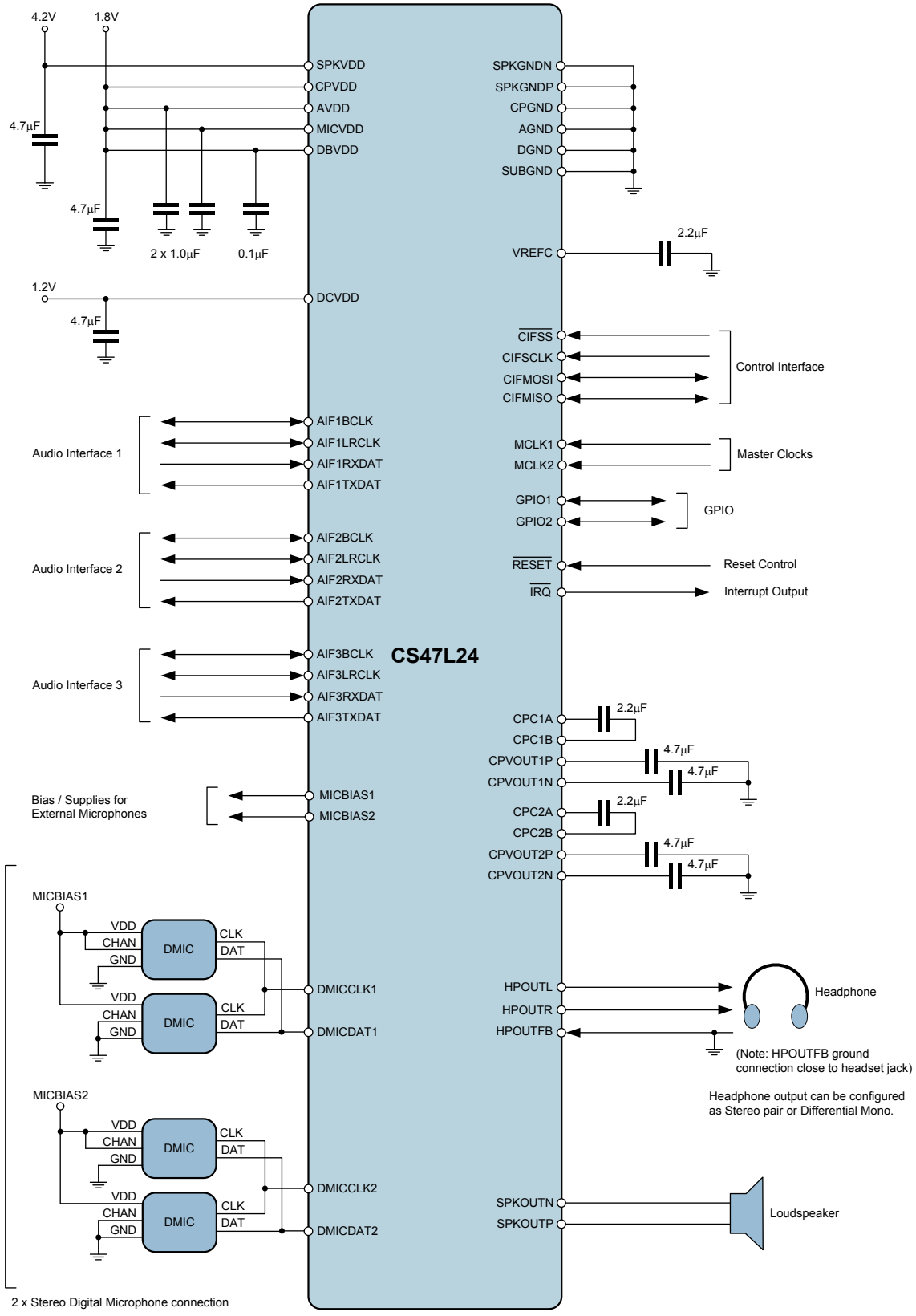
DESCRIPTION	CAPACITOR
CPVOUT1P decoupling	Required capacitance is 2.0µF at 2V. Suitable component typically 4.7µF.
CPVOUT1N decoupling	Required capacitance is 2.0µF at 2V. Suitable component typically 4.7µF.
CP fly-back 1 (connect between CPC1A and CPC1B)	Required capacitance is 1.0µF at 2V. Suitable component typically 2.2µF.
CPVOUT2P decoupling	Required capacitance is 2.0µF at 2V. Suitable component typically 4.7µF.
CPVOUT2N decoupling	Required capacitance is 2.0µF at 2V. Suitable component typically 4.7µF.
CP fly-back 2 (connect between CPC2A and CPC2B)	Required capacitance is 1.0µF at 2V. Suitable component typically 2.2µF.

Table 97 Charge Pump External Capacitors

Ceramic capacitors are recommended for these Charge Pump requirements. Note that, due to the wide tolerance of many types of ceramic capacitors, care must be taken to ensure that the selected components provide the required capacitance across the required temperature and voltage ranges in the intended application. Ceramic capacitors with X5R dielectric are recommended.

The positioning of the Charge Pump capacitors is important, particularly the fly-back capacitors. These capacitors should be placed as close as possible to the CS47L24.

RECOMMENDED EXTERNAL COMPONENTS DIAGRAM



RESETS SUMMARY

The contents of Table 98 provide a summary of the CS47L24 registers and other programmable memory under different reset conditions. The associated events and conditions are listed below.

- A Power-On Reset occurs when DCVDD, DBVDD or AVDD is below its respective reset threshold.
- A Hardware Reset occurs when the $\overline{\text{RESET}}$ input is asserted (logic 0).
- A Software Reset occurs when register R0 is written to.

	CONTROL SEQUENCER MEMORY	DSP FIRMWARE MEMORY	ALL OTHER REGISTERS
Power-On Reset	Reset	Reset	Reset
Hardware Reset	Retained	Configurable (see note)	Reset
Software Reset	Retained	Configurable (see note)	Reset

Table 98 Memory Reset Summary

See “DSP Firmware Control” for details of the configurable DSP memory behaviour.

Note that, to retain the DSP firmware memory contents during Hardware Reset or Software Reset, it must be ensured that DCVDD is held above its reset threshold.

OUTPUT SIGNAL DRIVE STRENGTH CONTROL

The CS47L24 supports configurable drive strength control for the digital output pins. This can be used to assist system-level integration and design considerations.

The drive strength control registers are described in Table 99. Note that, in the case of bi-directional pins (e.g., GPIOn), the drive strength control registers are only applicable when the pin is configured as an output.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3120 (0C30h) Misc Pad Ctrl 7	10	CIFMISO_DRV_STR	1	CIFMISO output drive strength 0 = 4mA 1 = 8mA
R3122 (0C32h) Misc Pad Ctrl 9	10	AIF1LRCLK_DRV_STR	1	AIF1LRCLK output drive strength 0 = 4mA 1 = 8mA
	2	GPIO1_DRV_STR	1	GPIO1 output drive strength 0 = 4mA 1 = 8mA
R3123 (0C33h) Misc Pad Ctrl 10	10	AIF1BCLK_DRV_STR	1	AIF1BCLK output drive strength 0 = 4mA 1 = 8mA
	2	AIF1TXDAT_DRV_STR	1	AIF1TXDAT output drive strength 0 = 4mA 1 = 8mA
R3124 (0C34h) Misc Pad Ctrl 11	10	AIF2LRCLK_DRV_STR	1	AIF2LRCLK output drive strength 0 = 4mA 1 = 8mA
	2	GPIO2_DRV_STR	1	GPIO2 output drive strength 0 = 4mA 1 = 8mA
R3125 (0C35h) Misc Pad Ctrl 12	10	AIF2BCLK_DRV_STR	1	AIF2BCLK output drive strength 0 = 4mA 1 = 8mA
	2	AIF2TXDAT_DRV_STR	1	AIF2TXDAT output drive strength 0 = 4mA 1 = 8mA
R3126 (0C36h) Misc Pad Ctrl 13	10	AIF3LRCLK_DRV_STR	1	AIF3LRCLK output drive strength 0 = 4mA 1 = 8mA
R3127 (0C37h) Misc Pad Ctrl 14	10	AIF3BCLK_DRV_STR	1	AIF3BCLK output drive strength 0 = 4mA 1 = 8mA
	2	AIF3TXDAT_DRV_STR	1	AIF3TXDAT output drive strength 0 = 4mA 1 = 8mA
R3129 (0C39h) Misc Pad Ctrl 16	10	IRQ_DRV_STR	1	IRQ output drive strength 0 = 4mA 1 = 8mA

Table 99 Output Drive Strength and Slew Rate Control

DIGITAL AUDIO INTERFACE CLOCKING CONFIGURATIONS

The digital audio interfaces (AIF1, AIF2, AIF3) can be configured in Master or Slave modes. In all applications, it is important that the system clocking configuration is correctly designed. Incorrect clock configurations will lead to audible clicks arising from dropped or repeated audio samples; this is caused by the inherent tolerances of multiple asynchronous system clocks.

To ensure reliable clocking of the audio interface functions, it is a requirement that the external interface clocks (e.g., BCLK, LRCLK) are derived from the same clock source as SYSCLK (or ASYNCCLK, where applicable).

In AIF Master mode, the external BCLK and LRCLK signals are generated by the CS47L24 and synchronisation of these signals with SYSCLK (or ASYNCCLK) is ensured. In this case, clocking of the AIF is typically derived from the MCLK1 or MCLK2 inputs, either directly or via one of the Frequency Locked Loop (FLL) circuits. It is also possible to use a different interface to provide the reference clock to which the AIF Master can be synchronised.

In AIF Slave mode, the external BCLK and LRCLK signals are generated by another device, as inputs to the CS47L24. In this case, it must be ensured that the applicable system clock (SYSCLK or ASYNCCLK) is generated from a source that is synchronised to the external BCLK and LRCLK inputs.

In a typical Slave mode application, the BCLK input is selected as the clock reference, using the FLL to perform frequency shifting. It is also possible to use the MCLK1 or MCLK2 inputs, but only if the selected clock is synchronised externally to the BCLK and LRCLK inputs.

The valid AIF clocking configurations are listed in Table 100 for AIF Master and AIF Slave modes.

The applicable system clock (SYSCLK or ASYNCCLK) depends on the AIFn_RATE setting for the relevant digital audio interface; if AIFn_RATE < 1000, then SYSCLK is applicable; if AIFn_RATE ≥ 1000, then ASYNCCLK is applicable.

AIF MODE	CLOCKING CONFIGURATION
AIF Master Mode	SYSCLK_SRC (ASYNCCLK_SRC) selects MCLK1 or MCLK2 as SYSCLK (ASYNCCLK) source.
	SYSCLK_SRC (ASYNCCLK_SRC) selects FLLn as SYSCLK (ASYNCCLK) source; FLLn_REFCLK_SRC selects MCLK1 or MCLK2 as FLLn source.
	SYSCLK_SRC (ASYNCCLK_SRC) selects FLLn as SYSCLK (ASYNCCLK) source; FLLn_REFCLK_SRC selects a different interface (BCLK, LRCLK) as FLLn source.
AIF Slave Mode	SYSCLK_SRC (ASYNCCLK_SRC) selects FLLn as SYSCLK (ASYNCCLK) source; FLLn_REFCLK_SRC selects BCLK as FLLn source.
	SYSCLK_SRC (ASYNCCLK_SRC) selects MCLK1 or MCLK2 as SYSCLK (ASYNCCLK) source, provided MCLK is externally synchronised to the BCLK input.
	SYSCLK_SRC (ASYNCCLK_SRC) selects FLLn as SYSCLK (ASYNCCLK) source; FLLn_REFCLK_SRC selects MCLK1 or MCLK2 as FLLn source, provided MCLK is externally synchronised to the BCLK input.
	SYSCLK_SRC (ASYNCCLK_SRC) selects FLLn as SYSCLK (ASYNCCLK) source; FLLn_REFCLK_SRC selects a different interface as FLLn source, provided the other interface is externally synchronised to the BCLK input.

Table 100 Audio Interface (AIF) Clocking Confgurations

In each case, the SYSCLK (ASYNCCLK) frequency must be a valid ratio to the LRCLK frequency; the supported clocking rates are defined by the SYSCLK_FREQ (ASYNC_CLK_FREQ) and SAMPLE_RATE_n (ASYNC_SAMPLE_RATE_n) registers.

The valid AIF clocking configurations are illustrated in Figure 59 to Figure 65 below. Note that, where MCLK1 is illustrated as the clock source, it is equally possible to select MCLK2 as the clock source. Similarly, in cases where FLL1 is illustrated, it is equally possible to select FLL2.

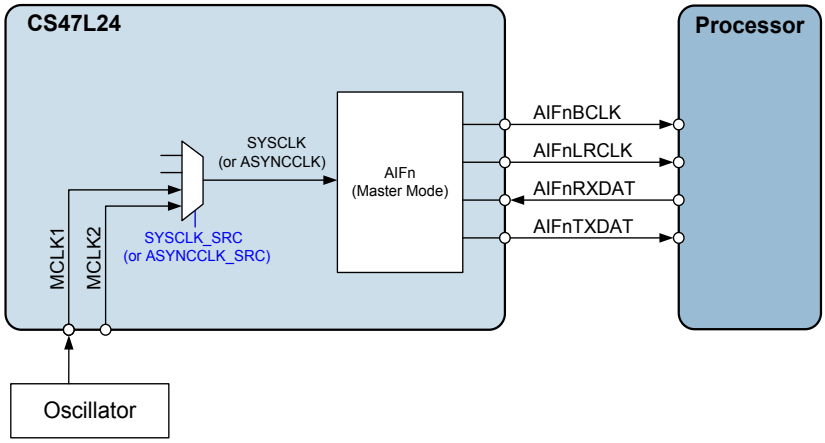


Figure 59 AIF Master Mode, using MCLK as Reference

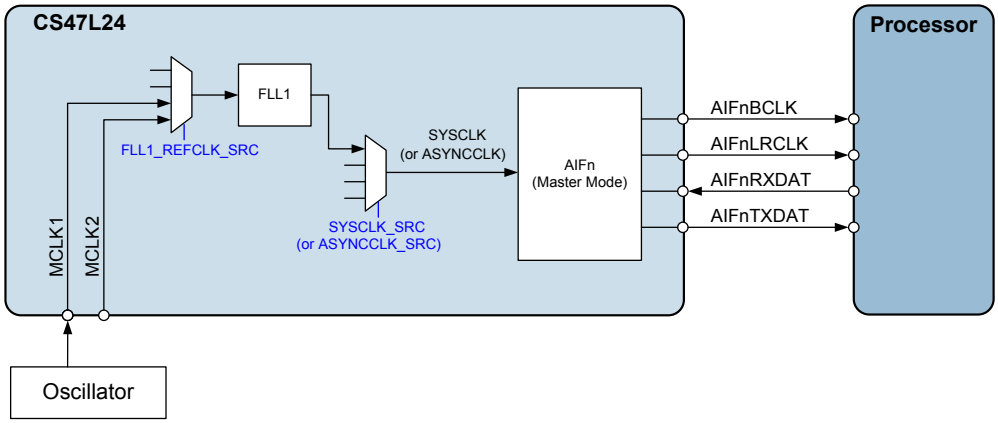


Figure 60 AIF Master Mode, using MCLK and FLL as Reference

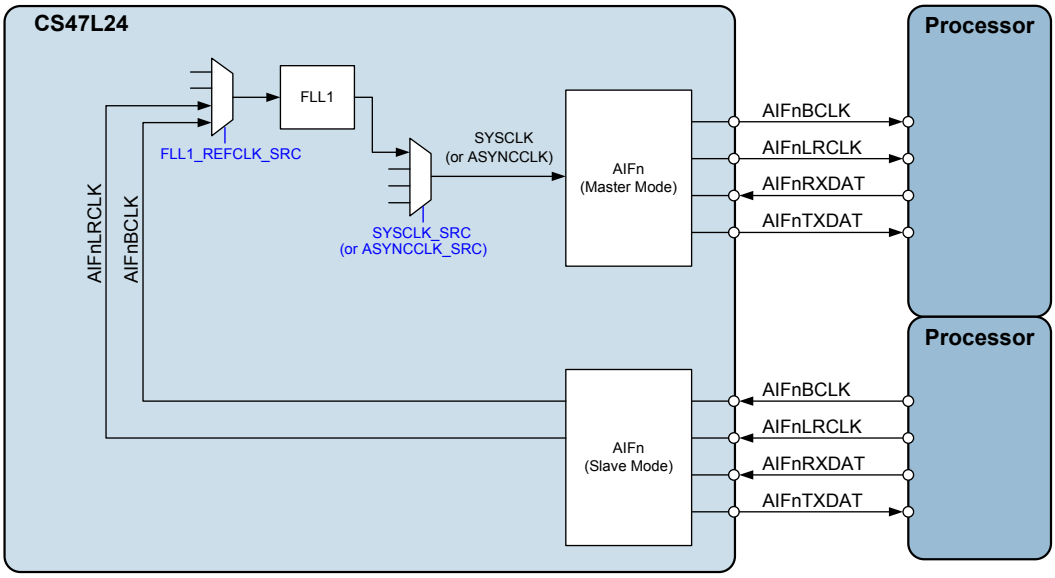


Figure 61 AIF Master Mode, using another Interface as Reference

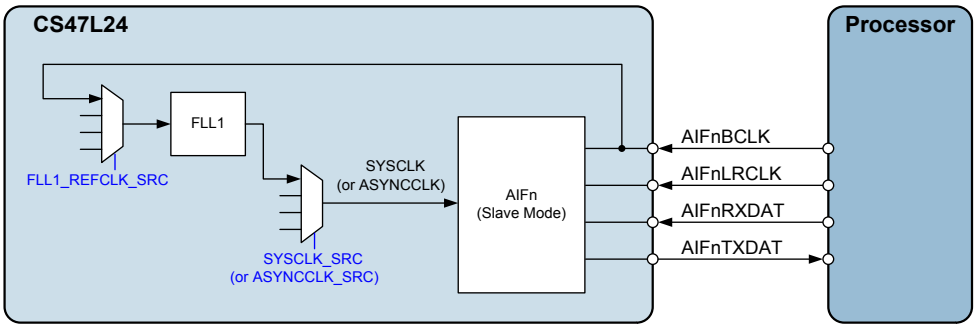


Figure 62 AIF Slave Mode, using BCLK and FLL as Reference

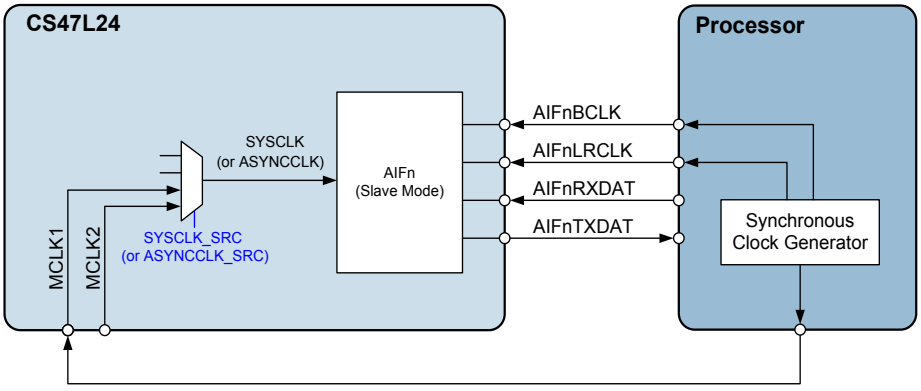


Figure 63 AIF Slave Mode, using MCLK as Reference

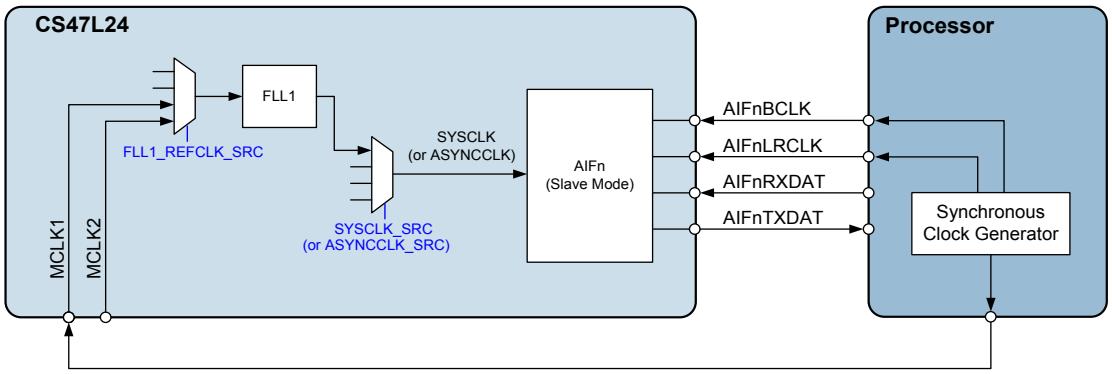


Figure 64 AIF Slave Mode, using MCLK and FLL as Reference

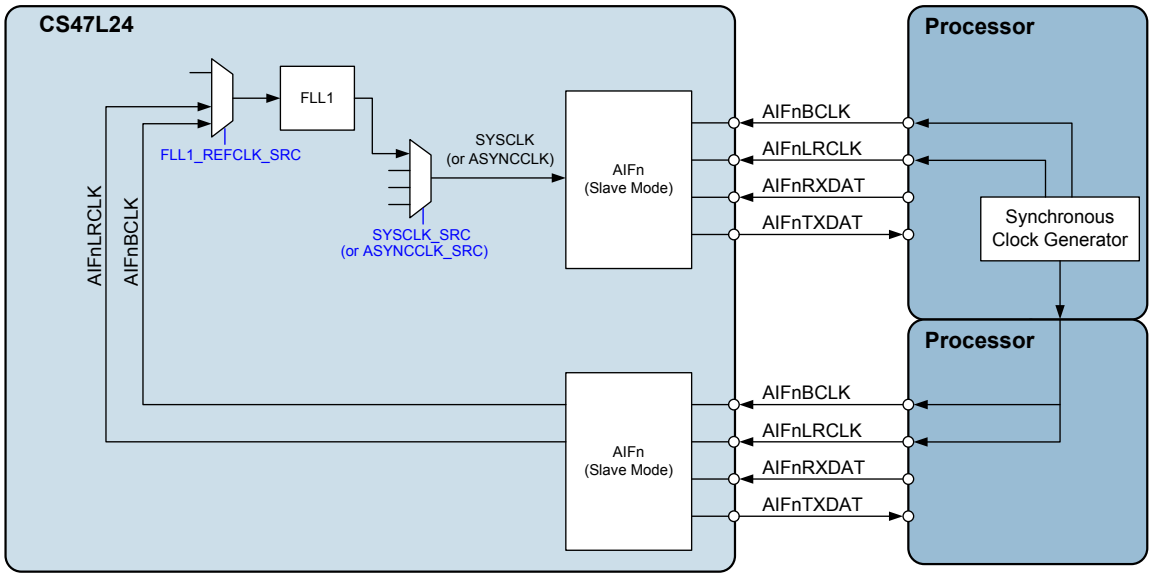


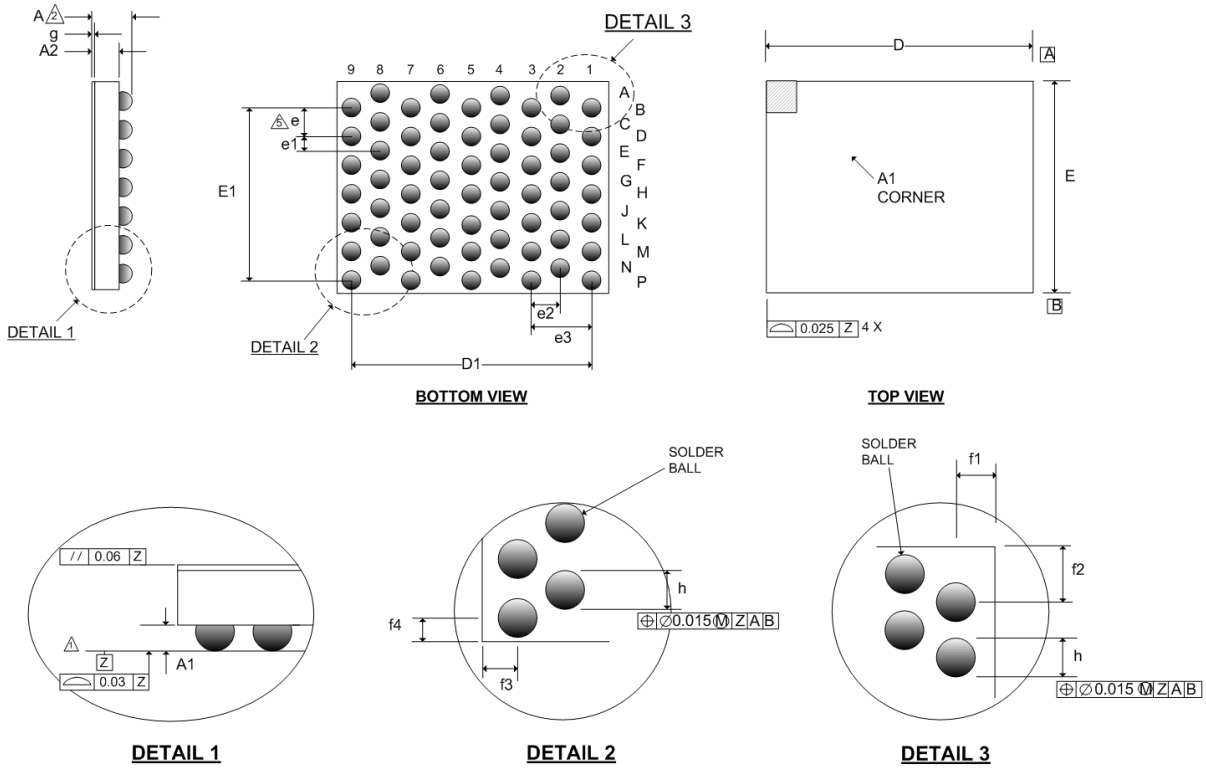
Figure 65 AIF Slave Mode, using another Interface as Reference

PCB LAYOUT CONSIDERATIONS

Poor PCB layout will degrade the performance and be a contributory factor in EMI, ground bounce and resistive voltage losses. All external components should be placed as close to the CS47L24 device as possible, with current loop areas kept as small as possible.

PACKAGE DIMENSIONS

B: 63 BALL WL-CS PACKAGE 3.394 x 2.971 x 0.504 mm BODY, 0.40 mm BALL PITCH DM132.B



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.470	0.504	0.538	2
A1	0.172	0.202	0.232	
A2	0.286	0.302	0.318	
D	3.364	3.394	3.424	
D1		2.7712 BSC		
E	2.941	2.971	3.001	
E1		2.4000 BSC		
e		0.4000 BSC		5
e1		0.2000 BSC		5
e2		0.3464 BSC		5
e3		0.6928 BSC		5
f1		0.3114 BSC		
f2		0.3855 BSC		
f3		0.3114 BSC		
f4		0.1855 BSC		
g		0.022		
h	0.236	0.262	0.288	

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1'.
3. A1 CORNER IS IDENTIFIED BY INL/LASER MARK ON TOP PACKAGE.
4. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
5. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
7. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.

REVISION HISTORY

Table 101 Revision History

Revision	Changes
1.0 AUG '14	• Initial version
2.0 OCT '14	• Noted inversion in Class D output path • Amendment to DBVDD operating range • Reverted to OUT4L signal path name for Class D speaker • Sample rate limit for DRC is 96kHz • Note to disable PWM when SYSCLK unavailable • Bus-keeper on GPIOs is removed • Clocking requirements for Interrupts noted • Amendment to MICBn_LVL voltage control
2.0 NOV '14	• Correction to DBVDD Absolute Maximum Rating • Package Outline Drawing updated
2.1 NOV '14	• DSP clock status & DMA control register descriptions updated • HPOUT load conditions updated • PWM override control register updated
2.2 DEC '14	• Converted to Cirrus document template • Corrected AIFn_RATE, FX_RATE, DSPn_RATE bit field positions • Updated Recommended External Connections to include MICBIAS1
3.0 MAR '15	• Electrical Characteristics updated • SPI_AUTO_INC register deleted
4.0 AUG '15	• Digital I/O pull-up/pull-down resistance specification updated • Digital mixer control requirements updated (*RATE, *FSL, and *FSH registers) • Correction to FLLn_SS_SEL description • Noted constraints for using WSEQ_START to trigger write sequencer
4.1 DEC '16	• Clarification of PDM input/output digital signal levels • Electrical characteristics updated • Typical performance data added • FLL configuration and example settings updated

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.