

CY8CKIT-062-WiFi-BT PSoC 6 WiFi-BT Pioneer Kit

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Drawing Numbers

PCBA	121-60435-01
PCB	600-60435-01
FAB DRW	610-60435-01
ASSY DRW	620-60435-01
SCH DRW	630-60435-01



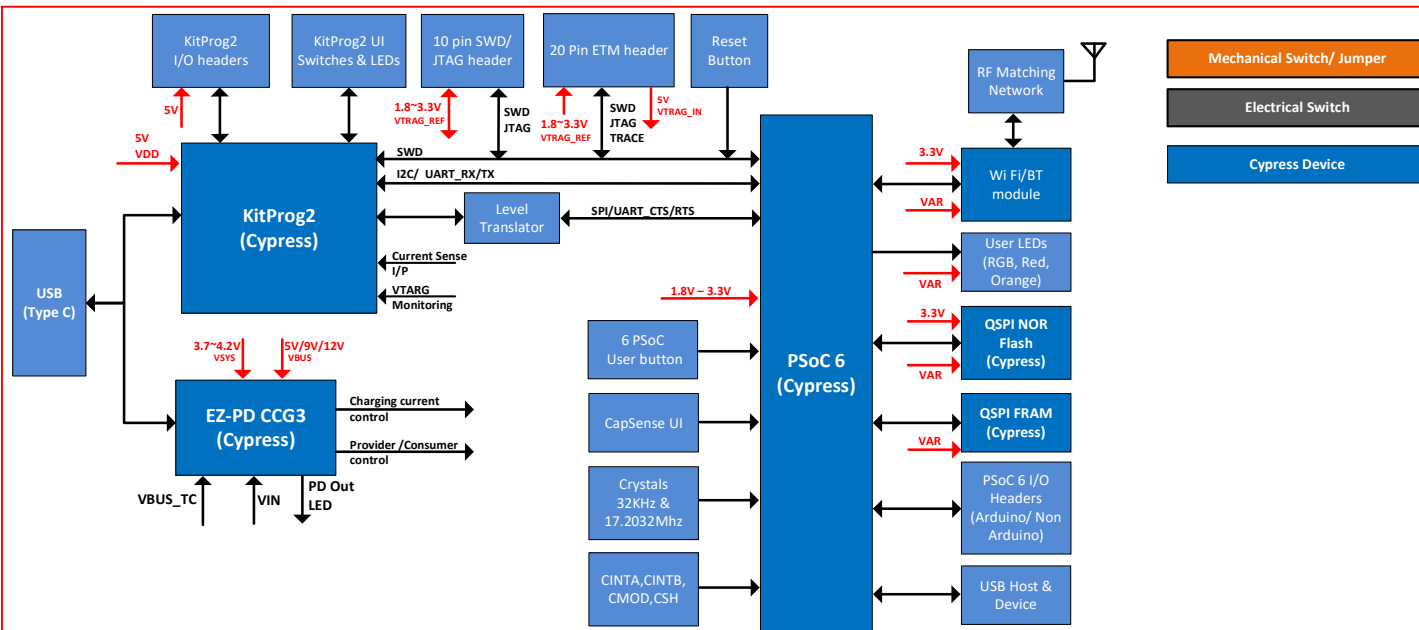
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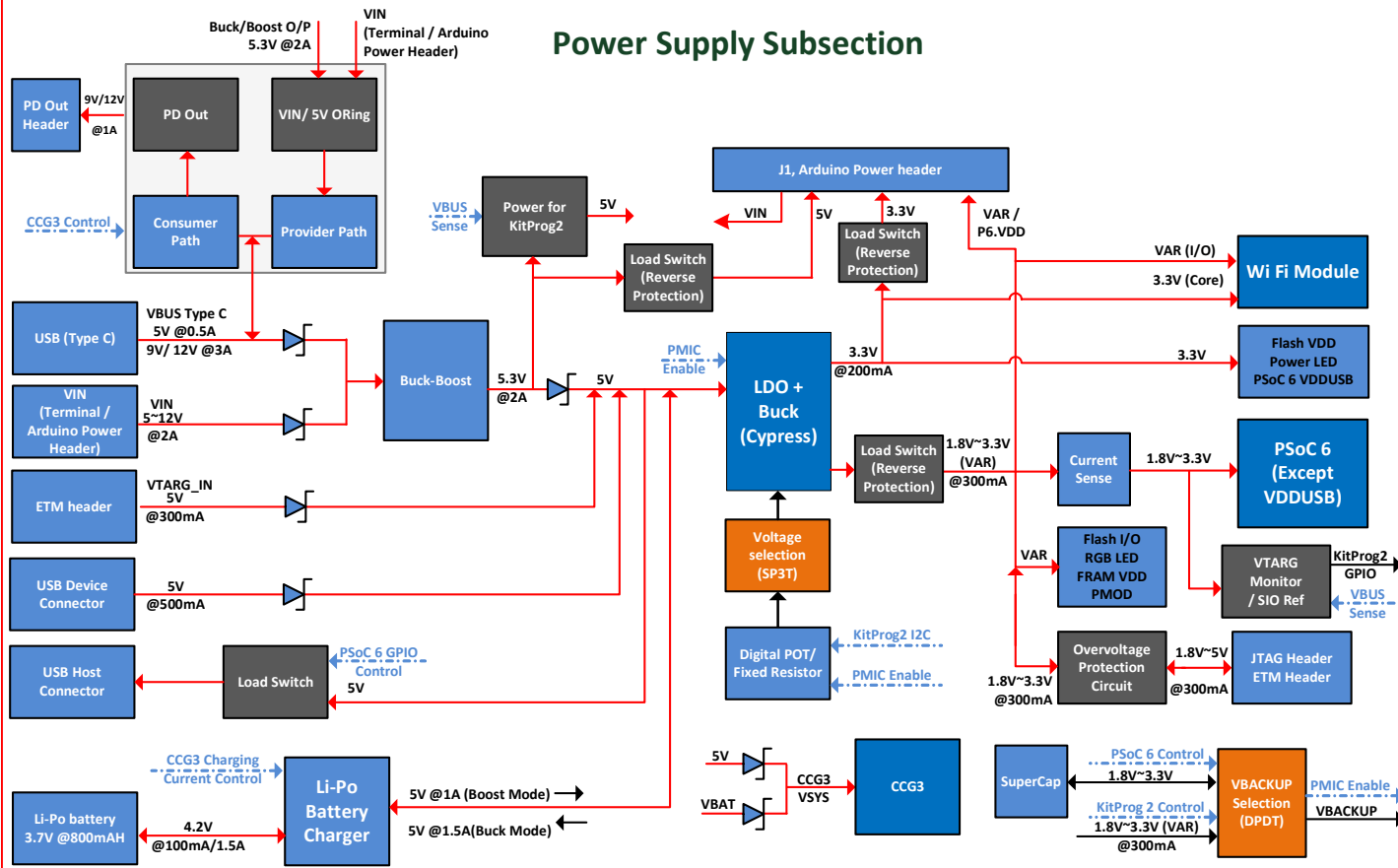
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Page Title :Title Page

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Power Supply Subsection



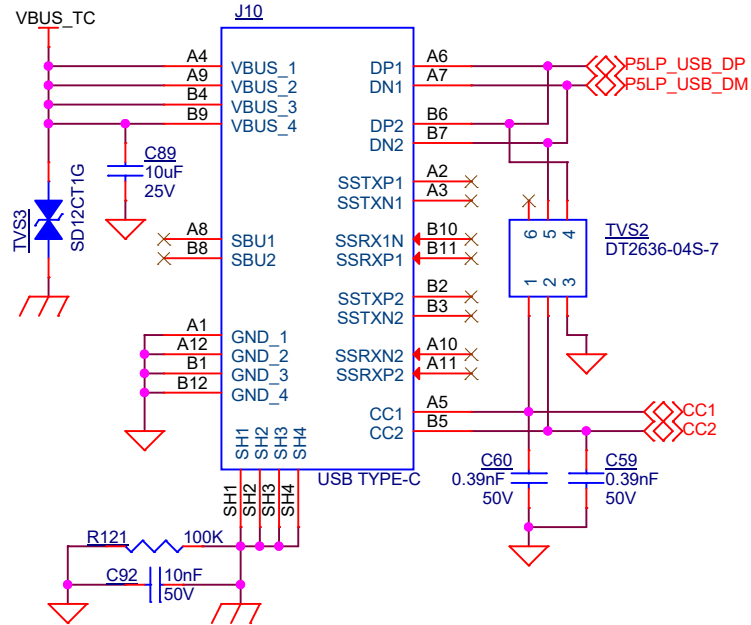
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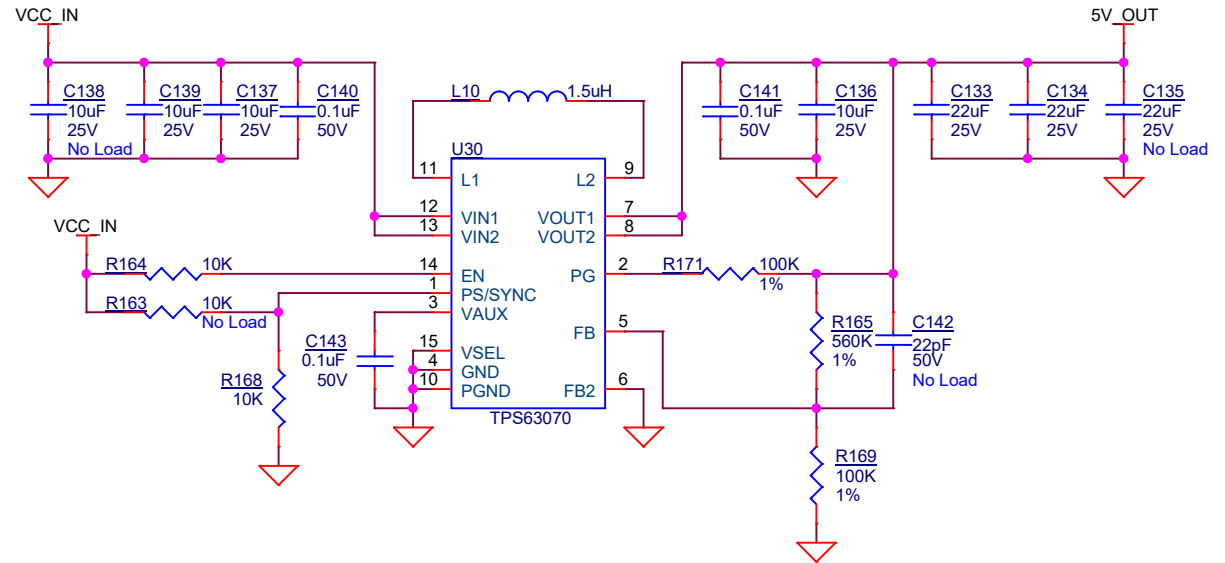
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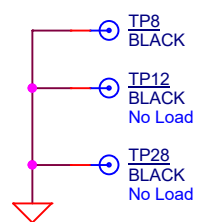
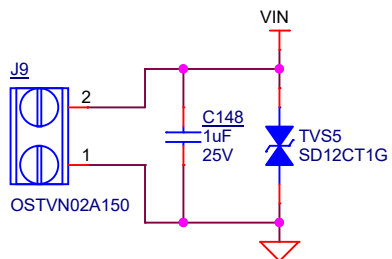
KitProg2 USB Type-C Connector



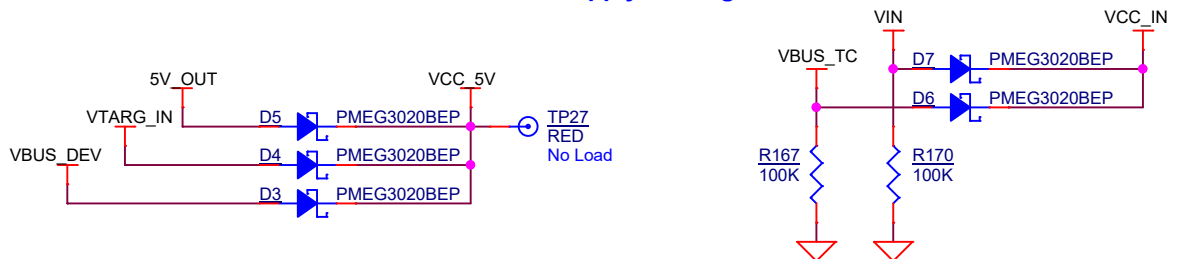
5V Buck-Boost Regulator



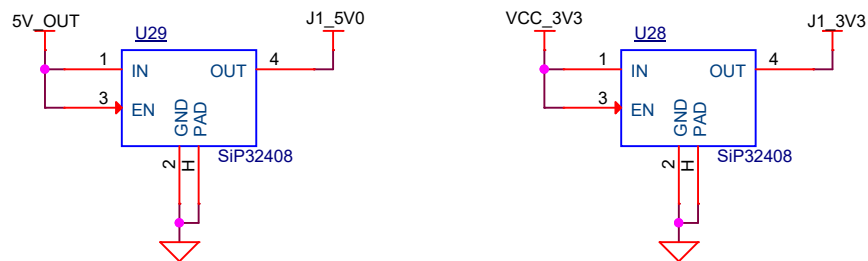
VIN Header



Power Supply 'OR'ing



Arduino Header O/P



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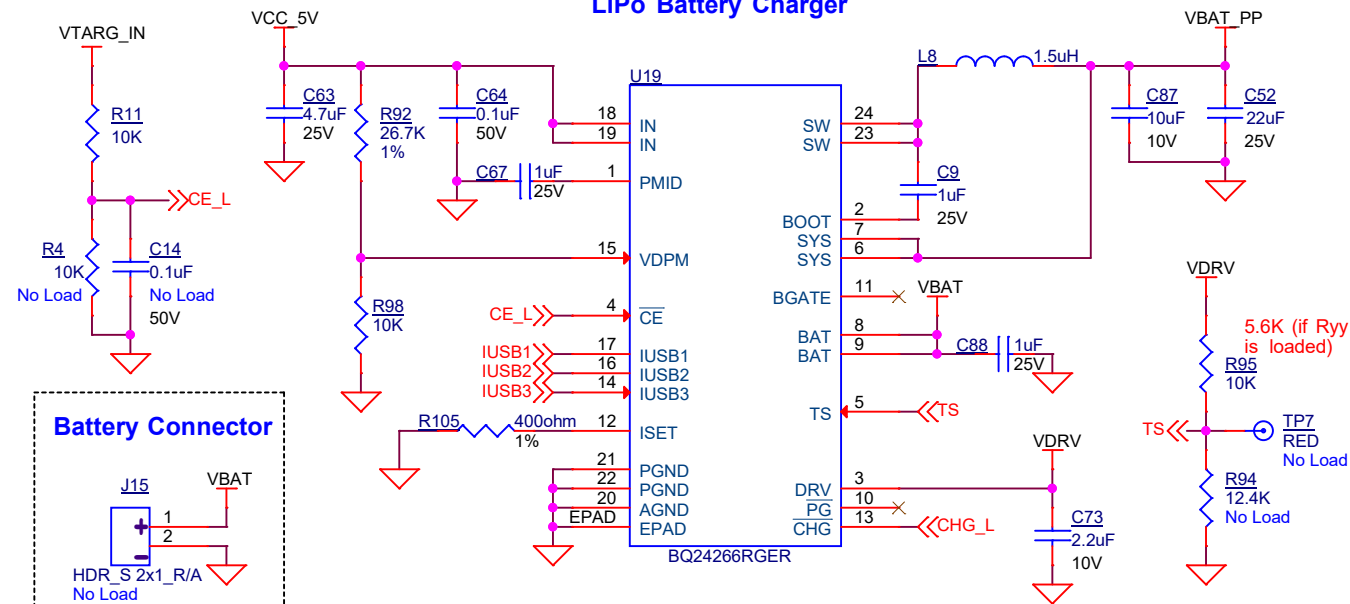
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Page Title :5V Buck/Boost Regulator

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LiPo Battery Charger



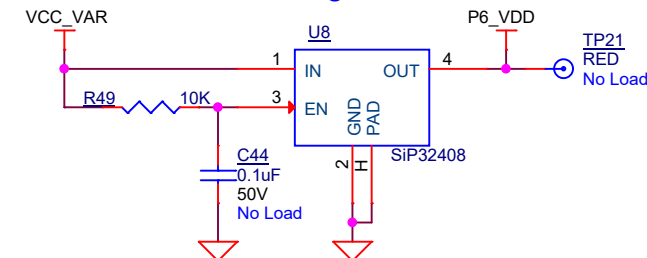
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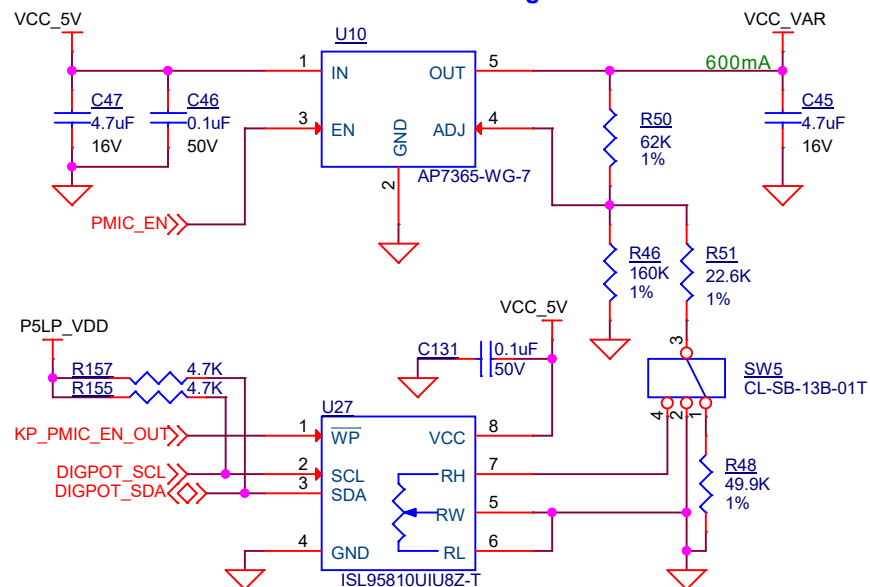
Power LED



Reverse Voltage Protection

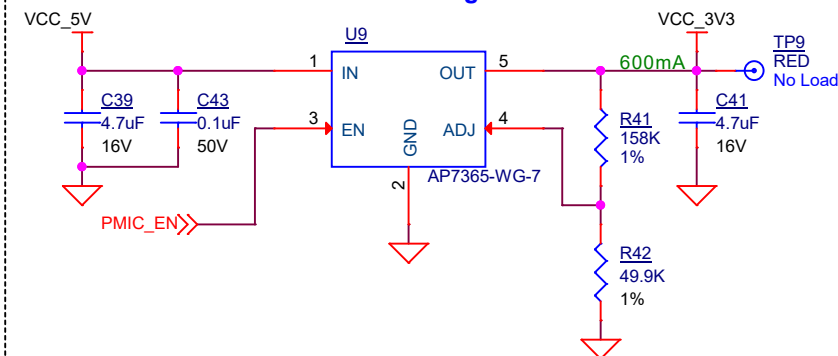


1.8V - 3.3V Variable Regulator



SW5	Source
POS1	1.8V
POS2	3.3V
POS3	Variable (1.8-3.3V)

3.3V Regulator



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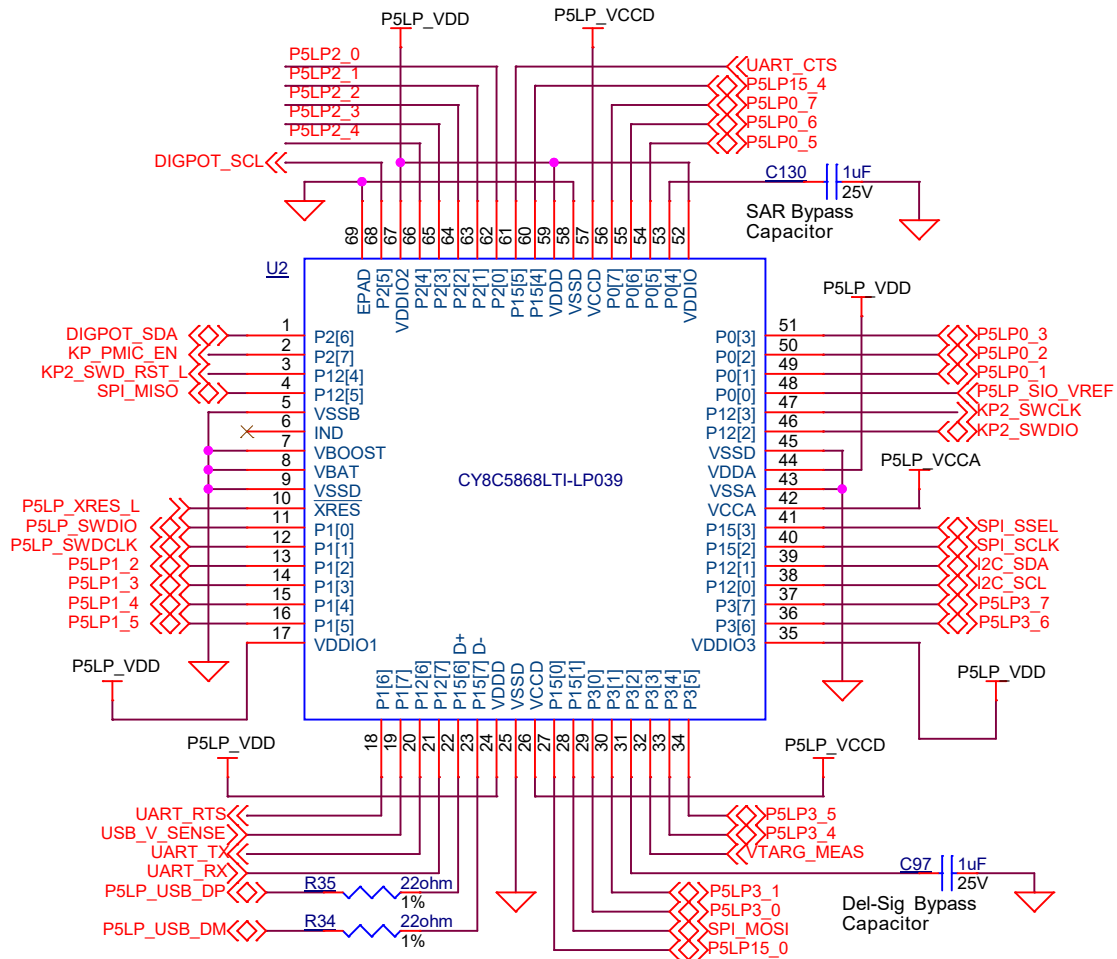
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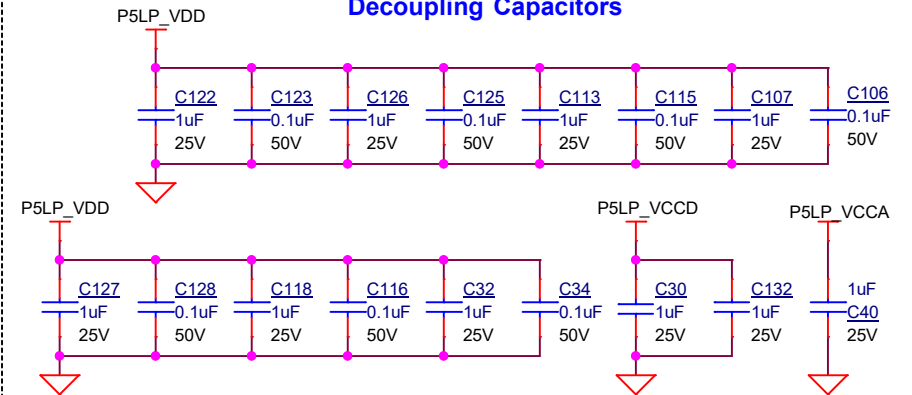
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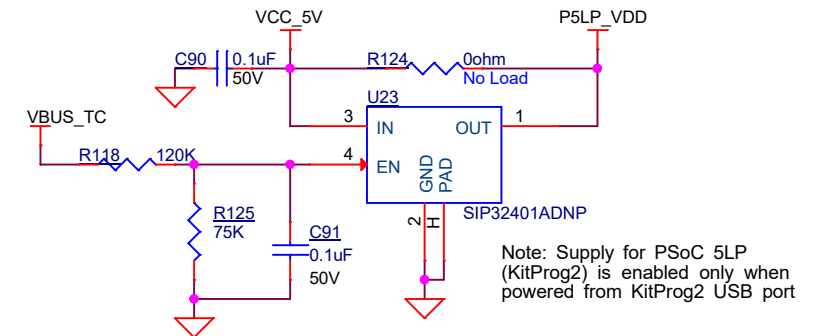
PSoC 5LP based KitProg2



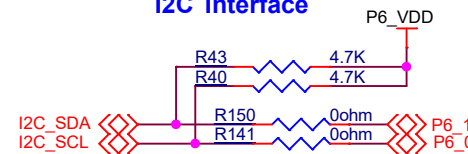
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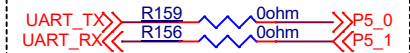
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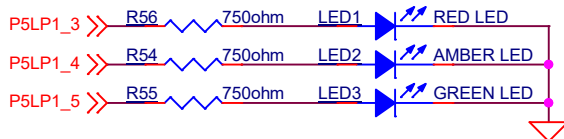
I2C Interface



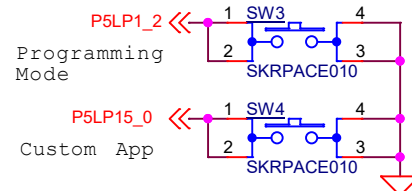
UART Interface



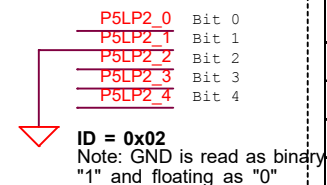
PSoC 5LP Status LEDs



PSoC 5LP User Switches



KitProg2 HW Revision



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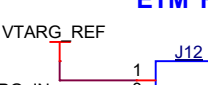
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Target PSoC Program/Debug Header

The diagram illustrates the Target PSoC Program/Debug Header. It features a 5V regulator circuit with a 1uF capacitor (C147) and a TVS4 ESD3V3D5-TP diode. The circuit is connected to a J11 connector. The J11 connector has 10 pins, with pins 1-5 connected to the TVS4 diode and pins 6-10 connected to the PSoC's debug pins: TMS_SWDIO, TCLK_SWCLK, TDO_SWO, TDI, and SWD_RST_L. The PSoC is labeled HDR_S 5x2.

ETM Header



The ETM Header pinout diagram shows a 20-pin connector. The pins are numbered 1 through 20. The connections are as follows:

- Pin 1: VTARG_REF
- Pin 2: TMS_SWDIO
- Pin 3: VTARG_IN
- Pin 4: TCLK_SWCLK
- Pin 5: TDO_SWO
- Pin 6: TDI
- Pin 7: SWD_RST_L
- Pin 8: TRACECLK
- Pin 9: TRACEDATA_0
- Pin 10: TRACEDATA_1
- Pin 11: TRACEDATA_2
- Pin 12: TRACEDATA_3
- Pin 13: J12
- Pin 14: J12
- Pin 15: J12
- Pin 16: J12
- Pin 17: J12
- Pin 18: J12
- Pin 19: J12
- Pin 20: J12

PSoC 6 SWD/JTAG Interface

The diagram illustrates the pinout for the PSoC 6 SWD/JTAG interface. It shows two rows of pins, each with a signal name, a pin number, a 0ohm resistor, and a target pin. The top row includes TDO_SWO, TDI, KP2_SWDIO, and KP2_SWCLK. The bottom row includes KP2_SWD_RST_L, TMS_SWDIO, TCLK_SWCLK, and SWD_RST_L. The target pins are P6_4, P6_5, P6_6, P6_7, and XRES_L. Below the diagram, there are two instructions: 'Remove Ryy, Ryy, Ryy to isolate KitProg2' and 'Remove Ryy, Ryy, Ryy for programming external target'.

Signal	Pin	Resistor	Target Pin
TDO_SWO			P6_4
TDI			P6_5
KP2_SWDIO	R194	0ohm	P6_6
TMS_SWDIO	R192	0ohm	P6_6
KP2_SWCLK	R183	0ohm	P6_7
TCLK_SWCLK	R191	0ohm	P6_7
KP2_SWD_RST_L	R182	0ohm	XRES_L
SWD_RST_L	R190	0ohm	XRES_L

Remove Ryy, Ryy, Ryy to isolate KitProg2

Remove Ryy, Ryy, Ryy for programming external target

PSoC 5LP Custom Application Header

PSoC 5LP GPIO Expansion Header

The diagram illustrates the PSoC 5LP GPIO Expansion Header (J6) connections. The header is an 8x2 pin connector. The connections are as follows:

Header Pin	Function / Signal	Target Pin / Label
1	P5LP_VDD	
2		
3	SPI_MOSI	P5LP15_1
4		
5	SPI_SCLK	P5LP15_2
6		
7		
8		
9	SPI_SSEL	P5LP15_3
10		
11	SPI_MISO	P5LP12_5
12		
13	P5LP3_4	CUSTOM
14	UART_RX	P5LP12_7
15	P5LP3_6	CUSTOM
16		
17	UART_CTS	
18	P5LP0_1	CUSTOM
19	I2C_SCL	P5LP12_0
20	P5LP3_0	CUSTOM
21	I2C_SDA	P5LP12_1
22	P5LP3_5	CUSTOM
23	UART_TX	P5LP12_6
24		
25		

The connector is labeled **CON 8x2** and **No Load**.

Voltage Monitoring

Voltage Monitoring

The circuit diagram illustrates the voltage monitoring setup for the P5LP_VDD and VTARG_MON signals. The monitoring is performed using the **SIP32402ADNP** (U26) comparator.

Comparator (U26) Connections:

- IN (Pin 3):** Connected to **VTARG_BUF**.
- EN (Pin 4):** Connected to **P5LP_VDD**.
- OUT (Pin 1):** Connected to **VTARG_MON**.
- GND PAD (Pin 2):** Connected to ground.

Capacitors:

- C124:** 0.1uF, 50V, No Load, connected between **P5LP_VDD** and ground.
- C129:** 0.1uF, 50V, connected between **VTARG_BUF** and ground.

Voltage Dividers:

- USB_V_SENSE:** Connected to **P5LP_VDD**. Resistors: **R37** (15K) and **R33** (30K).
- VTARG_MEAS:** Connected to **VTARG_MON**. Resistors: **R130** (15K) and **R136** (30K).
- P5LP_SIO_VREF:** Connected to **VTARG_MON**. Resistors: **R123** (49.9K, 1%) and **R119** (49.9K, 1%, No Load).

Program/Debug Overvoltage Protection

Level Translator for SPI and UART flow control

The diagram illustrates a level translator circuit for SPI and UART flow control, centered around the FXMA108BQX IC (U17).

Power and Ground Connections:

- VCCB:** Connected to P5LP_VDD. A 1uF capacitor (C56) is connected to ground.
- VCCA:** Connected to P6_VDD. A 1uF capacitor (C55) is connected to ground.
- DAP:** Connected to ground (pin 21).
- GND:** Connected to ground (pin 10).
- OE:** Connected to ground via a 10K resistor (R100).


Signal Connections:

- SPI Signals:**
 - SPI_MOSI (pin 19, B0) to P12_0
 - SPI_SCLK (pin 18, B1) to P12_2
 - SPI_MISO (pin 17, B2) to P12_1
 - SPI_SSEL (pin 16, B3) to P5LP_SSEL_P12_4
- UART Signals:**
 - UART_RTS (pin 15, B4) to P5_3
 - UART_CTS (pin 14, B5) to P5_2
- Other Connections:**
 - Pin 2 (A0) to P12_0 via 0ohm resistor (R77).
 - Pin 3 (A1) to P12_2 via 0ohm resistor (R81).
 - Pin 4 (A2) to P12_1 via 0ohm resistor (R85).
 - Pin 6 (A4) to P5LP_SSEL_P12_4 via 0ohm resistor (R88).
 - Pin 7 (A5) to P5_3 via 0ohm resistor (R93).
 - Pin 11: Connected to ground via a 10K resistor (R104) and to P6_VDD via a 10K resistor (R204).

IC Pinout:

- Left Side (B0-B7, DAP, GND, OE):** Pins 19, 18, 17, 16, 15, 14, 13, 12, 21, 10.
- Right Side (A0-A7):** Pins 2, 3, 4, 5, 6, 7, 8, 9.



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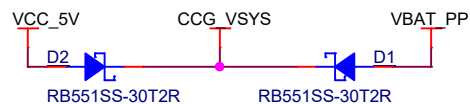
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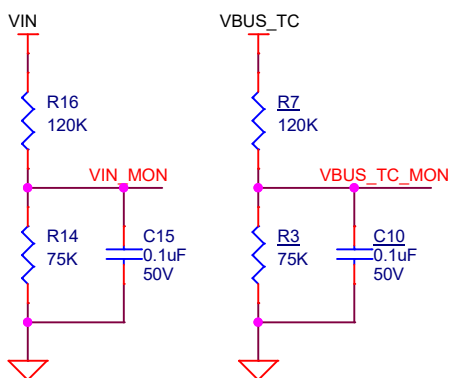
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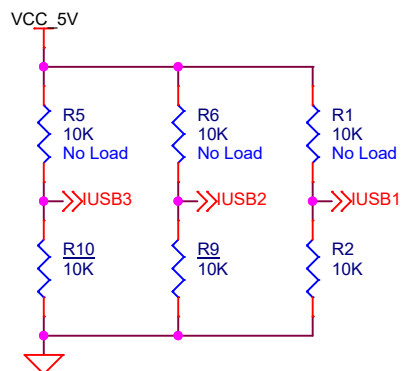
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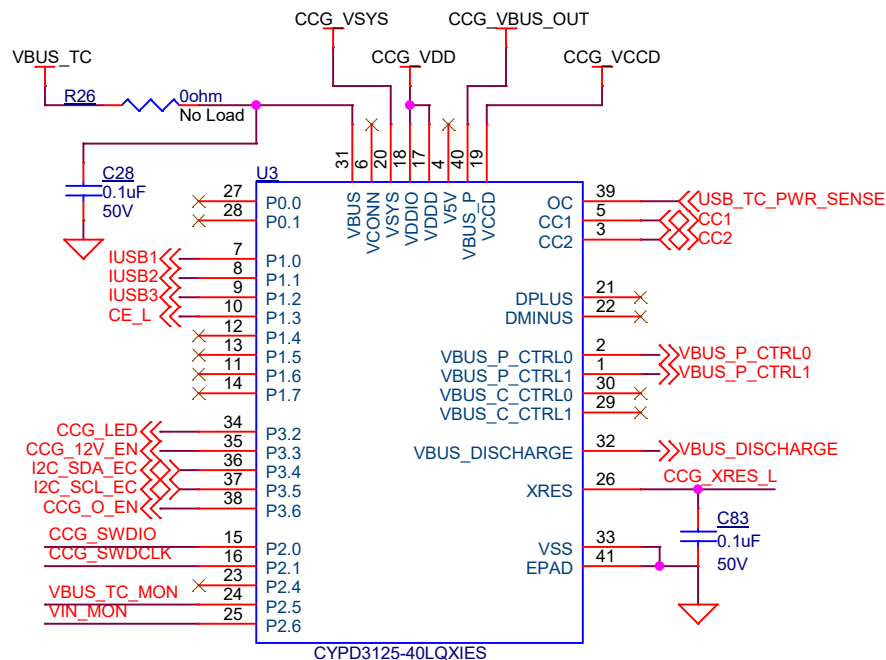
VBUS & VIN Voltage Monitoring



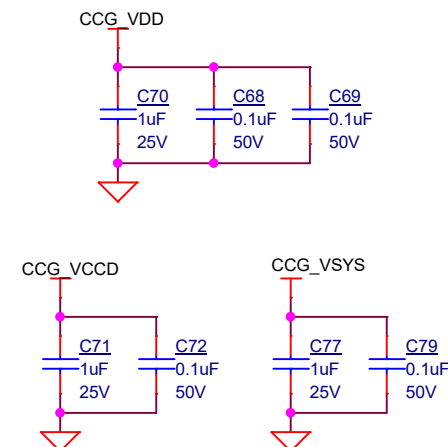
LiPo Battery Charger Pull Up



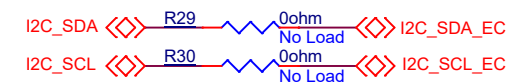
CCG3 USB Type-C Controller



Decoupling Capacitors



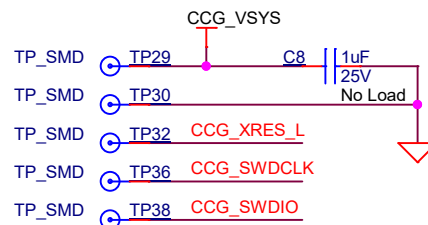
I2C Bootloader



Output Indication



CCG3 Programming



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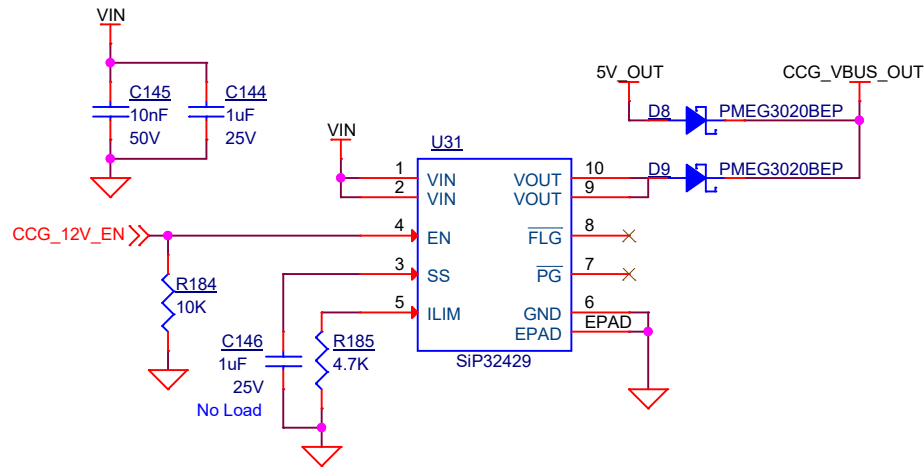
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Page Title :Type-C Controller

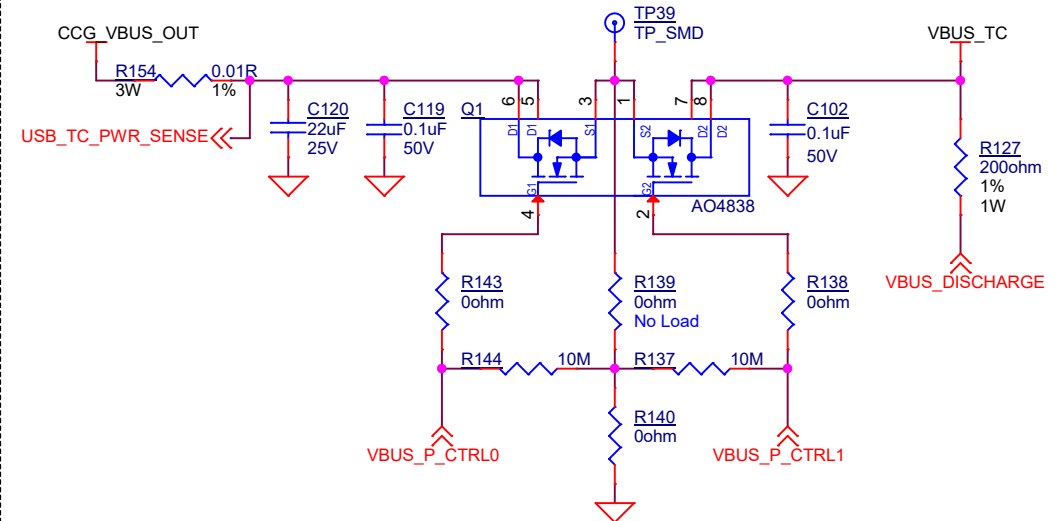
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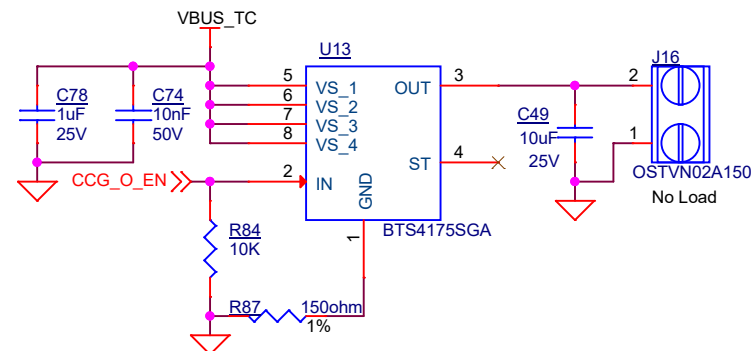
CCG3 Provider Path 'OR'ing



VBUS Provider Path



CCG3 Consumer Path



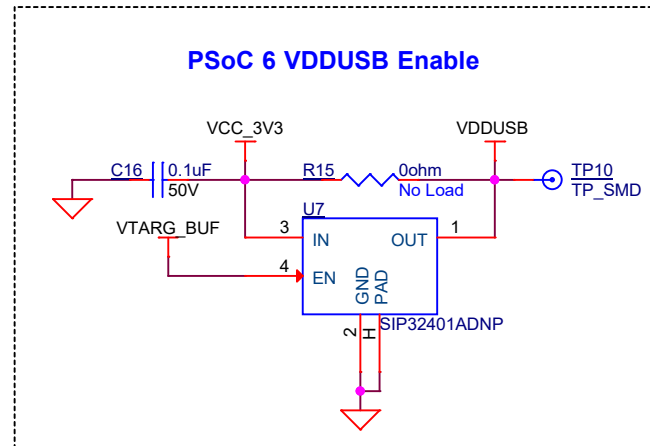
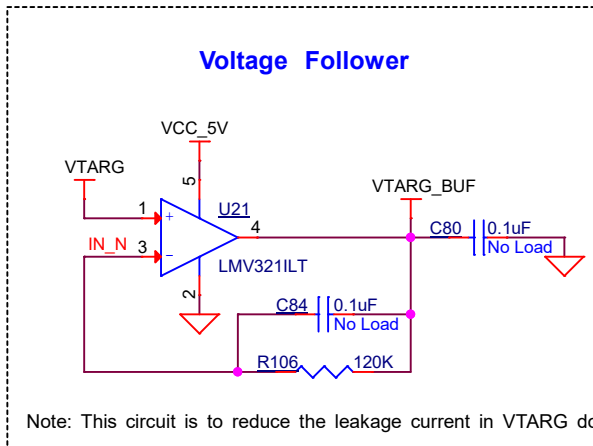
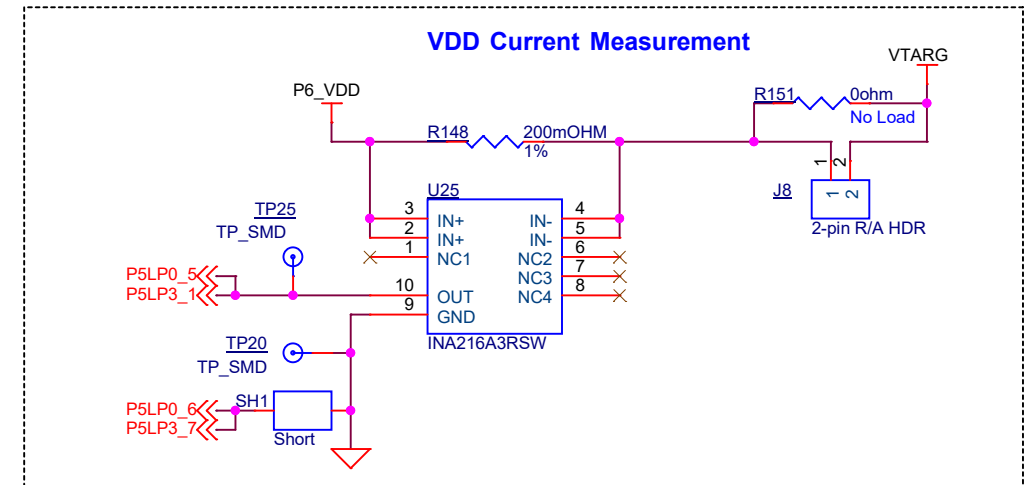
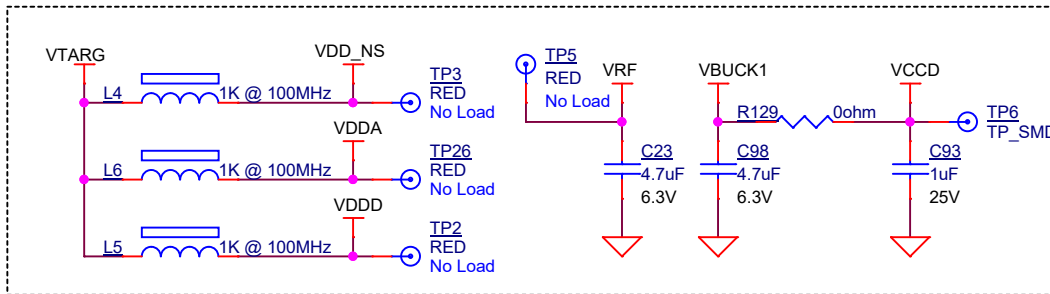
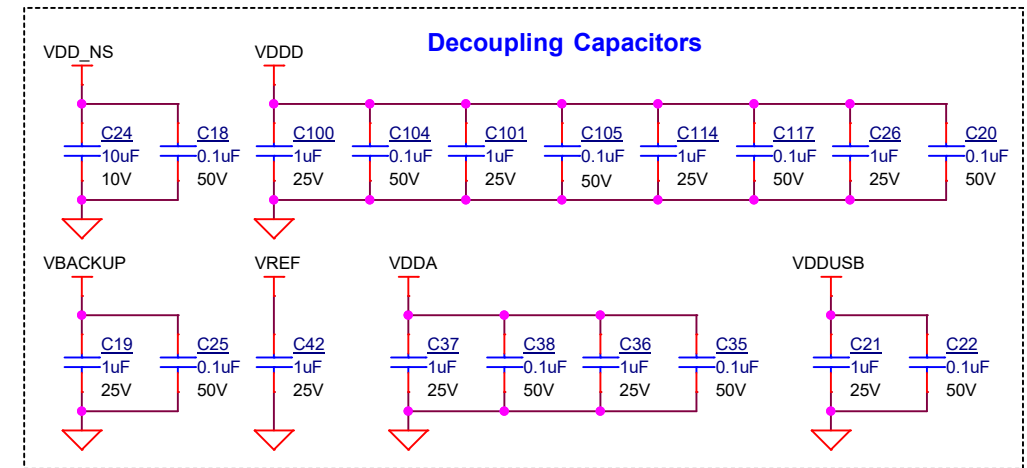
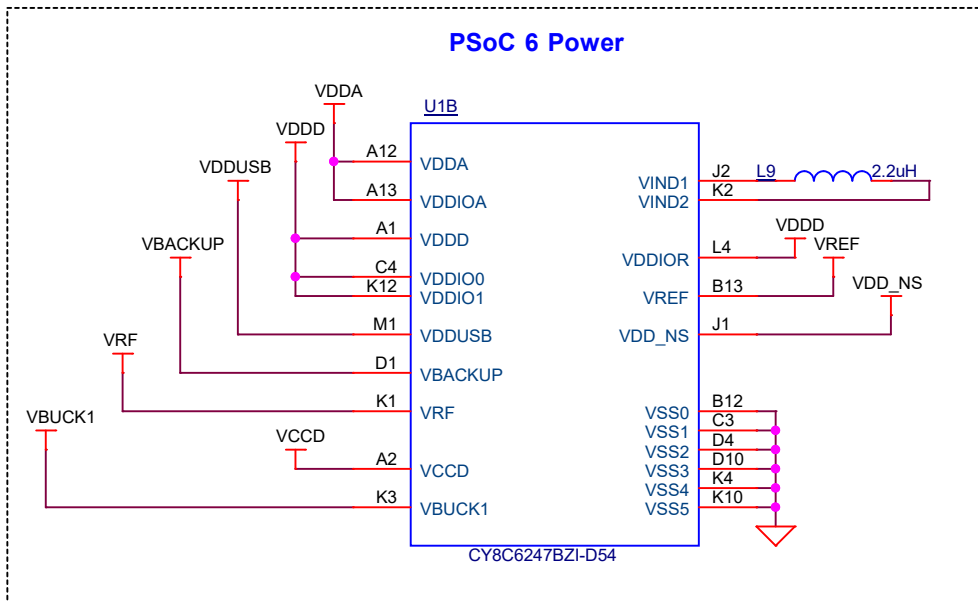
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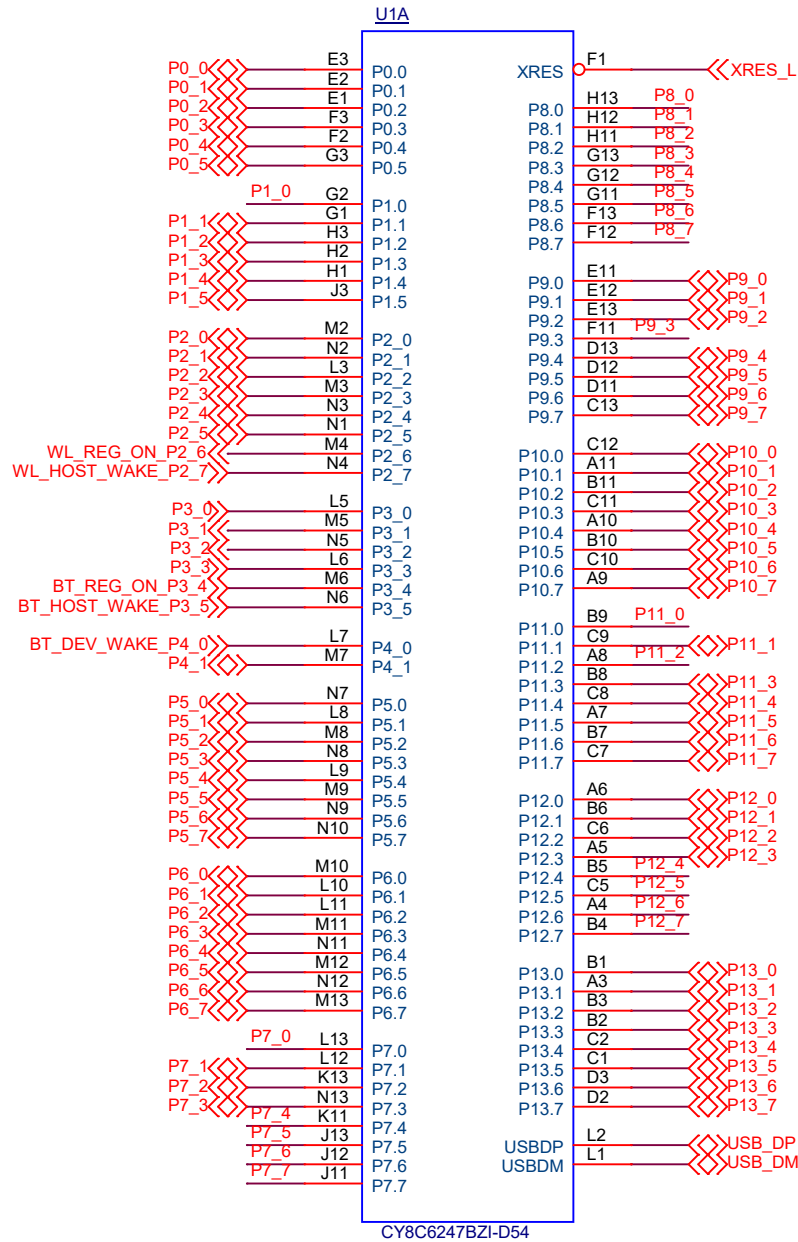
Page Title :Type-C Power Path

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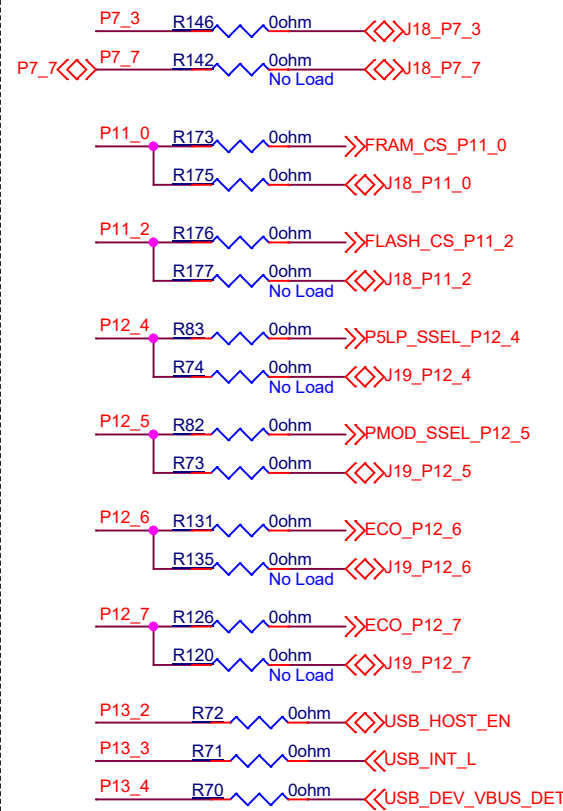
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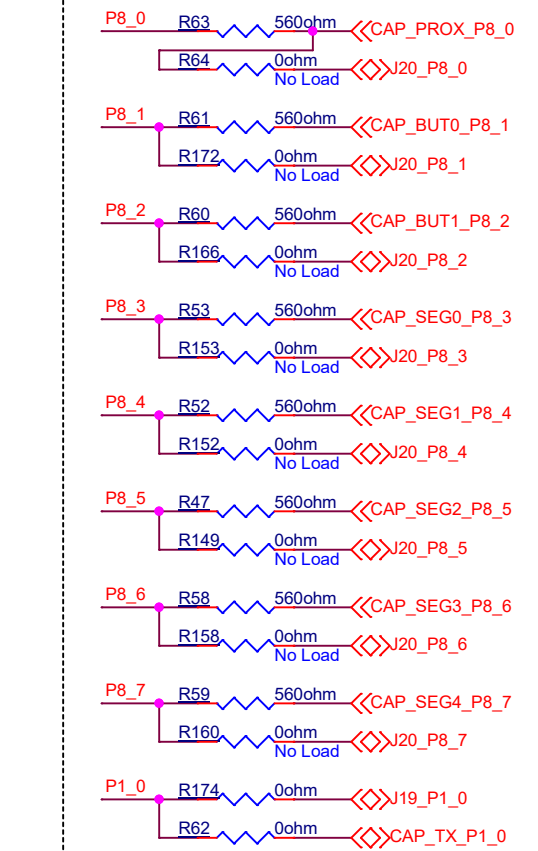
PSoC 6 Signals



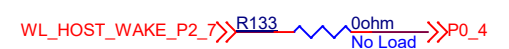
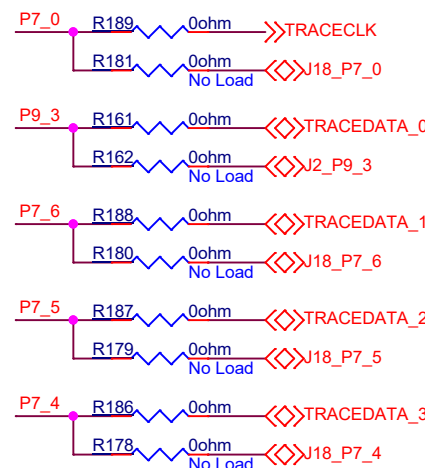
Additional Multiplexed Pins



CapSense Multiplexed Pins



TRACE Multiplexed Pins



Note: Option for WLAN to wake PSoC 6 from Hibernate

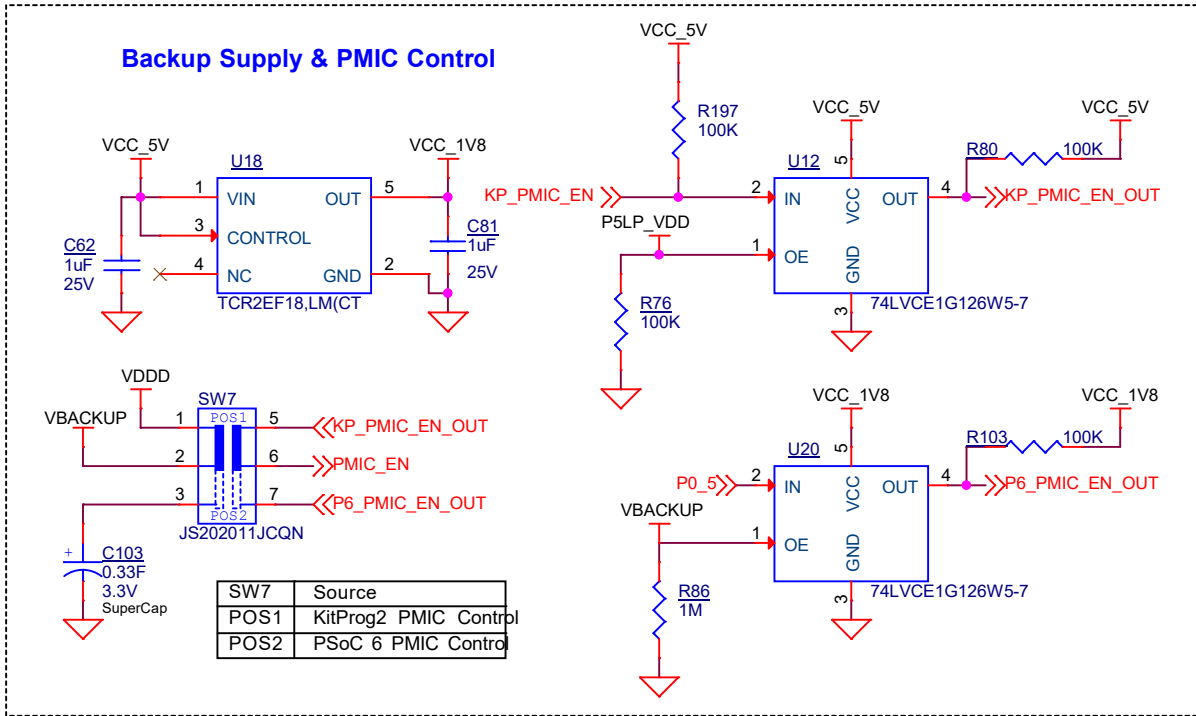
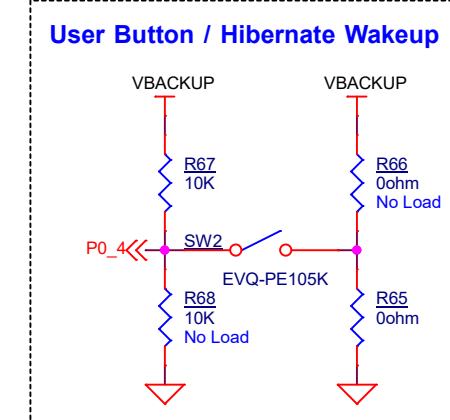
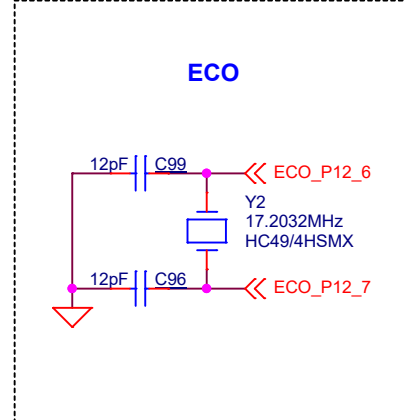
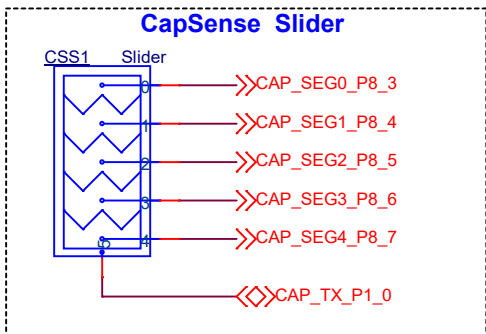
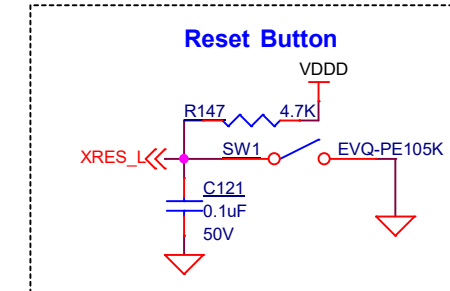
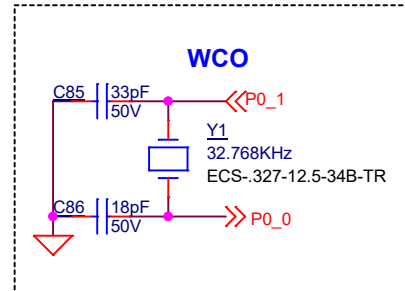
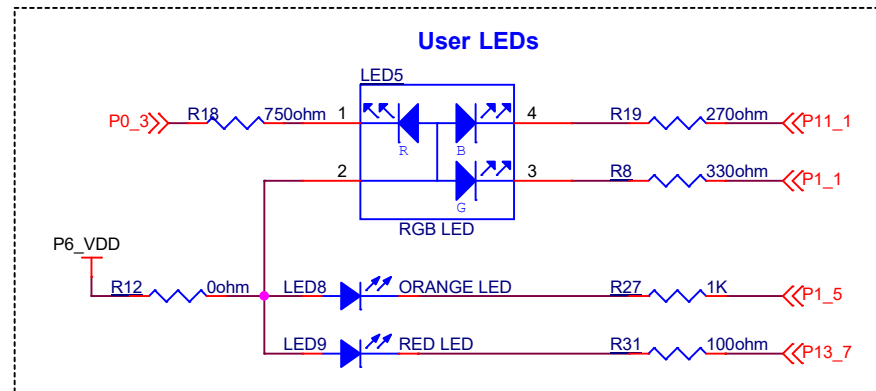
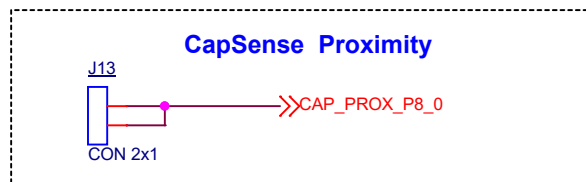
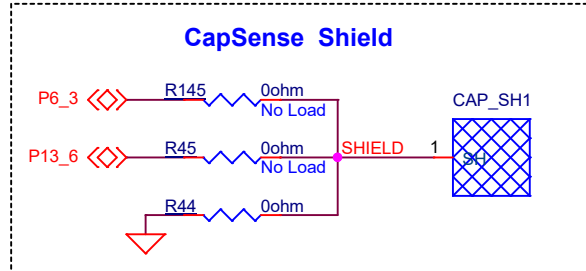
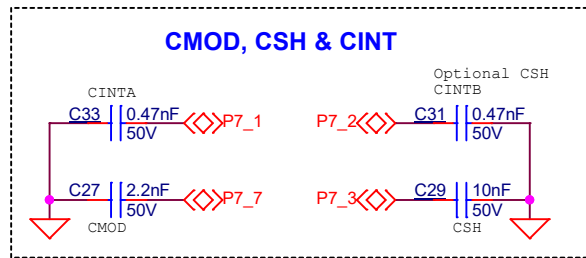
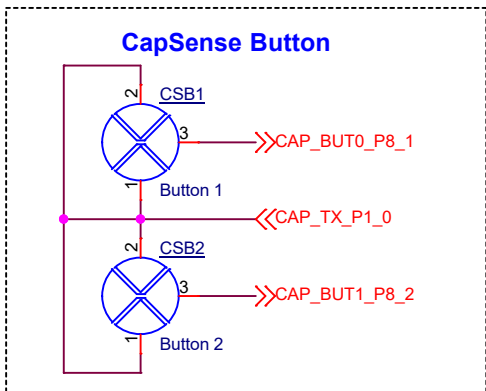


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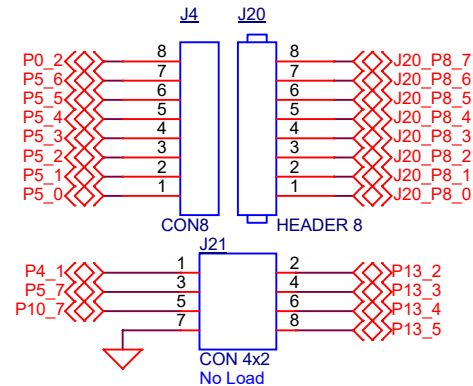
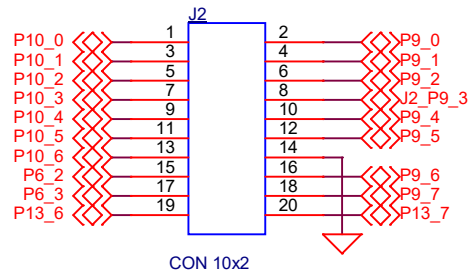
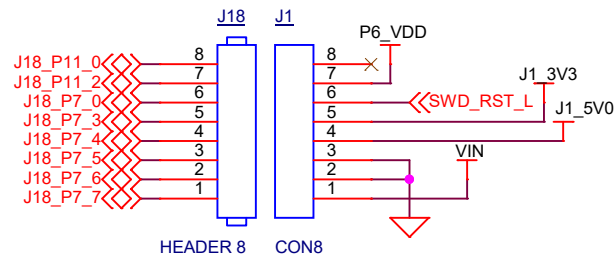
SCH Title : CY8CKIT-062-WiFi-BT PSoC 6 WiFi-BT Pioneer Kit

Page Title : PSoC 6 Signals

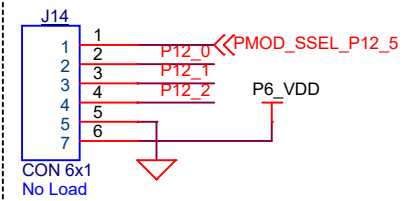
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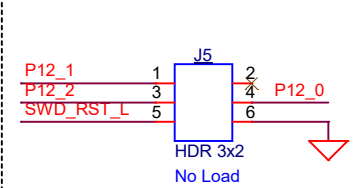
Arduino & Extended Headers



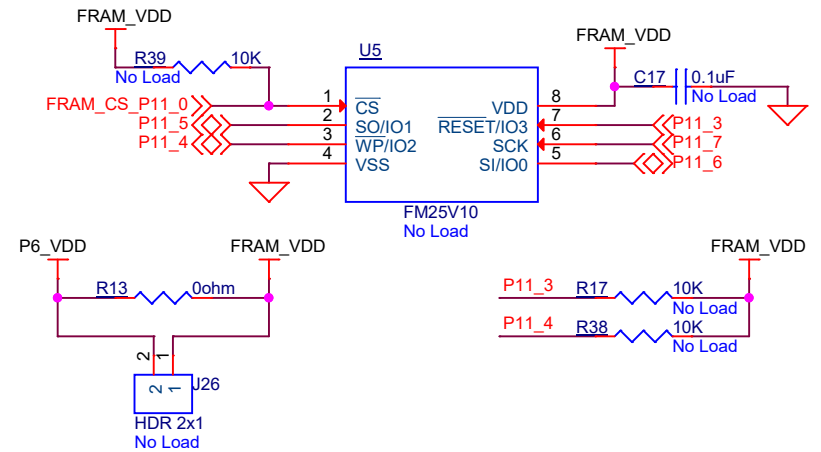
PMOD Header



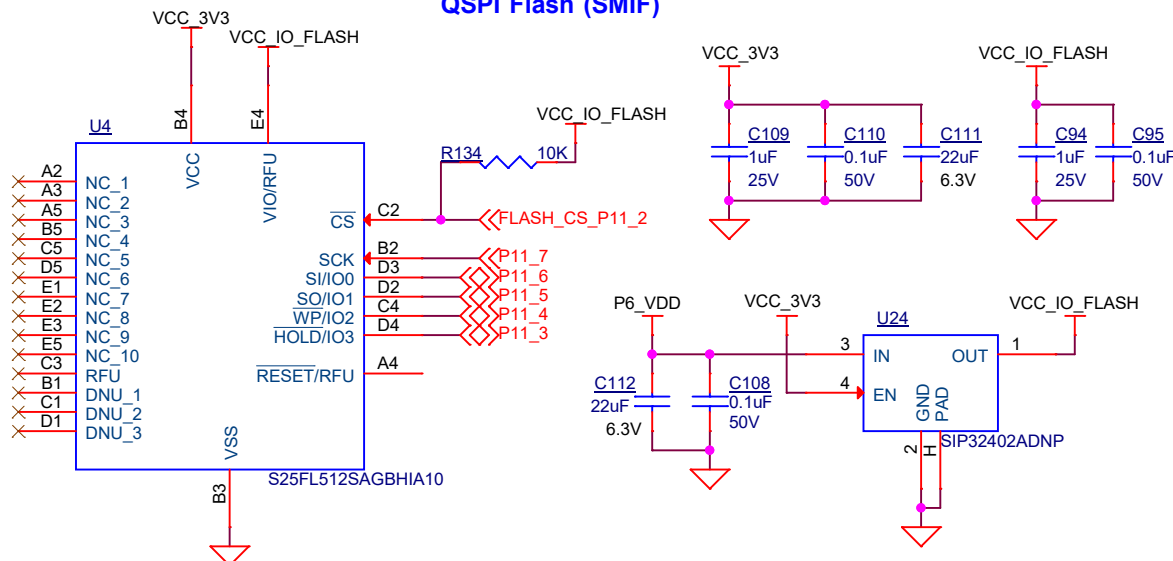
ICSP Header



FRAM



QSPI Flash (SMIF)



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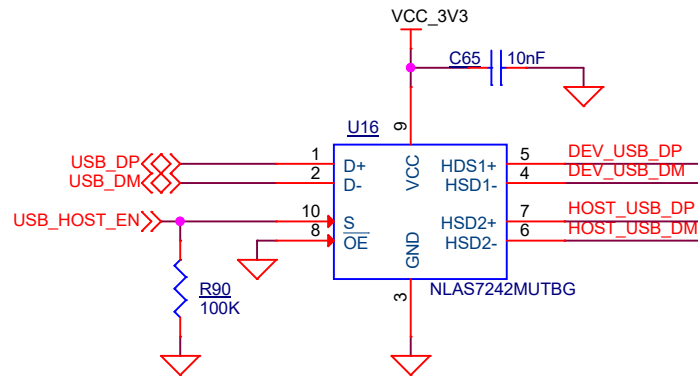
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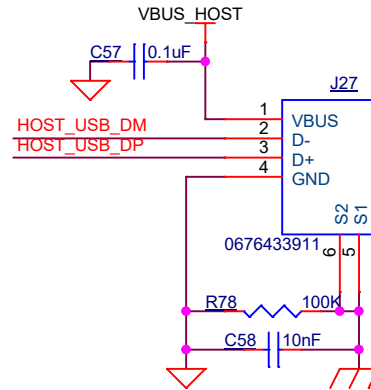
Page Title :Expansion headers & Memory

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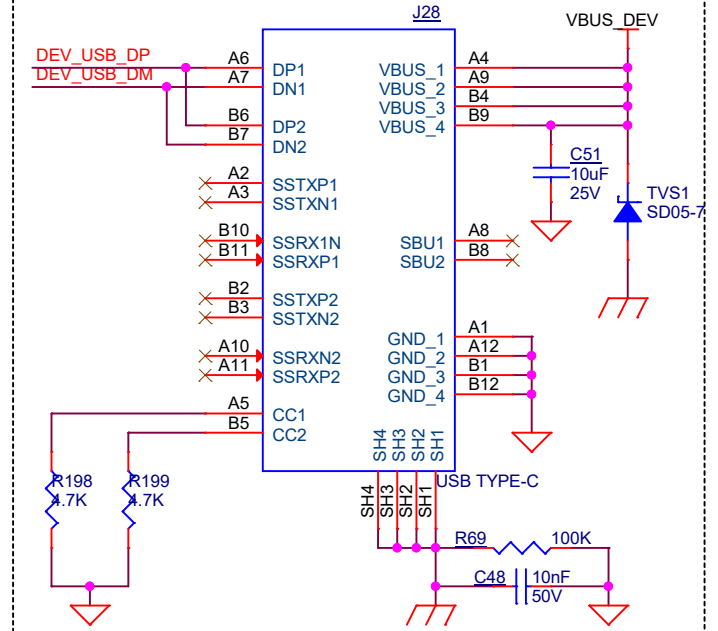
USB Multiplexer



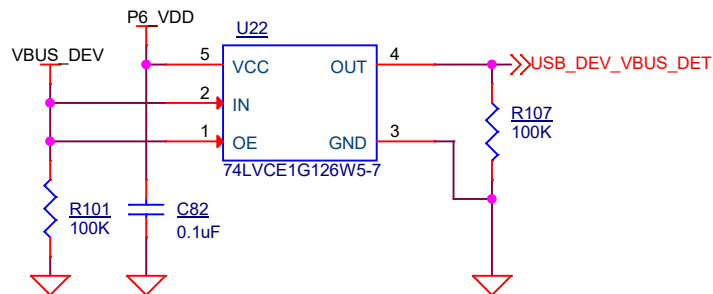
USB Type-A Receptacle (Host)



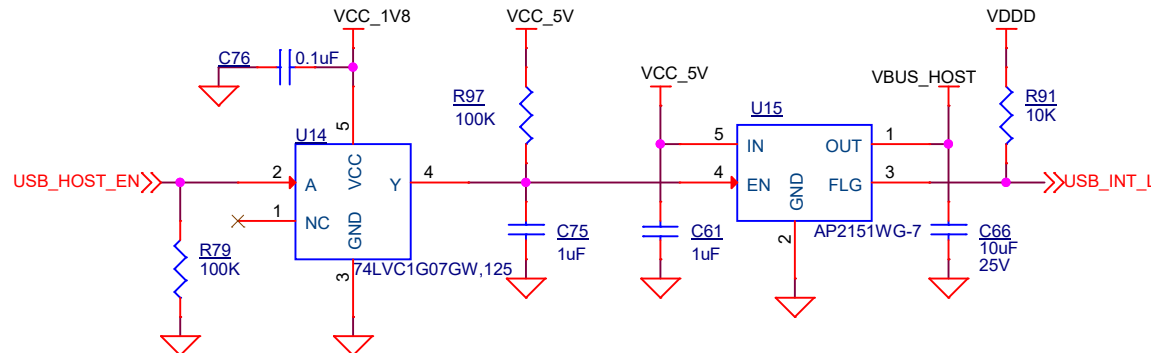
USB Type-C Connector (Device)



USB Device Port VBUS Detect



USB Host VBUS Enable



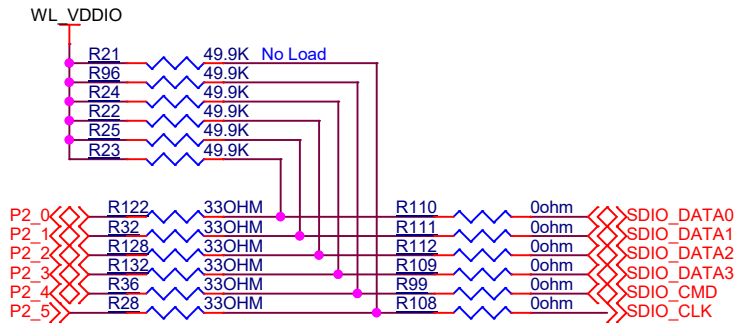
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SCH Title : CY8CKIT-062-WiFi-BT PSoc 6 WiFi-BT Pioneer Kit

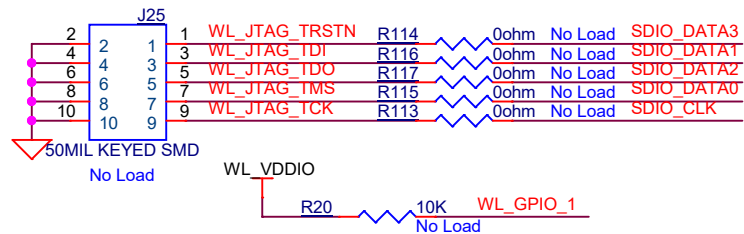
Page Title :USB Host & Device Interface

Size	Document Number	Drawn By	Approved By	Rev
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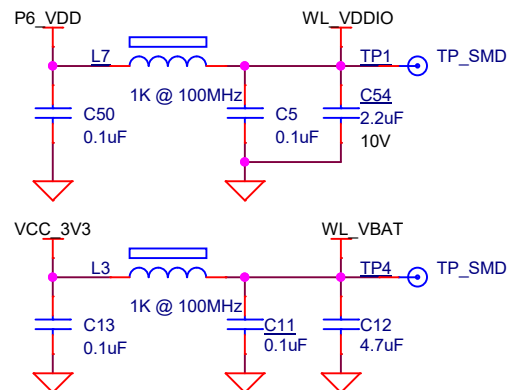
WiFi Interface with PSOC 6



Optional JTAG Interface



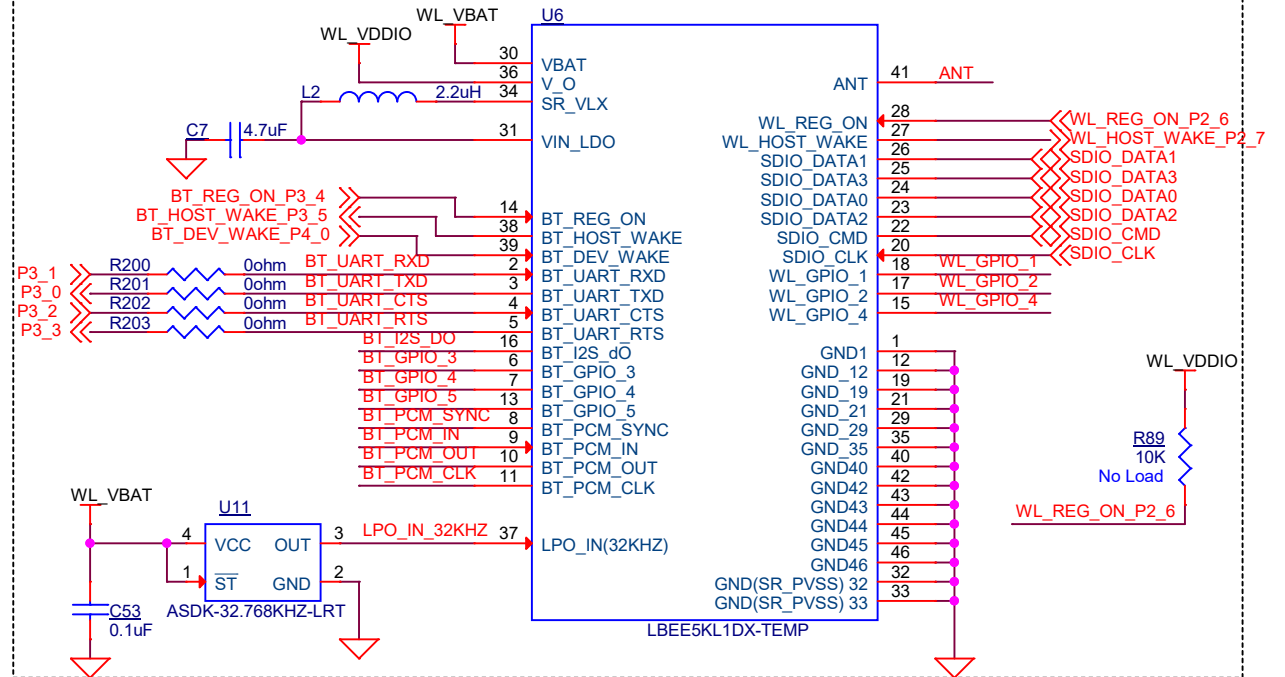
Supply for WiFi Module



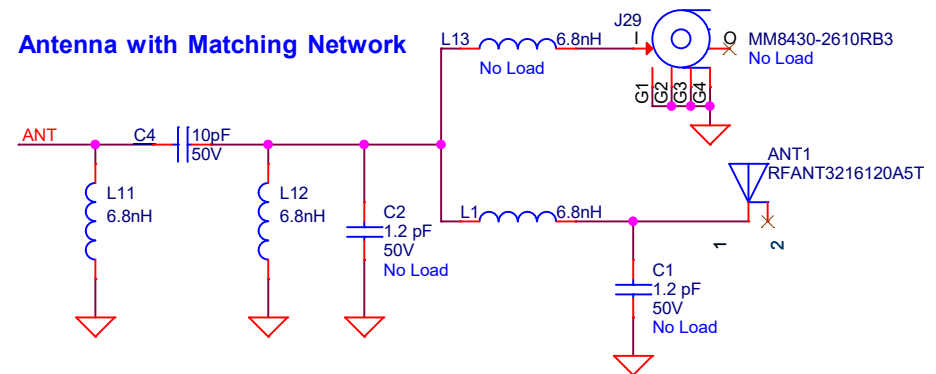
Testpoints

WL_GPIO_1	TP16	TP_SMD
WL_GPIO_2	TP11	TP_SMD
WL_GPIO_4	TP19	TP_SMD
WL_REG_ON_P2_6	TP33	TP_SMD
WL_HOST_WAKE_P2_7	TP34	TP_SMD
BT_REG_ON_P3_4	TP37	TP_SMD
BT_HOST_WAKE_P3_5	TP31	TP_SMD
BT_DEV_WAKE_P4_0	TP35	TP_SMD
BT_GPIO_3	TP22	TP_SMD
BT_GPIO_4	TP23	TP_SMD
BT_GPIO_5	TP17	TP_SMD
BT_I2S_DO	TP18	TP_SMD
BT_PCM_SYNC	TP24	TP_SMD
BT_PCM_IN	TP13	TP_SMD
BT_PCM_OUT	TP14	TP_SMD
BT_PCM_CLK	TP15	TP_SMD
BT_UART_RXD	TP40	TP_SMD
BT_UART_TXD	TP41	TP_SMD
BT_UART_CTS	TP42	TP_SMD
BT_UART_RTS	TP43	TP_SMD

WiFi / BT Module



Antenna with Matching Network



Layout: Overlap the L13.2 and L1.2 pads



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SCH Title : CY8CKIT-062-WiFi-BT PSoc 6 WiFi-BT Pioneer Kit

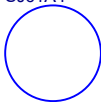
Page Title :WiFi Module Interface

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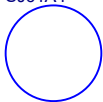
Accessories

Cylindrical Bumper

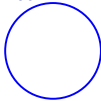
SJ61A4



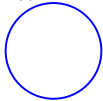
SJ61A4



SJ61A4



SJ61A4



Acrylic Overlay

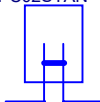
Acrylic Overlay

Color: Clear, Transparent
Finish: Matt

40 x 34 x 1mm

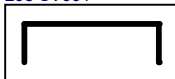
Jumper Shunt

SPC02SYAN

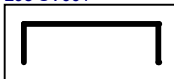


USB Type-C Connector Brackets

298 SV001



298 SV001



PCBA label

LBL PCA Label



LBL QR Code



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Page Title :Accessories

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REVISION HISTORY

REV	DESCRIPTION OF CHANGE	DATE
01	Initial Release	2017/03/13
02	Initial Release	2017/09/01
2.1	Changes done in brief below. See Perforce Rev-21 change Description. - P7_7 off-page connectors added - R197, R198 , R199 resistors added	2017/10/20
2.2	Changes done by Plato: See the description of Rev#25, changelist#1015299. Changes done by TAVA: added 0-ohm resistors (R200, R201, R202, R203) and Test points (TP40, 41, 42, 43) on the 4 UART lines (U6.2, 3, 4, 5)	2017/10/23
2.3	Antenna Network is modified. The RF connector is moved from series path to Y-connection. Additional series inductor is added before the RF connector.	2017/10/24
2.4	UART_CTS PSoC 5LP connection is terminated to J6.2 header pin	2017/11/02
2.5	Net names modified : BT_UART_RXD_P3_1, BT_UART_TXD_P3_0, BT_UART_CTS_P3_2, BT_UART_RTS_P3_3	2017/11/06
2.6	Net names modified : TP40 - 43 connected nets	2017/11/06
2.7	R195 10k pull-down resistor is added on the UART_CTS - PSoC 6 (P5_2) line after the Level Translator.	2017/11/07
2.8	R101 1M re resistor is replaced by a 100k resistor. This resistor is on VBUS_DEV net. This is copied from R90.	2017/11/07
2.9	<ul style="list-style-type: none"> - Component Properties updated (partially) to match with BoM and Arena - J25 is changed to No Load - J2 : Initially Asym Instruction was No Load. This was manually corrected in BoM and Arena to make Populated. Hence updated in the schematic. - R188 made 0-ohm, R180 made "0-ohm No Load" - R187 made 0-ohm, R179 made "0-ohm No Load" - R186 made 0-ohm, R178 made "0-ohm No Load" - R175 made 0-ohm, from "0-ohm No Load" <p>Need to do: The J28 Type-C module pin CC1 and CC2 needs 5.1k pull-down.</p>	2017/11/09

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