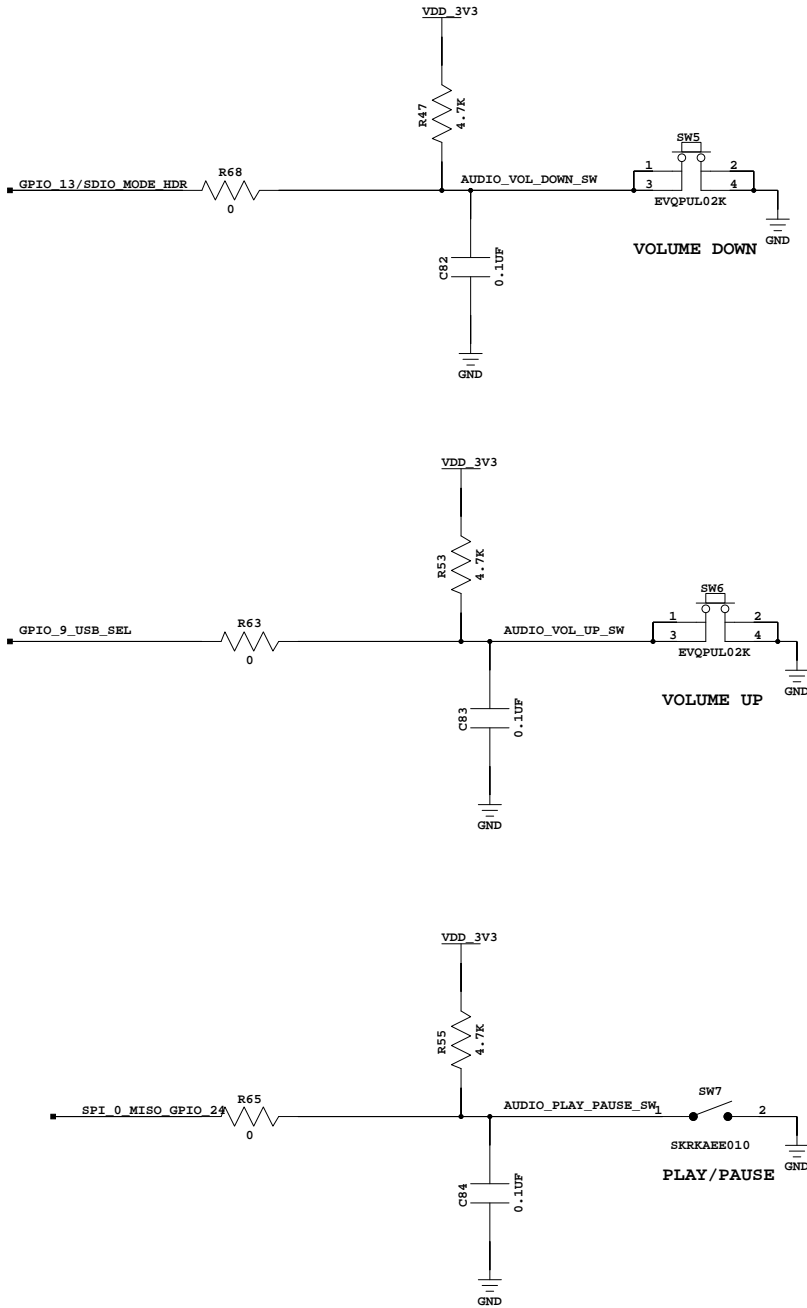
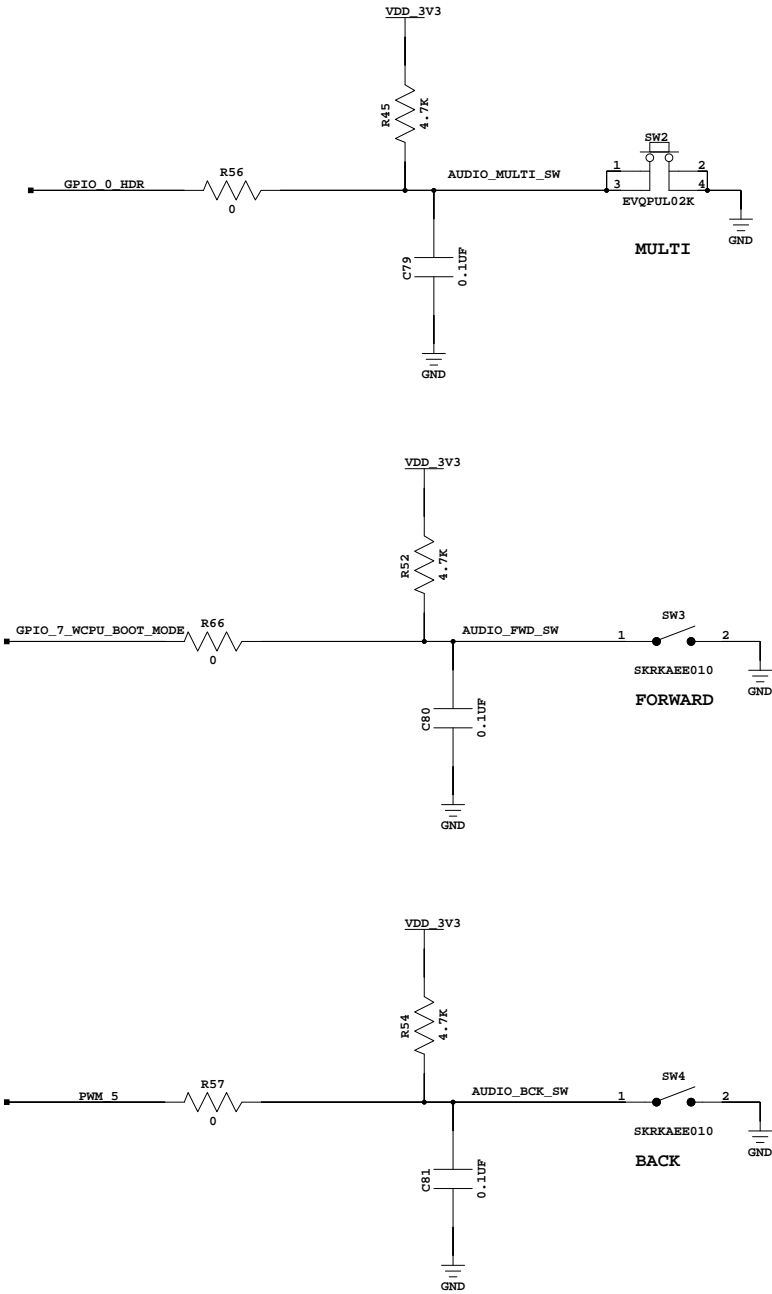
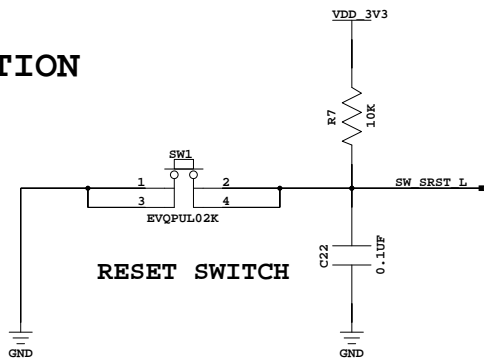


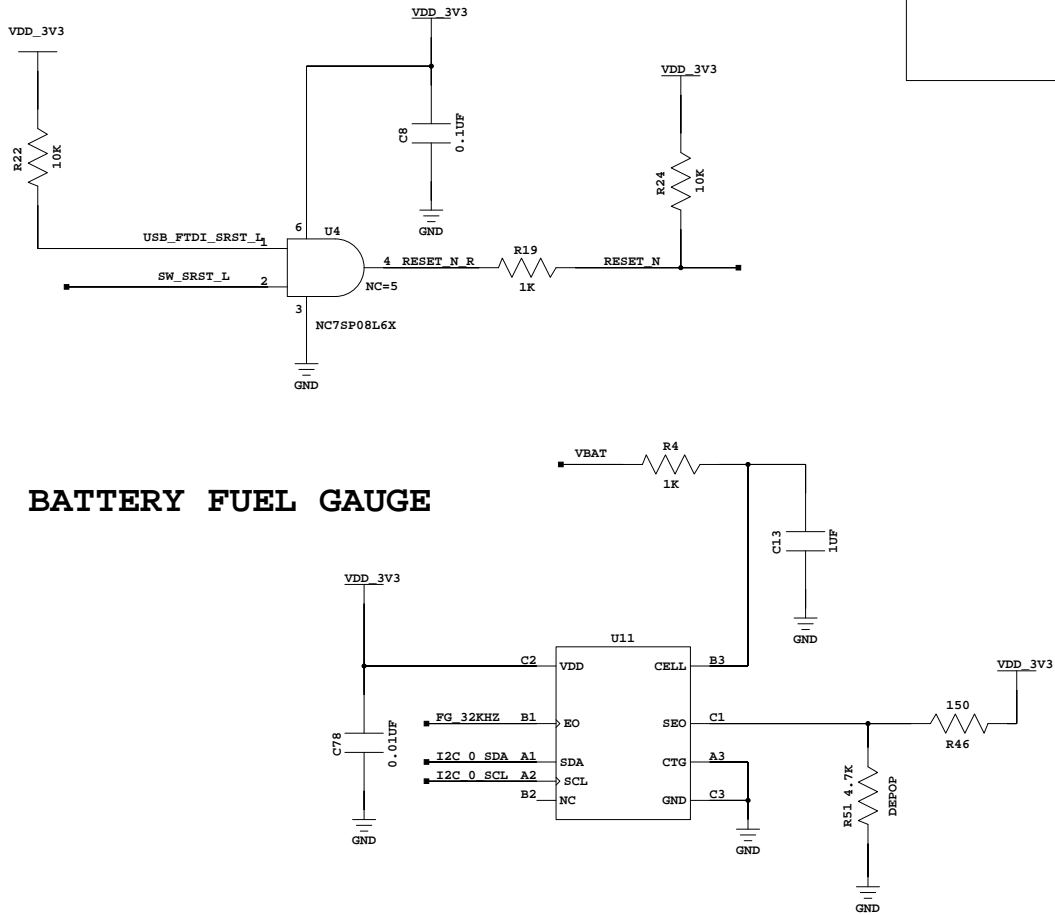
AUDIO SWITCHES ARRAY



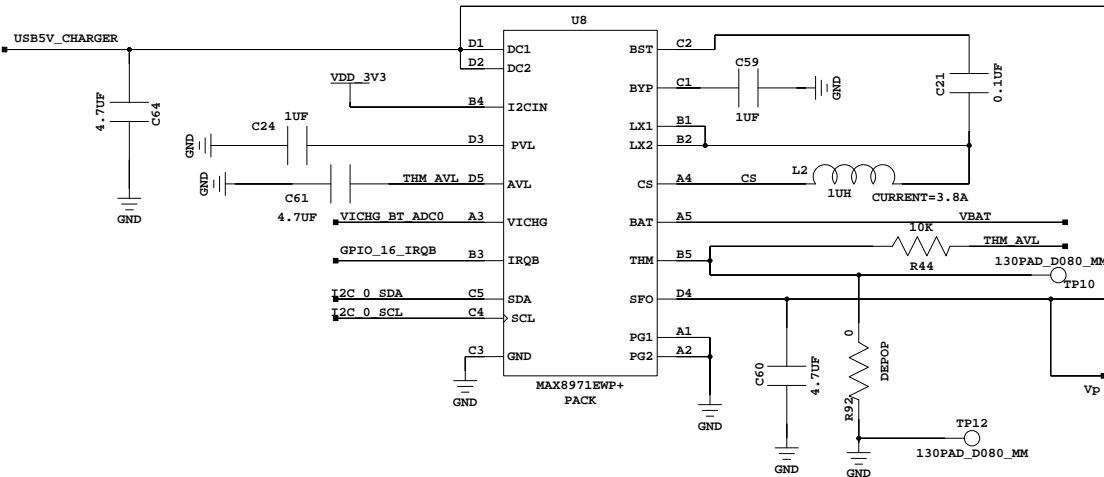
RESET FUNCTION



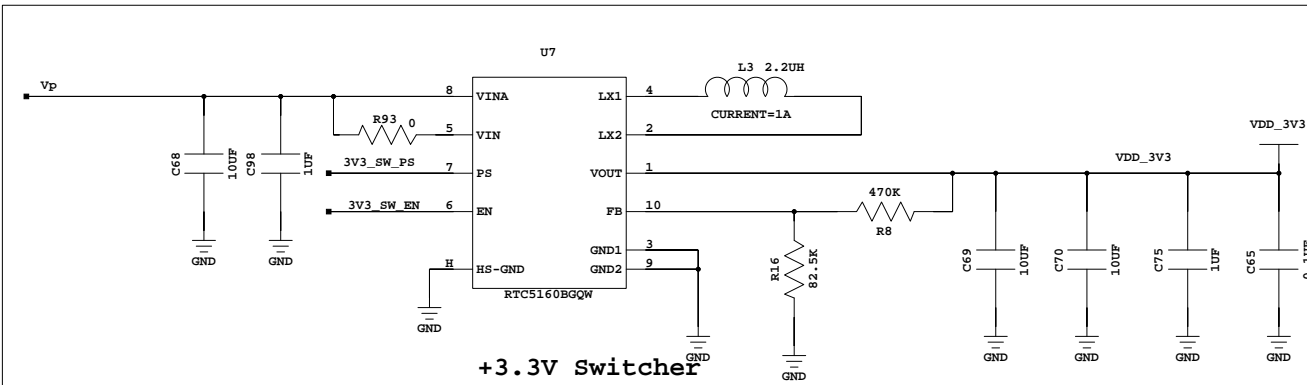
BATTERY FUEL GAUGE



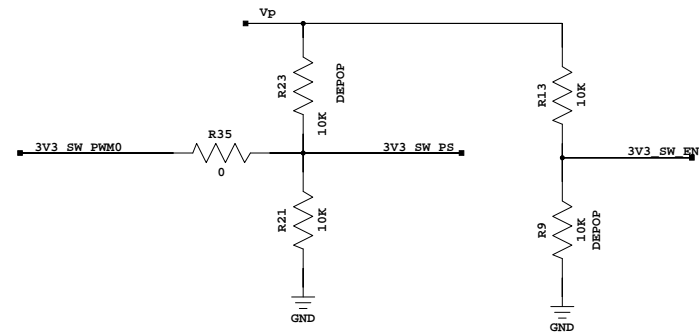
BATTERY CHARGER



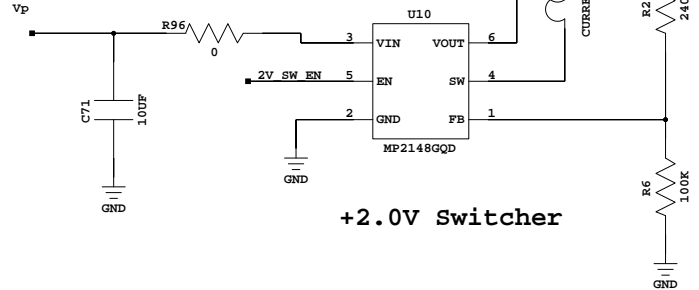
+3.3V Switcher



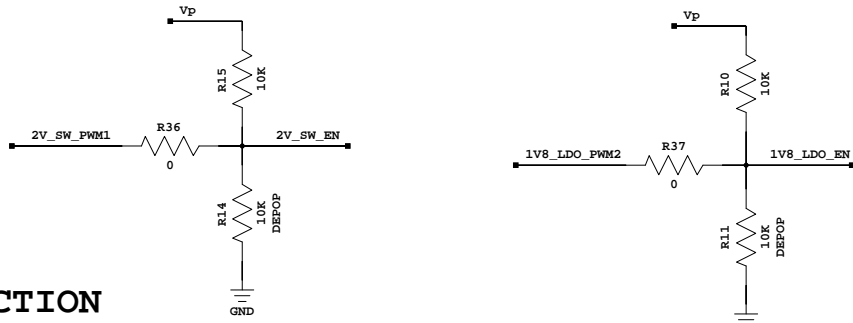
+3.3V SECTION



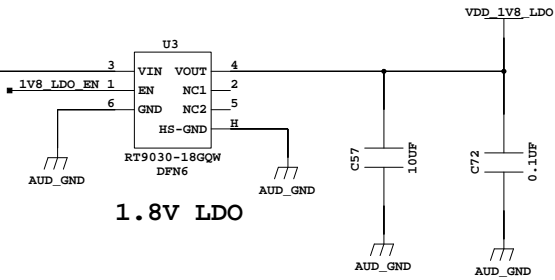
+2.0V Switcher



+1.8V SECTION



1.8V LDO



Power Supplies

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D

C

B

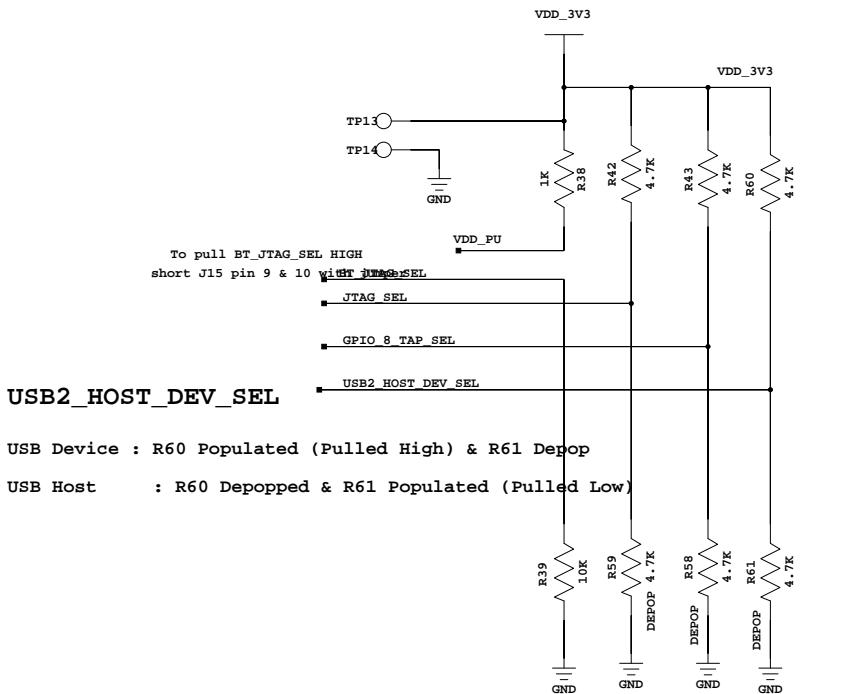
A

D

C

B

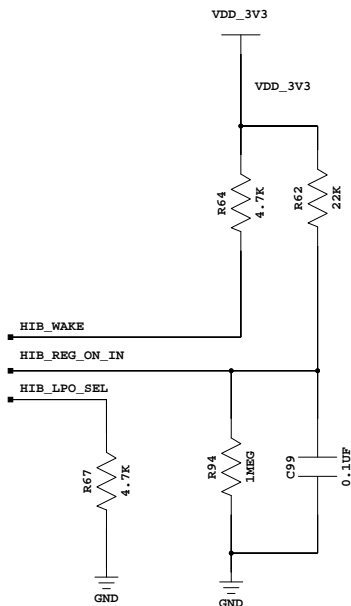
A



USB2_HOST_DEV_SEL

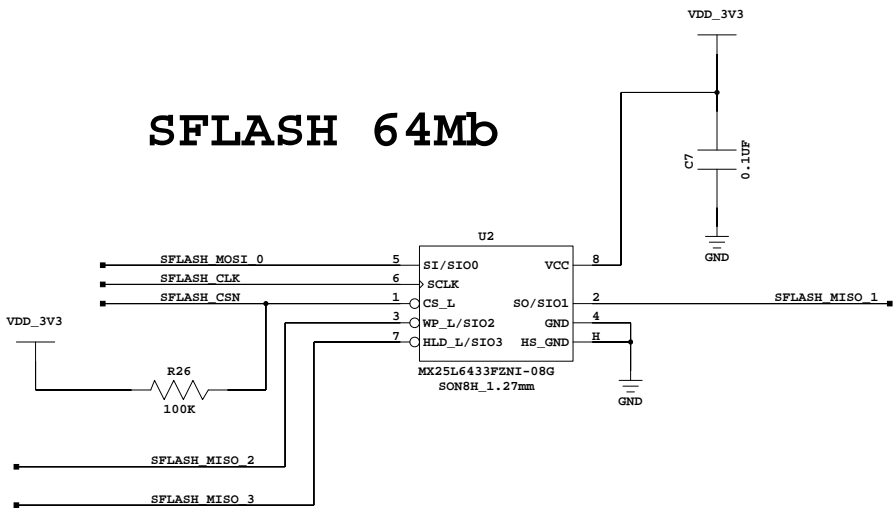
USB Device : R60 Populated (Pulled High) & R61 Depop

USB Host : R60 Depopped & R61 Populated (Pulled Low)

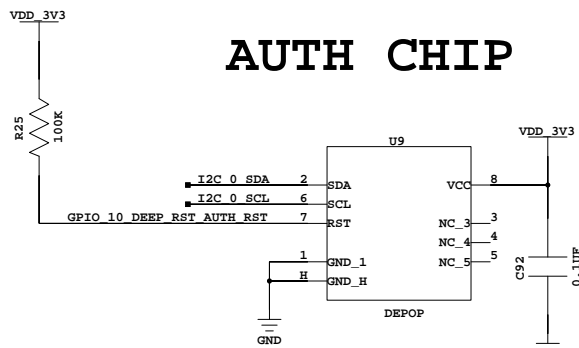


HIBERNATION STRAPPING

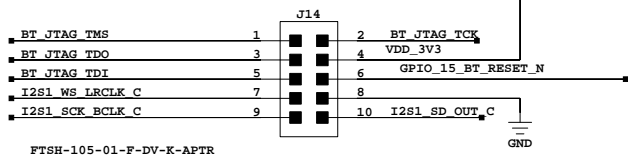
Pin	Strap Function	Strap Pull	
		Chip Default	Board Default
GPIO_1	gSPI Mode	0	
GPIO_7	WCPU Boot Mode0 := TCROM Boot 1 = TCMSRAM Boot	0	1 REFER TO AUDIO SWITCHES ARRAY
GPIO_9	USB/HSIC Sel :0 = HSIC PHY 1 = USB PHY	0	1 REFER TO AUDIO SWITCHES ARRAY
GPIO_11	ACPU Boot Mode0 := SOCROM Boot 1 = SOCSRAM Boot	0	
GPIO_13	SDIO Mode : 0 = SDIO Device 1 = SDIO Host	0	
RF_SW_CTRL_5	Host DAP Clock Sel	0	
RF_SW_CTRL_7	Host RSRC Init	0	



SFLASH 64Mb

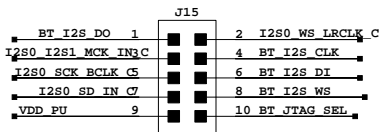


AUTH CHIP



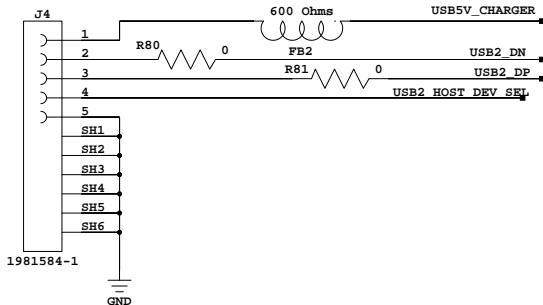
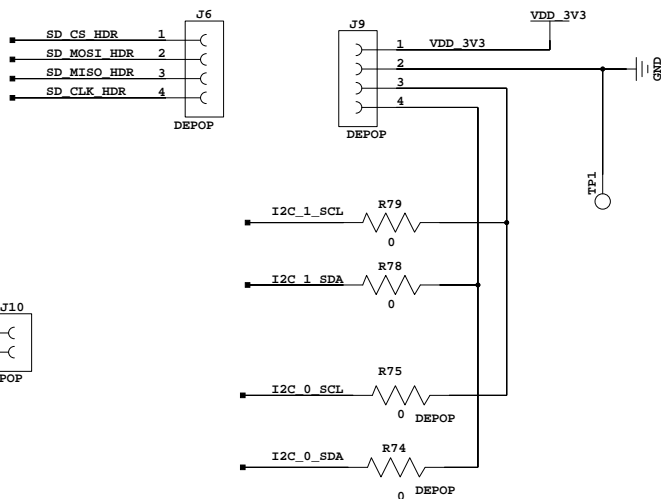
BT JTAG/UART, WLAN I2S1 Micro Header

BT UART lines mulitplexed on BT JTAG signals as shown on Page5

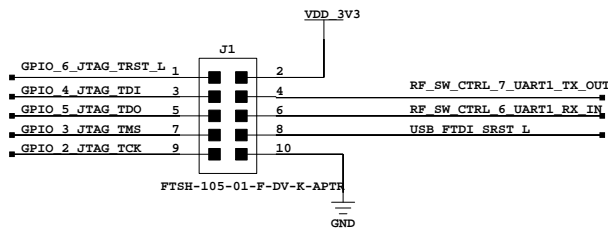


BT I2S, WLAN I2S0 Micro Header

Display 2.54mm Header

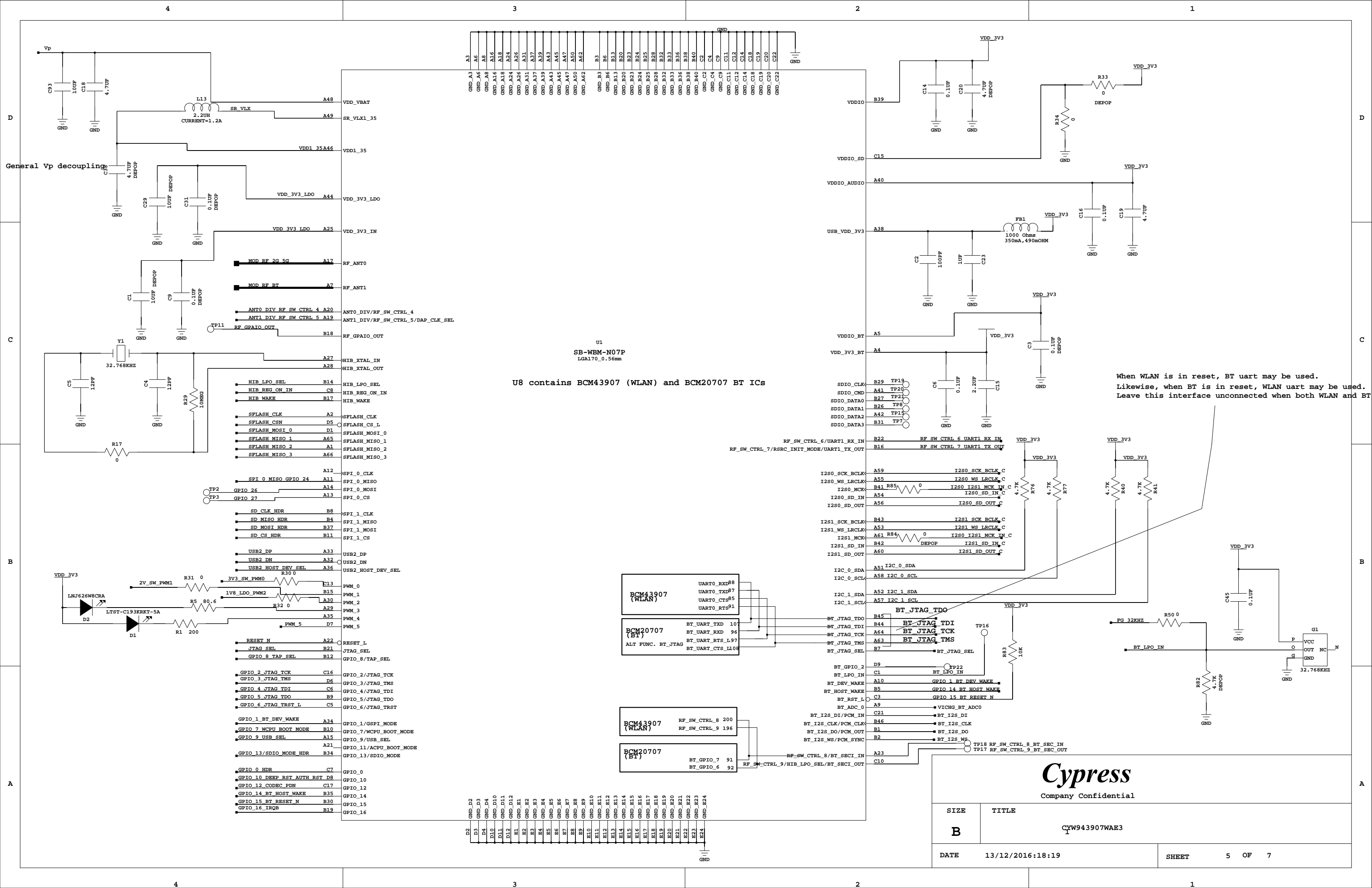


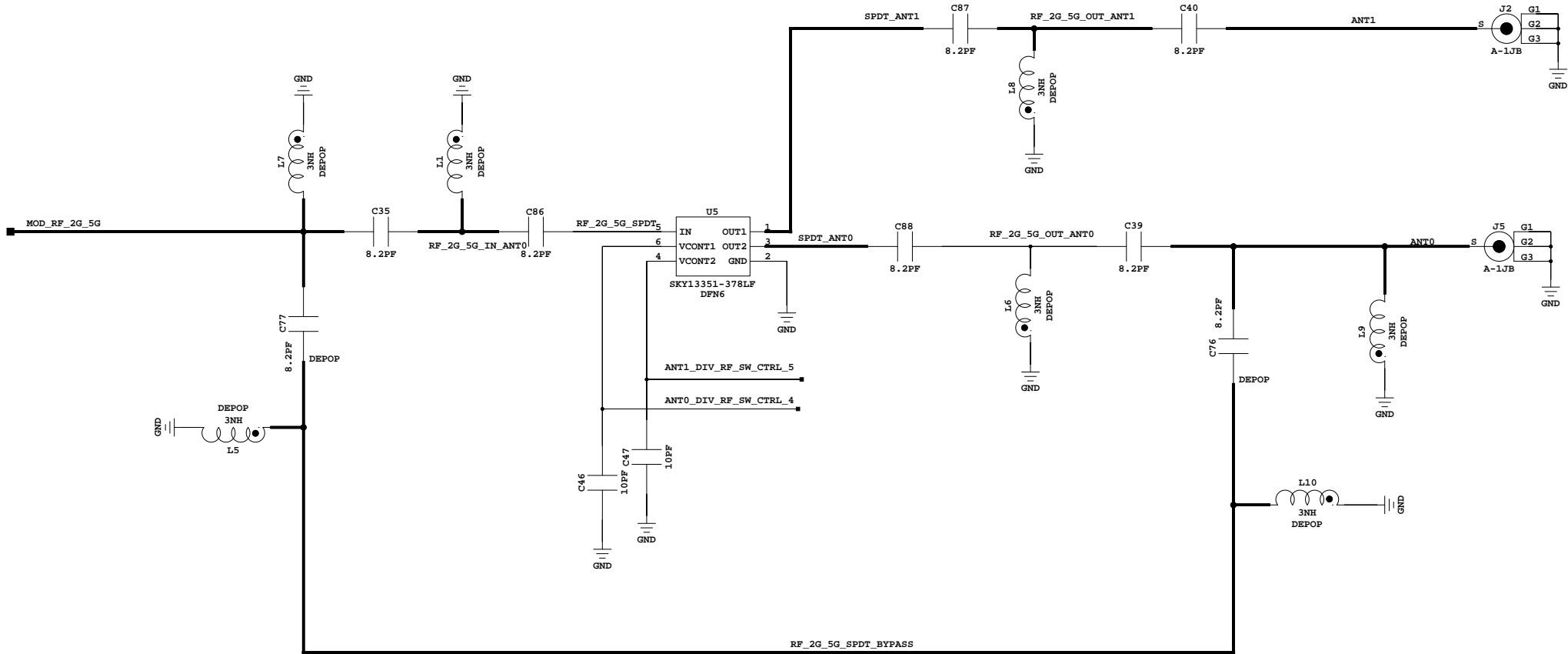
Micro USB WLAN JTAG/UART1 Micro Header



Straps + SFLASH + MI

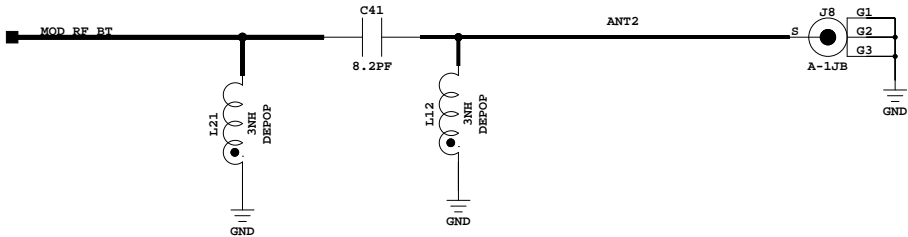
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U5 2G/5G SPDT Antenna Diversity Switch Control Table		
MODE OF OPERATION Ant Diversity	ANT0_DIV_RF_SW_CTRL_4 SPDT (U5 VCONT1)	ANT1_DIV_RF_SW_CTRL_5 DPDT (U5 VCONT2)
RF_2G_5G to Ant0	1	0
RF_2G_5G to Ant1	0	1

ALL OTHER STATES UNDEFINED

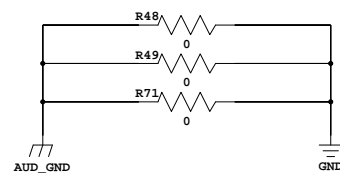
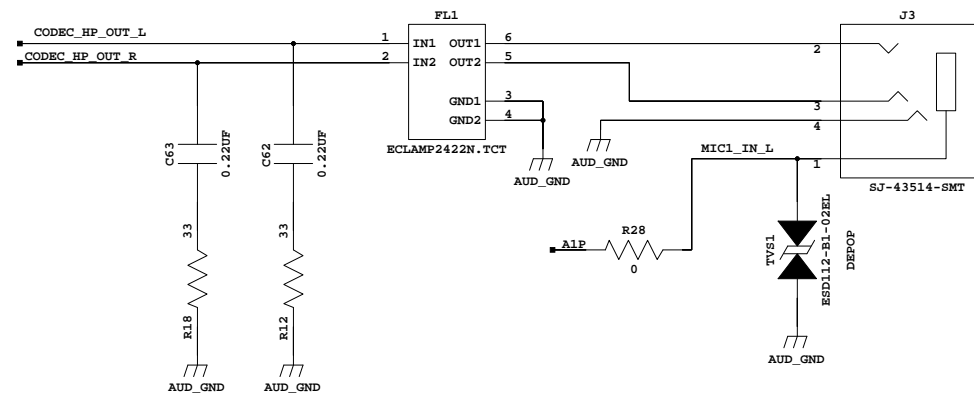
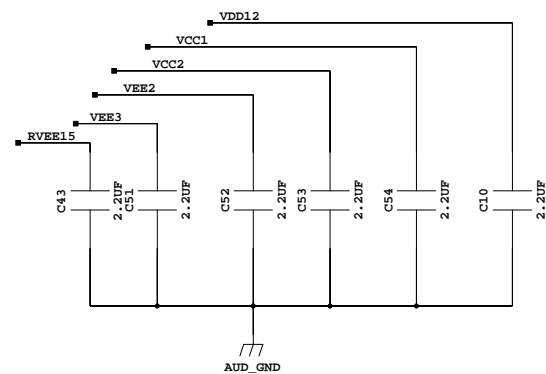
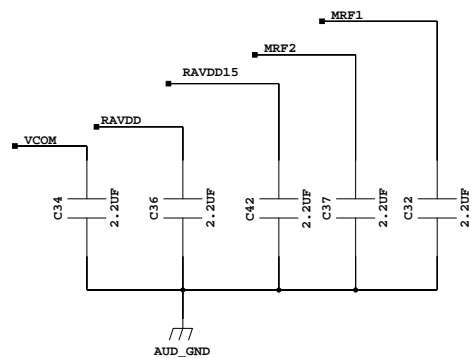
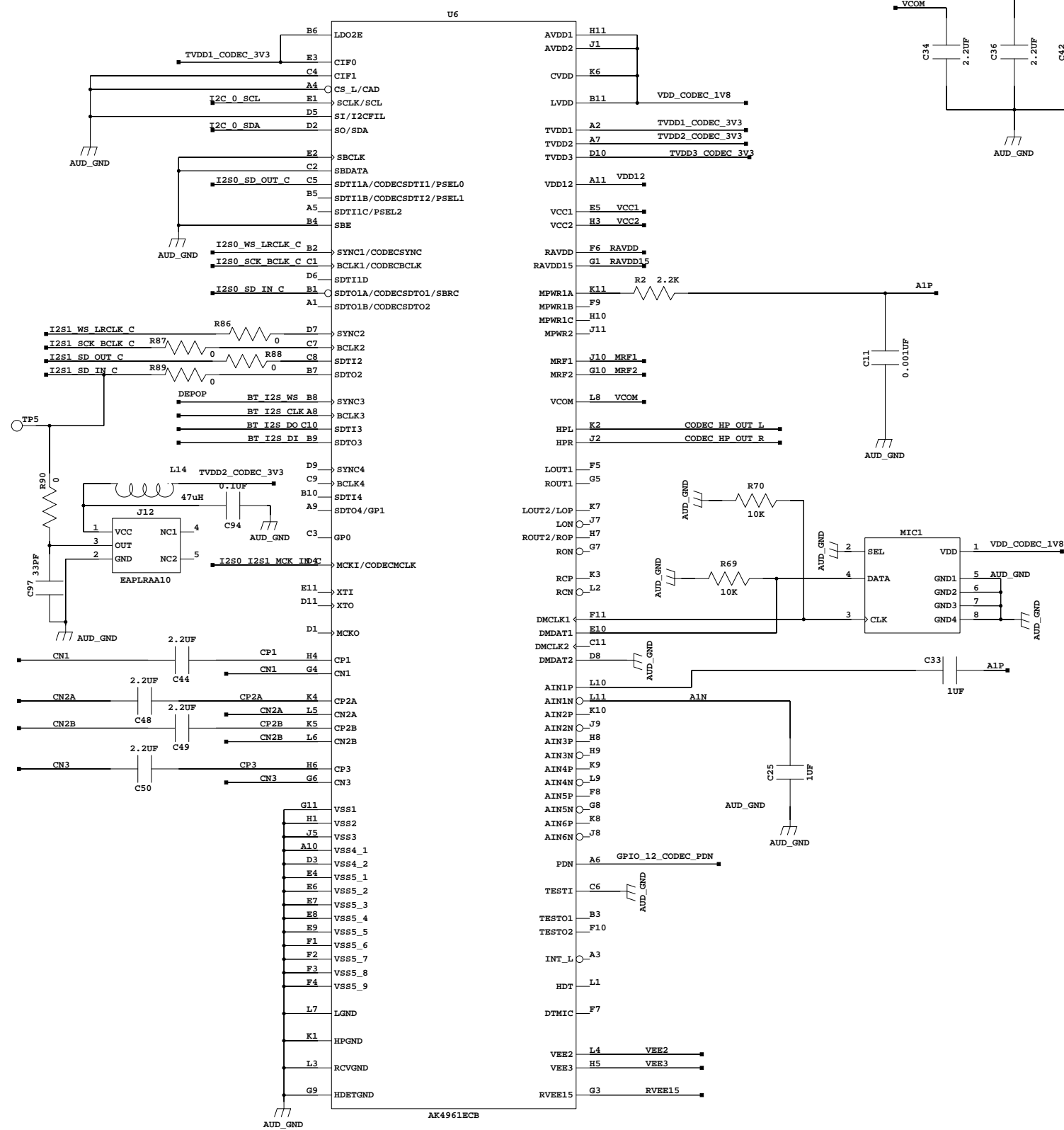


ANTENNA DIVERSITY

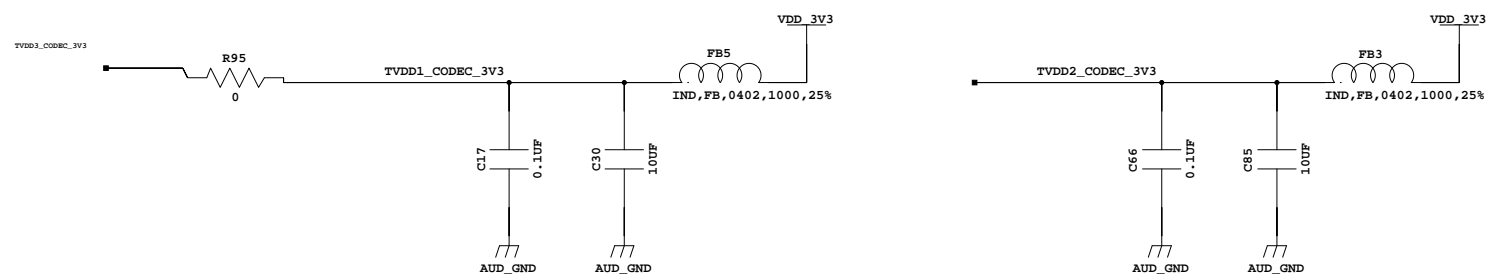
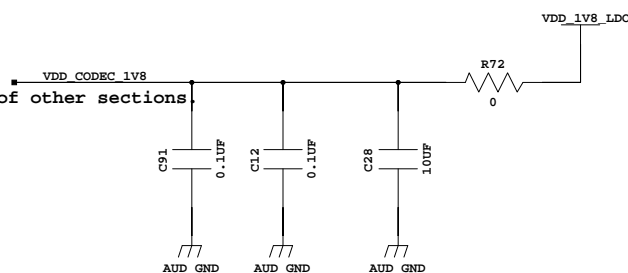
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Audio Section has a separate Audio GND to isolate from noise of other sections
It connects to common GND (GND) with a 0 Ohms Resistors



AUDIO CODEC

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