CY8CKIT-062-WiFi-BT PSoC 6 WiFi-BT Pioneer Kit

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Drawing Numbers	
PCBA	121-60435-01
PCB	600-60435-01
FAB DRW	610-60435-01
ASSY DRW	620-60435-01
SCH DRW	630-60435-01

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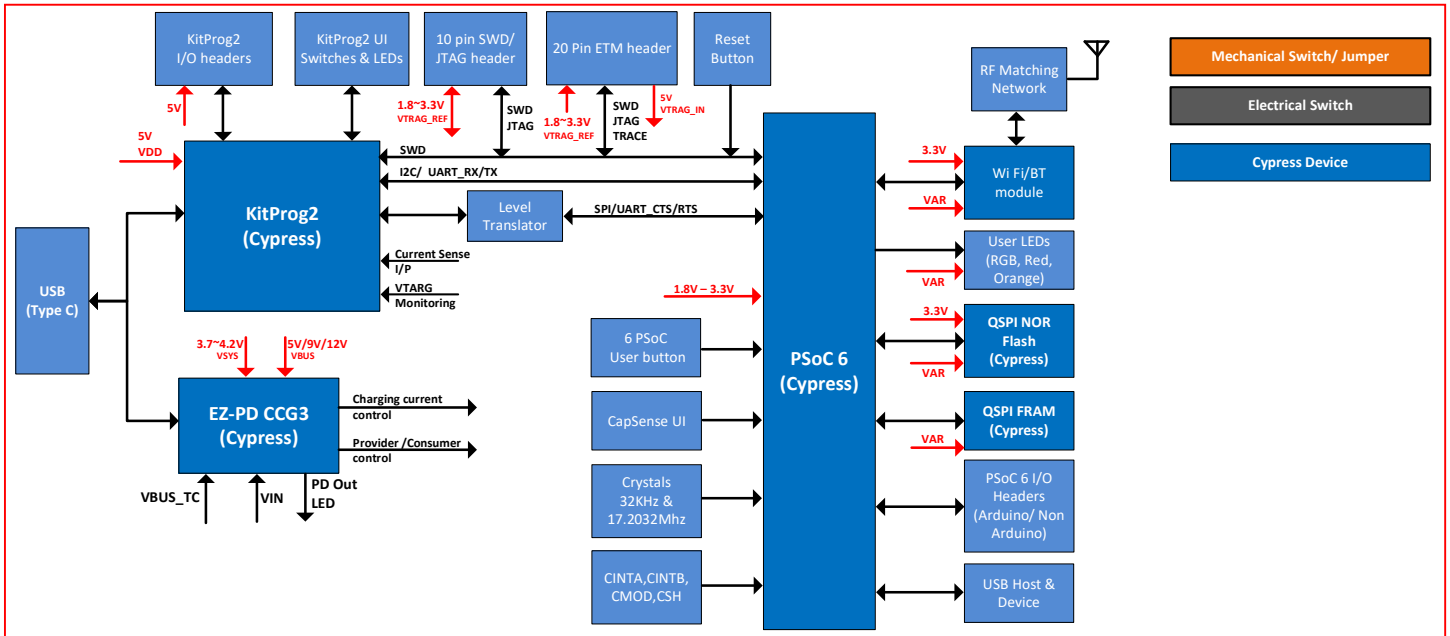
SCH Title : CY8CKIT-062-WiFi-BT PSoC 6 WiFi-BT Pioneer Kit

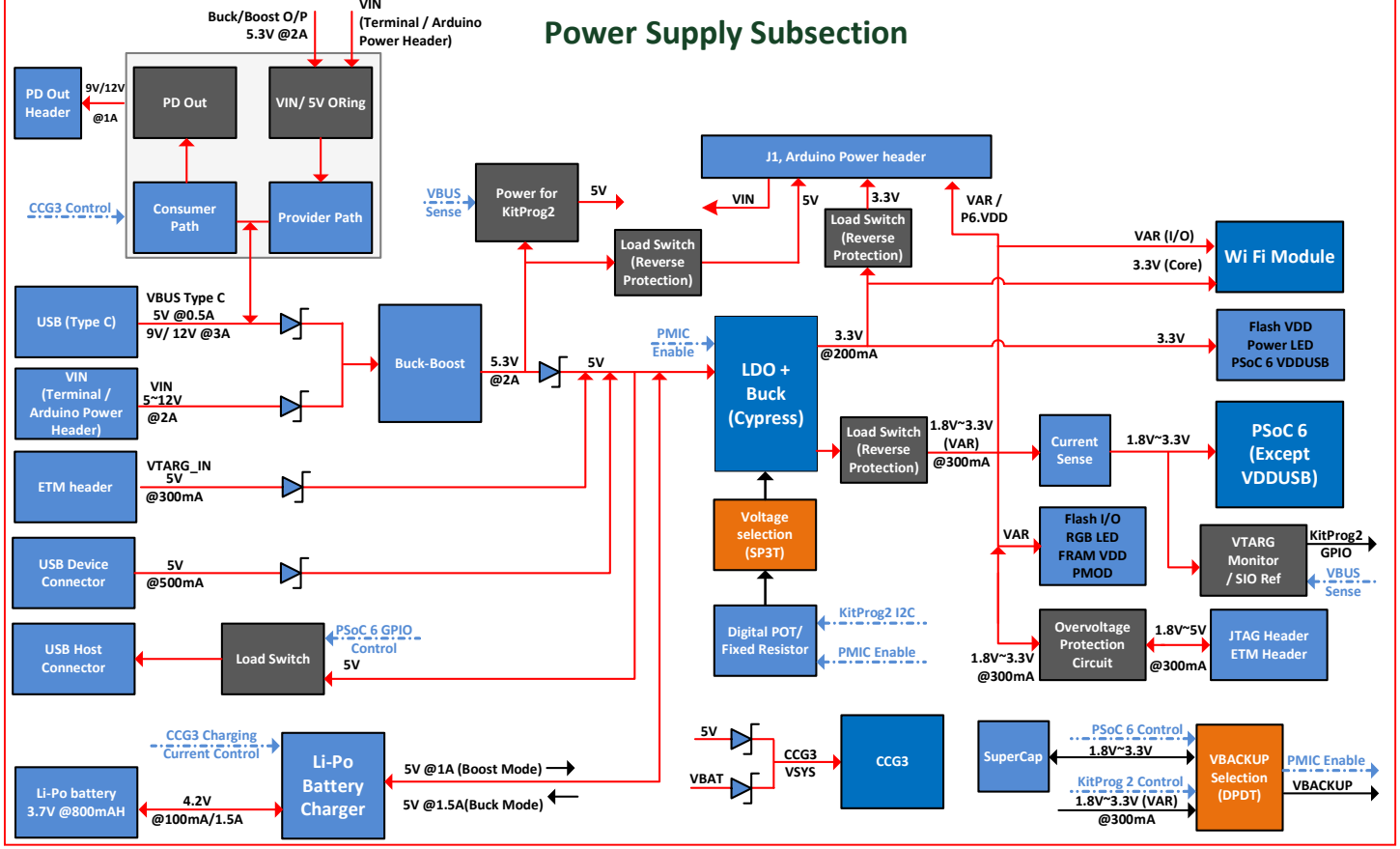
Page Title :Title Page

Size	Document Number	Drawn By	Approved By	Rev
A4	630-60435-01	AARA	RKAD	2.9

Date: Thursday, November 09, 2017 Sheet 1 of 16



Power Supply Subsection



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SCH Title : CY8CKIT-062-WiFi-BT PSoC 6 WiFi-BT Pioneer Kit				
Page Title :Block Diagram				
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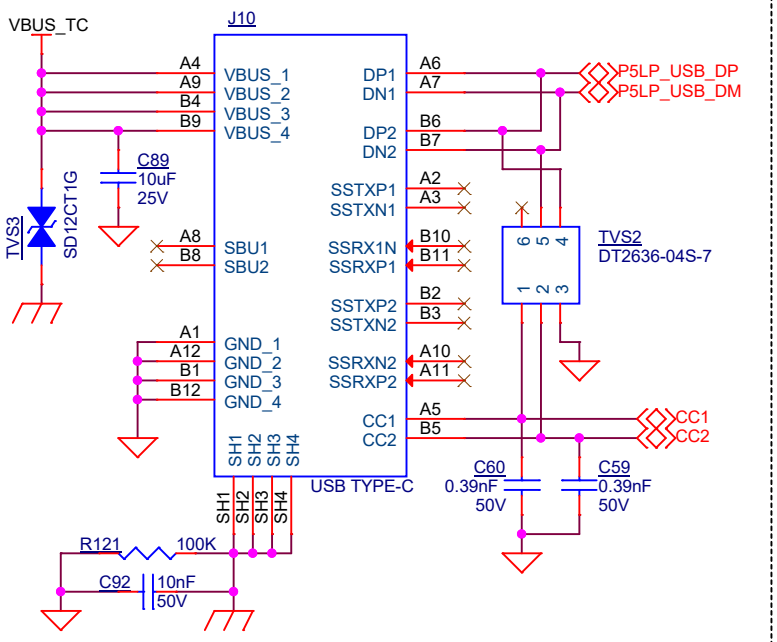
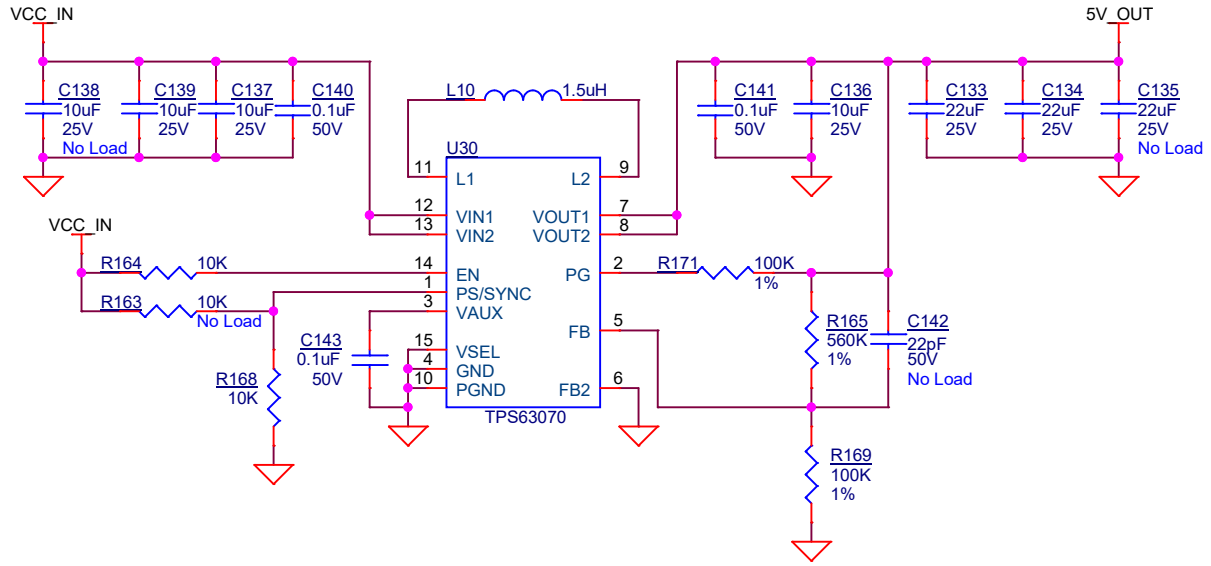
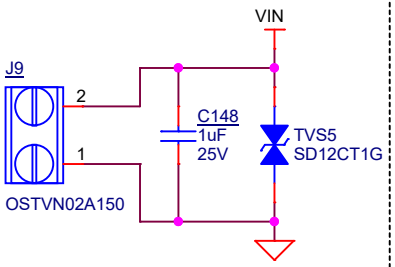
KitProg2 USB Type-C Connector

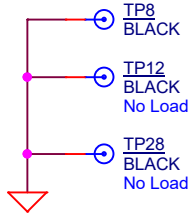


5V Buck-Boost Regulator

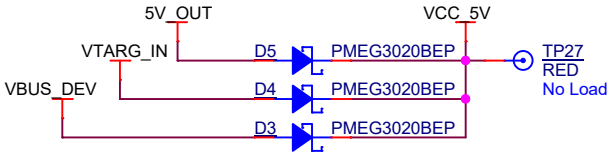


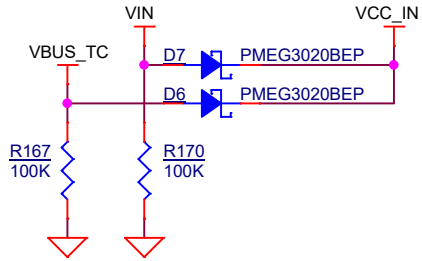
VIN Header



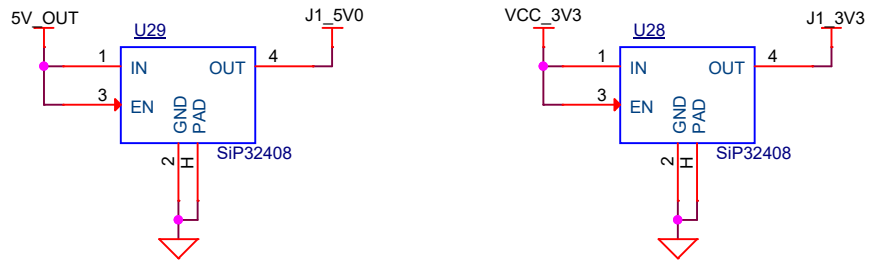


Power Supply 'OR'ing





Arduino Header O/P



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Page Title :5V Buck/Boost Regulator

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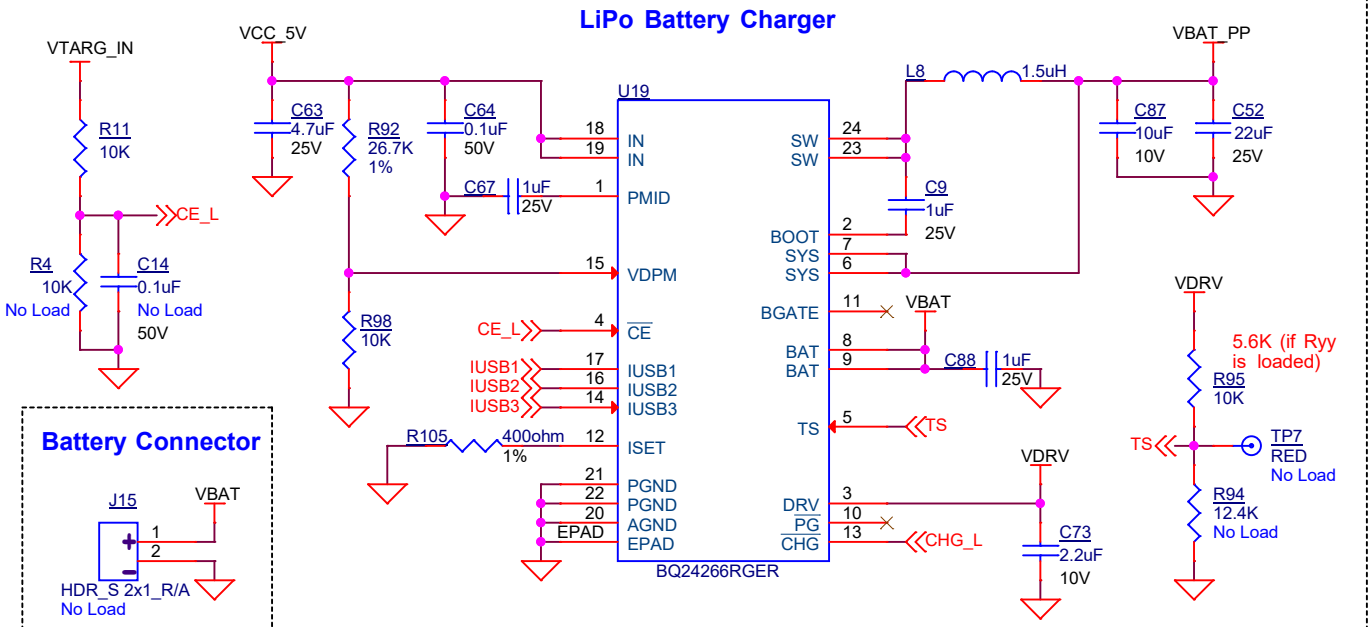
LiPo Battery Charger

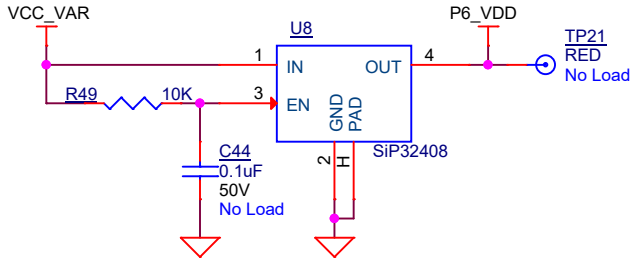


Battery Connector

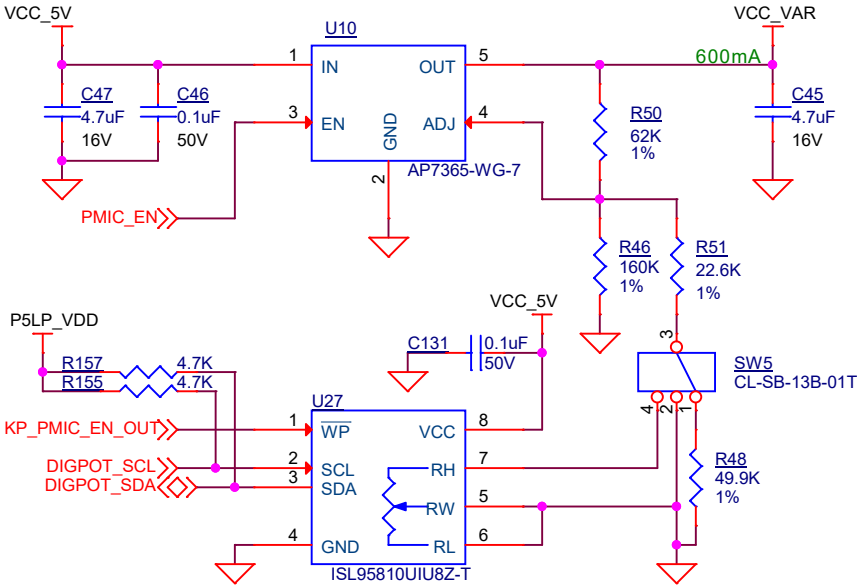
Charging LED

Power LED

Reverse Voltage Protection

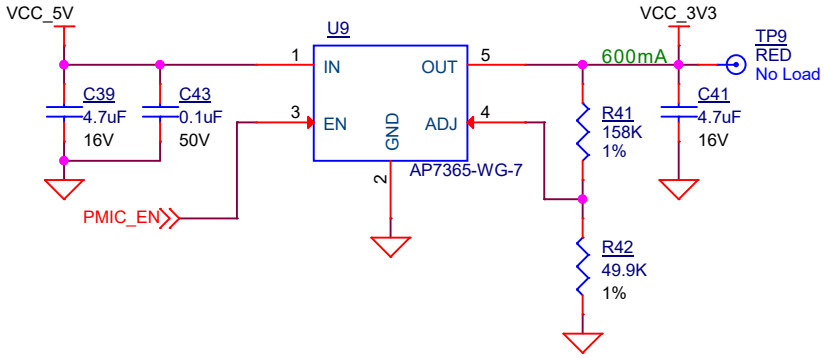


1.8V - 3.3V Variable Regulator



SW5	Source
POS1	1.8V
POS2	3.3V
POS3	Variable (1.8-3.3V)

3.3V Regulator



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Page Title :Variable Regulator, Charger

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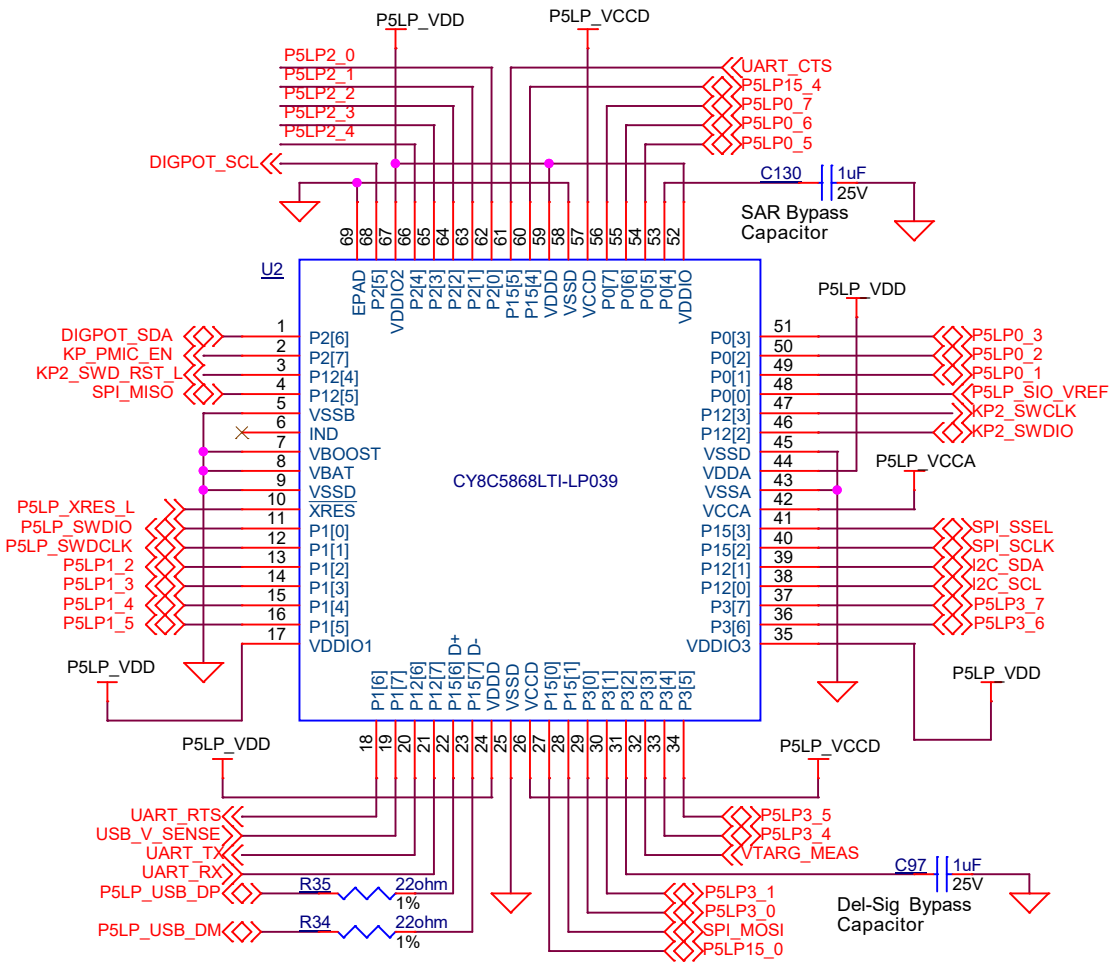
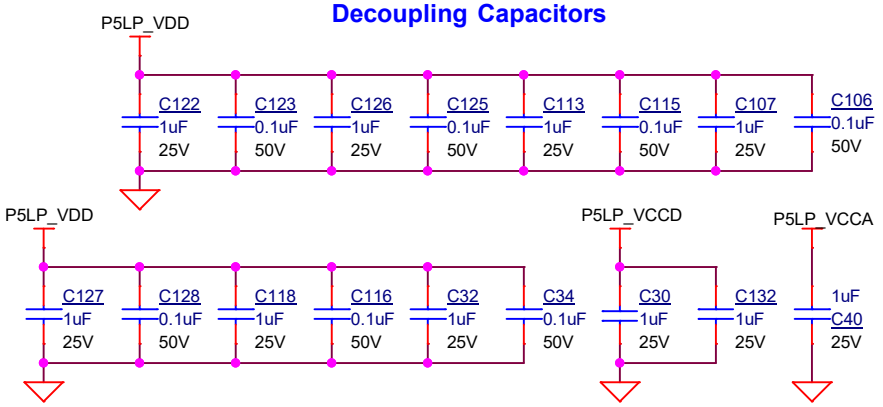
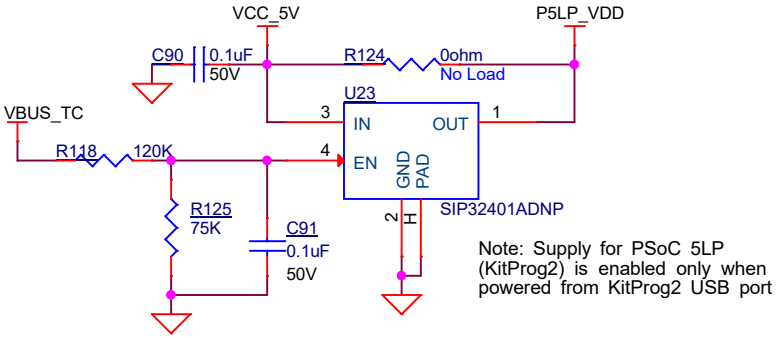
PSoC 5LP based KitProg2



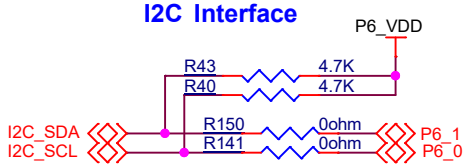
Decoupling Capacitors



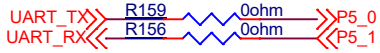
Supply for PSoC 5LP



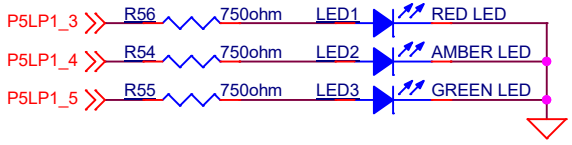
I2C Interface



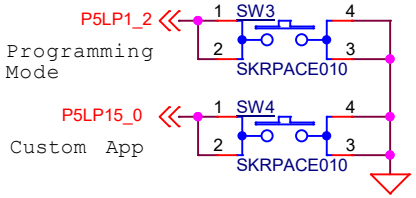
UART Interface



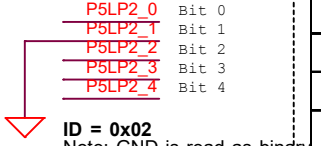
PSoC 5LP Status LEDs



PSoC 5LP User Switches



KitProg2 HW Revision



ID = 0x02
Note: GND is read as binary "1" and floating as "0"

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Page Title :KitProg2 Controller				
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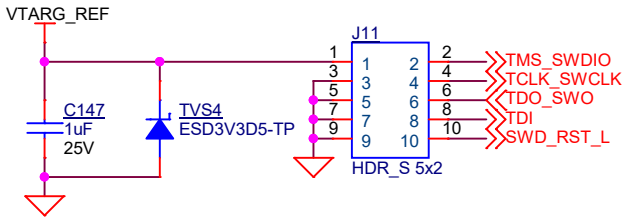
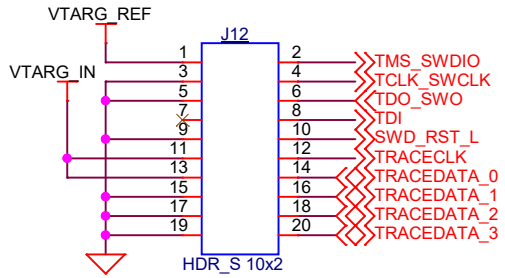
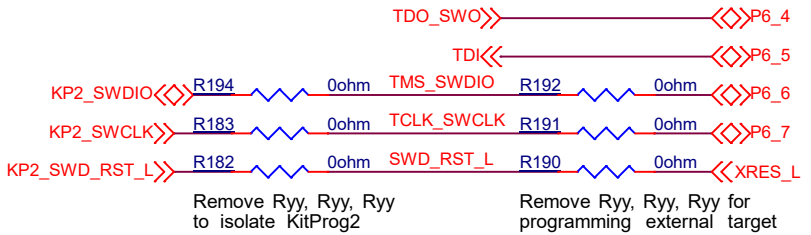
Target PSoC Program/Debug Header



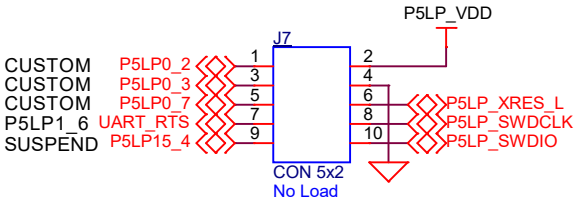
ETM Header



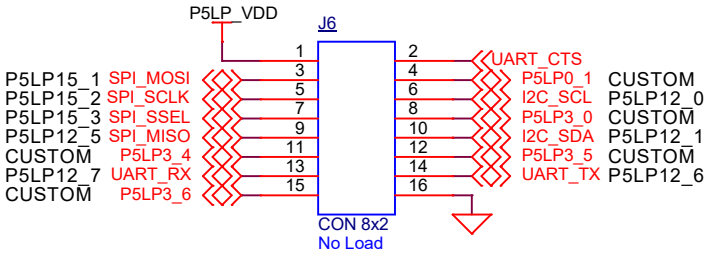
PSoC 6 SWD/JTAG Interface



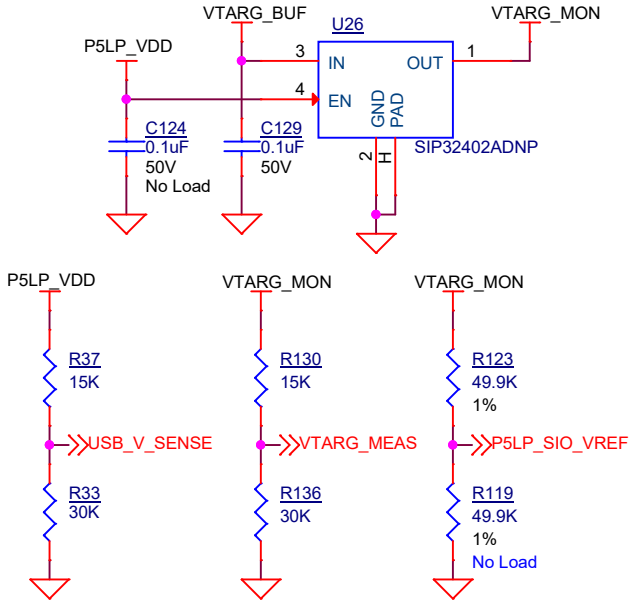
PSoC 5LP Custom Application Header



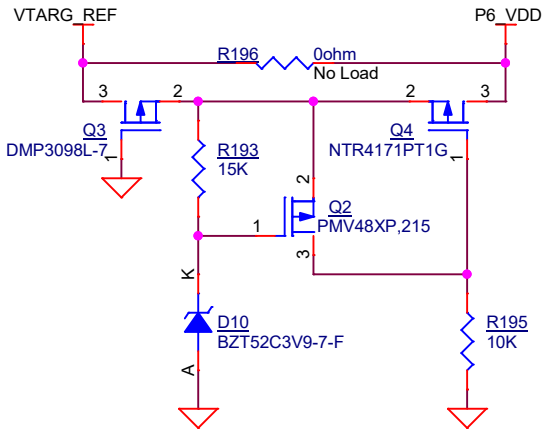
PSoC 5LP GPIO Expansion Header



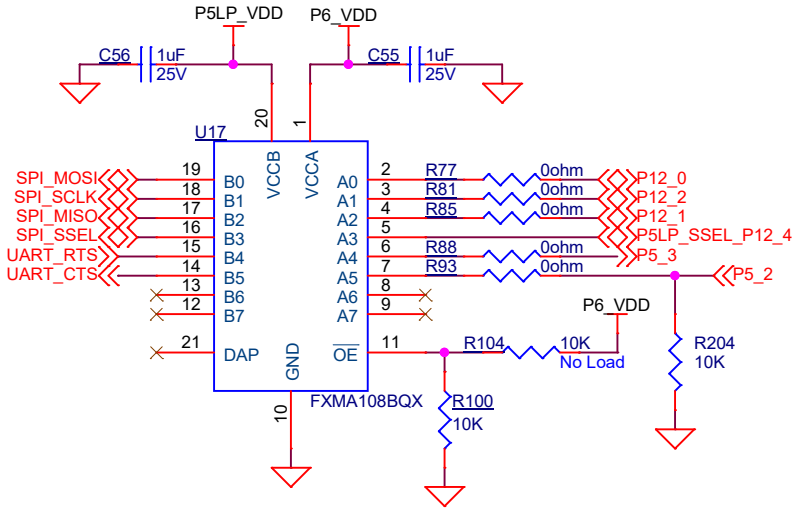
Voltage Monitoring



Program/Debug Overvoltage Protection



Level Translator for SPI and UART flow control



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Page Title :Kitprog2 Power & Headers

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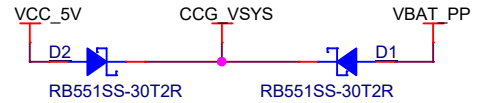
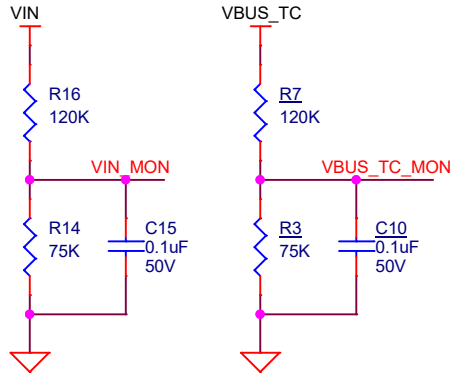
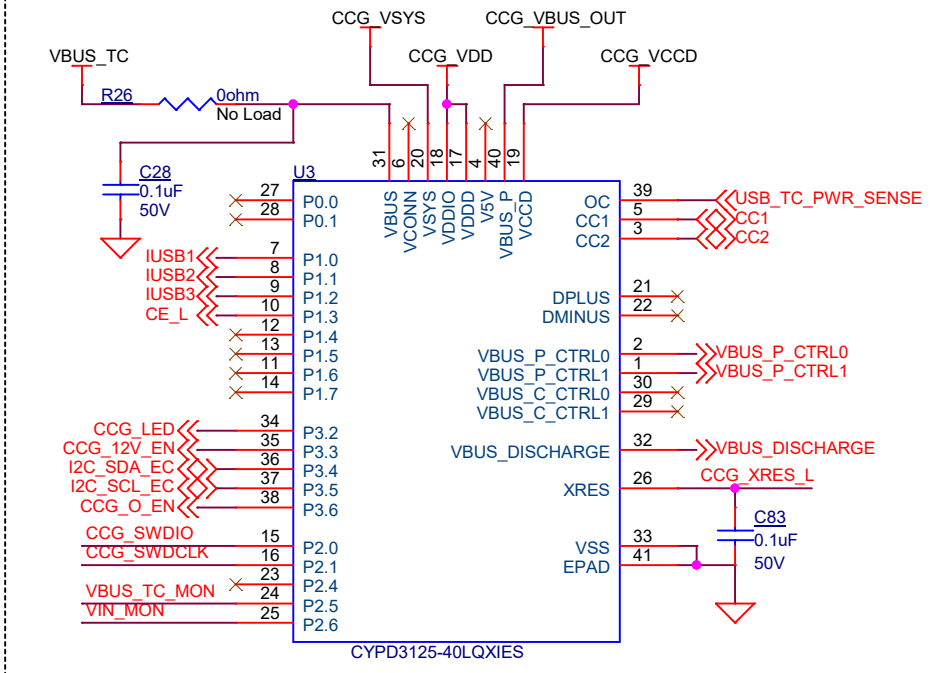
CCG3 Supply Selection



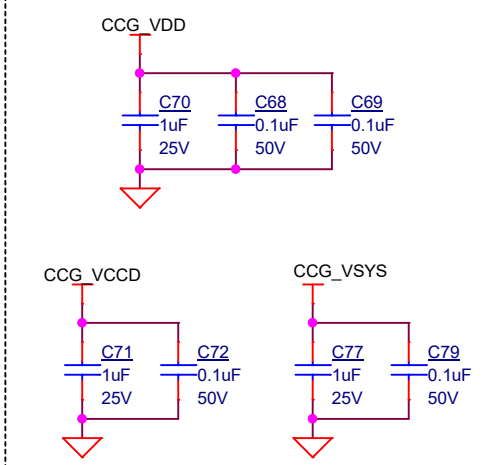
VBUS & VIN Voltage Monitoring



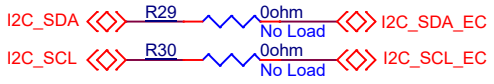
CCG3 USB Type-C Controller



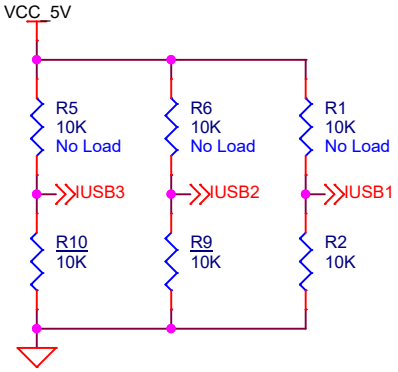
Decoupling Capacitors



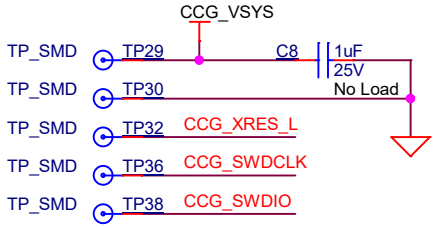
I2C Bootloader



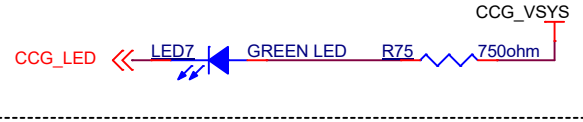
LiPo Battery Charger Pull Up



CCG3 Programming



Output Indication



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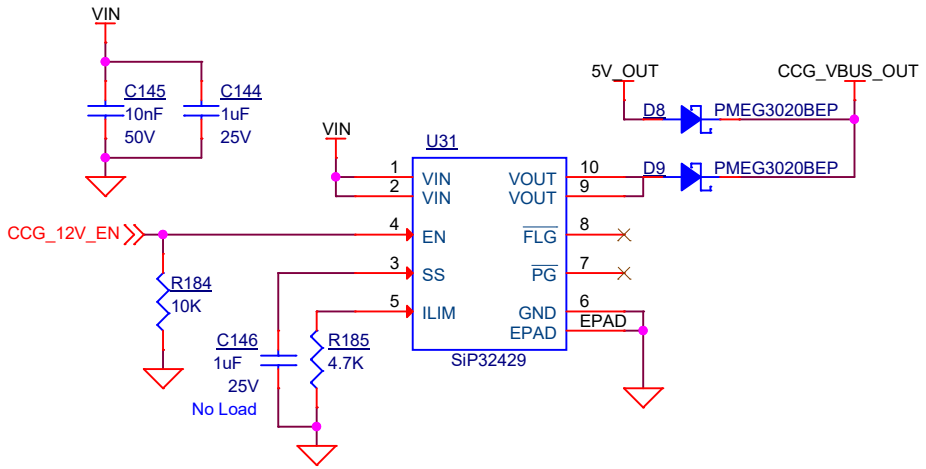
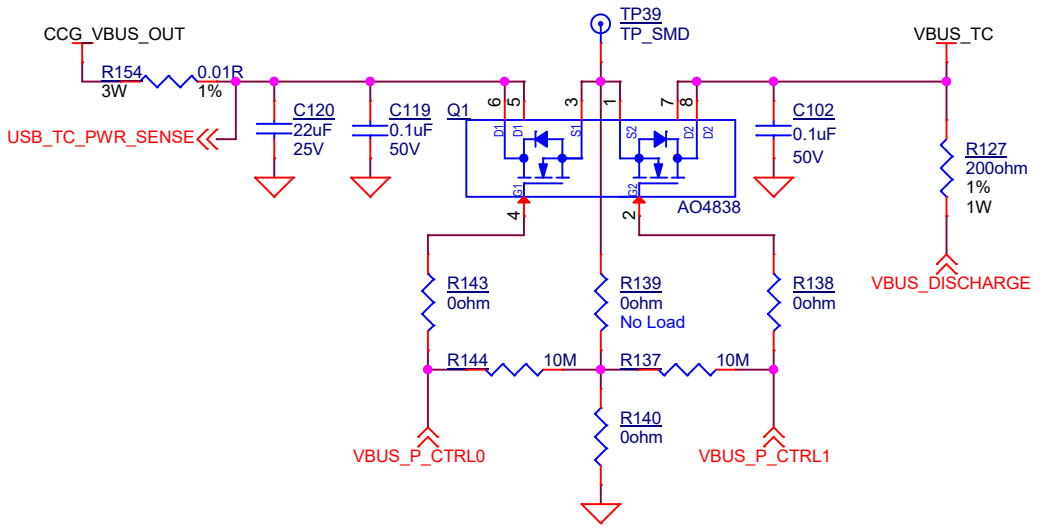
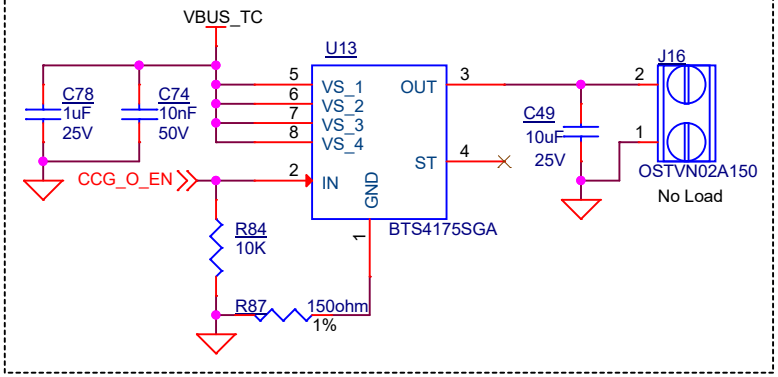
CCG3 Provider Path 'OR'ing



VBUS Provider Path



CCG3 Consumer Path



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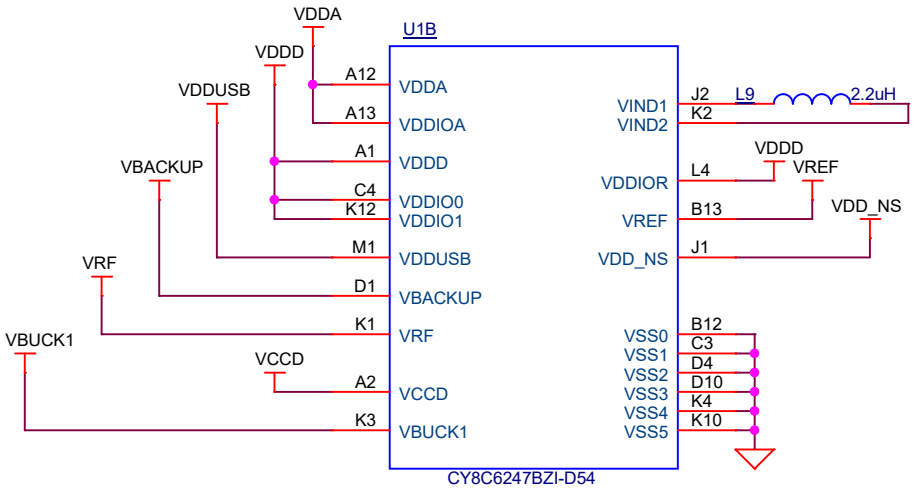
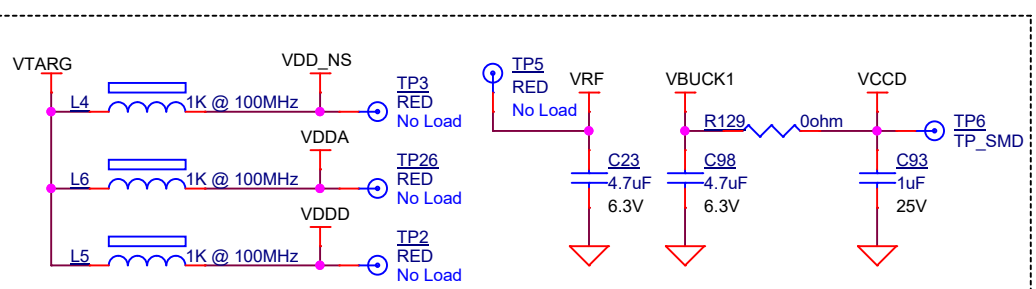
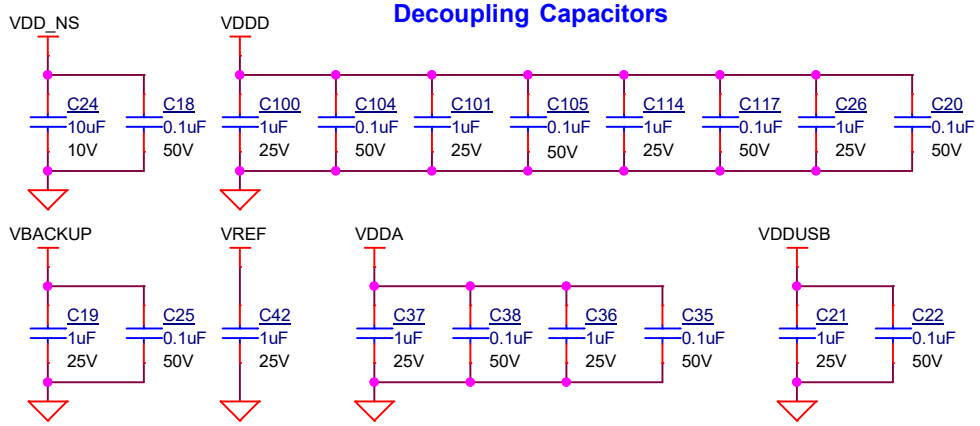
PSoC 6 Power

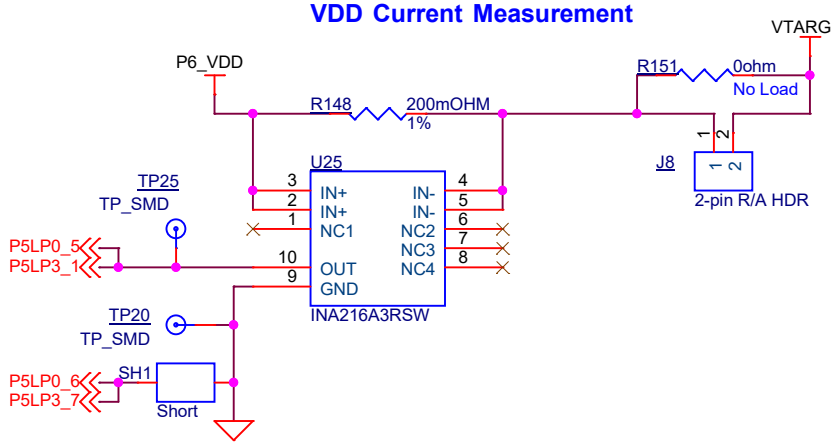




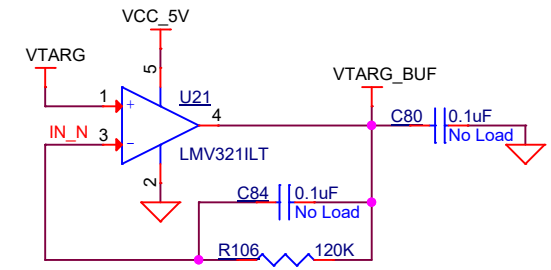
Decoupling Capacitors



VDD Current Measurement

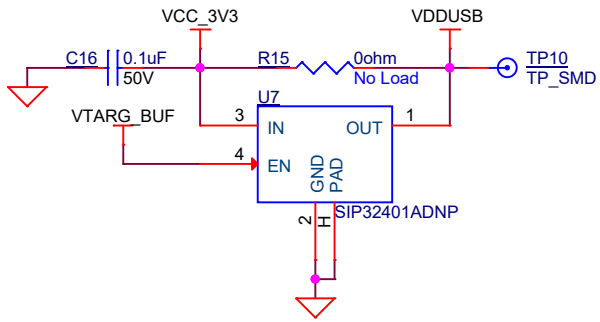


Voltage Follower



Note: This circuit is to reduce the leakage current in VTARG domain

PSoC 6 VDDUSB Enable



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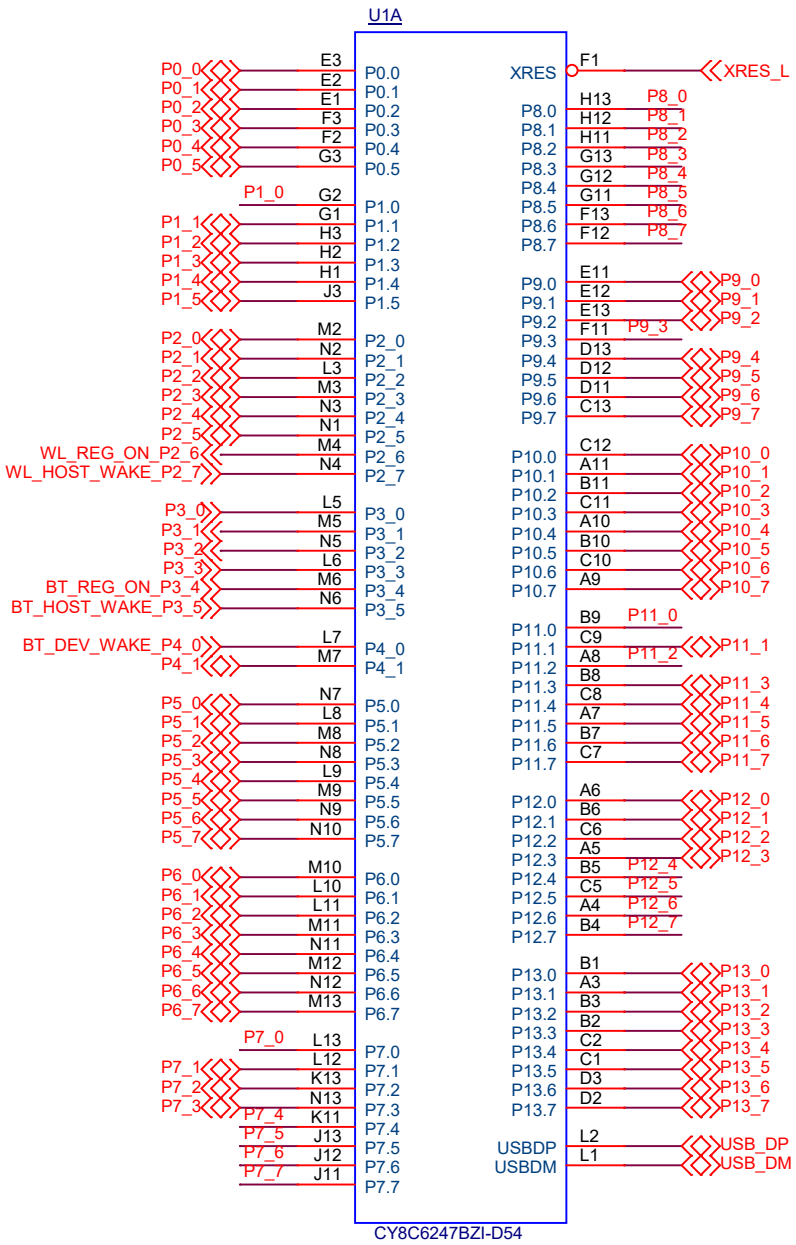
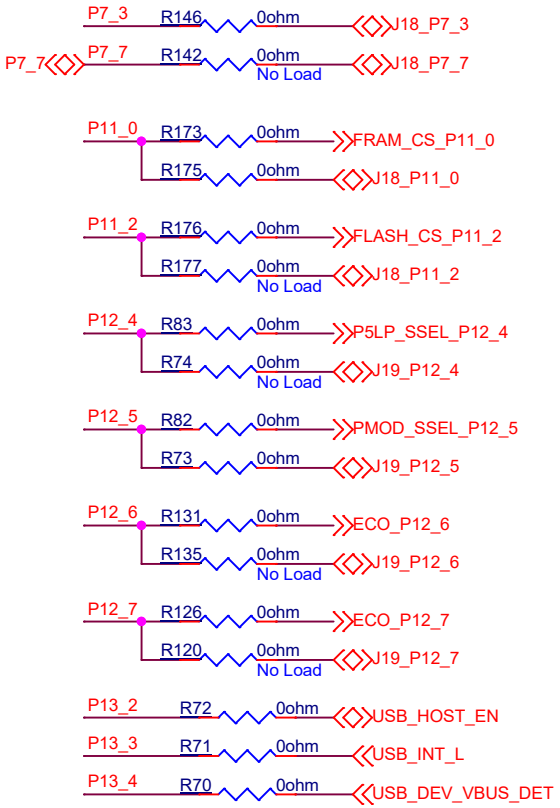
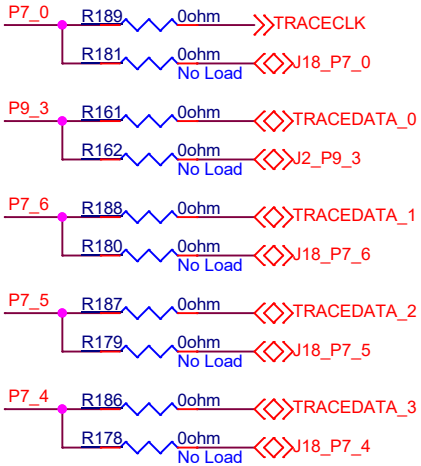
PSoC 6 Signals



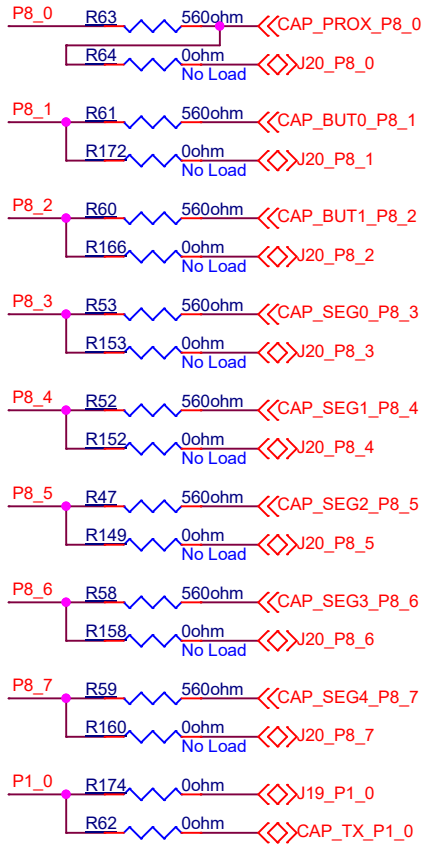
Additional Multiplexed Pins



TRACE Multiplexed Pins



CapSense Multiplexed Pins



Note: Option for WLAN to wake PSoC 6 from Hibernate

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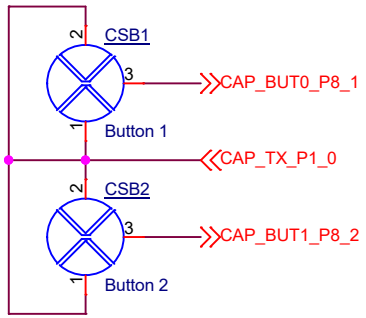
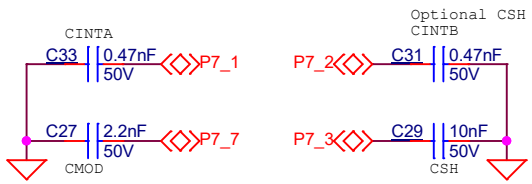
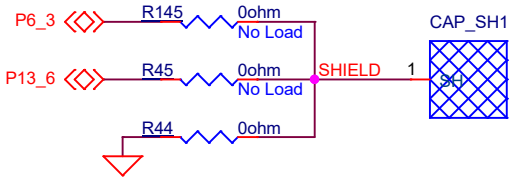
CapSense Button



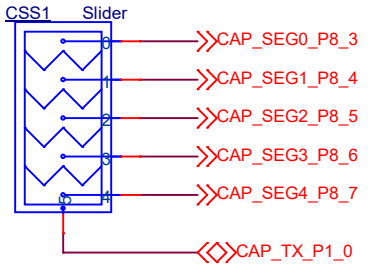
CMOD, CSH & CINT



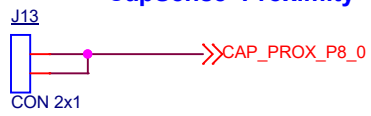
CapSense Shield



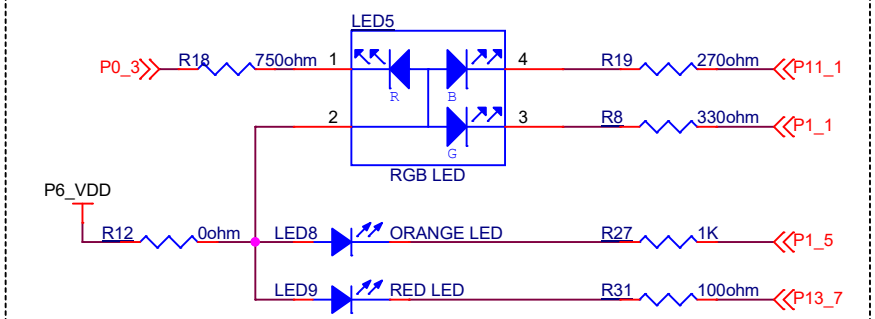
CapSense Slider



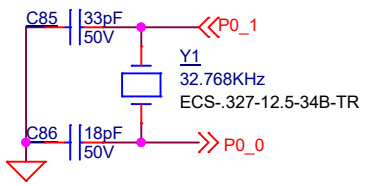
CapSense Proximity



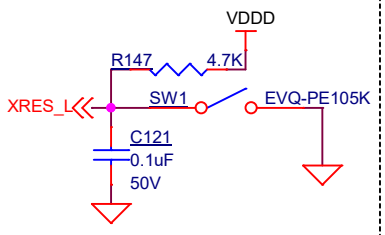
User LEDs



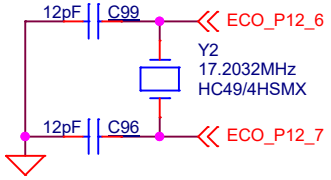
WCO



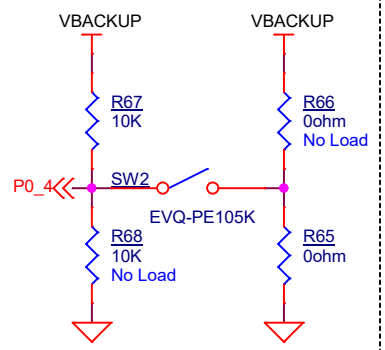
Reset Button



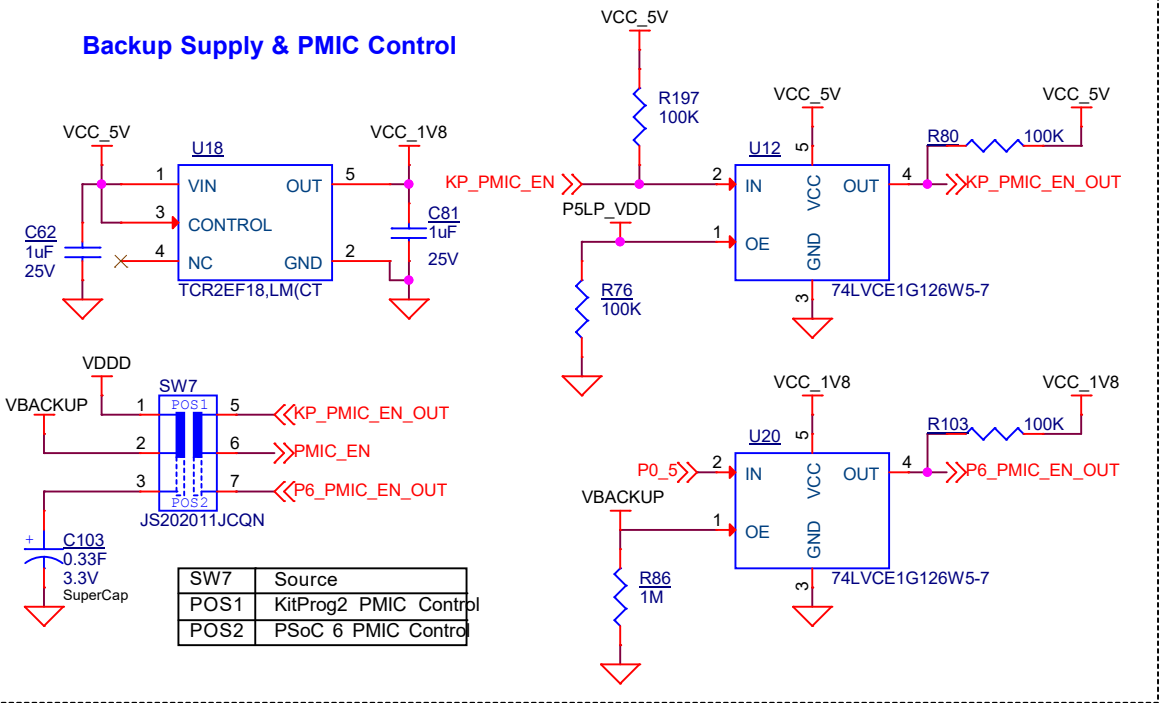
ECO



User Button / Hibernate Wakeup



Backup Supply & PMIC Control



SW7	Source
POS1	KitProg2 PMIC Control
POS2	PSoC 6 PMIC Control

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Page Title :On-board peripherals

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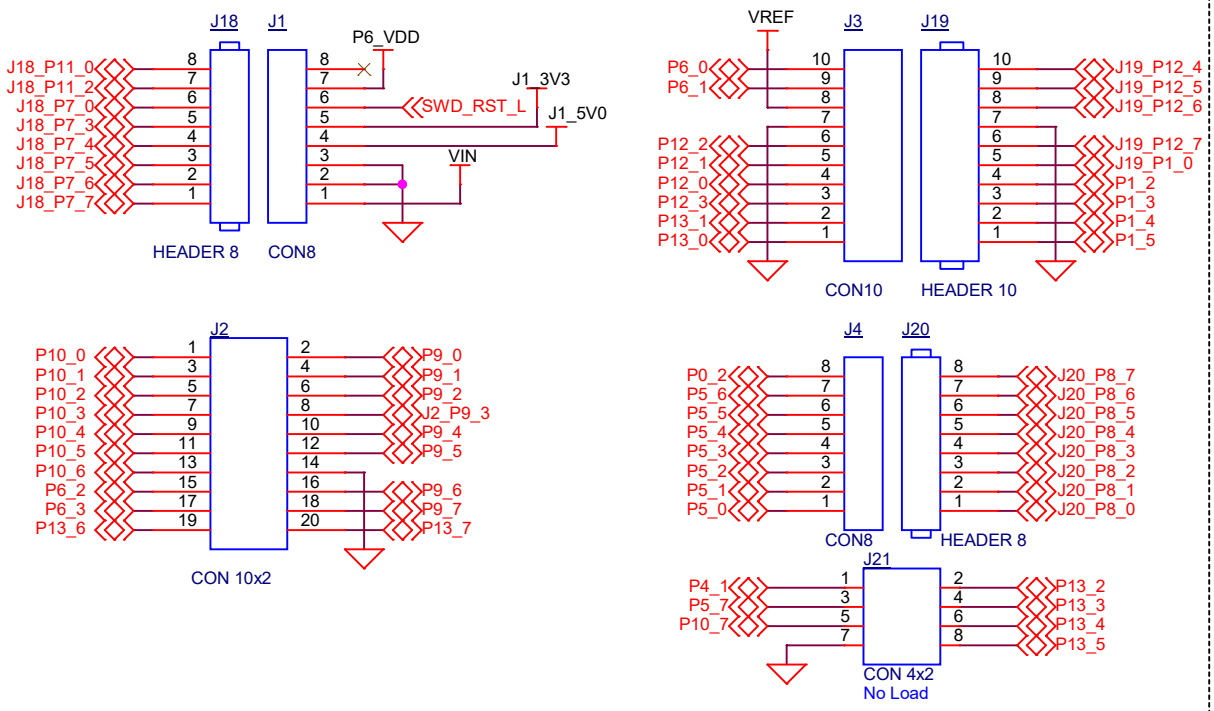
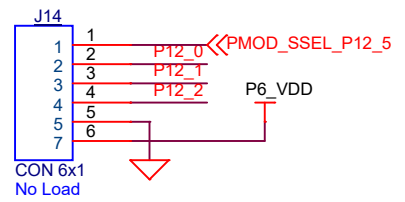
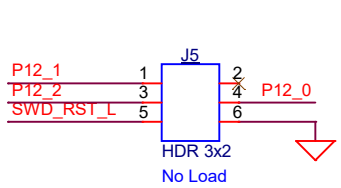
Arduino & Extended Headers



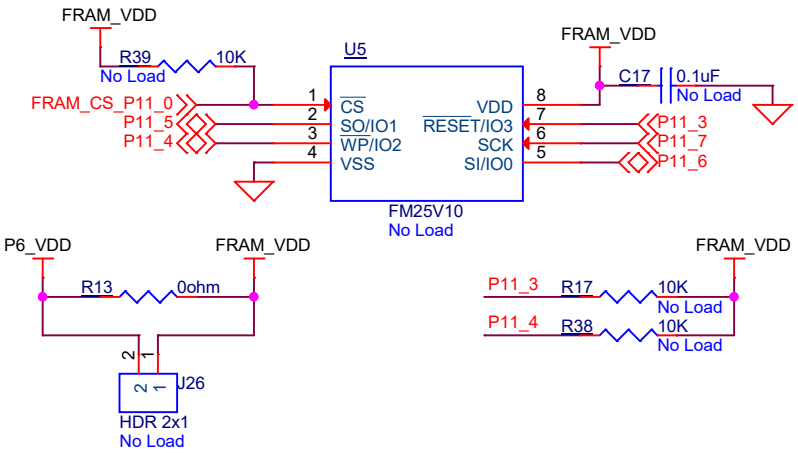
PMOD Header



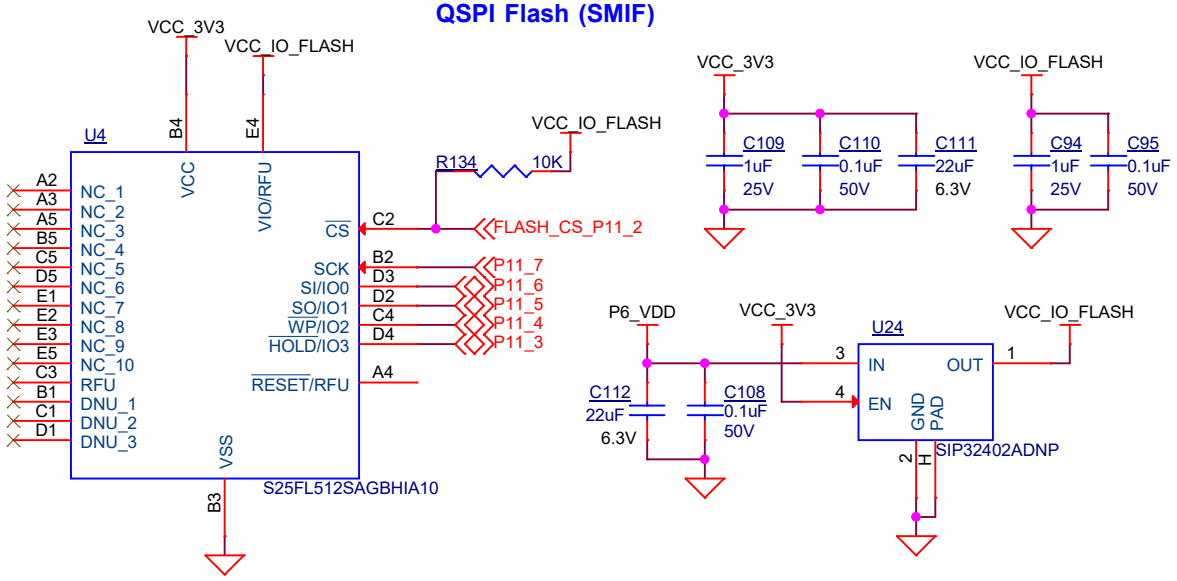
ICSP Header



FRAM



QSPI Flash (SMIF)



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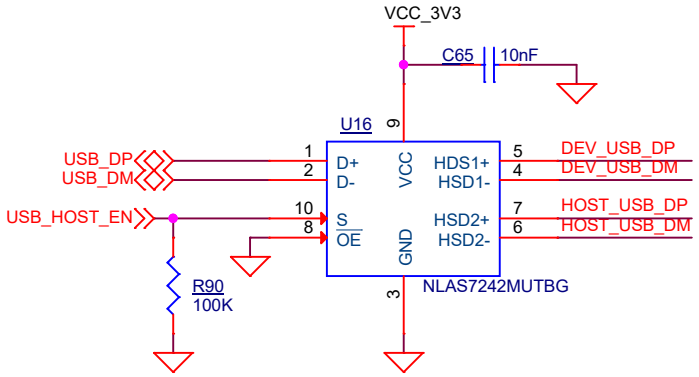
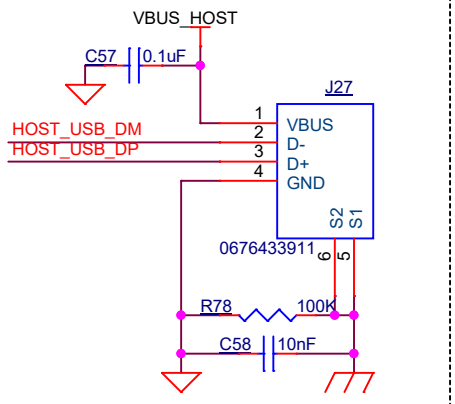
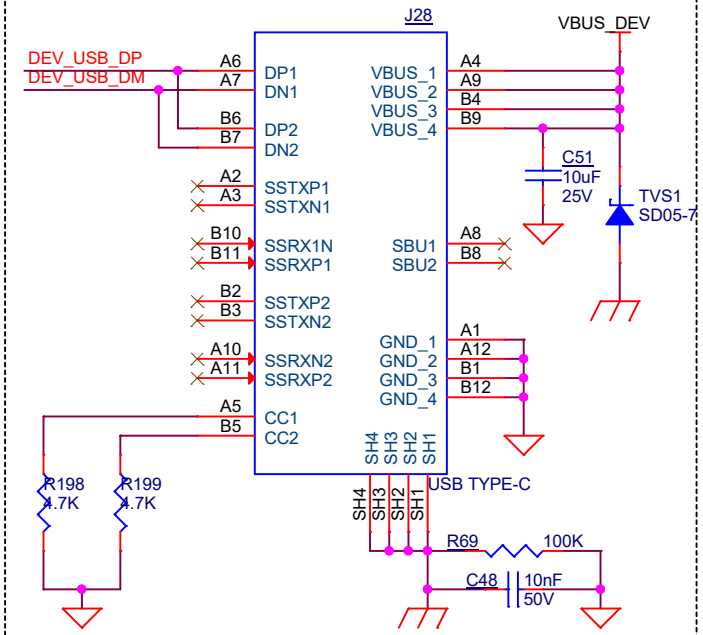
USB Multiplexer



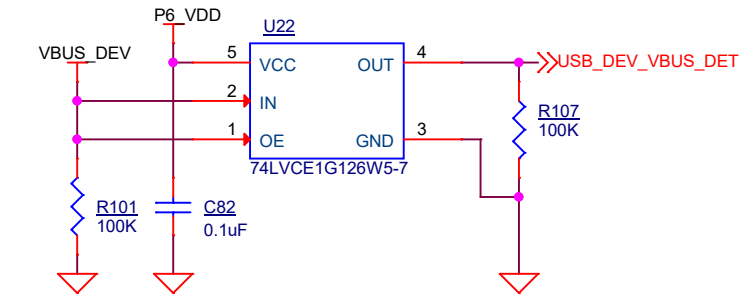
USB Type-A Receptacle (Host)



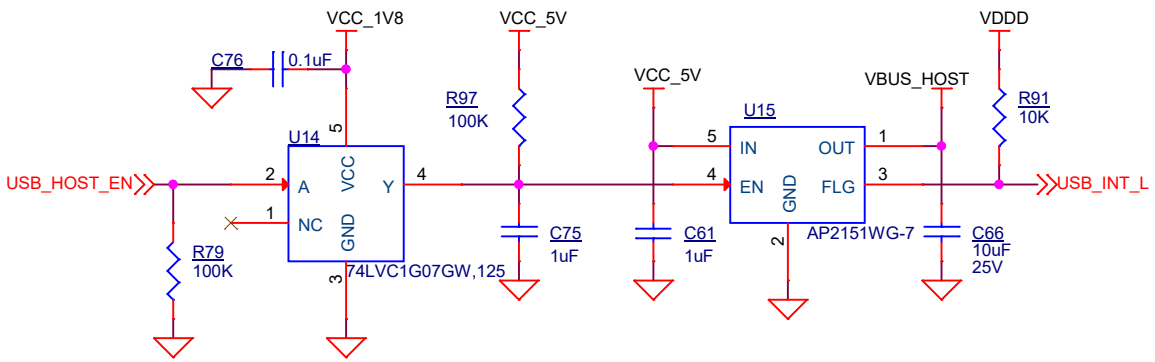
USB Type-C Connector (Device)



USB Device Port VBUS Detect



USB Host VBUS Enable



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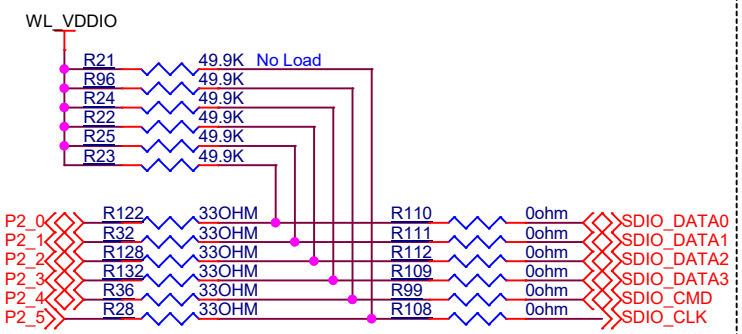
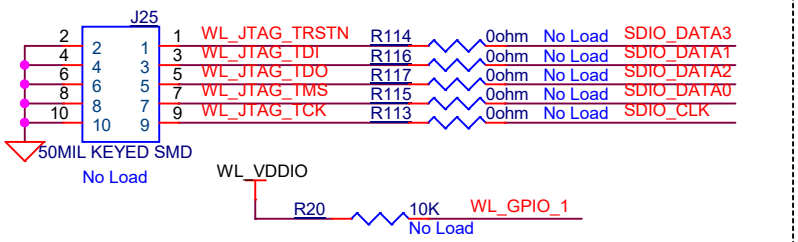
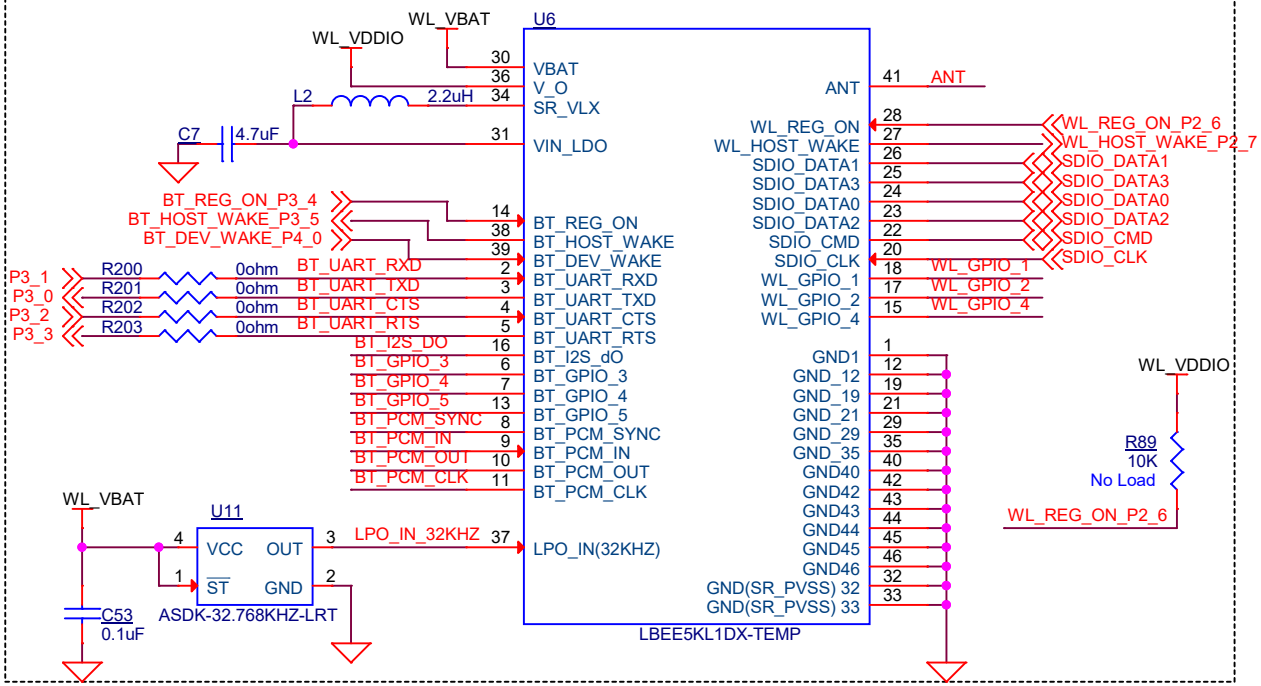
WiFi Interface with PSoC 6



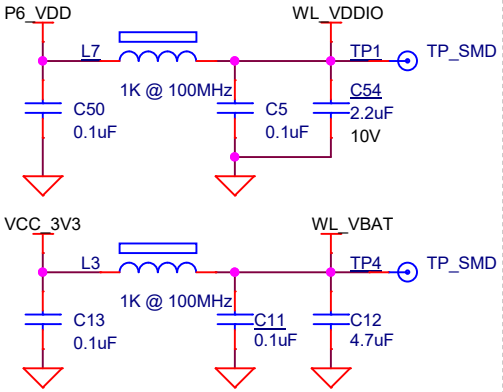
Optional JTAG Interface



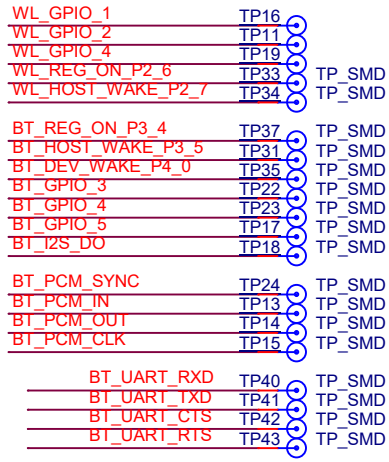
WiFi / BT Module



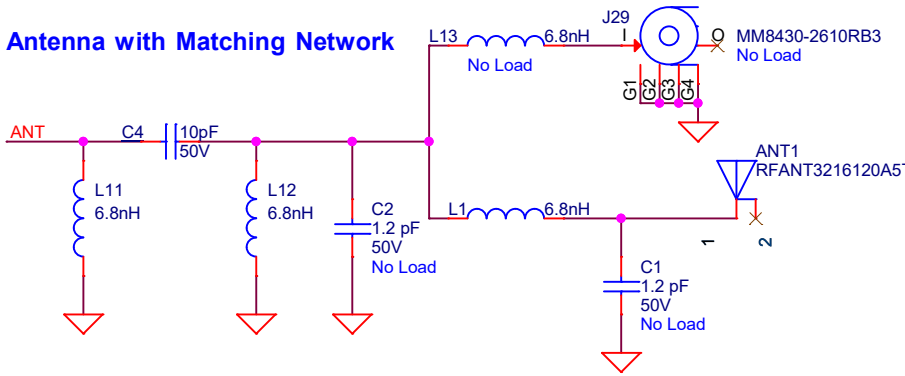
Supply for WiFi Module



Testpoints



Antenna with Matching Network



Layout: Overlap the L13.2 and L1.2 pads

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Accessories

Cylindrical Bumper

SJ61A4 SJ61A4

SJ61A4 SJ61A4

Acrylic Overlay

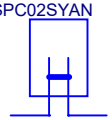
Acrylic Overlay

Color: Clear, Transparent
Finish: Matt

40 x 34 x 1mm

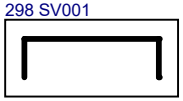
Jumper Shunt

SPC02SYAN

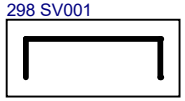


USB Type-C Connector Brackets

298 SV001



298 SV001



PCBA label

LBL PCA Label

LBL QR Code

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Page Title :Accessories

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REVISION HISTORY

REV	DESCRIPTION OF CHANGE	DATE
01	Initial Release	2017/03/13
02	Initial Release	2017/09/01
2.1	Changes done in brief below. See Perforce Rev-21 change Description. - P7_7 off-page connectors added - R197, R198 , R199 resistors added	2017/10/20
2.2	Changes done by Plato: See the description of Rev#25, changelist#1015299. Changes done by TAVA: added 0-ohm resistors (R200, R201, R202, R203) and Test points (TP40, 41, 42, 43) on the 4 UART lines (U6.2, 3, 4, 5)	2017/10/23
2.3	Antenna Network is modified. The RF connector is moved from series path to Y-connection. Additional series inductor is added before the RF connector.	2017/10/24
2.4	UART_CTS PSoC 5LP connection is terminated to J6.2 header pin	2017/11/02
2.5	Net names modified : BT_UART_RXD_P3_1, BT_UART_TXD_P3_0, BT_UART_CTS_P3_2, BT_UART_RTS_P3_3	2017/11/06
2.6	Net names modified : TP40 - 43 connected nets	2017/11/06
2.7	R195 10k pull-down resistor is added on the UART_CTS - PSoC 6 (P5_2) line after the Level Translator.	2017/11/07
2.8	R101 1M re resistor is replaced by a 100k resistor. This resistor is on VBUS_DEV net. This is copied from R90.	2017/11/07
2.9	- Component Properties updated (partially) to match with BoM and Arena - J25 is changed to No Load - J2 : Initially Asym Instruction was No Load. This was manually corrected in BoM and Arena to make Populated. Hence updated in the schematic. - R188 made 0-ohm, R180 made "0-ohm No Load" - R187 made 0-ohm, R179 made "0-ohm No Load" - R186 made 0-ohm, R178 made "0-ohm No Load" - R175 made 0-ohm, from "0-ohm No Load" Need to do: The J28 Type-C module pin CC1 and CC2 needs 5.1k pull-down.	2017/11/09

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