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DOCUMENT

SCHEMATIC DIAGRAM

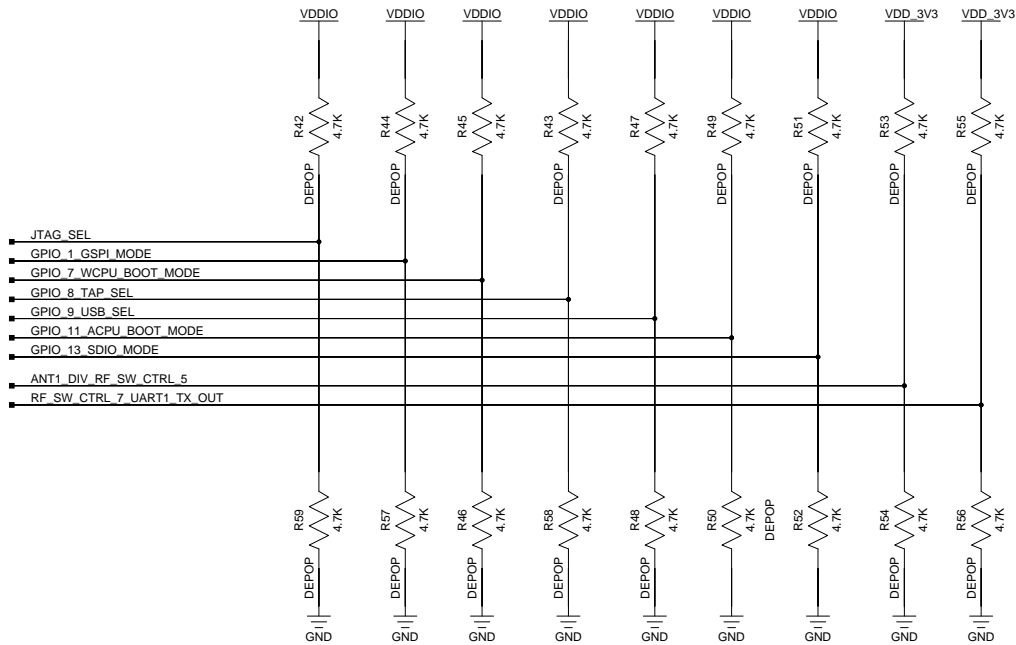
824-129289-0020

PRINTED CIRCUIT BOARD

200-129289-0020

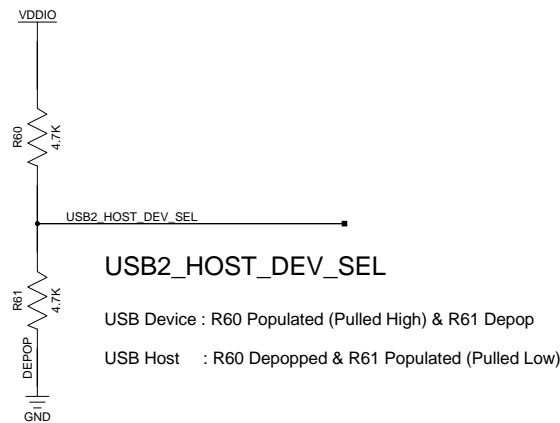
Approvals		<div><div>Cypress</div><div>Company Confidential</div></div>			
Designer	Date				
Reviewer	Date	SIZE	TITLE		
		B	BCM943907WCD2_2		
Reviewer	Date	Designer		Drawing Number	Version
		VIJAY DESAI		824-129289-0020	13
Reviewer	Date	DATE		SHEET	
		14/10/2015:19:38		1 OF 6	

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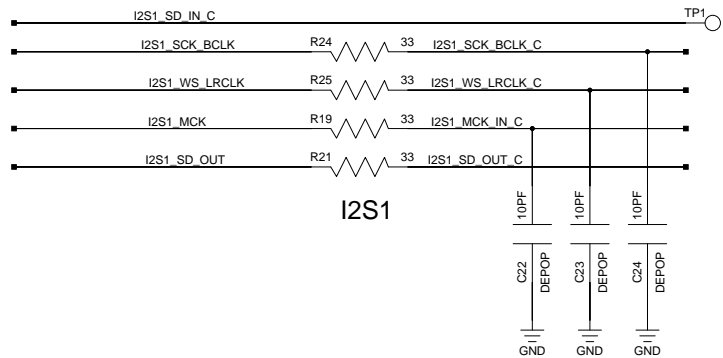
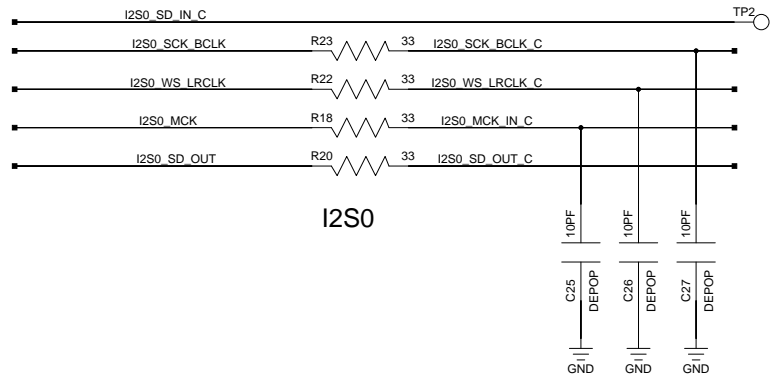
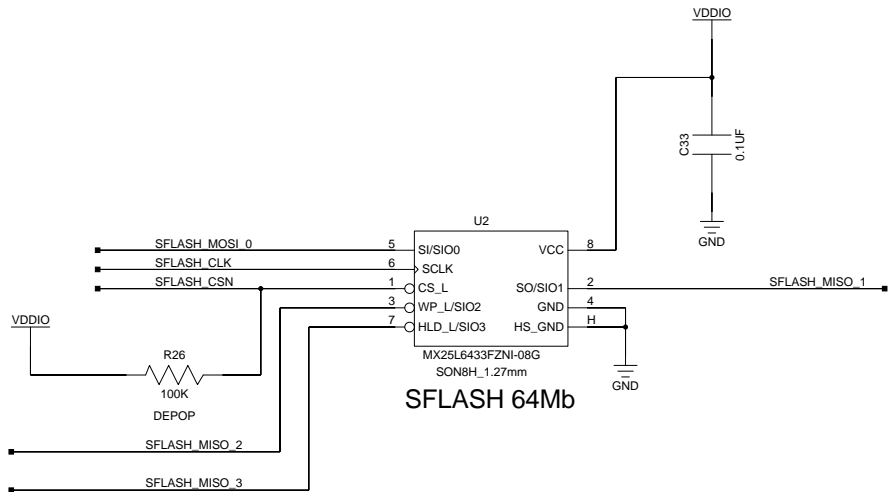
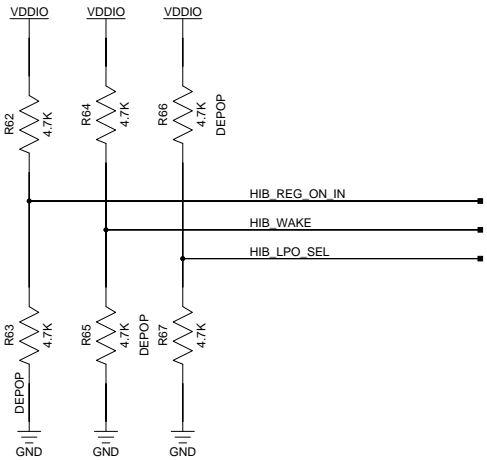
Pin	Strap Function	Strap Pull	
		Chip Default	Board Default
GPIO_1	gSPI Mode	0	0
GPIO_7	WCPU Boot Mode : 0 = TCROM Boot 1 = TCMSRAM Boot	0	1 R45= 4.7K to VDDIO
GPIO_9	USB/HSIC Sel : 0 = HSIC PHY 1 = USB PHY	0	1 R47= 4.7K to 3.3V
GPIO_11	ACPU Boot Mode : 0 = SOCROM Boot 1 = SOCSRAM Boot	0	0
GPIO_13	SDIO Mode : 0 = SDIO Device 1 = SDIO Host	0	0 R52= 4.7K to GND
GPIO_15	Note : GPIO_15 not a strap Option for B0 IC	0	0
RF_SW_CTRL_5	Host DAP Clock Sel	0	0
RF_SW_CTRL_7	Host RSRC Init	0	0
RF_SW_CTRL_9	LPO Sel : 0 = LPO from HIB	0	0

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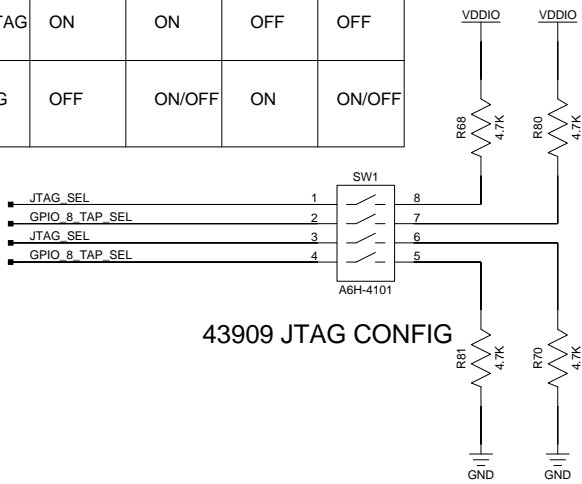
USB2_HOST_DEV_SEL

USB Device : R60 Populated (Pulled High) & R61 Depop
USB Host : R60 Depopped & R61 Populated (Pulled Low)

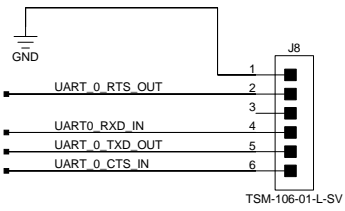


APPS/WLAN JTAG Enable SW1 Switch Control

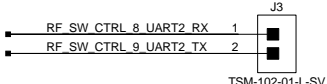
Mode	SW1 Pin1	SW1 Pin2	SW1 Pin3	SW1 Pin4
WLAN JTAG	ON	OFF	OFF	ON
APPS JTAG	ON	ON	OFF	OFF
NO JTAG	OFF	ON/OFF	ON	ON/OFF



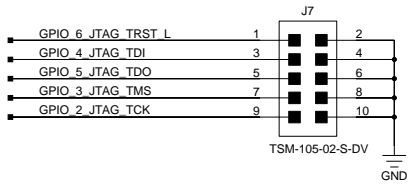
43909 JTAG CONFIG



FAST UART0 HEADER



SLOW UART2 HEADER



43909 JTAG HEADER

Straps + SFLASH + MISC

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SIZE B	TITLE BCM943907WCD2_1		
DATE	14/10/2015:19:39	SHEET	3 OF 6

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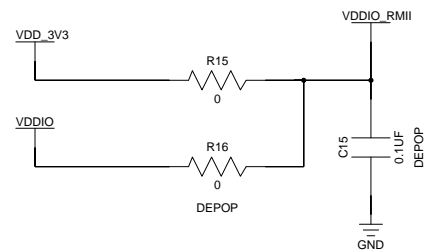
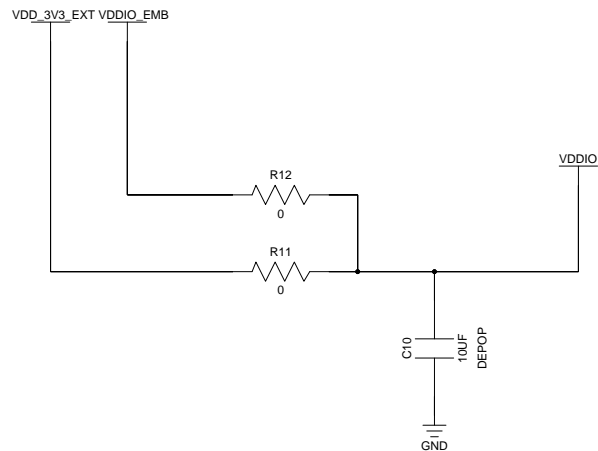
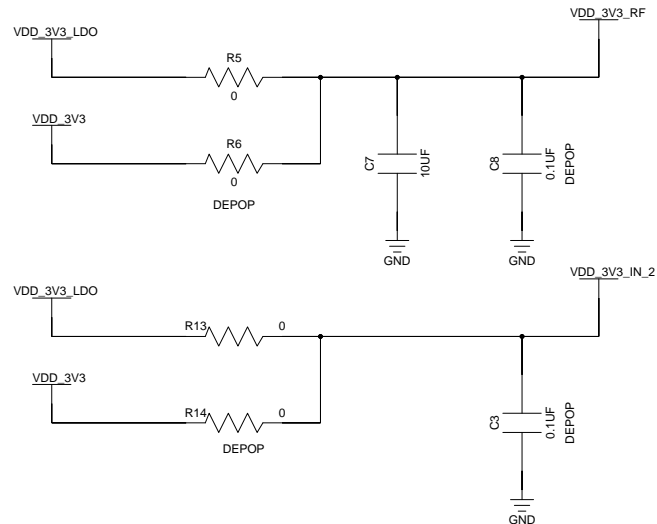
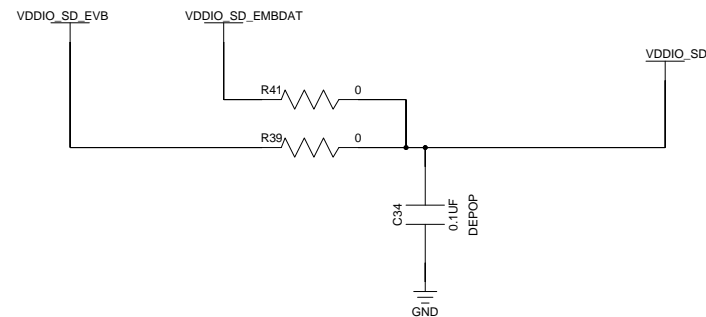
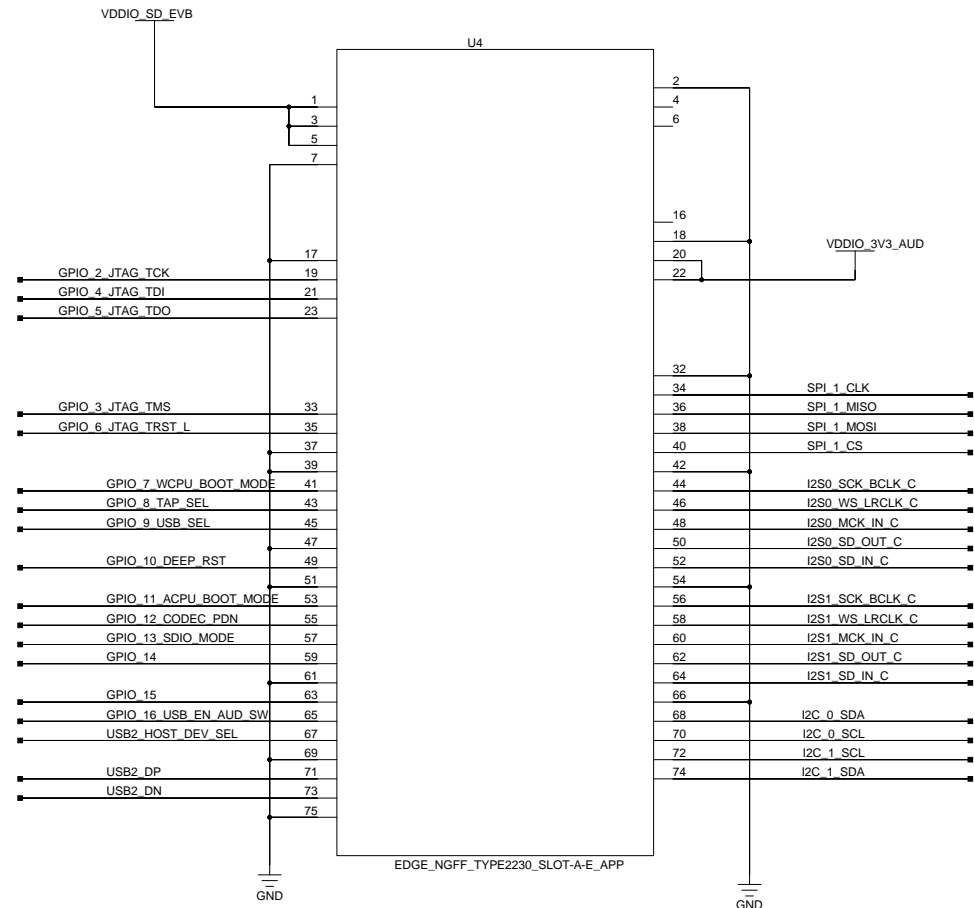
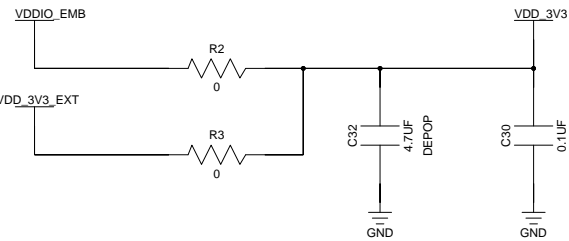
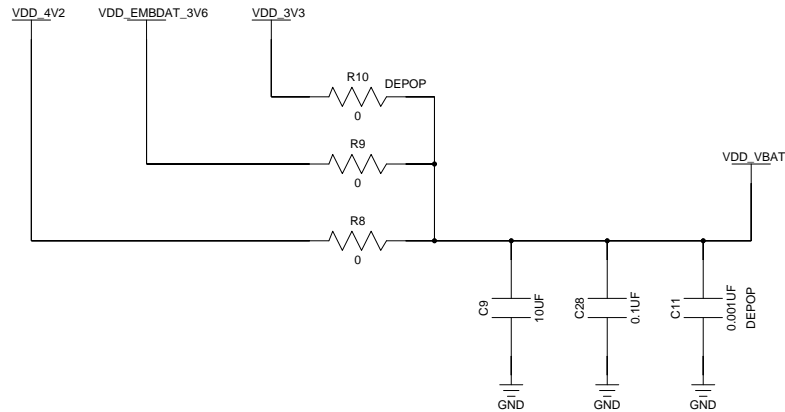
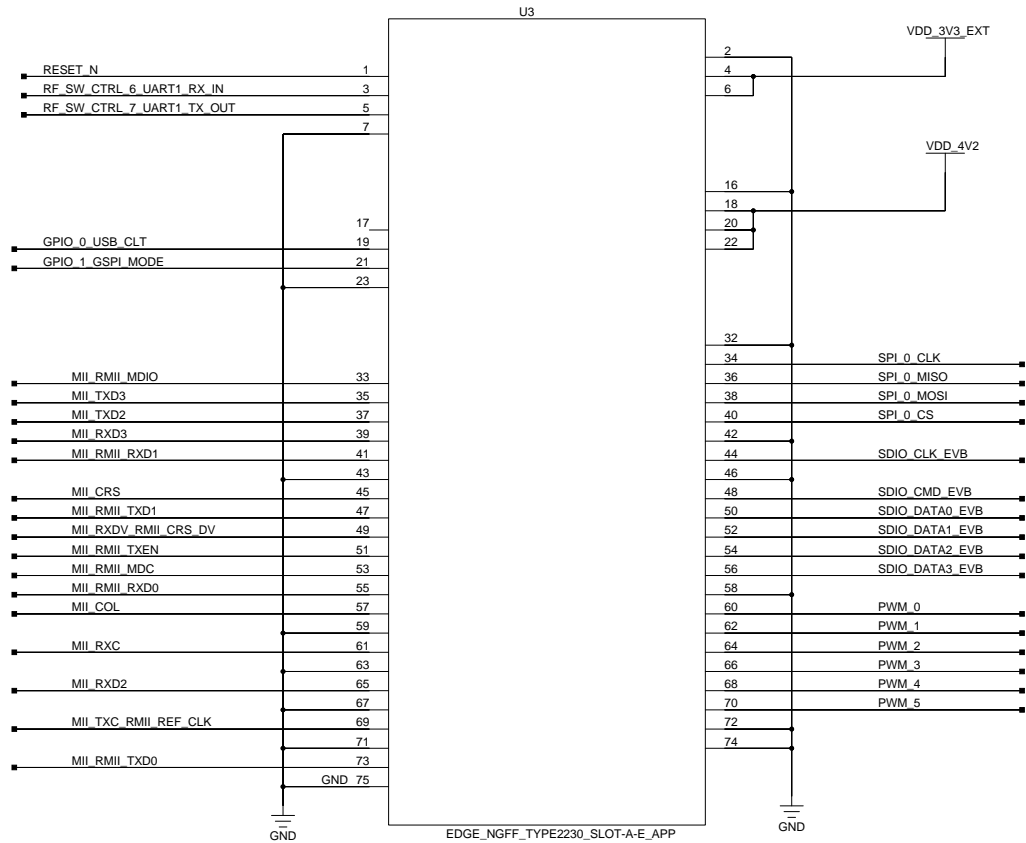
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M.2 Connectors

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SIZE	TITLE
B	BCM943907WCD2_1
DATE	06/04/2015:14:40
SHEET	4 OF 6

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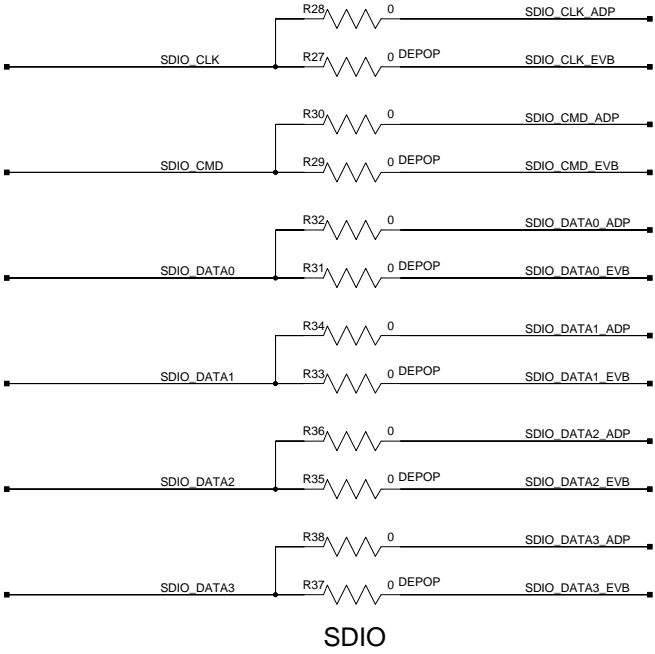
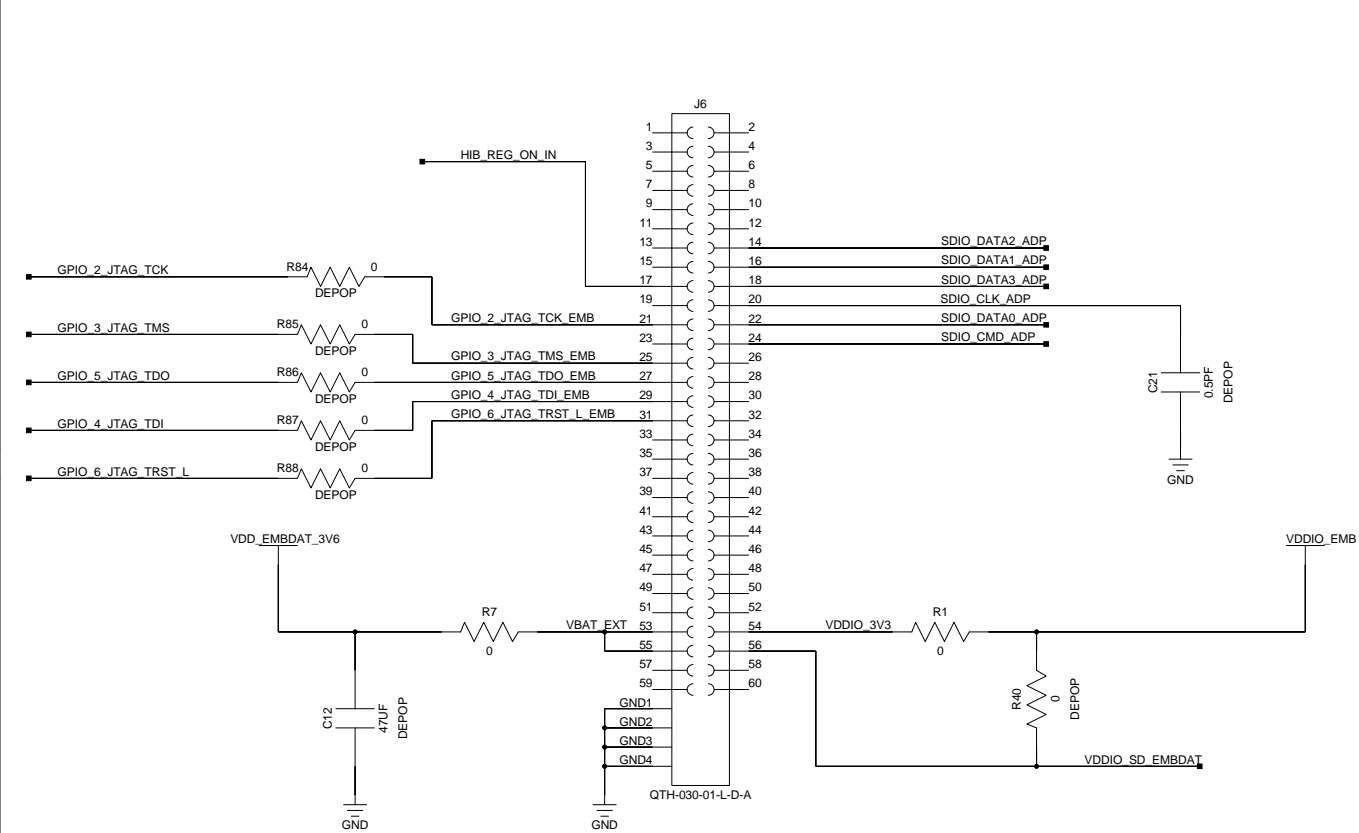
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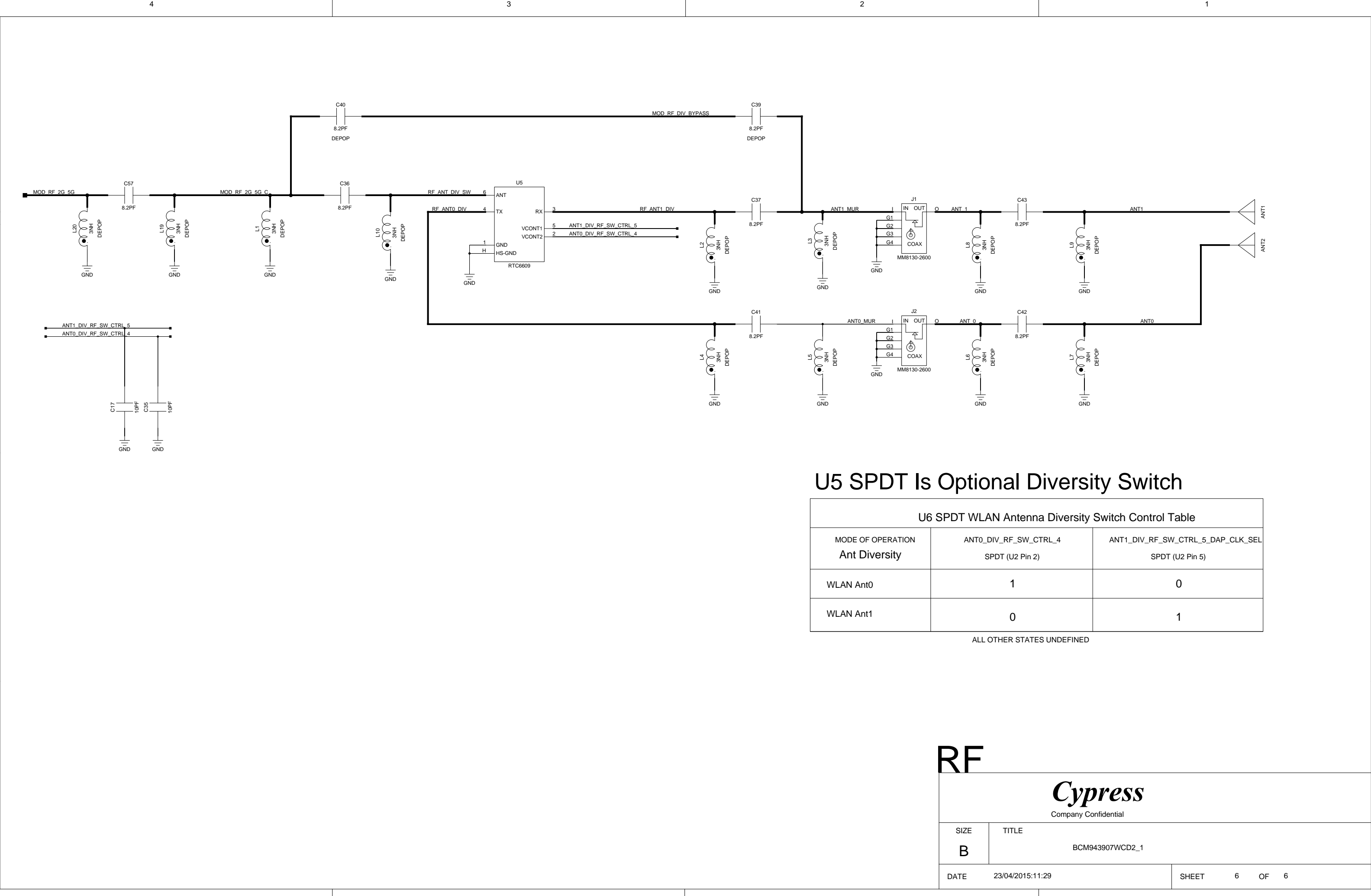
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60 Pin Connector

<div>Cypress</div> <div>Company Confidential</div>			
SIZE	TITLE		
B	BCM943907WCD2_1		
DATE	26/03/2015:13:14	SHEET	5 OF 6



RF

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SIZE	TITLE	DATE	23/04/2015:11:29	SHEET	6	OF	6
B	BCM943907WCD2_1						