FACULTAD
DE INGENIERIA
Universidad de Buenos Aires

Protocolos de comunicación en sistemas embebidos

Quad-SPI (QSPI)

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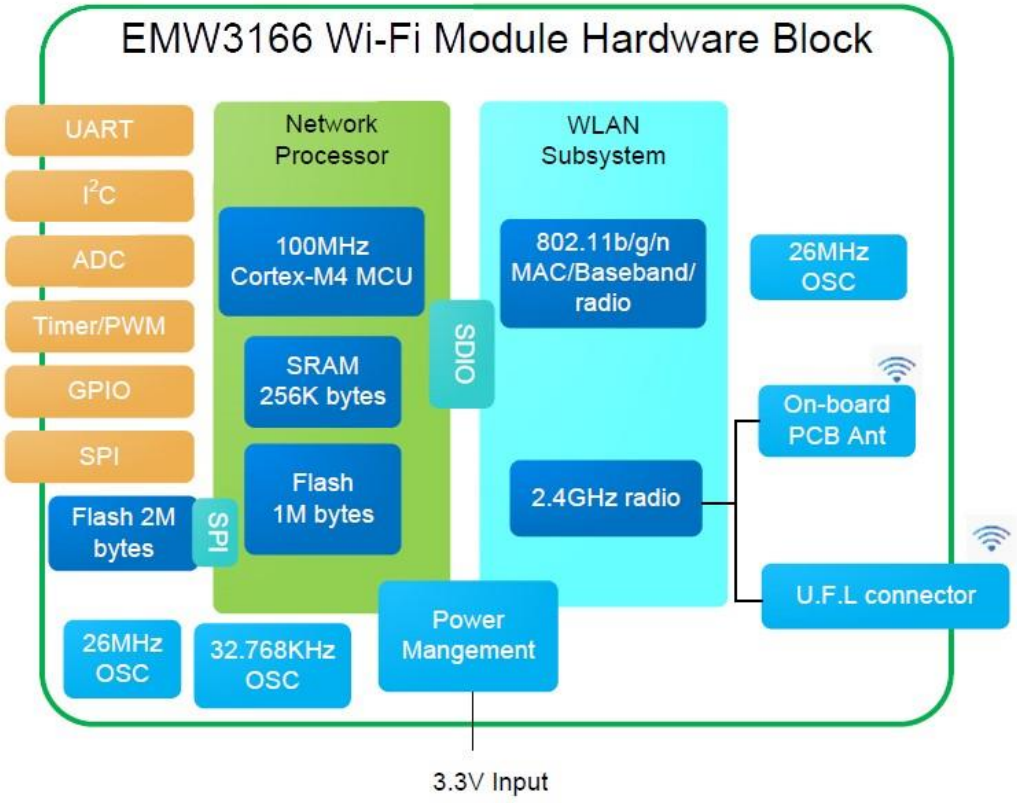
Introducción

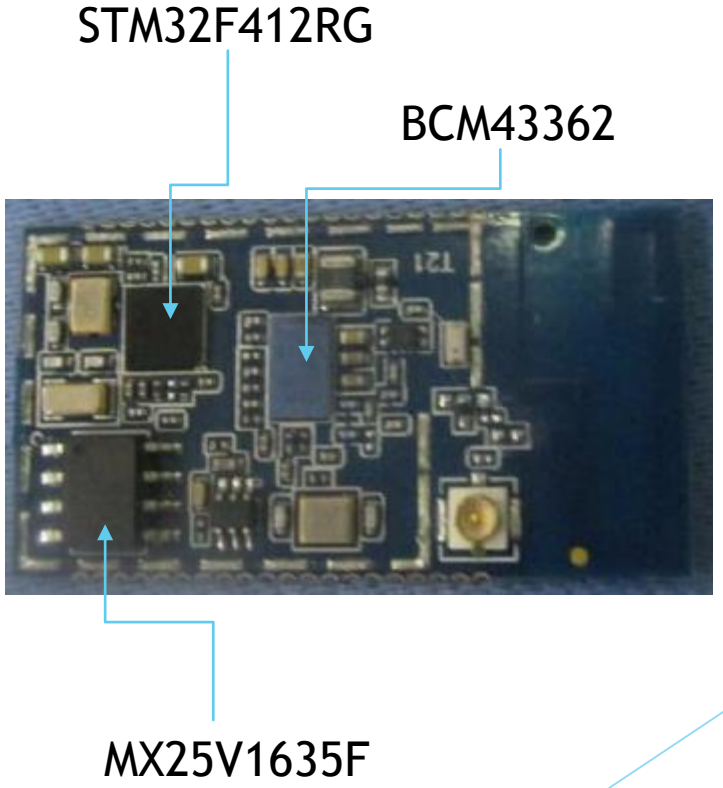
¿Para qué se utiliza la interfaz QSPI?

- Se utiliza para la conexión de memorias externas al microcontrolador
- Permite una tasa de transferencia de datos superior a las memorias SPI tradicionales manteniendo un bajo footprint en relación a las memorias de acceso paralelo
- Puede ser usada para el almacenamiento de datos y ejecución de código

Hardware

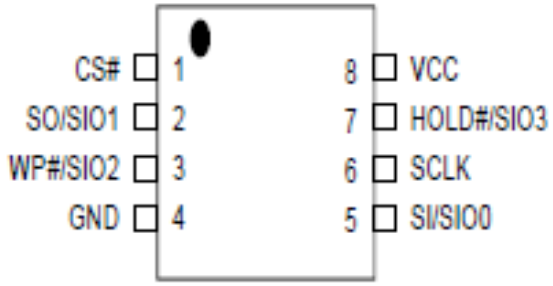
- Microcontrolador: ST STM32F412RG 1MB Flash 256KB RAM
- Chip WiFi: Broadcom BCM43362
- Memoria Flash QSPI 2MB MX25V1635F





Memoria Flash QSPI 2MB MX25V1635F

8-PIN SOP (150mil/200mil)



SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 4xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 4xI/O read mode)
SCLK	Clock Input
WP#/SIO2	Write Protection Active Low or Serial Data Input & Output (for 4xI/O read mode)
HOLD#/SIO3	To pause the device without deselecting the device or Serial Data Input & Output (for 4xI/O read mode)
VCC	Power Supply
GND	Ground

Características generales

- Se escriben en la memoria bloques (páginas) de hasta 256 bytes.
- La unidad mínima de borrado es un bloque de 4096 bytes.
- Durante el proceso de borrado de un sector se escriben “unos”.
- Durante el proceso de escritura de una página se escriben sólo “ceros”.
- La escritura demora un tiempo superior al de la transferencia de datos. Por lo cual antes de volver a escribir hay que verificar la finalización de la escritura anterior.
- El tiempo de borrado es proporcional a la cantidad de bloques borrados. Se debe verificar finalización de borrado.

Características - tiempos

tBP		Byte-Program		30	100	us
		Byte-Program (Applied Vhv at WP# pin)		30	100	us
tPP		Page Program Cycle Time		0.8	4	ms
		Page Program Cycle Time (Applied Vhv at WP# pin)		0.56	3.6	ms
tSE		Sector Erase Cycle Time		38	240	ms
		Sector Erase Cycle Time (Applied Vhv at WP# pin)		34	210	ms
tBE32K		Block Erase (32KB) Cycle Time		0.225	1.5	s
		Block Erase (32KB) Cycle Time (Applied Vhv at WP# pin)		0.2	1	s
tBE		Block Erase (64KB) Cycle Time		0.45	3	s
		Block Erase (64KB) Cycle Time (Applied Vhv at WP# pin)		0.4	2.1	s
tCE		Chip Erase Cycle Time		12	38	s
		Chip Erase Cycle Time (Applied Vhv at WP# pin)		11	34	s

Comandos de lectura

I/O	1	1	2	2	4	4
Command (byte)	READ (normal read)	FAST READ (fast read data)	2READ (2 x I/O read command)	DREAD (1I / 2O read command)	4READ (4 x I/O read)	QREAD (1I/4O read)
1st byte	03 (hex)	0B (hex)	BB (hex)	3B (hex)	EB (hex)	6B (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte		Dummy	Dummy	Dummy	Dummy	Dummy
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	n bytes read out by 2 x I/O until CS# goes high	n bytes read out by Dual Output until CS# goes high	Quad I/O read with 6 dummy cycles	n bytes read out by Quad output until CS# goes high

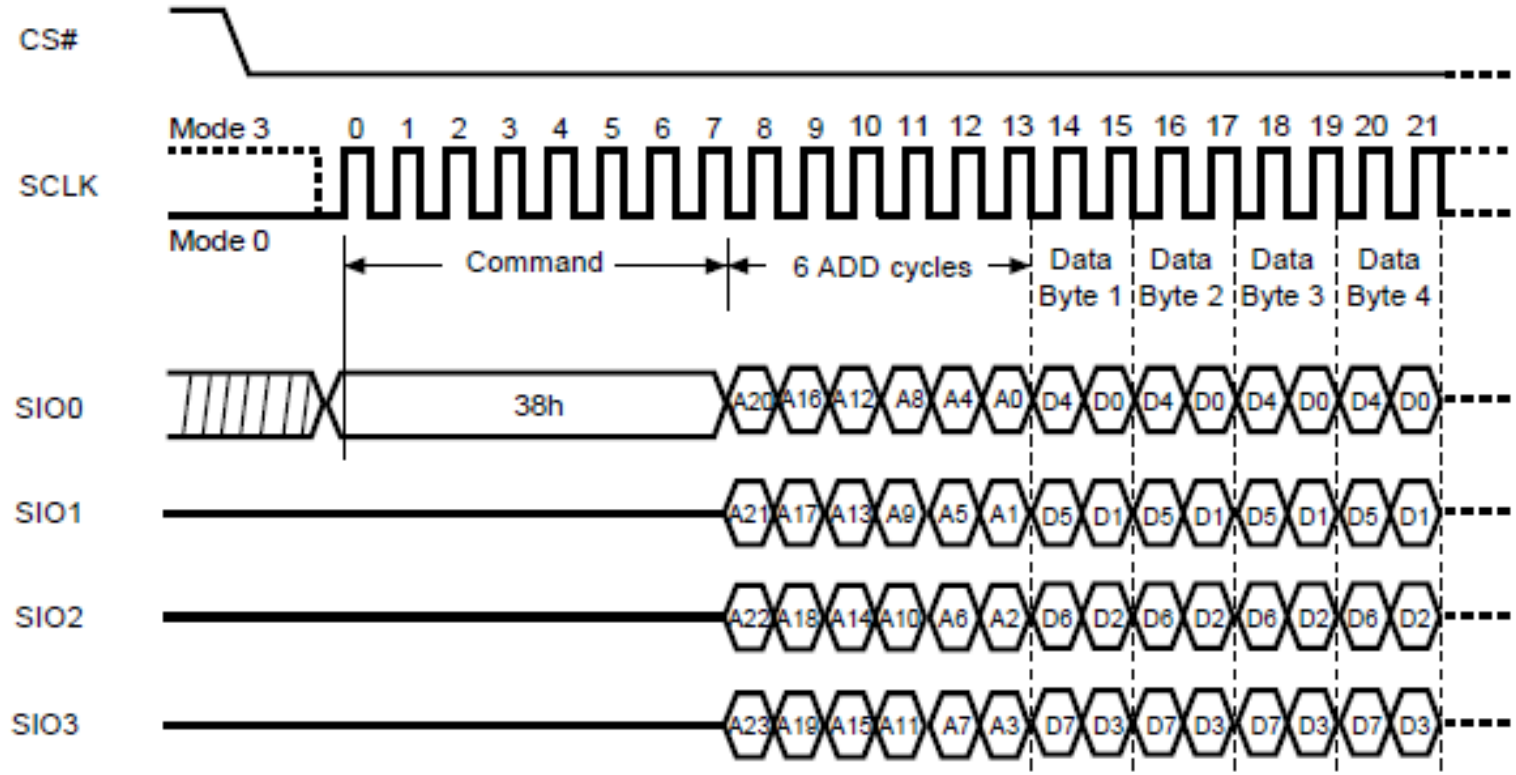
Comandos de escritura

I/O	1	4	1	1	1	1	1
Command (byte)	PP (page program)	4PP (quad page program)	SE (sector erase)	BE 32K (block erase 32KB)	BE (block erase 64KB)	CE (chip erase)	RDSFDP (Read SFDP)
1st byte	02 (hex)	38 (hex)	20 (hex)	52 (hex)	D8 (hex)	60 or C7 (hex)	5A (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1		ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2		ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3		ADD3
5th byte							Dummy
Action	to program the selected page	quad input to program the selected page	to erase the selected sector	to erase the selected 32KB block	to erase the selected block	to erase whole chip	Read SFDP mode

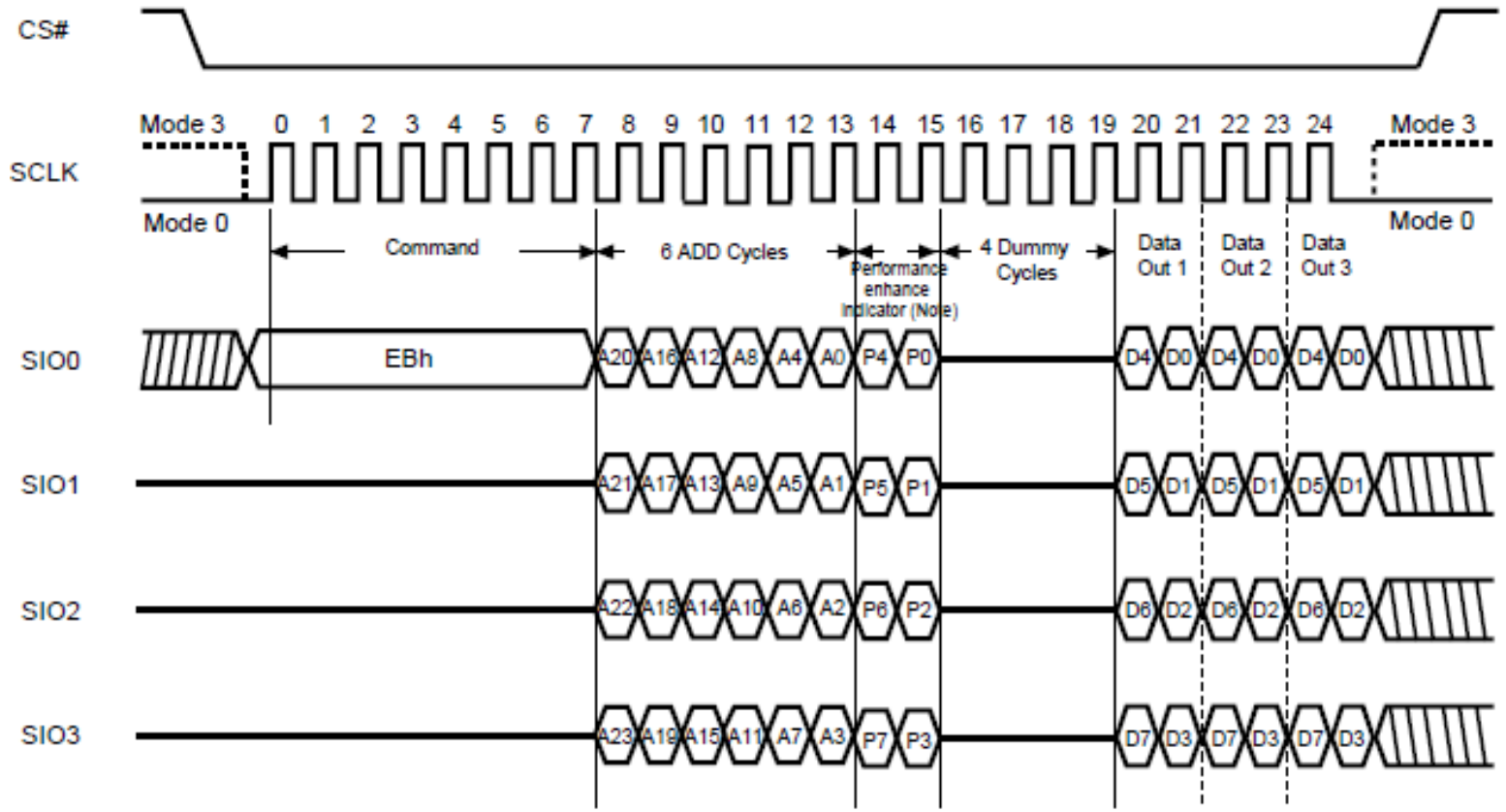
Comandos de lectura/escritura de registros

Command (byte)	WREN (write enable)	WRDI (write disable)	RDSR (read status register)	RDCR (read configuration register)	WRSR (write status register)	PGM/ERS Suspend (Suspends Program/Erase)
1st byte	06 (hex)	04 (hex)	05 (hex)	15 (hex)	01 (hex)	75 or B0 (hex)
2nd byte					Values	
3rd byte					Values	
4th byte						
5th byte						
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	to read out the values of the status register	to read out the values of the configuration register	to write new values of the configuration/ status register	program/erase operation is interrupted by suspend command

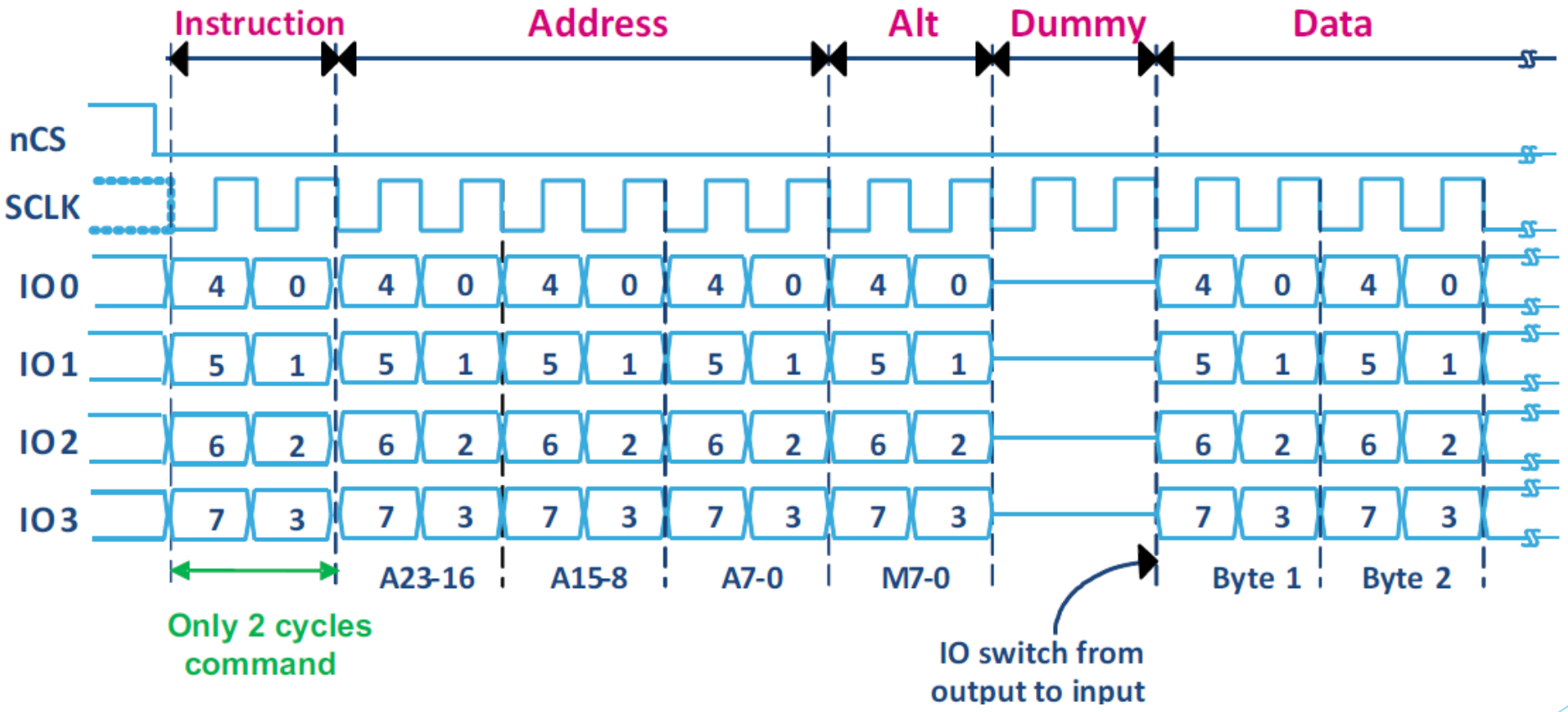
Operación de escritura



Operación de lectura



Periférico QSPI de ST



Bugs en STM32F412xE/xG (en.DM00183231.pdf)

In some specific cases, DMA2 data corruption occurs when managing AHB and APB2 peripherals in a concurrent way

Description

When the DMA2 is managing concurrent requests of AHB and APB2 peripherals, the transfer on the AHB could be performed several times.

Impacted peripheral are:

- **Quad-SPI**: indirect mode read and write transfers
- **FSMC**: read and write operation with external device having FIFO
- **GPIO**: DMA2 transfers to GPIO registers (in memory-to-peripheral transfer mode).The transfers from GPIOs register are not impacted.

The data corruption is due to multiple DMA2 accesses over AHB peripheral port impacting peripherals embedding a FIFO.

For transfer to the internal SRAM through the DMA2 AHB peripheral port the accesses could be performed several times but without data corruptions in cases of concurrent requests.

Workaround

- The DMA2 AHB memory port must be used when reading/writing from/to Quad-SPI and FSMC instead of DMA2 AHB default peripheral port.
- The DMA2 AHB memory port must be used when writing to GPIOs instead of DMA2 AHB default peripheral port.

Bugs en STM32F412xE/xG (en.DM00183231.pdf)

QuadSPI limitations

First nibble of data is not written after dummy phase

Description:

- The first nibble of data to be written to an external flash is lost if:
- QUADSPI is used in indirect write mode, and
- at least one dummy cycle is used

Workaround

Do not use dummy cycles for creating latency between address phase and data phase, in indirect write mode. Instead, use alternate bytes to substitute the dummy cycles.

¿Preguntas?