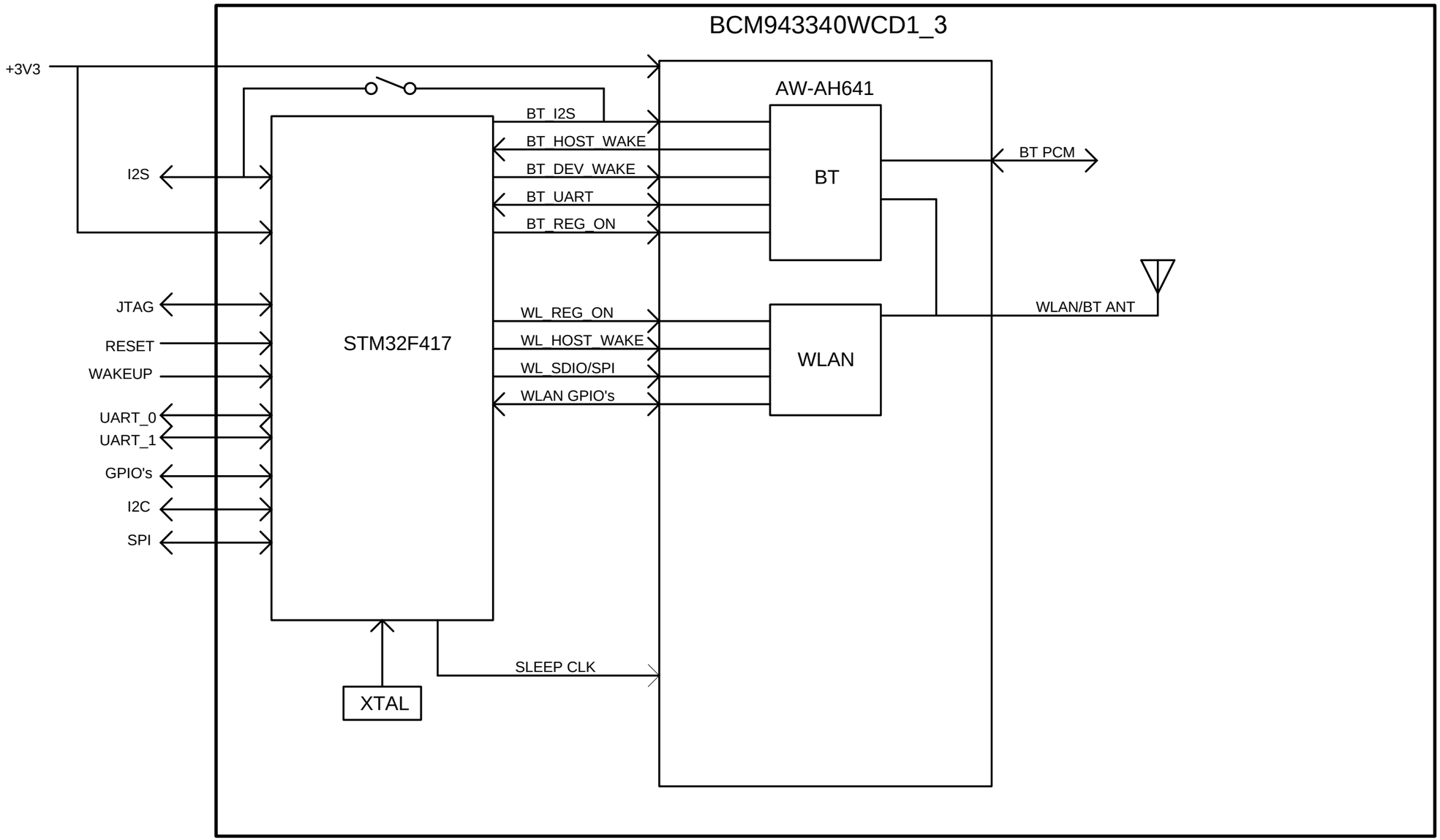

PAGE 1 - MODULE BLOCK DIAGRAM
PAGE 2 - MODULE TOP-LEVEL PINOUT
PAGE 3 - MICROCONTROLLER INTERFACE
PAGE 4 - 43340 SiP INTERFACE

Approvals	
Designer	Date
Reviewer	Date
Reviewer	Date
Reviewer	Date

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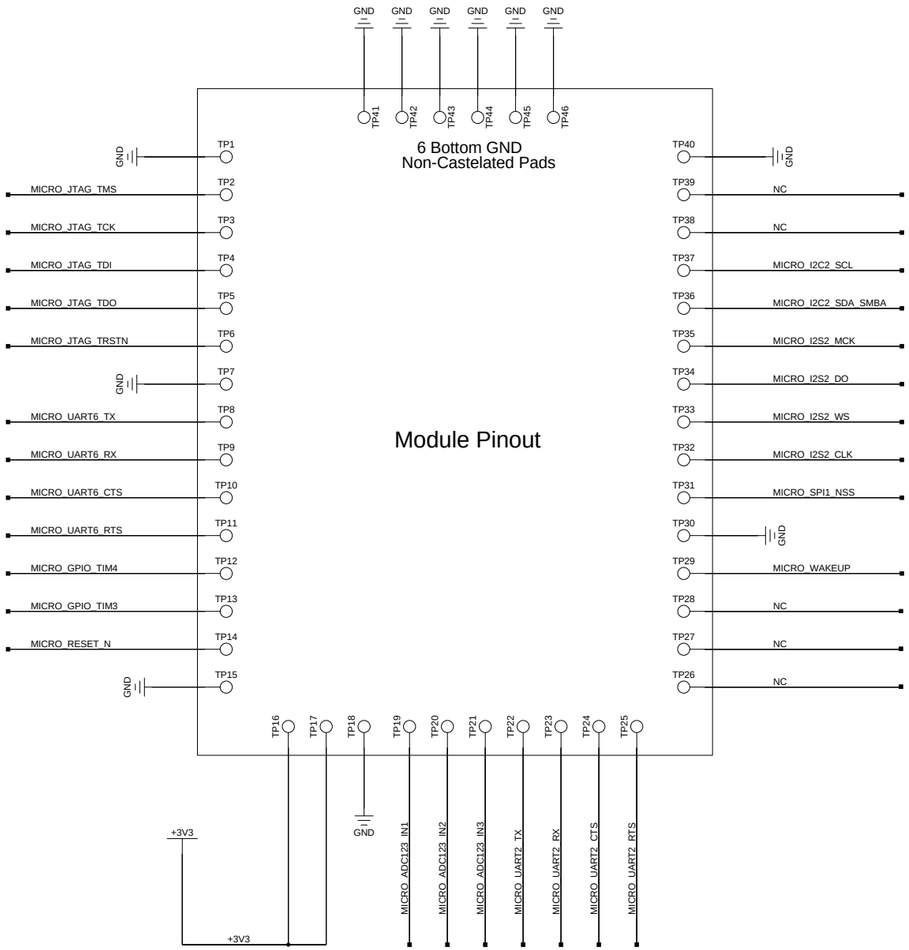
SIZE	TITLE		
B	BCM943340WCD1_3		
Designer	Drawing Number	Version	
ALEXIS ESPIRITU	824-126357-0030	02	
DATE 28/10/2014:14:06	SHEET 1 OF 4		



WLAN strapping options:

GPIO6_SDIO_SPI_SELECT	SDIO_DATA2_SPI_NC	MODE
0	X	SDIO
1	0	gSPI

SDIO/gSPI pin mapping:

	STM32F417 ball	STM32F417 port		AW-AH641 ball	Function
SDIO	A12	PC12	<--->	C2	SDIO_CLK
	D12	PD2	<--->	D2	SDIO_CMD
	G14	PC8	<--->	E2	SDIO_DATA_0
	F14	PC9	<--->	E3	SDIO_DATA_1
	B14	PC10	<--->	F3	SDIO_DATA_2
	B13	PC11	<--->	G3	SDIO_DATA_3
gSPI	P13	PB13	<--->	C2	SPI_CLK
	R15	PB15	<--->	D2	SPI_MOSI
	R14	PB14	<--->	E2	SPI_MISO
	B13	PC11	<--->	G3	SPI_CS
	F14	PC9	<--->	E3	SPI_IRQ

Note:
Only one set of communication lines are required to be connected between the microcontroller and wlan device (either SDIO or SPI).
This reference module connects up both for evaluation purposes only.

DOC?
DOCUMENT
SCHEMATIC DIAGRAM 824-126357-0030

PCB?
PRINTED CIRCUIT BOARD
200-126357-0030

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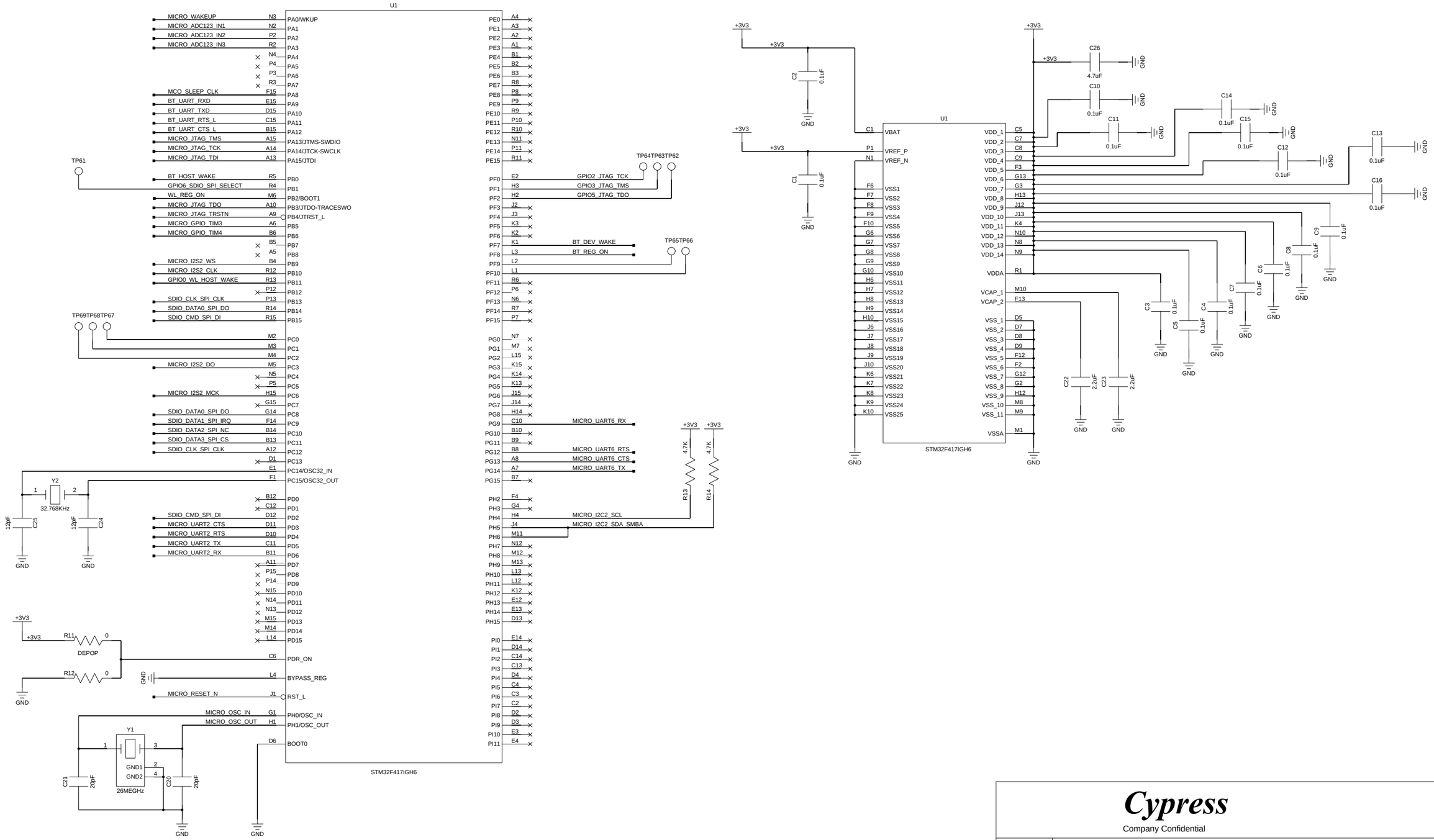
SIZE	TITLE	
B	BCM943340WCD1_3	
DATE 14/10/2014:14:49		SHEET 2 OF 4



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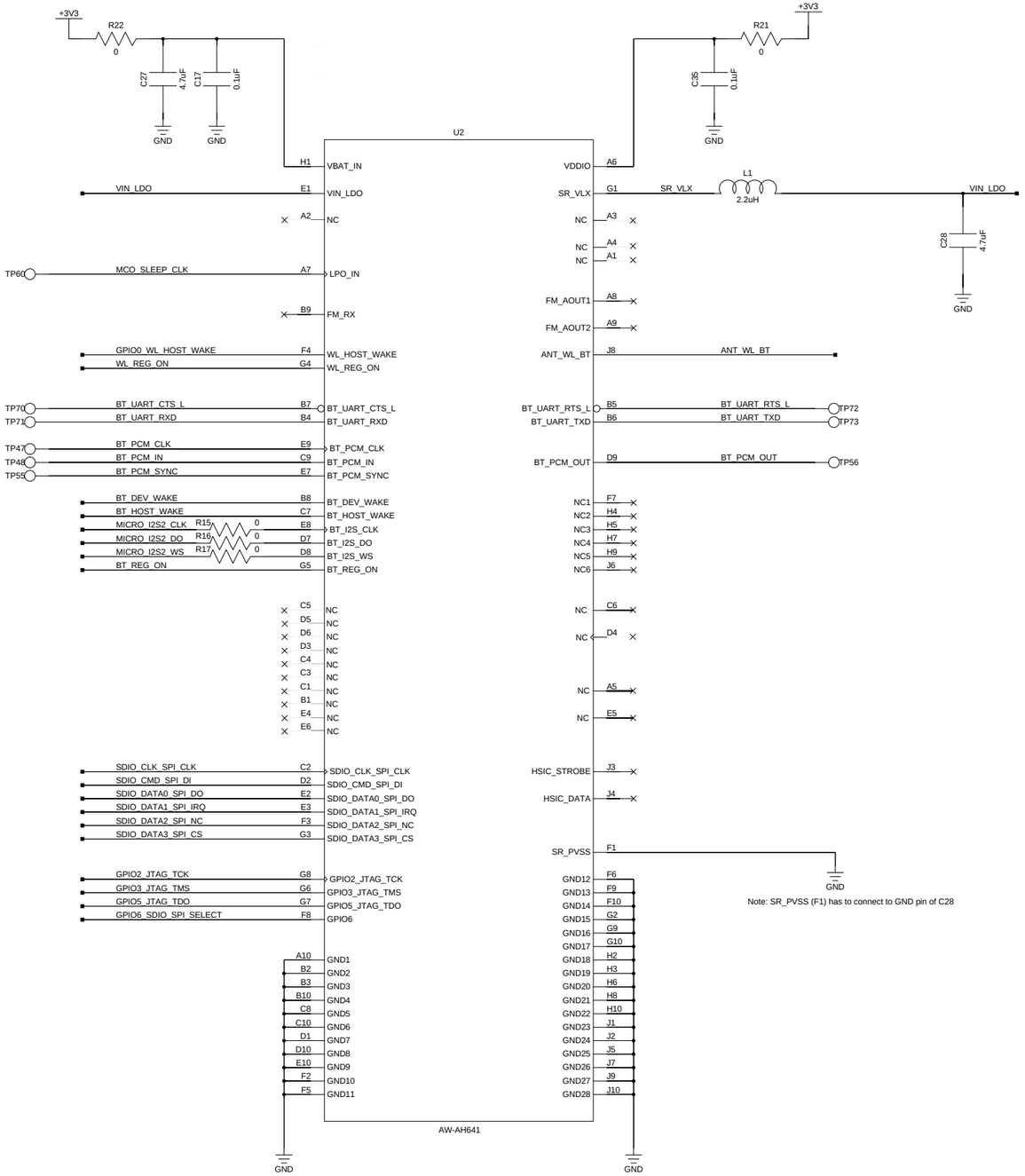
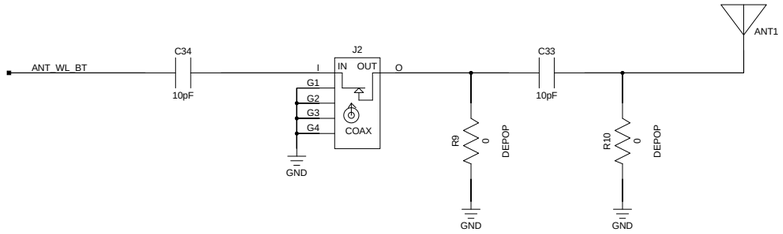
SIZE	TITLE
B	BCM943340WCD1_3
DATE 14/10/2014:14:49	SHEET 3 OF 4





WLAN/BT antenna network

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SIZE B	TITLE BCM943340WCD1_3	
DATE 27/10/2014:11:17		SHEET 4 OF 4