REVISION HISTORY:

BCM943362WCD6 Rev01

1) Initial release.

BCM943362WCD6_3 Rev01

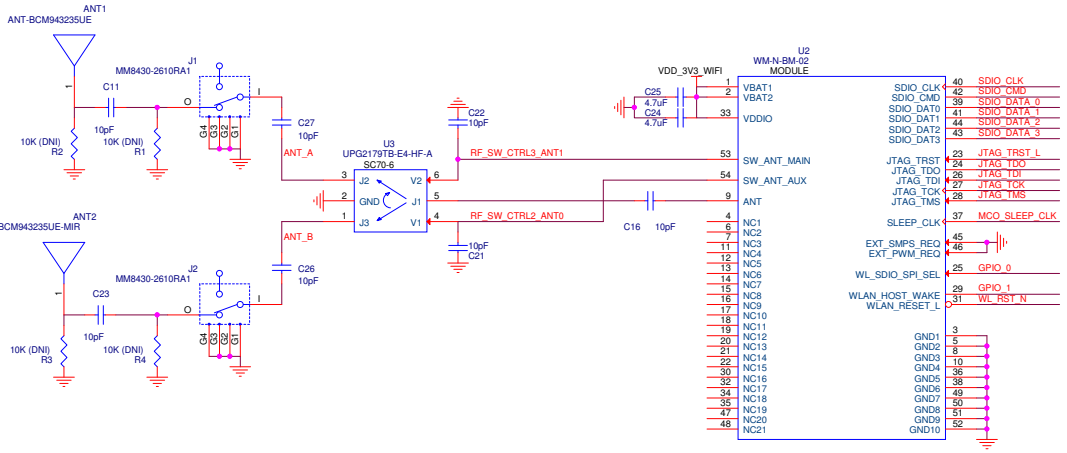
1) Added 10k resistors R94, R95, R96 for identifying board revision.

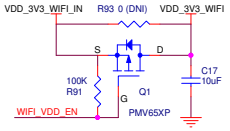
2) Renamed "32K_PWM_OUT" net to "MCO_SLEEP_CLK" and moved from using PA11 to PA8.

(Note: When using WICED Powersave API, it is critical that an accurate 32.768kHz clock is used for the sleep clock input pin of the WLAN chip.

The MCO1 pin (PA8) can be used to route out the highly accurate 32.768kHz LSE clock and is now used as the source for the sleep clock into the WLAN chip.

The LSE clock is more accurate than generating a PWM signal out of PA11.)





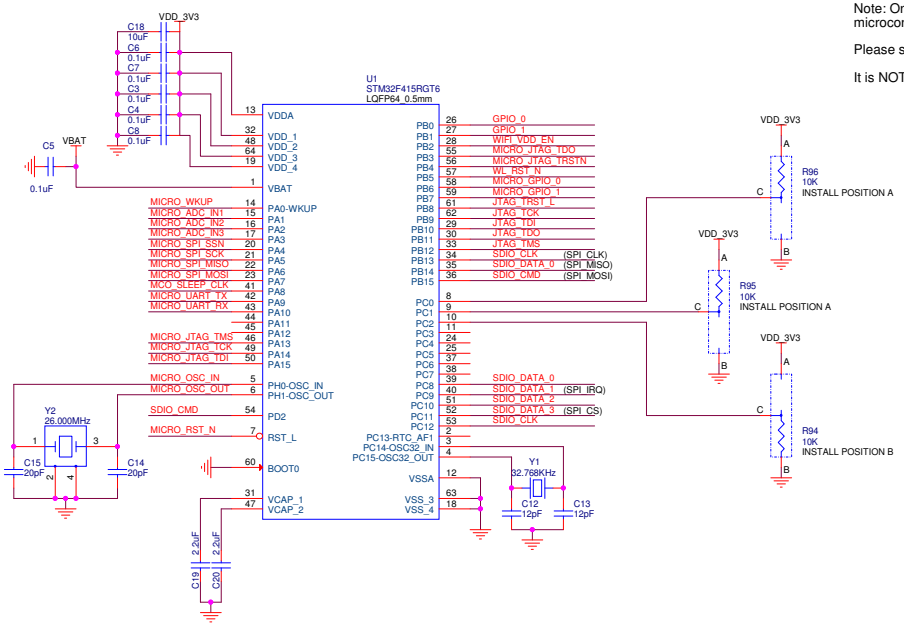
SDIO / SPI Interface Options:

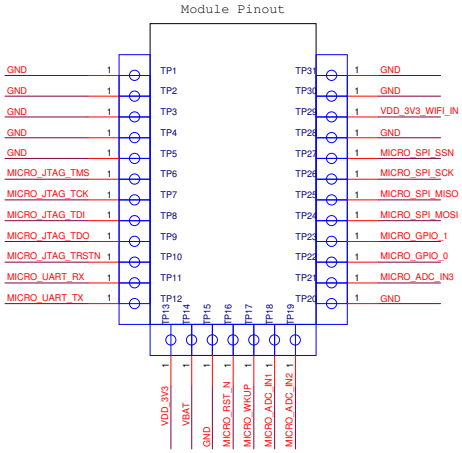
SDIO	STM32F205 Pin Number	STM32F205 Port/Pin		WM-N-BM-02 Pin Number	Function
	53	PC12	<--->	40	SDIO_CLK
	54	PD2	<--->	42	SDIO_CMD
	39	PC8	<--->	39	SDIO_DATA_0
	40	PC9	<--->	41	SDIO_DATA_1
	51	PC10	<--->	42	SDIO_DATA_2
	52	PC11	<--->	43	SDIO_DATA_3
SPI	**STM32F205 Pin Number**	**STM32F205 Port/Pin**		**WM-N-BM-02 Pin Number**	**Function**
	34	PB13	<--->	40	SPI_CLK
	36	PB15	<--->	42	SPI_MOSI
	35	PB14	<--->	39	SPI_MISO
	52	PC11	<--->	43	SPI_CS
	40	PC9	<--->	41	SPI_IRQ

Note: Only one set of communication lines are required to be connected between the microcontroller and wlan device (either SDIO or SPI).

Please select one set based on the table above.

It is NOT necessary to connect both SPI and SDIO.





PC1
PCB NUMBER: 200-125211-0030
PCB NAME: BCM943362WCD6_3

ZHI
SCHEMATIC DIAGRAM

CYPRESS EMBEDDED IN TOMORROW™	Cypress Corporation <OrgAddr1> <OrgAddr2> <OrgAddr3>		
	BCM943362WCD6_3		
	Size: C	DWG NO: 824-125211-0030	Rev: Rev 01
Wednesday, July 10, 2013	Scale:		Sheet: 1 of 1