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DOCUMENT

SCHEMATIC DIAGRAM

824-127858-0030

PRINTED CIRCUIT BOARD

200-127858-0030

Approvals		<div><div>Cypress</div><div>Company Confidential</div></div>		
Designer	Date			
Reviewer	Date	SIZE	TITLE	
		B	BCM943909WCD1_3	
Reviewer	Date	Designer		Drawing Number
		VIJAY DESAI		824-127858-0030
Reviewer	Date			Version
				02
		DATE	04/03/2015:12:06	
		SHEET	1 OF 9	

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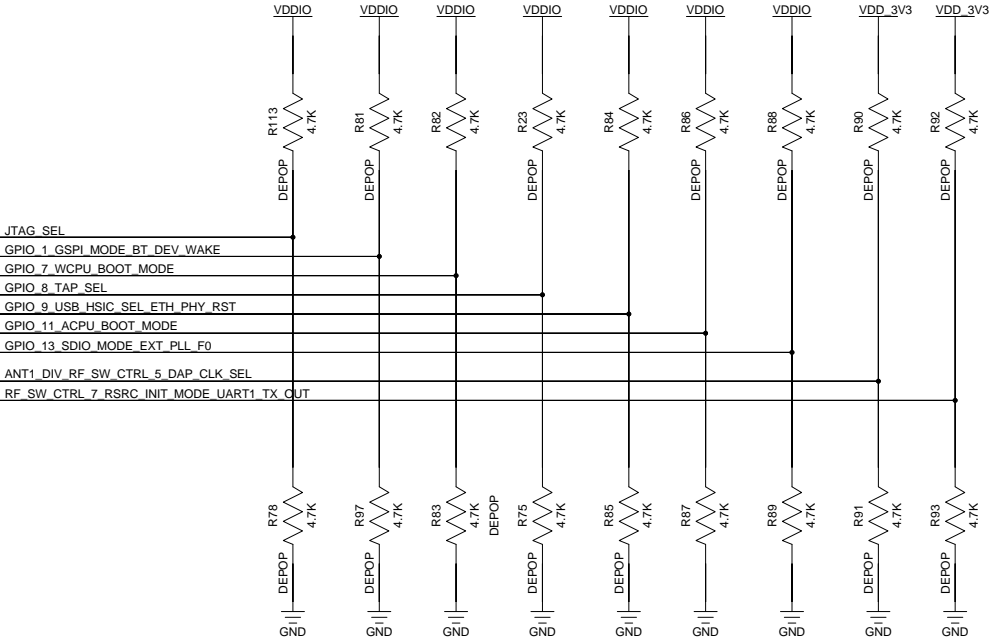
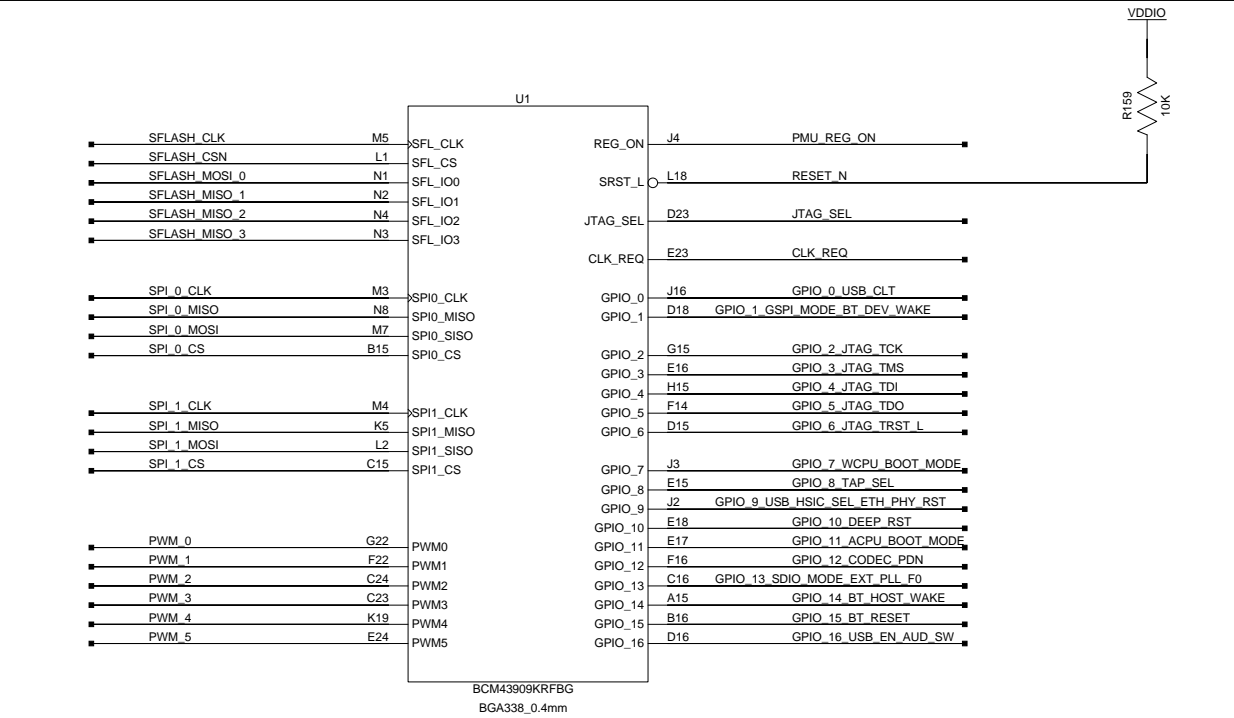
A

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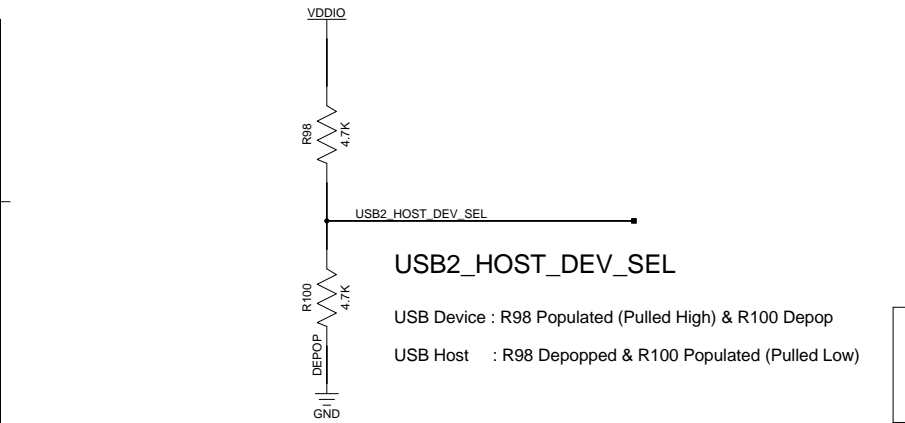
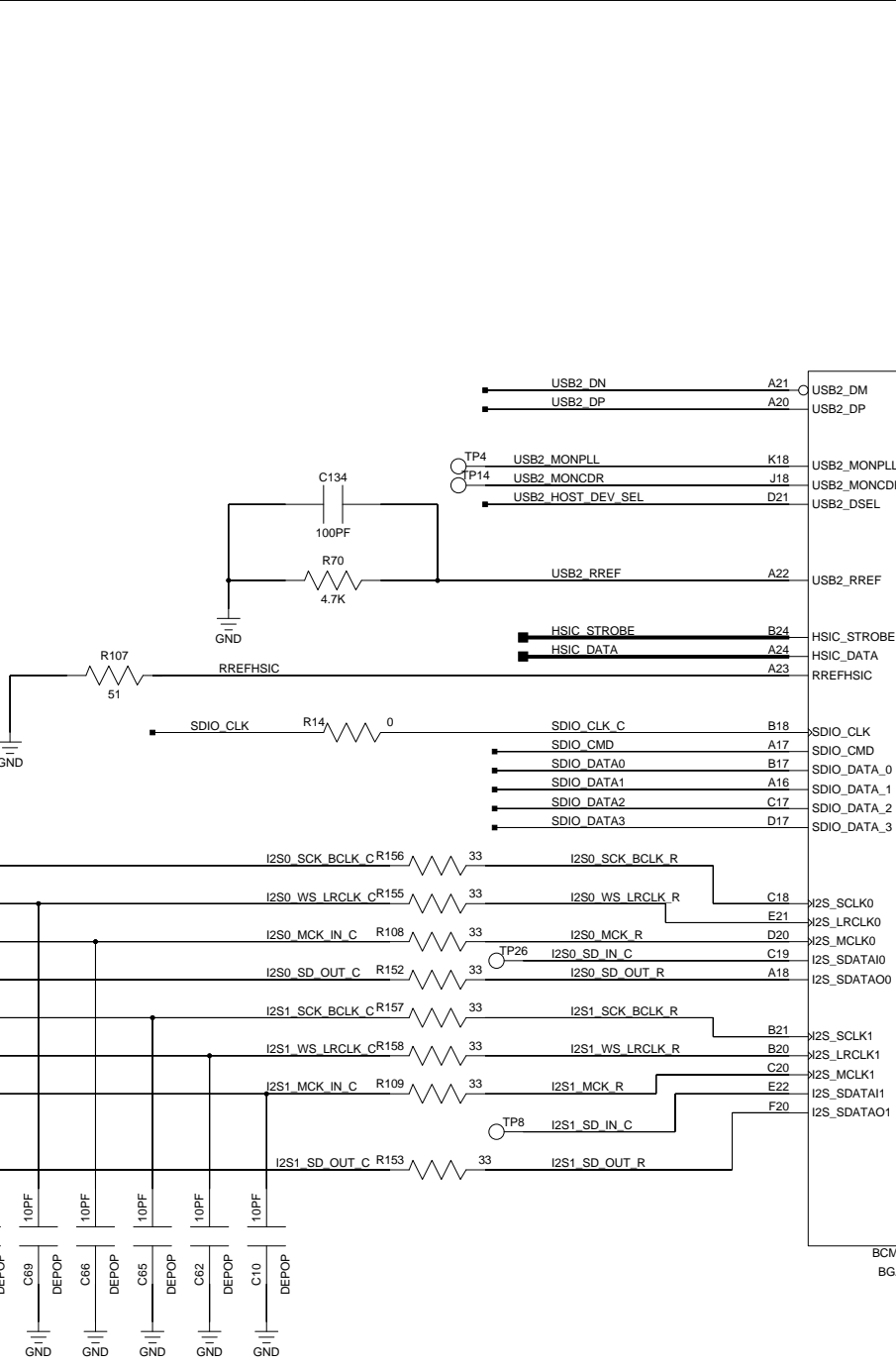
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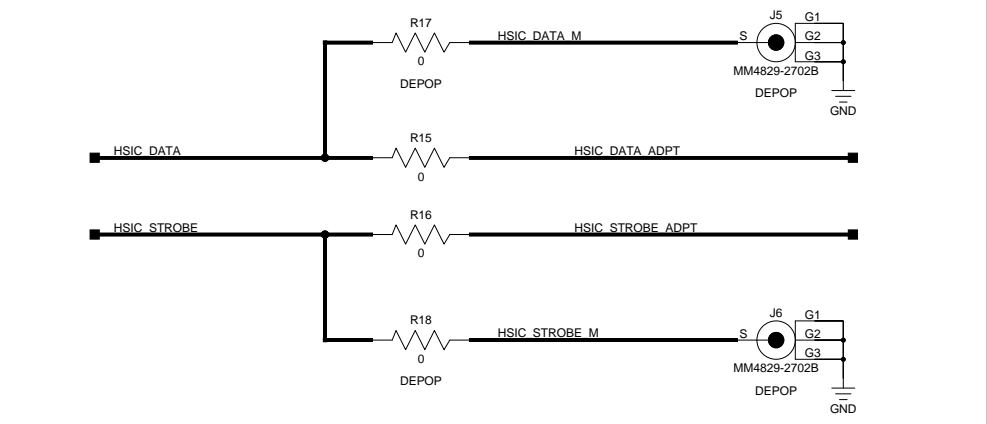
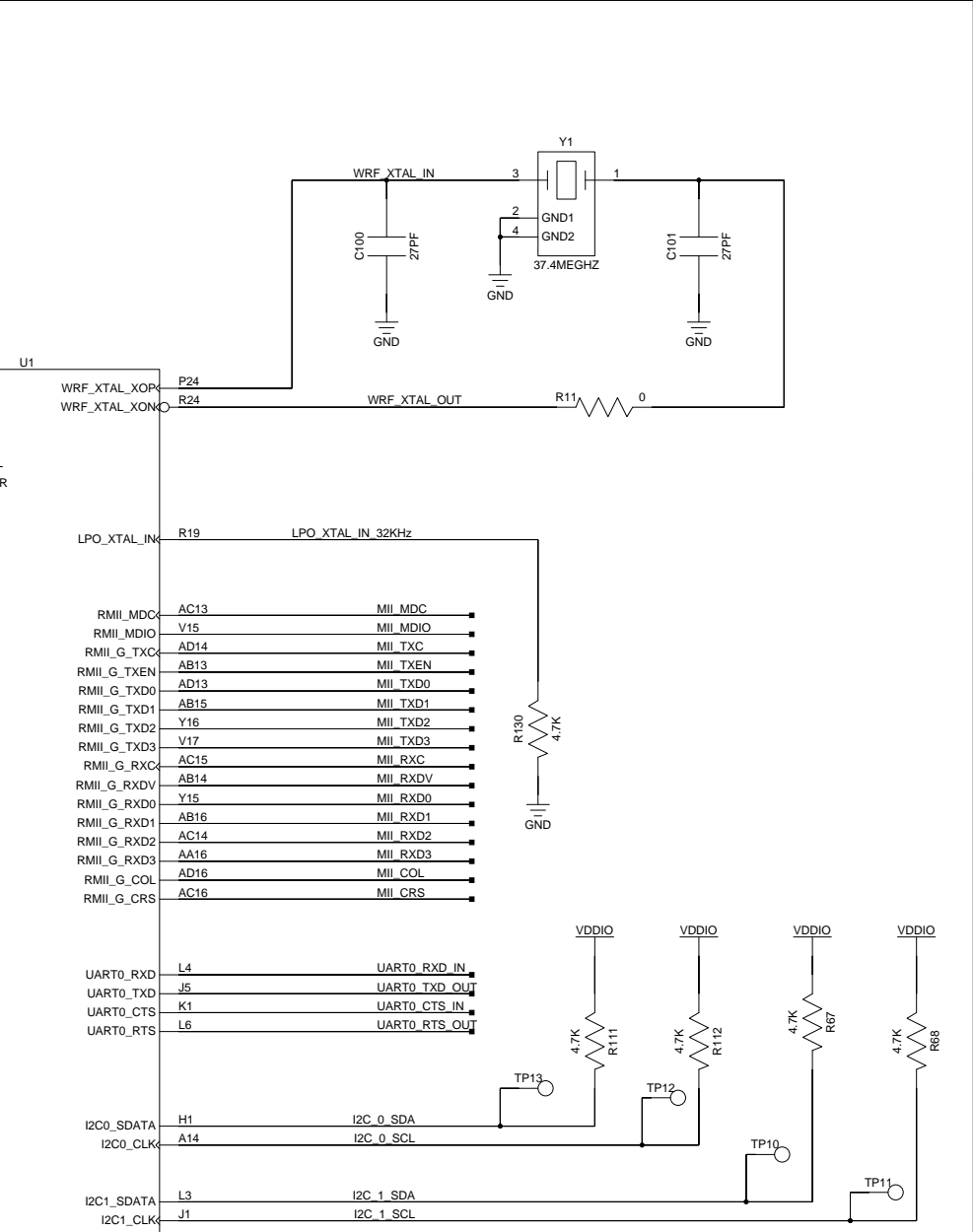


Pin	Strap Function	Strap Pull	
		Chip Default	Board Default
GPIO_1	gSPI Mode	0	0
GPIO_7	WCPU Boot Mode : 0 = TCROM Boot 1 = TCMSRAM Boot	0	0 R83= 4.7K to GND
GPIO_9	USB/HSIC Sel : 0 = HSIC PHY 1 = USB PHY	0	1 R84= 4.7K to 3.3V
GPIO_11	ACPU Boot Mode : 0 = SOCROM Boot 1 = SOCSRAM Boot	0	0 R87= 4.7K to GND
GPIO_13	SDIO Mode : 0 = SDIO Device 1 = SDIO Host	0	1 R88= 4.7K to GND
GPIO_15	Strap Removed in B0		
RF_SW_CTRL_5	Host DAP Clock Sel	0	0
RF_SW_CTRL_7	Host RSRC Init	0	0
RF_SW_CTRL_9	LPO Sel : 0 = LPO from HIB 1 = Internal 32KHz LPO	0	0



USB2_HOST_DEV_SEL

USB Device : R98 Populated (Pulled High) & R100 Depop
USB Host : R98 Depopped & R100 Populated (Pulled Low)



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SIZE	TITLE
B	BCM943909WCD1_3
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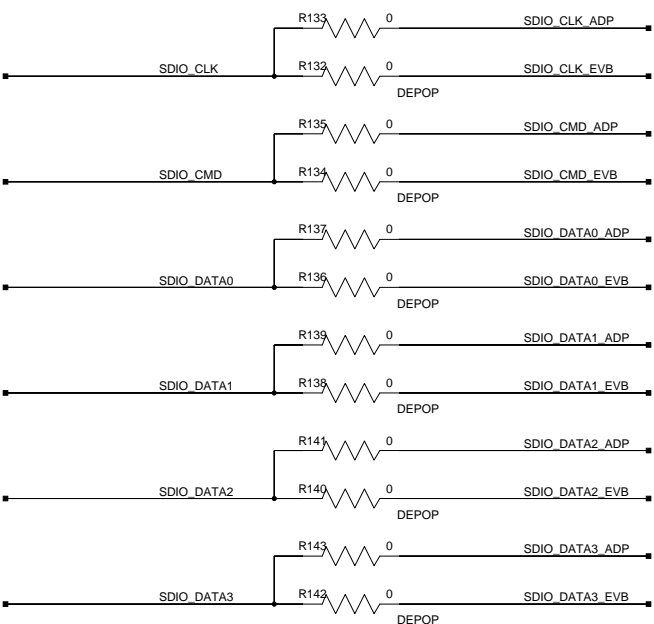
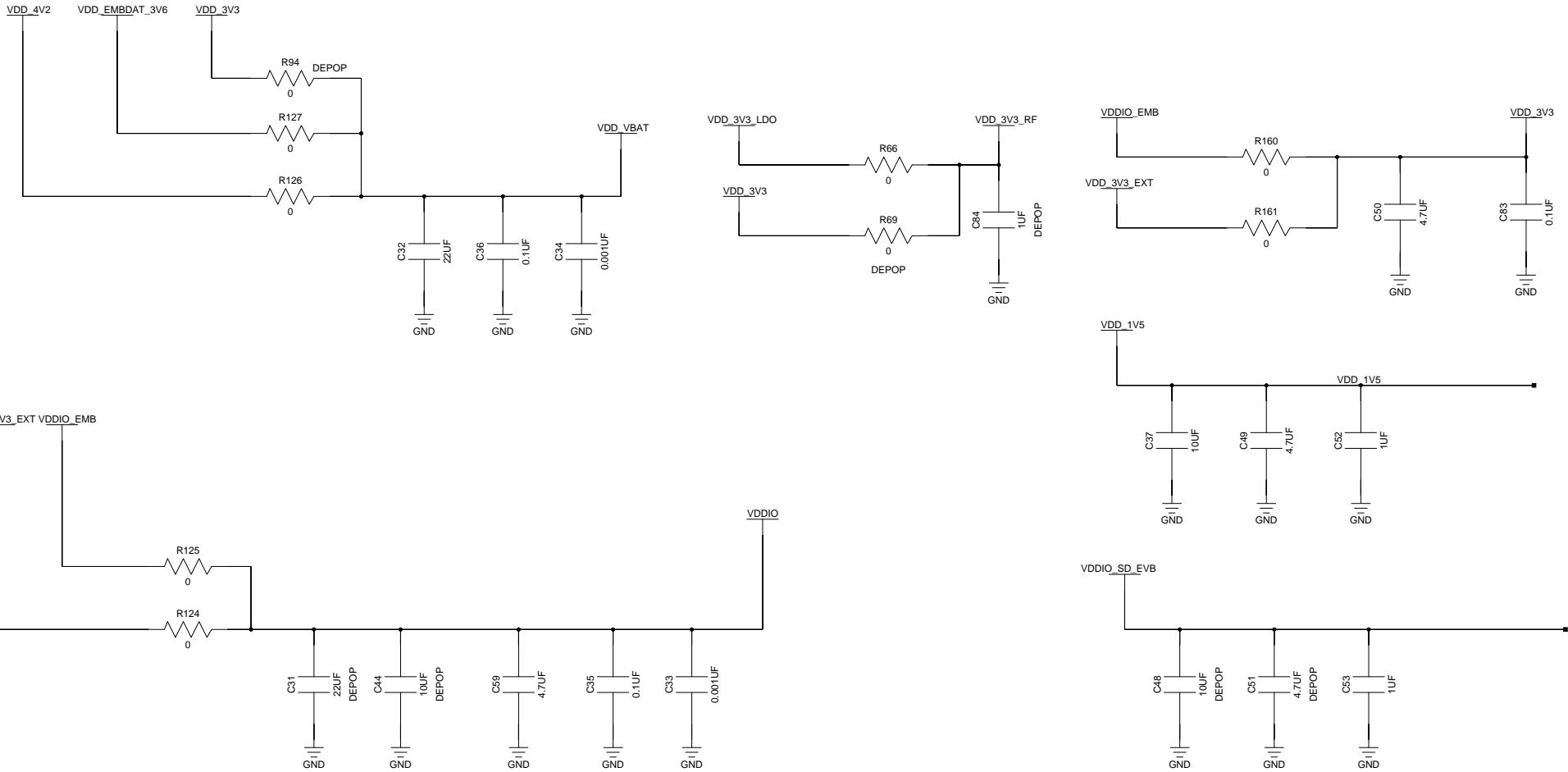
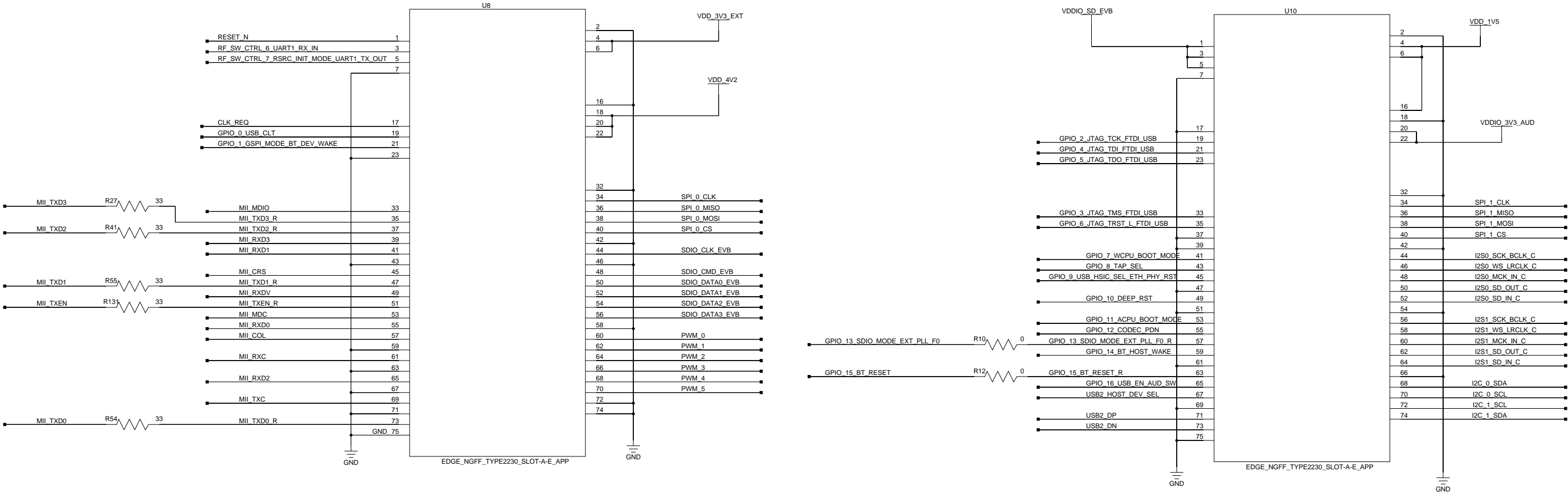
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M.2 Connectors

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SIZE	TITLE		
B	BCM943909WCD1_3		
DATE	04/03/2015:12:10	SHEET	3 OF 9

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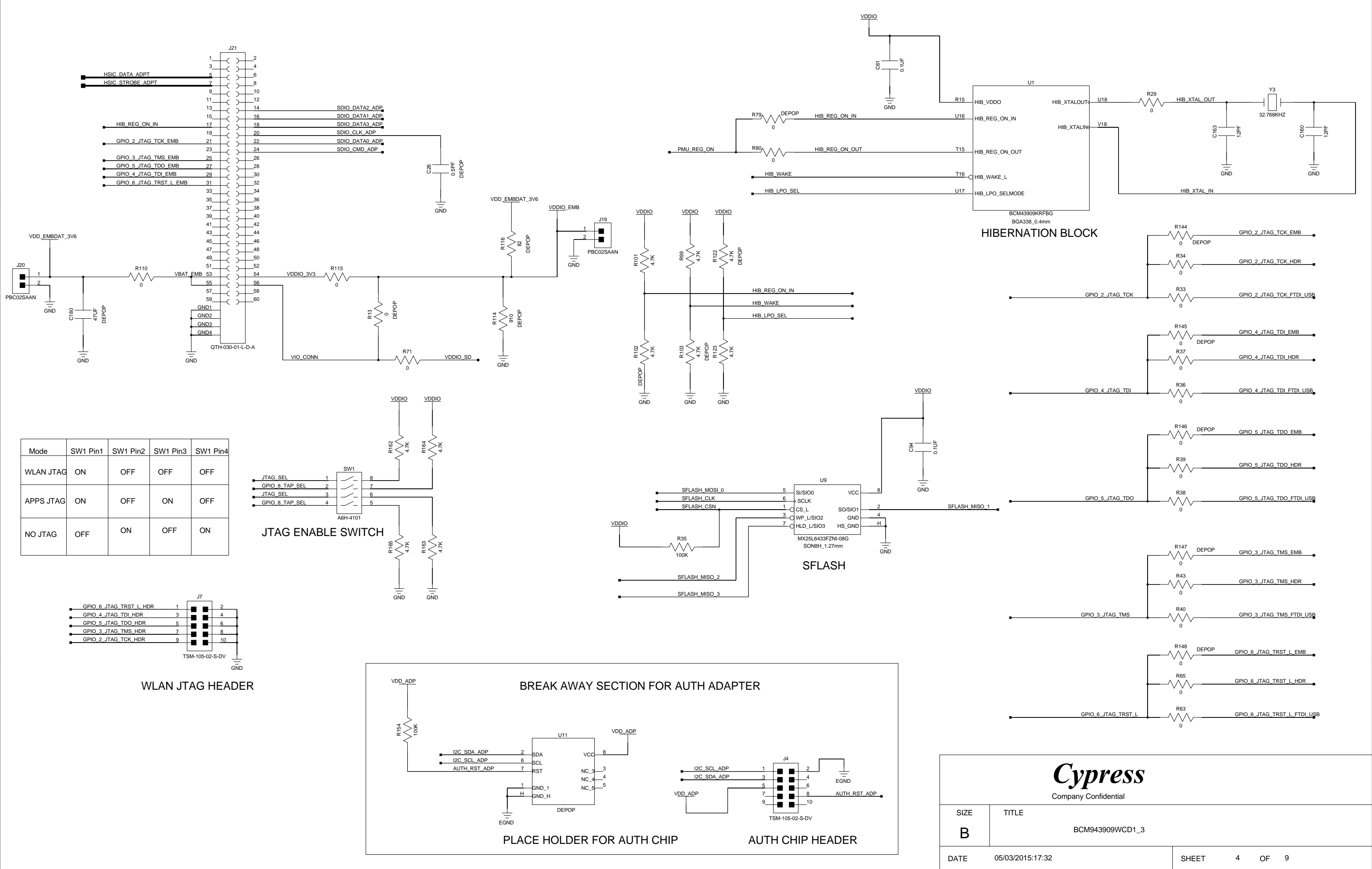
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Mode	SW1 Pin1	SW1 Pin2	SW1 Pin3	SW1 Pin4
WLAN JTAG	ON	OFF	OFF	OFF
APPS JTAG	ON	OFF	ON	OFF
NO JTAG	OFF	ON	OFF	ON

WLAN JTAG HEADER

JTAG ENABLE SWITCH

BREAK AWAY SECTION FOR AUTH ADAPTER

PLACE HOLDER FOR AUTH CHIP

AUTH CHIP HEADER

HIBERNATION BLOCK

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SIZE	TITLE	DATE	SHEET	4	OF	9
B	BCM943909WCD1_3	05/03/2015:17:32				

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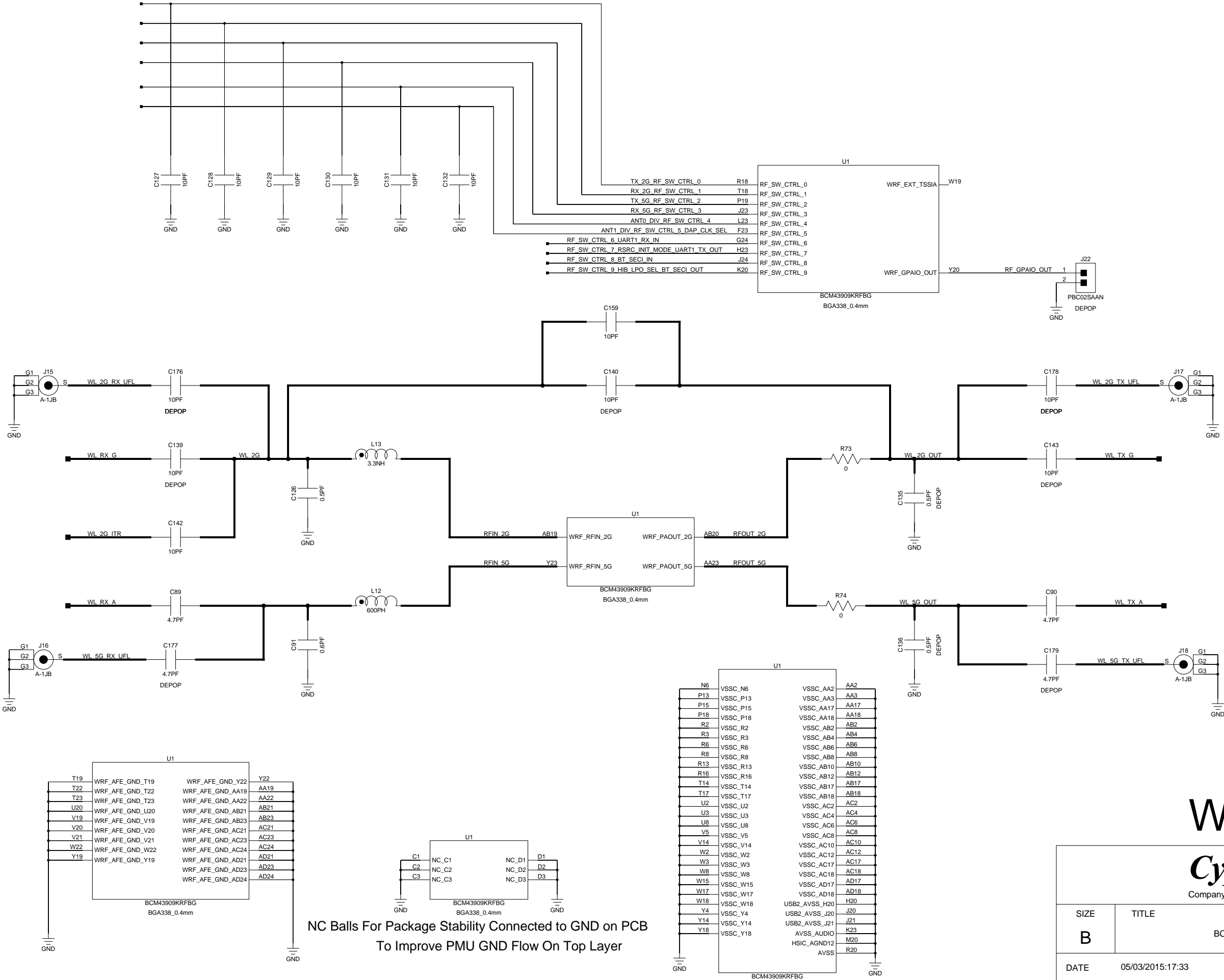
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WLAN RF

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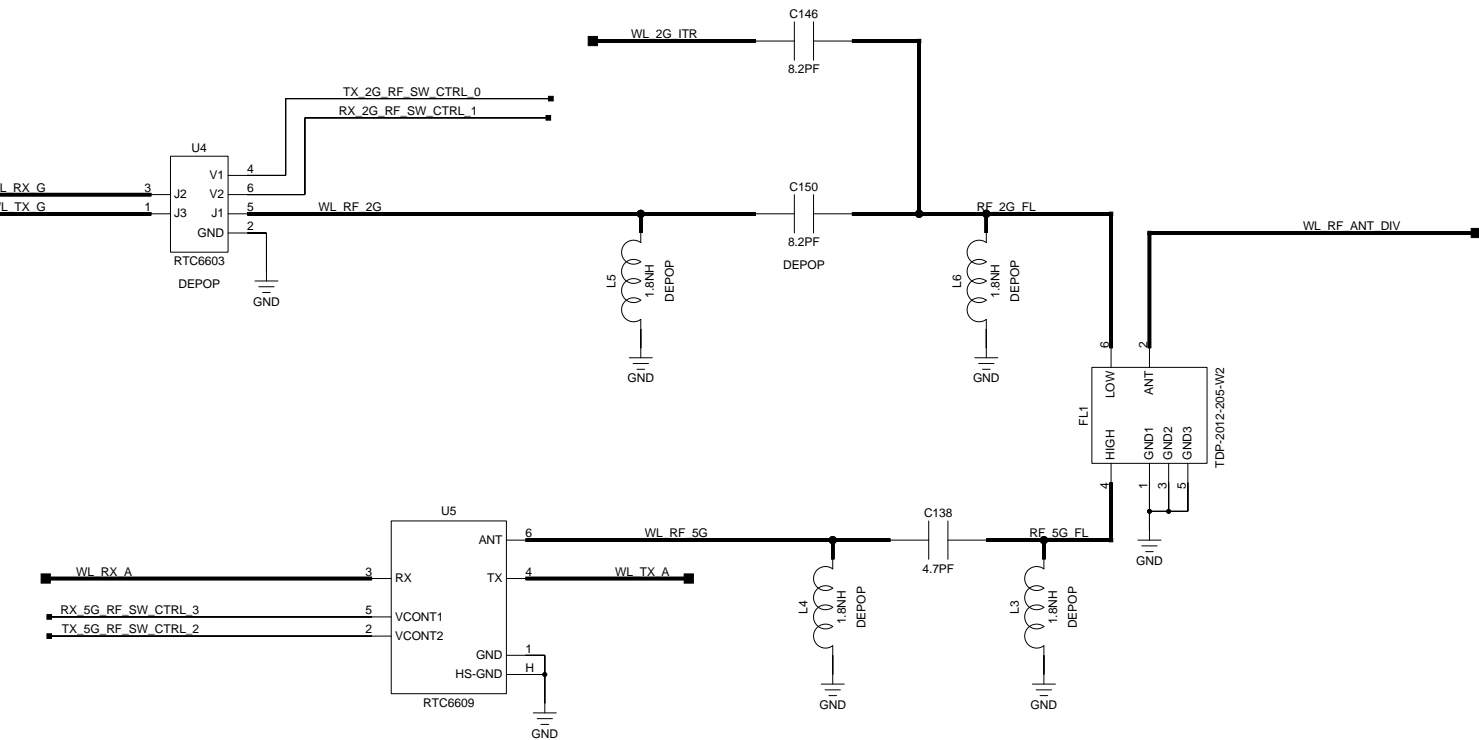
SIZE		TITLE	
B		BCM943909WCD1_3	
DATE	05/03/2015:17:33	SHEET	7 OF 9

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2G T/R Switch Control Table

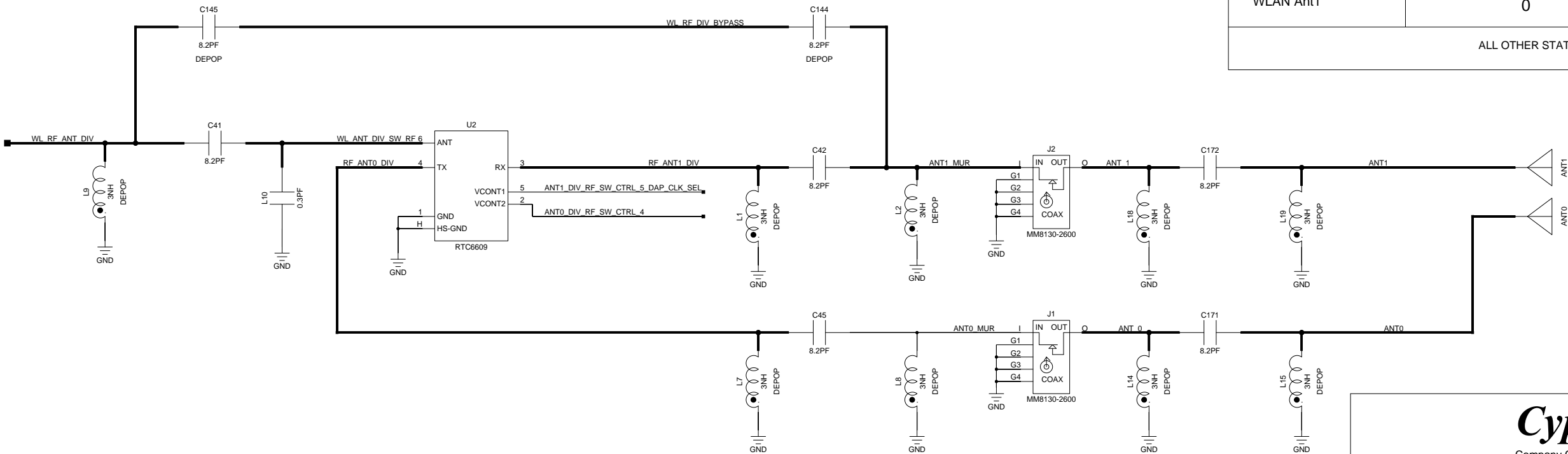
MODE OF OPERATION 2GHz SW (U4)	TX_2G_RF_SW_CTRL_0 2G SPDT (U4 Pin 4)	RX_2G_RF_SW_CTRL_1 2G SPDT (U4 Pin 6)
WLAN TX 2G	1	0
WLAN RX 2G	0	1
ALL OTHER STATES UNDEFINED		

5G T/R Switch Control Table

MODE OF OPERATION 5GHz SW (U5)	TX_5G_RF_SW_CTRL_2 5G SPDT (U5 Pin 2)	RX_5G_RF_SW_CTRL_3 5G SPDT (U5 Pin 5)
WLAN TX 5G	1	0
WLAN RX 5G	0	1
ALL OTHER STATES UNDEFINED		

Antenna Diversity Switch Control Table

MODE OF OPERATION Ant Diversity	ANT0_DIV_RF_SW_CTRL_4 SPDT (U2 Pin 2)	ANT1_DIV_RF_SW_CTRL_5_DAP_CLK_SEL SPDT (U2 Pin 5)
WLAN Ant0	1	0
WLAN Ant1	0	1
ALL OTHER STATES UNDEFINED		



WLAN RF

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B	BCM943909WCD1_3
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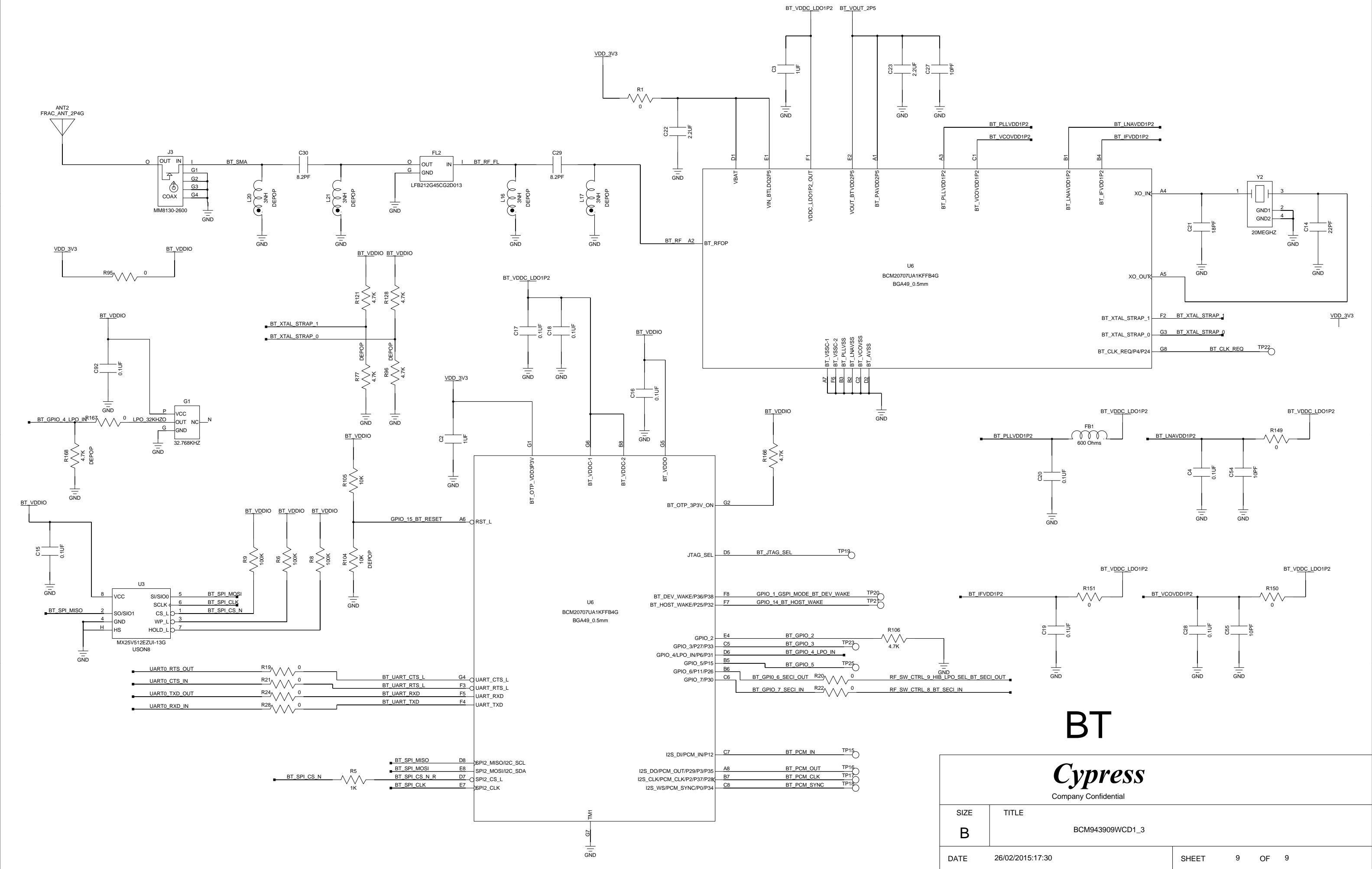
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SIZE	TITLE		DATE		SHEET		9 OF 9	
B	BCM943909WCD1_3		26/02/2015:17:30		9		9	