

Lab3: Y86-64 ISA + SEQ implementation

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Architecture and Code Optimization (ARC) Lab

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Overview

- **In this lab,**
 - You will learn about the design and implementation of sequential Y86-64 processor
- **Part A : Y86-64 Assembly Programming**
 - Write programs in Y86-64 assembly : **sum, rsum, copy**
- **Part B : Sequential Implementation**
 - Implement a new Instruction : **IADDQ**

Configuration

■ A Linux environment

- with flex and bison (installed on Martini)
- Martini recommended, but not necessary

■ Download archlab-handout.tar from eTL

```
$> tar xvf archlab-handout.tar
```

```
$> cd sim
```

```
$> make
```

Part A : Y86-64 Assembly Programming

■ Your Task : Write `sum`, `rsum`, `copy` in Y86-64 assembly

- Working directory : `sim/misc`
- File to modify and submit : `sum.js`, `rsum.js`, `copy.js`
- C versions of the programs : `sim/misc/examples.c`
- To test :

```
$> cd sim/misc
```

```
$> make
```

```
$> ./yas sum.js
```

```
$> ./yis sum.yo
```

Part B : Sequential Implementation

■ Your Task : Implement IADDQ instruction

- Working directory : sim/seq
- File to modify and submit : seq-full.hcl
- Standard implementation (for reference) : seq-std.hcl
- To test IADDQ :

```
$> cd sim/seq
$> make VERSION=full      // use seq-full.hcl to simulate
$> ../misc/yas ../y86-code/asumi.js
$> ssim ../y86-code/asumi.yo
```
- You can also test with the standard SEQ simulator

```
$> make      // use seq-std.hcl to simulate
$> ssim ../y86-code/you_want_to_execute.yo
```

Part B : Sequential Implementation

■ Verify your SEQ simulator by running tests

- First, prepare your version of simulator

```
$> cd sim/seq
```

```
$> make VERSION=full
```

- To run the benchmark programs :

```
$> cd sim/y86-code
```

```
$> make testssim
```

- To run the regression test :

```
$> cd sim/ptest
```

```
$> make SIM=../seq/ssim // tests simulator except IADDQ
```

```
$> make SIM=../seq/ssim TFLAGS=-i // including IADDQ
```

Submission Guideline

- Zip your files into **Lab3.tar**

```
$> tar cvf Lab3.tar sim/misc/*.ys \  
sim/seq/seq-full.hcl
```
- Submit **Lab3.tar** on eTL
- Due Date: **Oct 30th(Tue) 11:59PM**
 - Cut-off Date : **Nov 2nd(Fri) 11:59PM**

Grading Policy

- **Part A : 45 points**
 - 15 points for each program's correctness
- **Part B : 55 points**
 - 25 points for passing the benchmark programs
 - 30 points for passing the regression tests in /ptest
- **Check `archlab.pdf` for more details**
- **[Important] Next homework will be implemented based on current homework.**

Grading Policy

■ Late submission penalty

- ~ 24 hrs: -20% of maximum score
- ~ 48 hrs: -40% of maximum score
- ~ 72 hrs: -60% of maximum score
- 72 hrs ~: cut-off (no more submission)
- Grace Days: no late penalties up to 3 days through this semester (automatically applied to HW #1 through #5)

■ Plagiarism

- 0 for all assignments (worth of 35% of total grade!)
- We may use a plagiarism detector program over your codes
- OK to discuss ideas, but never share your codes in any form

Q&A

- Thank you for paying attention.