4190.309A: Electrical and Electronic Circuits Exam #3 December 13th, 2018 Professor Jae W. Lee

Student ID #	•	
Name:	TAs	

This is a closed book, closed notes exam.

80 Minutes

16 Pages

Total Score: 200 points

Notes:

- Please turn off all of your electronic devices (phones, tablets, notebooks, netbooks, and so on). A clock is available on the lecture screen.
- Please stay in the classroom until the end of the examination.
- You must not discuss the exam's contents with other students during the exam.
- You must not use any notes on papers, electronic devices, desks, or part of your body.

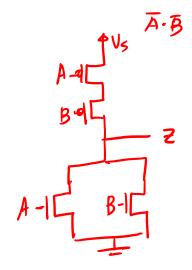
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Part A: CMOS Logic (44 points)

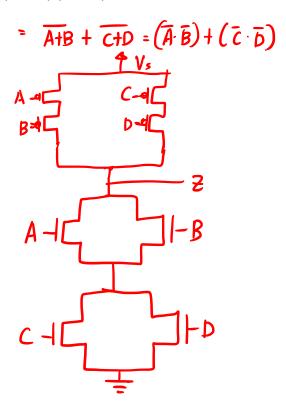
Question 1 (16 points)

Draw a schematic of CMOS logic for each given Boolean function.

(1)
$$Z = \overline{A + B}$$



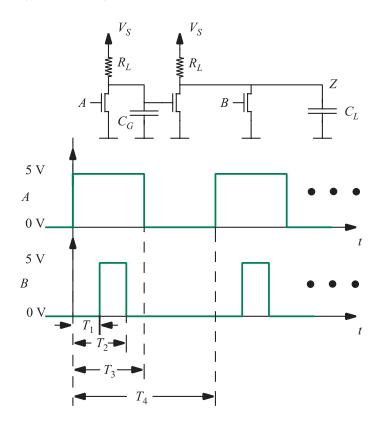
(2)
$$Z = \overline{(A+B)(C+D)}$$



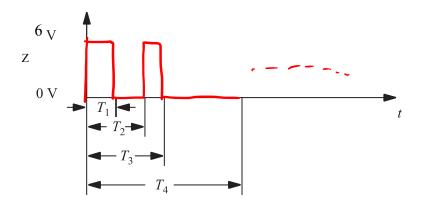
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Question 2 (28 points)

Ben Bitdiddle has designed a small digital circuit. He wants to estimate the power dissipated by the circuit he designed. This circuit has two inputs, A and B, and one output, Z. Inputs are assumed to be periodic with a period of T_4 . Assume $V_S = 5V$, $C_G = 100 \mathrm{fF}$, $C_L = 1 \mathrm{pF}$, $T_1 = 100 \mathrm{ns}$, $T_2 = 200 \mathrm{ns}$, $T_3 = 300 \mathrm{ns}$, $T_4 = 600 \mathrm{ns}$, $R_L = 10 \mathrm{k}\Omega$, and $R_L >> R_{ON}$.



(1) Draw the output waveform for $0 \le t \le T_4$. Assume C_G and C_L are both zero. What kind of logic gate does it implement (i.e., Z as a function of A and B)?



(2) Evaluate the time-average *static power* consumed by the circuit. The time-average power is the total energy dissipated by the circuit (during the period $0 \le t \le T_4$) divided by T_4 .

$$\frac{5^{2}}{10k} \times \frac{300+100+300}{600} = 2.91 \text{ mW}$$

(3) Evaluate the time-average *dynamic power* consumed by the circuit. The definition of time-average power is same as the one in (2).

$$\frac{10^{-13} \times 5^{2} + 10^{-12} \times 5^{2} \times 2}{600 \times 10^{-9}} = \frac{525 \times 10^{-13}}{600 \times 10^{-9}}$$

(4) What is the time-average total power if he converts this circuit to CMOS circuit? Explain why.

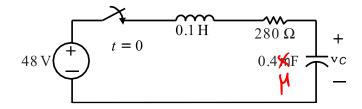
87.5 mW

No static Power.

Part B: Second-order Transients (44 points)

Question 3 (24 points)

Initially (at $t=0^{-}$), no energy is stored in the inductor (100 mH) and the capacitor (0.4 \times F). The switch is closed at $t=0^{+}$. Plot the $v_{C}(t)$ for $t \ge 0$ by using an intuitive analysis. When you do this, please clarify following conditions: value of convergence, underdamp or overdamp, and period of fluctuations. (Hint: 23040000 = $(4800)^{2}$)



Value of unvengence: 48V

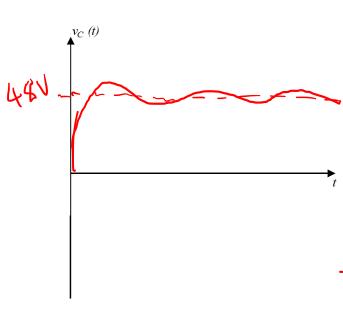
$$S^2 + \frac{R}{L}S + \frac{1}{1c} = 0$$

52+2800S+25×106=0

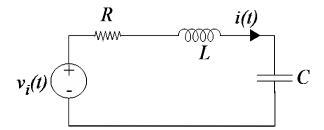
underdamped, (:'a2< W2)

period of fluctuation T:

$$T \approx \frac{2\pi}{4800}$$



Answer the questions about circuit given below where $v_i = V_i \cos(\omega t)$.



(1) Determine $\omega 0$ that maximizes power consumption of this circuit.

$$T = \frac{V_i}{R + i(WL - VWC)}$$

$$P = \frac{V_i^2}{R + i(WL - i/WC)}$$

$$P = \frac{V_i^2}{R + i(WL - i/WC)}$$

$$P = \frac{V_i^2}{R^2 + i(WL - i/WC)}$$

$$P = \frac{V_i^2}{R + i(WL - i/WC)}$$

(2) Calculate the maximum power of this circuit at $\omega = \omega 0$. (Hint: $\cos^2 \theta = \frac{1 + \cos 2\theta}{2}$)

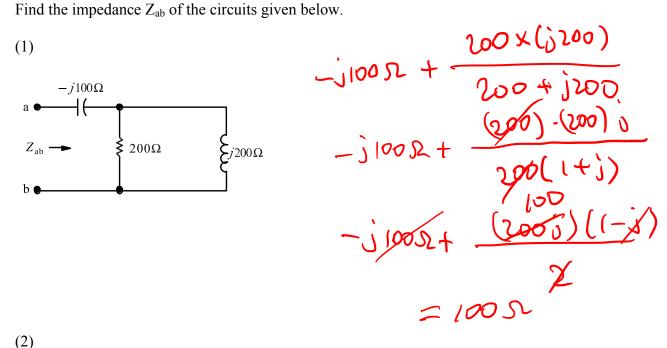
$$P = \frac{1}{T} \int_{0}^{T} \frac{(v_{i})^{2} \cos^{2} wt}{R} dt$$

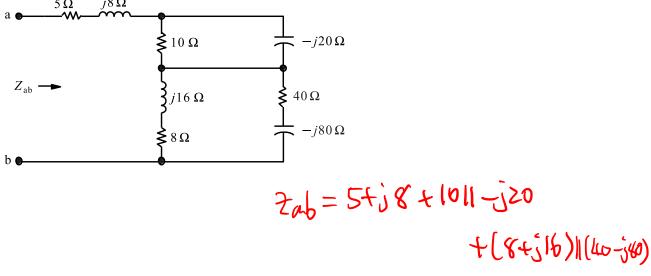
$$= \frac{1}{T} \left[\frac{(v_{i})^{2}}{R} \left(\frac{1}{2} + \cos^{2} 2wt \right) \right]_{0}^{T} = \frac{(v_{i})^{2}}{2R}$$

Part C: Sinusoidal Steady State (44 points)

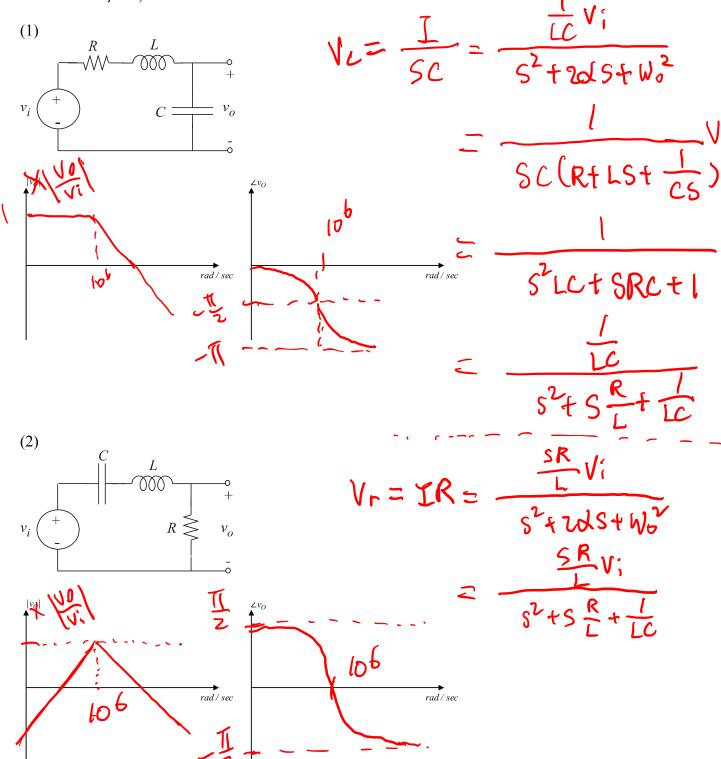
Question 5 (20 points)

Find the impedance Z_{ab} of the circuits given below.





Draw a Bode plot of $H(j\omega) = \frac{v_o}{v_i}$, including both magnitude and phase with clearly marking the cut-off frequency and other important data points (R = 1 Ω , L = 1 μ H, and C = 1 μ F at $\omega = 10^6 \ rad/sec$).

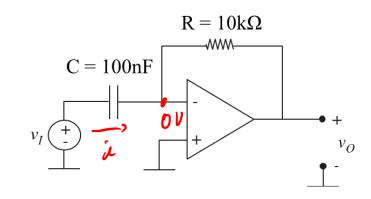


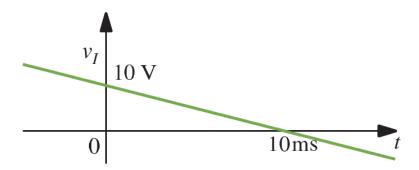
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Part D: The Operational Amplifier (68 points)

Question 7 (22 points)

Find the relationship between $v_O(t)$ and $v_I(t)$ in the circuit below. Assume an ideal operational amplifier, which has an infinite gain, infinite input resistance, and zero output resistance.





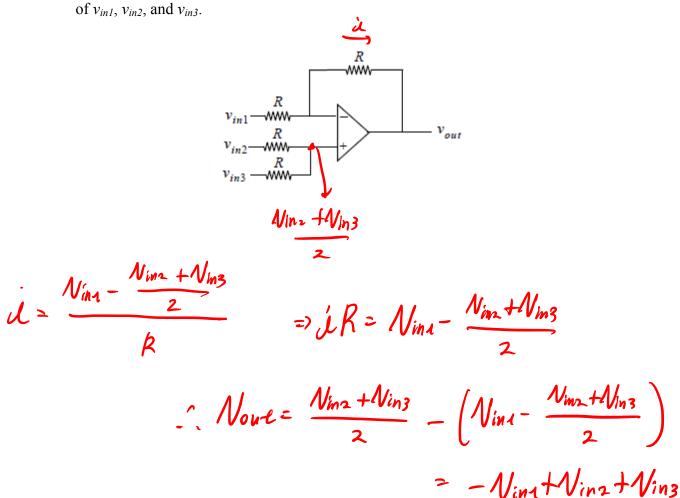
$$V_{0}=0-iR$$

$$i=C\frac{dv_{i}}{d\ell}$$

$$V_{0}=-RC\frac{dv_{k}}{d\ell}=-10x^{2}x^{2}x^{2}x^{2}x^{2}x^{2}-10^{3}x^{2}$$

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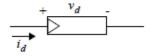
(1) For the operational amplifier circuit shown below, find an expression of v_{out} as a function of v_{int} , v_{in2} , and v_{in3} .



(2) A nonlinear device with voltage v_d and current i_d has a characteristic given by

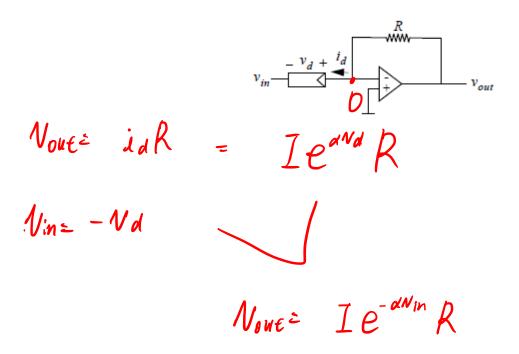
$$i_d = I e^{\alpha v_d}$$

where $v_d > 0$ and $i_d > 0$.



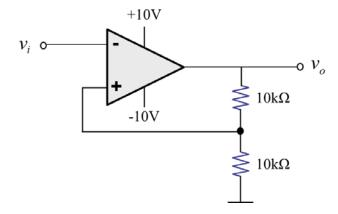
For all parts of this problem assume that the operational amplifiers are ideal, that they are operating in the active region and that the nonlinear device is operating with positive values of v_d and i_d .

For the nonlinear element connected as shown below, find an expression of v_{out} as a function of v_{in} .

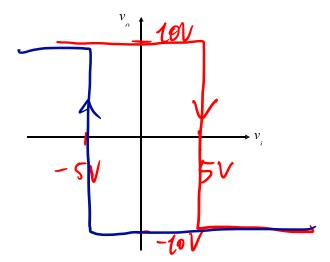


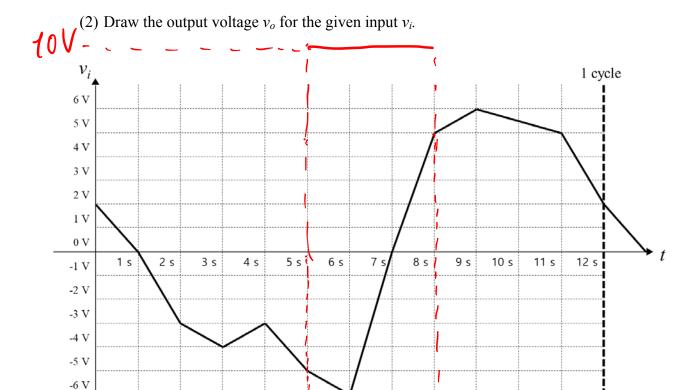
Question 9 (24 points)

Alice Hacker has designed the circuit the circuit in the figure below. Answer the following questions.



(1) Draw a hysteresis graph of given circuit when the input varies from -10V \rightarrow +10V, and back to -10V .





(3) What is the duty cycle of the output in (2)? The duty cycle is the percentage of the time when the output value is 1 within a single period. (e.g., a 50% duty cycle means the value is 1 during a half cycle and 0 during the other half.)

$$\frac{3}{12} \Rightarrow 25\%$$

-10V

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