# 4190.309A: Electrical and Electronic Circuits
# Exam #2
# November 15th, 2018
# Professor Jae W. Lee

Student ID #: _____

Name: _____

This is a closed book, closed notes exam.
80 Minutes
16 Pages

Total Score: 200 points

Notes:

- Please turn off all of your electronic devices (phones, tablets, notebooks, netbooks, and so on). A clock is available on the lecture screen.
- Please stay in the classroom until the end of the examination.

- You must not discuss the exam's contents with other students during the exam.
- You must not use any notes on papers, electronic devices, desks, or part of your body.

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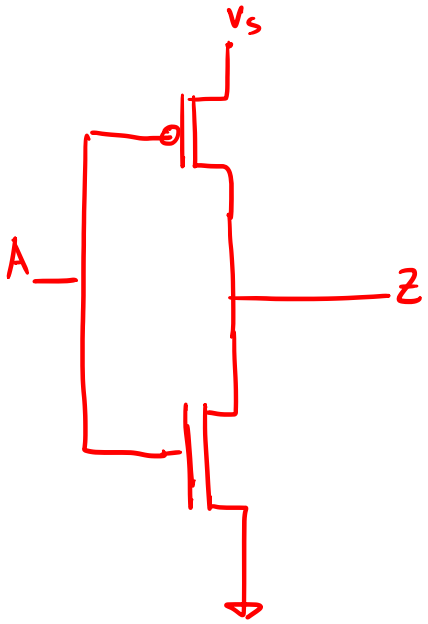
# Part A: Logic Gates (20 points)

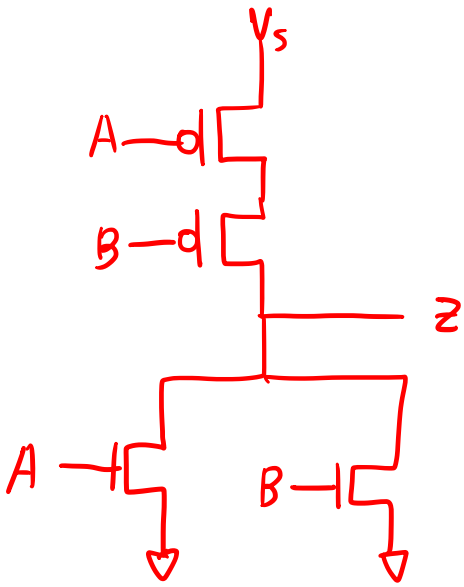
**Question 1 (20 points)**

Draw a schematic of **CMOS logic** for each given Boolean function.

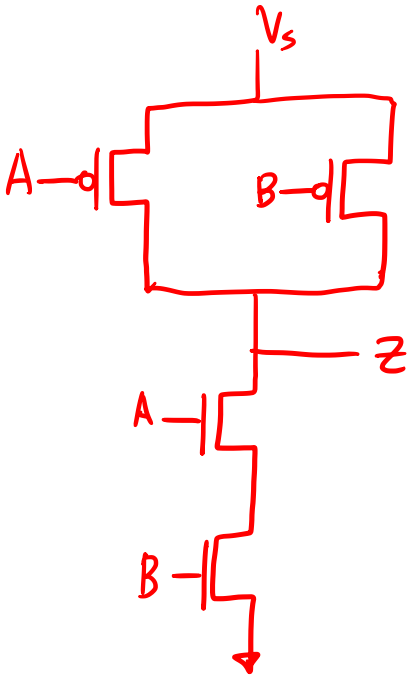
(1) $Z = \overline{A}$



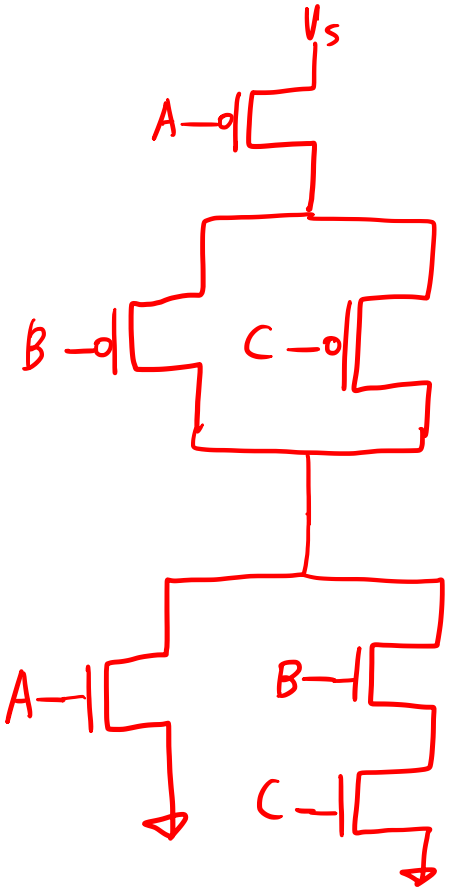

(2) $Z = \overline{A + B}$



(3) $Z = \overline{AB}$



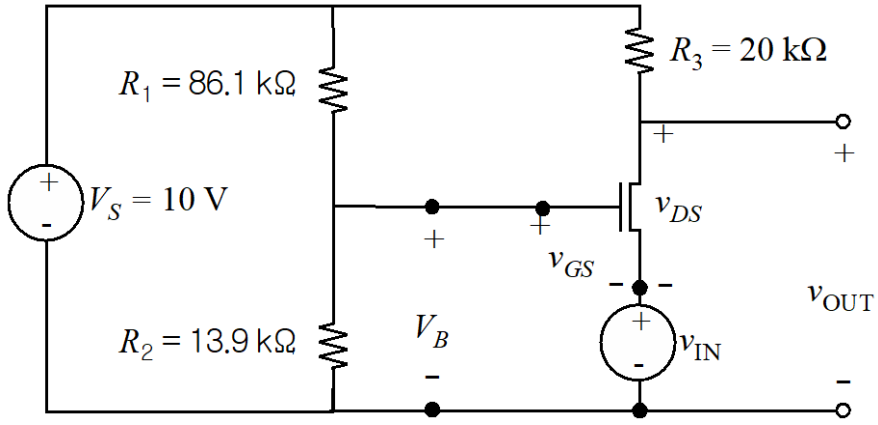

(4) $Z = \overline{A + B} + \overline{A}\,\overline{C}$



# Part B: The MOSFET Amplifier (28 points)

**Question 2 (28 points)**

The circuit shown below is a MOSFET amplifier. Assume that the MOSFET is in the saturation region with $V_T = 1\text{V}$ and $K = 0.1\text{mA/V}^2$. (1) Determine the large-signal output ($v_{OUT}$) as a function of the input voltage ($v_{IN}$). (2) Determine the valid range of $v_{IN}$ and $v_{OUT}$ over which the MOSFET operation remains in the saturation region.




(1) $v_{out} = V_S - \frac{R_3 k}{2}(V_B - v_{IN} - V_T)^2$

$= 10 - (0.39 - v_{IN})^2$ ($\because V_B = \frac{13.9}{100} \times 10$

$= 1.39\ \text{V}$)

(2) To operate on saturation region,

$v_{out} - v_{IN} \geq V_B - v_{IN} - V_T \geq 0$

② ①

① $V_B - V_T \geq v_{IN}$

$0.39 \geq v_{IN}$

② $10 - (0.39 - v_{IN})^2 \geq 0.39$

$9.61 \geq (0.39 - v_{IN})^2$

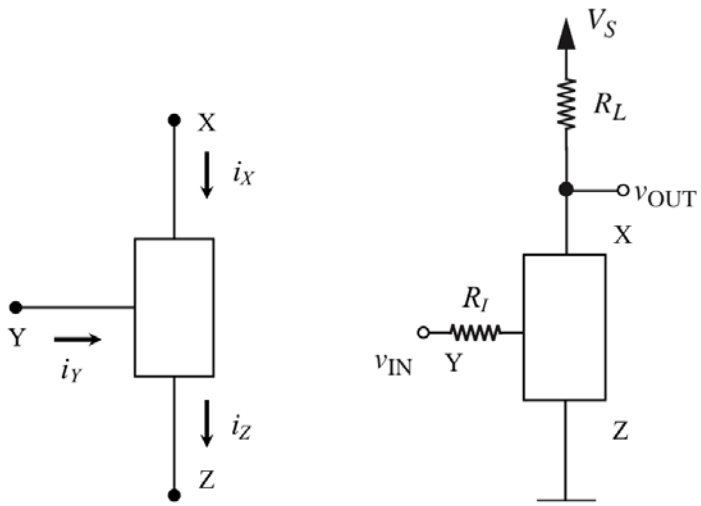
$-2.71 \leq v_{IN} \leq 0.39$

$0.39 \leq v_{out} \leq 10\text{V}$ $v_{IN} \geq -2.71$

# Part C: Small-Signal Models (60 points)

**Question 3 (28 points)**

We have an unknown 3-terminal device (shown as an empty box) whose large-signal current relationship between X, Y, and Z terminals is given as: $i_X = Ki_Y$ and $i_Z = i_X + i_Y$. (Note the reference directions of $i_X$, $i_Y$, and $i_Z$.)




(a) Device model (b) Amplifier circuit

"K is constant"

(1) Calculate the incremental change in small signal $i_x$ as a function of an incremental change in small signal $i_y$.

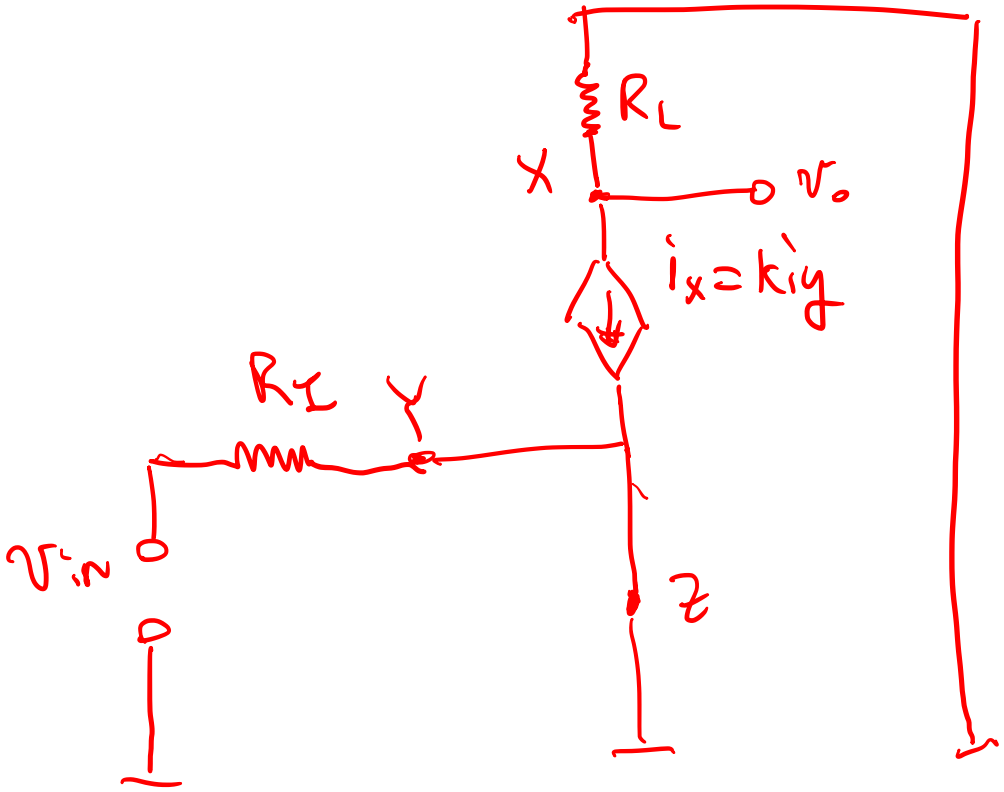
from $i_x = ki_y$, the relationship between the two incremental signal as follows:

$$i_x = \left.\frac{di_x}{di_Y}\right|_{i_Y = I_Y} \cdot i_y$$

$$= \left.\frac{dki_Y}{di_Y}\right|_{i_Y = I_Y} \cdot i_y$$

$$= k i_y.$$

(2) Draw a small-signal circuit diagram of the given amplifier circuit in (b). Also, calculate the small-signal gain ( $\frac{v_O}{v_I}$ ) of this amplifier.




$$v_o = -k i_y R_L$$

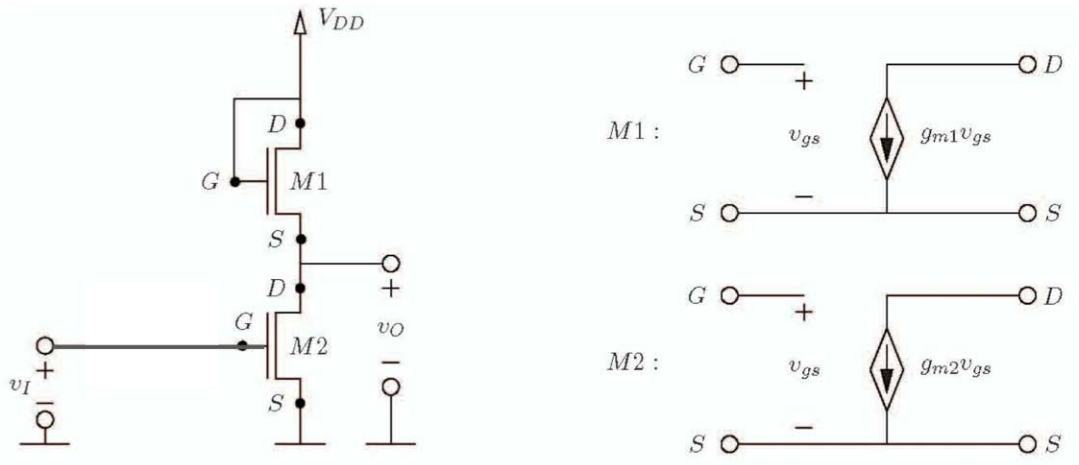
$$= -k \frac{v_{in}}{R_I} R_L$$

$$\therefore \frac{v_o}{v_{in}} = -k \frac{R_L}{R_I}$$

(small-signal gain)

**Question 4 (32 points)**

Answer the questions about the circuit given below.



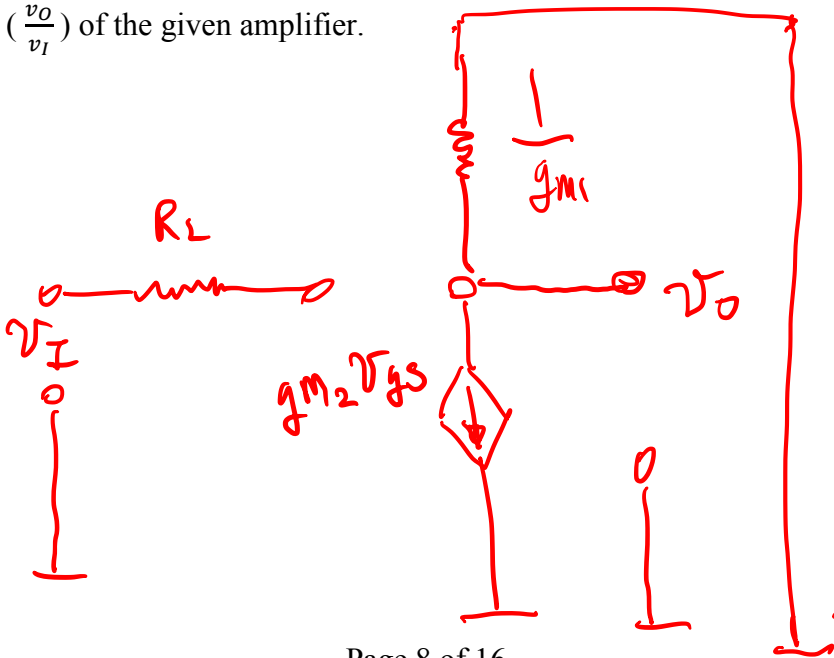

(1) Derive the *small-signal* resistance of M1 from its small signal model.

$V_{DS} = V_{GS}$

$g_{m1} V_{DS} = i_{DS}$ $\therefore \frac{V_{DS}}{i_{DS}} = \frac{1}{g_{m1}}$

$= r_{DS}$

(2) Assume that both MOSFETS are operating in the saturation region, determine the small signal gain ( $\frac{v_O}{v_I}$ ) of the given amplifier.




$V_o = -g_{m2} V_{GS} \times \frac{1}{g_{m1}}$

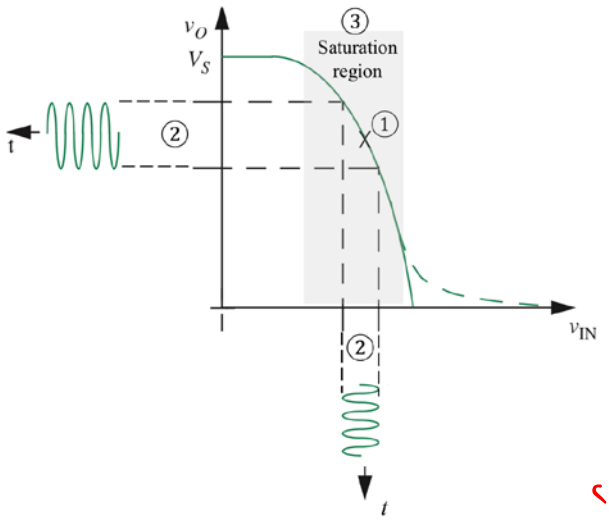
$= -\frac{g_{m2}}{g_{m1}} V_{GS}$

$V_o = -\frac{g_{m2}}{g_{m1}} V_I$

$\therefore \frac{V_o}{V} = -\frac{g_{m2}}{g_{m1}}$

(3) Assuming that two MOSFET transistor are identical, draw the $v_O$ versus $v_{IN}$ curve for the amplifier. Also, draw the output waveform when $v_I$ is a sinusoidal wave with a peak-to-peak voltage of 0.6 V and an DC offset ($V_I$) of 2 V.

$V_T = 1$




We provide an example drawing in the left. Be sure to indicate clearly ① DC bias point ($V_I$, $V_O$), ② range of swing for both $v_I$ and $v_O$, and ③ both endpoints of the saturation region in your drawing.

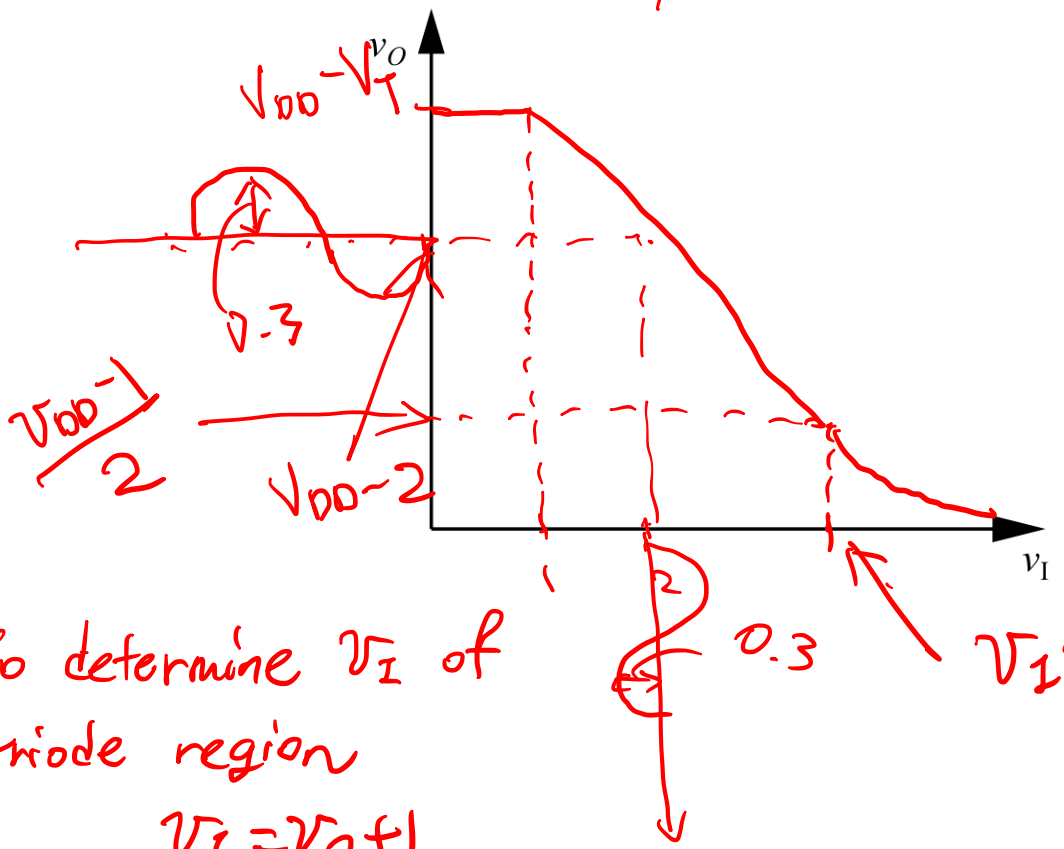
$M_2$ should operate in saturation

$v_{T2} \le v_I \le v_O + v_{T2}$

$i_{D1} = i_{D2}$

$\frac{1}{2}k_1(V_{DD} - v_O - v_{T1})^2 = \frac{1}{2}k_2(v_I - v_{T2})^2$

$k_1 = k_2$.




$V_{DD} - v_O = v_I$

$v_O = V_{DD} - v_I$

$v_I = \frac{V_{DD}+1}{2}$

To determine $v_I$ of triode region

$v_I = v_O + 1$

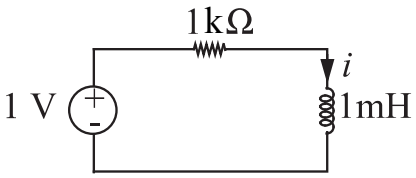
$v_I = \frac{V_{DD}+1}{2} = V_{DD} - v_I + 1$

$2v_I = V_{DD} + 1$

# Part D: First-order Transients (60 points)

**Question 5 (32 points)**

(1) Write the expression for $i(t)$ ($t > 0$) for the circuit. Assume a zero initial state. Don't forget the unit of the current.

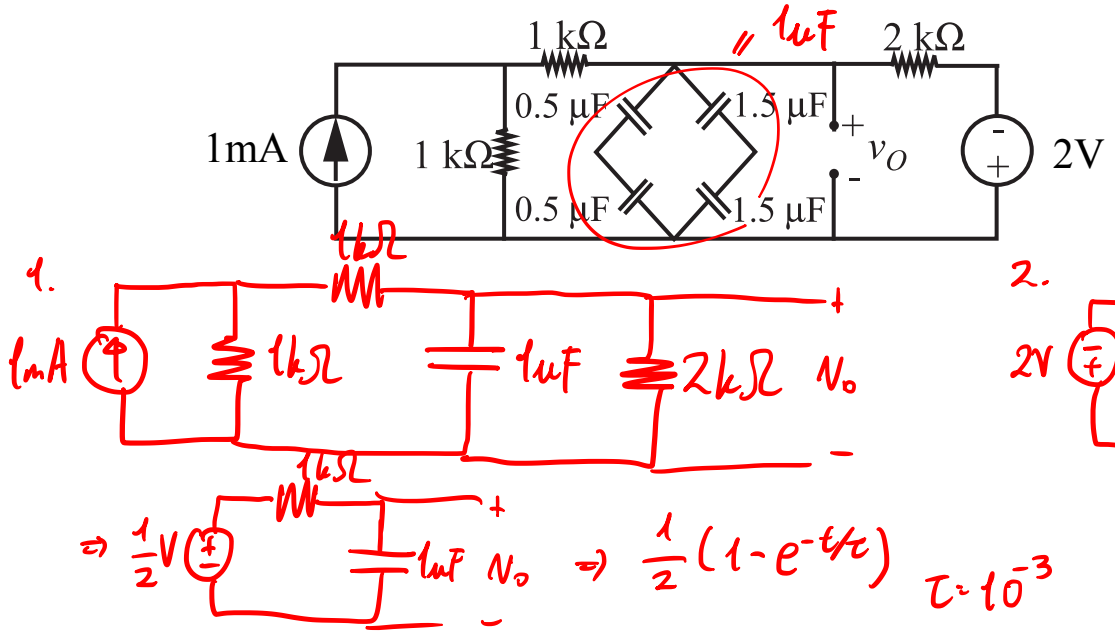



$i(t) = (1 - e^{-t/\tau})\,mA$ $\quad \tau = \frac{L}{R} = 10^{-6}$

(2) Write the expression for $v(t)$ ($t > 0$) for the circuit. Assume a zero initial state. Don't forget the unit of the voltage.


$v(t) = t\,kV$

(3) Write the expression for $v_O(t)$ ($t > 0$) for the circuit. Assume a zero initial state.




$\therefore -\frac{1}{2}(1-e^{-t/\tau})V$

$\tau = 10^{-3}$

1.

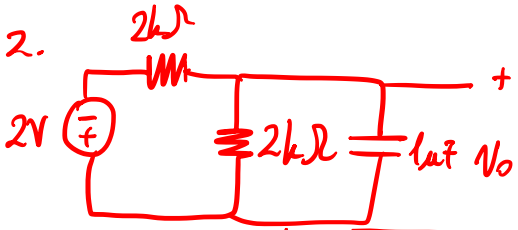



$\Rightarrow \frac{1}{2}V$

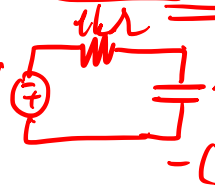



$\Rightarrow \frac{1}{2}(1-e^{-t/\tau})$ $\tau = 10^{-3}$

2.



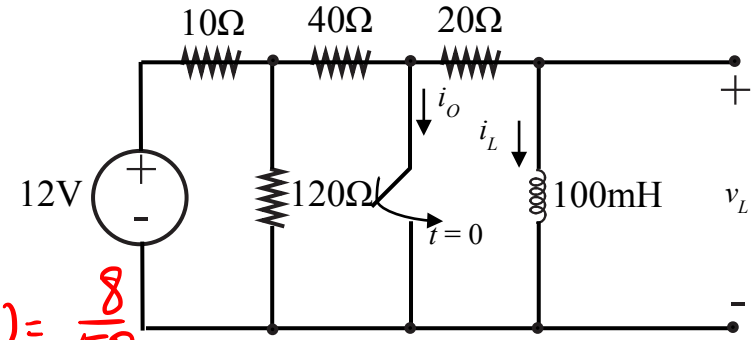

$\Rightarrow 1V$




$-(1-e^{-t/\tau})$

(4) Write the expression for $i_O(t)$ ($t > 0$) for the circuit. Assume the switch has been open for a long time before closing at t = 0.

$\tau = 10^{-3}$




$i_L(0-) = \frac{8}{50}$

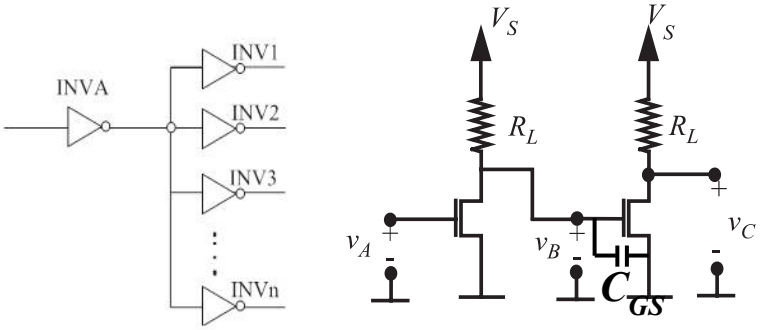
$i_o = \frac{9}{40} - \left(\frac{8}{50}e^{-t/\tau}\right) = \frac{9}{40} - \frac{4}{25}e^{-t/\tau}$

$\tau = \frac{1}{200}$

12V에서 3초 전류

**Question 6 (28 points)**

Figure (a) below illustrates an inverter *INV A* driving *n* other inverters *INV 1* through *INV n*. As in Figure (b), each of the inverters is constructed using a MOSFET and a resistor $R_L$ (we only show *INV 1* in the second stage for brevity), and the inverters satisfy the static discipline.




(a) (b)

(1) What is the rising delay ($t_r$) of *INV A* (i.e., the time for $v_B$ to switch from 0 to $V_{OH}$)?

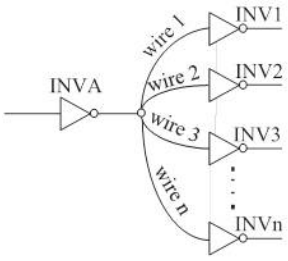
$$v_B = V_S - V_S e^{-t/\tau} \qquad \tau = R_L \cdot n C_{GS}$$

$$\Rightarrow V_{OH} = V_S - V_S e^{-t/\tau}$$

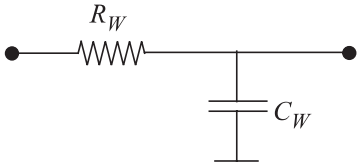
$$e^{-t/\tau} = \frac{V_S - V_{OH}}{V_S}$$

$$-t/\tau = \ln \frac{V_S - V_{OH}}{V_S} \qquad \therefore t = -\tau \ln \frac{V_S - V_{OH}}{V_S}$$

(2) Assume that each of the wires connecting the output of *INV A* to each of the inverters *INV 1* through *INV n* is non-ideal as depicted in Figure (c). We model each of the wires as shown in Figure (d). Assuming that the input of *INV A* makes a step transition from 1 to 0, find the rising delay at the input of any of the inverters *INV i* driven by *INV A*.




(c)




(d)

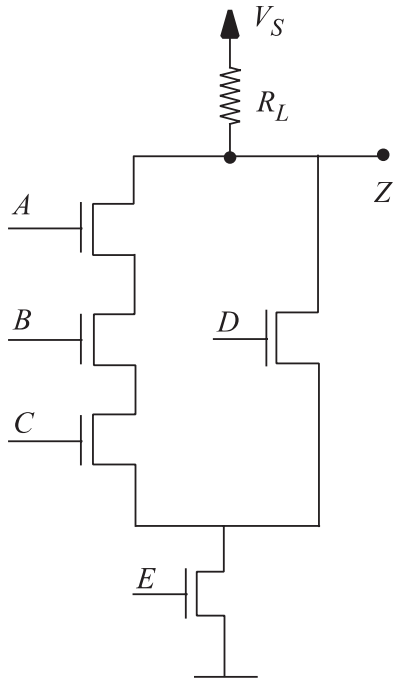
$$T = n(C_{GS} + C_W)\left(R_L + \frac{1}{n}R_W\right)$$

나머지 식은 동일.

# Part E: CMOS Circuit (32 points)

**Question 7 (32 points)**

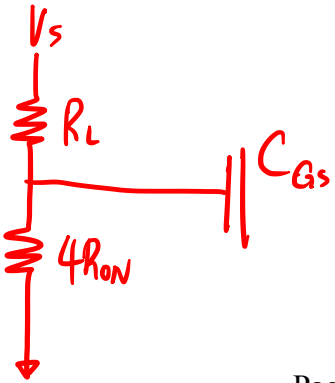
The circuit below is an NMOS logic function $Z = \overline{(ABC + D)E}$. Suppose the output of this circuit drives an inverter with a gate capacitance of $C_{GS}$. Assume that all the MOSFETs in the circuit have the same on-resistance $R_{ON}$, and same high and low voltage thresholds ($V_{IL} = V_{OL}$ and $V_{IH} = V_{OH}$).




(1) What is the input (A, B, C, D, E) that results in the worst-case falling delay for the circuit?

(A, B, C, D, E) = (1, 1, 1, 0, 1)

(2) Derive an expression for the worst-case falling delay (i.e., time for $v_{OUT}$ to switch from $V_S$ to $V_{OL}$)?




$$V_L = V_S \frac{4R_{ON}}{R_L + 4R_{ON}} + \left(V_S - V_S \frac{4R_{ON}}{R_L + 4R_{ON}}\right) e^{-t/\tau}$$

$$\tau = C_{GS} \frac{4R_{ON} R_L}{R_L + 4R_{ON}}$$

$$t = -\tau \ln \frac{V_L - V_S \frac{4R_{ON}}{R_L + 4R_{ON}}}{V_S - V_S \frac{4R_{ON}}{R_L + 4R_{ON}}}$$

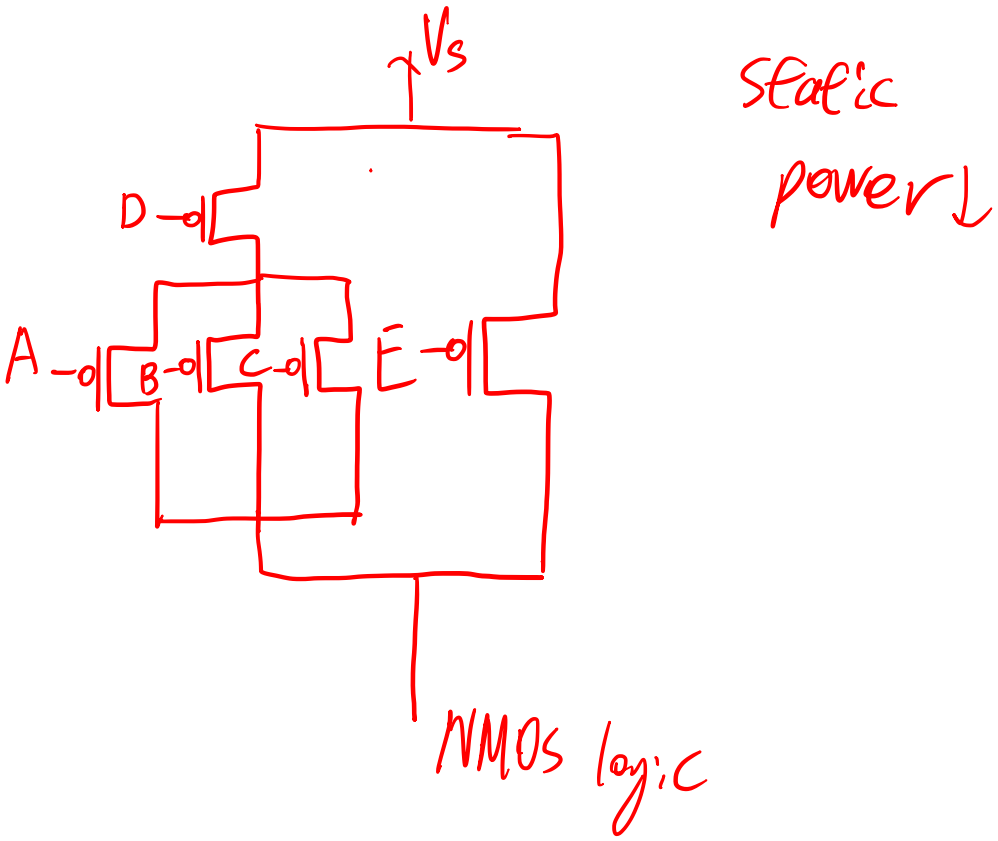
(3) What is the maximum power consumption of this circuit? Derive both the worst-case static power and dynamic power. Assume $C_{GS}$=1pF, $R_L$=10kΩ, $f$=50MHz, $V_s$=5V, and $R_L >> R_{ON}$.

$$\text{Static} = \frac{V_s^2}{2R_L} \quad (R_L \gg R_{on}) = \frac{25}{20}\,mW$$

$$\text{Dynamic} = C_{GS} V^2 f = 10^{-12} \times 5^2 \times 50 \times 10^6$$

$$= \frac{25}{20}\,mW \quad \therefore 2.5\,mW$$

(4) Convert this circuit to CMOS logic. How does the power consumption of this circuit differ from that of NMOS logic in (3)? Explain briefly in one paragraph.



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