

The MOSFET Switch

Lecture 5

September 20th, 2018

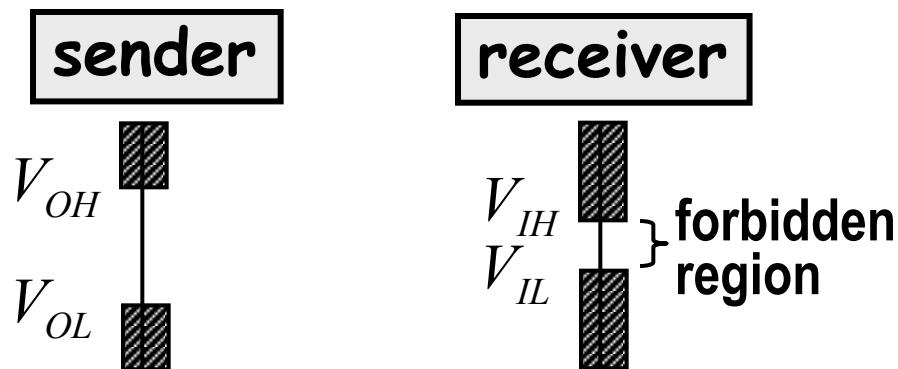
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Computer Science and Engineering
Seoul National University

Slide credits: Prof. Anant Agarwal at MIT

Review: The Digital Abstraction

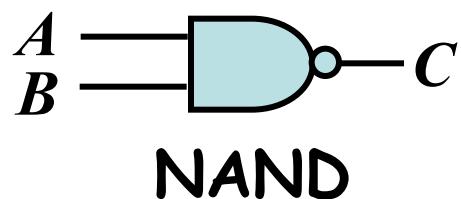
- Discretize value 0, 1
- Static discipline
meet voltage thresholds



Specifies how gates must be designed

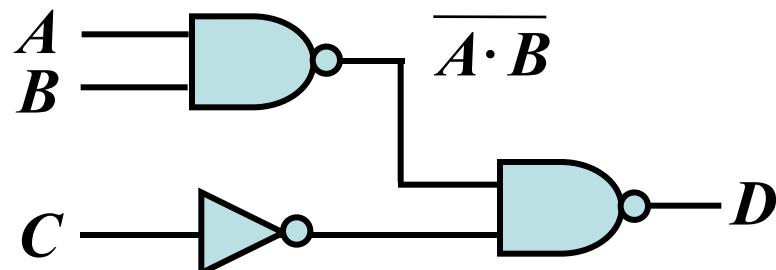
Review: Combinational gate abstraction

- outputs function of input alone
- satisfies static discipline



A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

For example: a digital circuit



$$D = (\overline{C} \cdot (\overline{A} \cdot \overline{B}))$$

3 gates here

- AMD's 32-core AMD Epyc processor (2017) has 19B transistors, which is equivalent to 3.16B NAND gates!

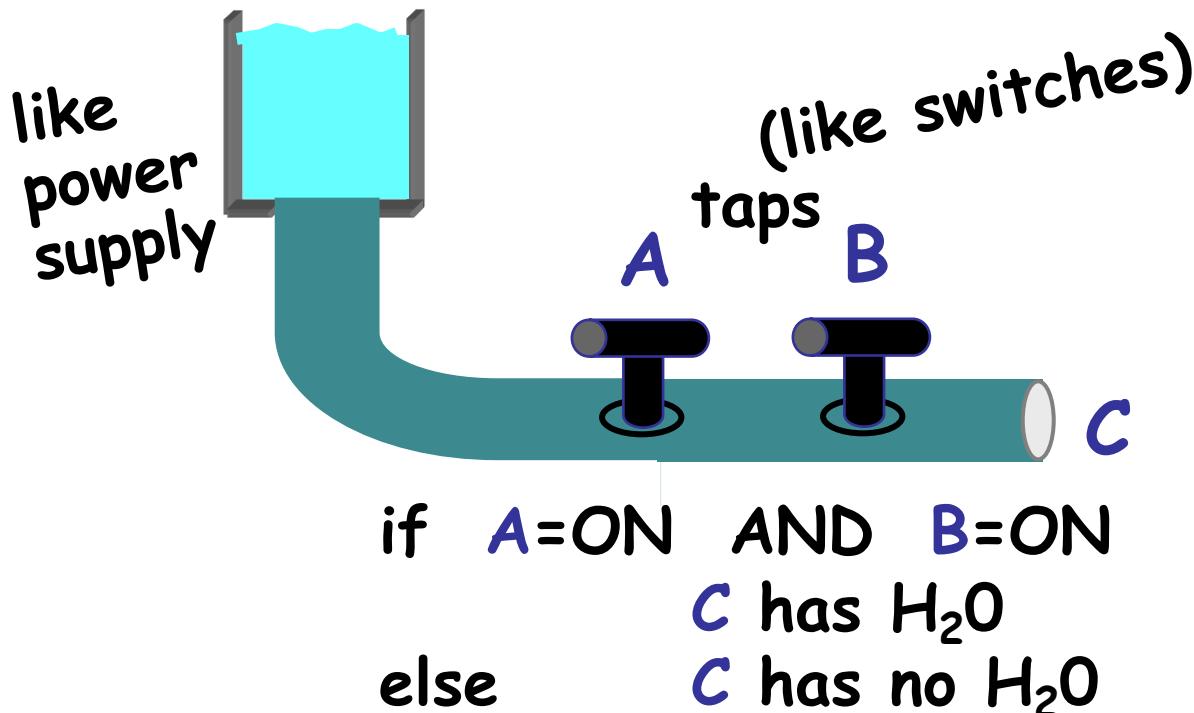
Outline

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How to build a digital gate

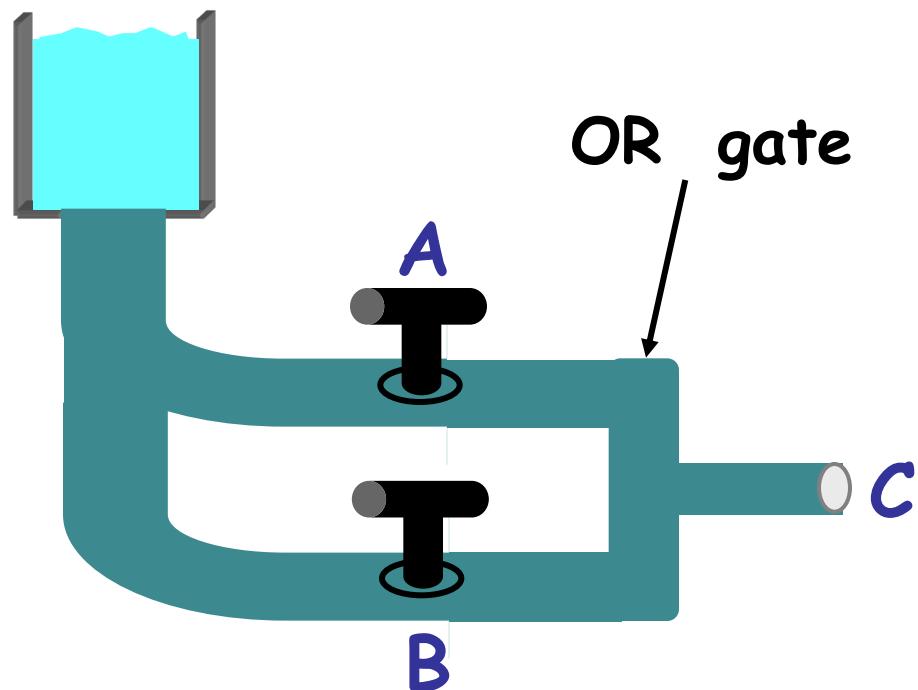
■ Analogy: AND gate



Use this insight to build an AND gate.

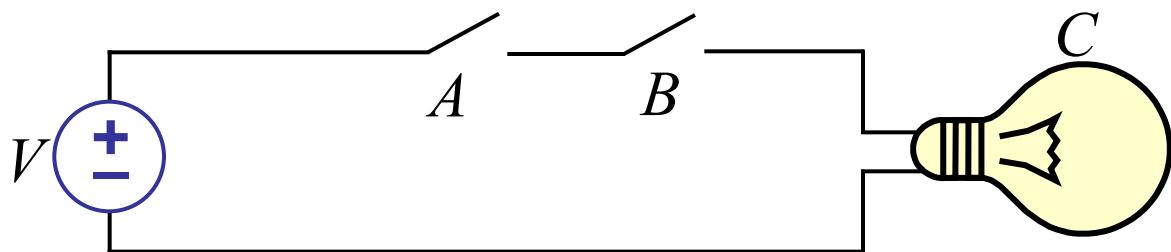
How to build a digital gate

- Analogy: OR gate



How to build a digital gate

■ Electrical Analogy



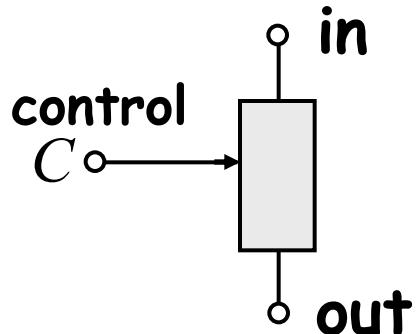
Bulb C is ON if A AND B are ON,
else C is off

Key: “switch” device

How to build a digital gate

- Key: “switch” device

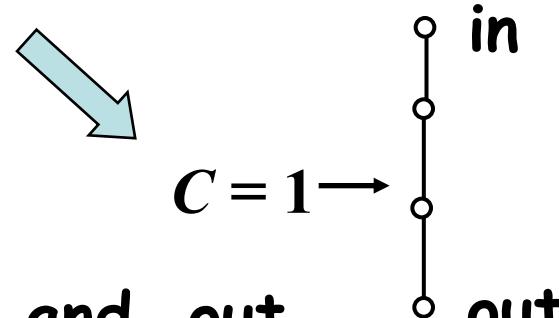
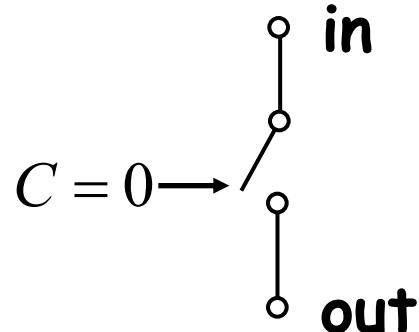
3-Terminal device
if $C = 0$



short circuit between in and out
else
open circuit between in and out

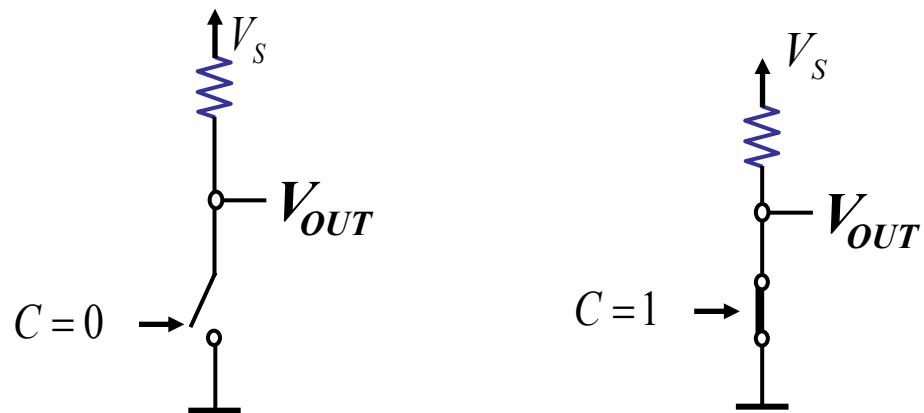
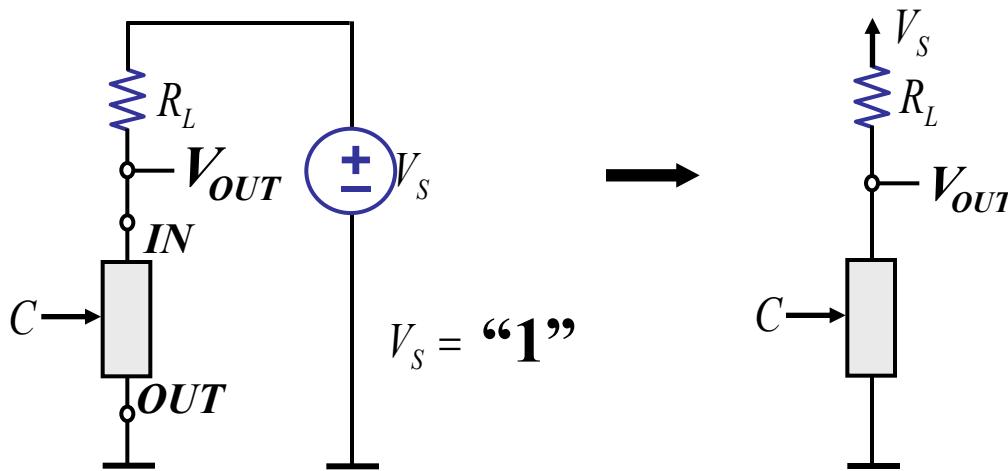
For mechanical switch,
control → mechanical pressure

equivalent ckt

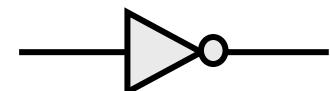


How to build a digital gate

■ Consider



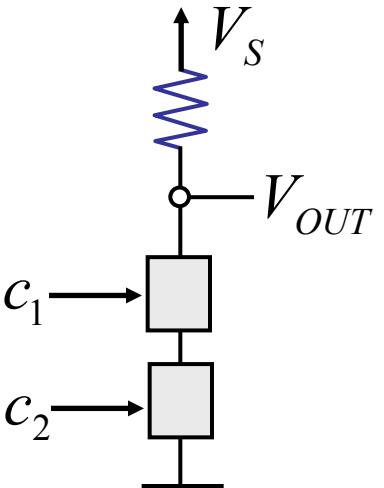
Truth table for



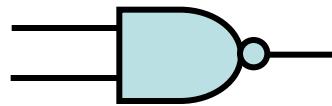
C	V _{OUT}
0	1
1	0

How to build a digital gate

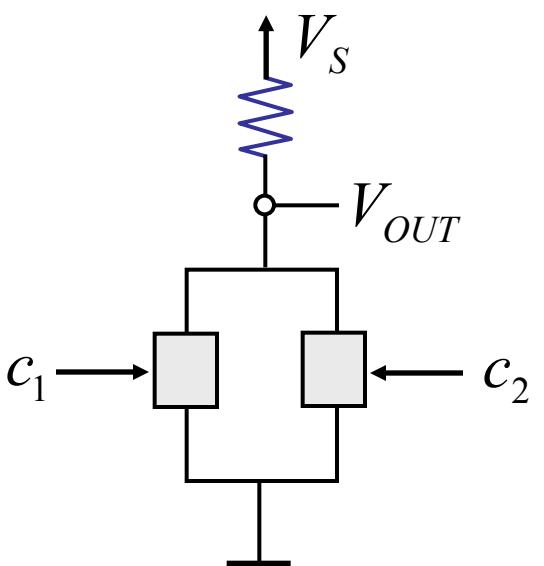
- What about..?



Truth table for



c_1	c_2	V_O
0	0	1
0	1	1
1	0	1
1	1	0



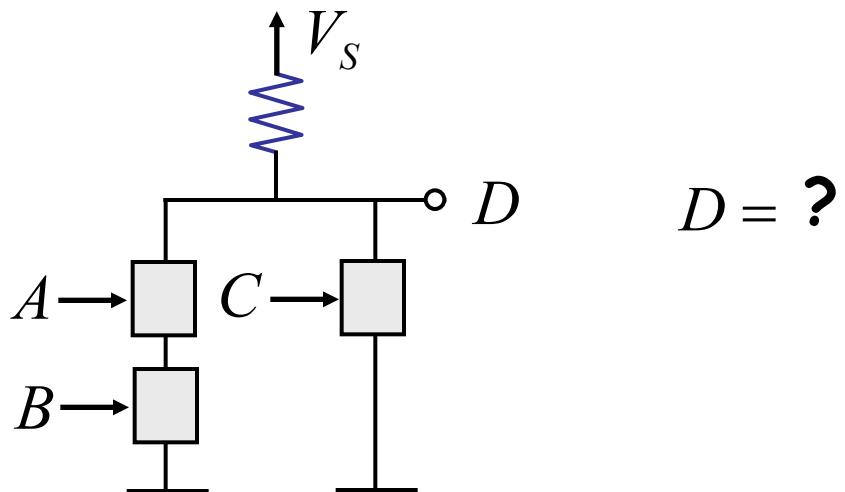
Truth table for



c_1	c_2	V_O
0	0	1
0	1	0
1	0	0
1	1	0

How to build a digital gate

- Can also build compound gates



$$D = ?$$

Exercise

- Draw the following logic circuit:

$$Y = \overline{A(B + C)}$$

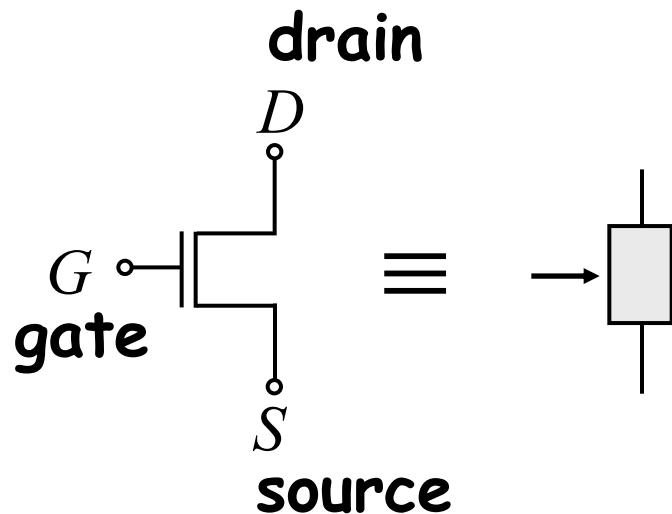
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The MOSFET Device

- MOSFET = Metal-Oxide Semiconductor Field-Effect Transistor



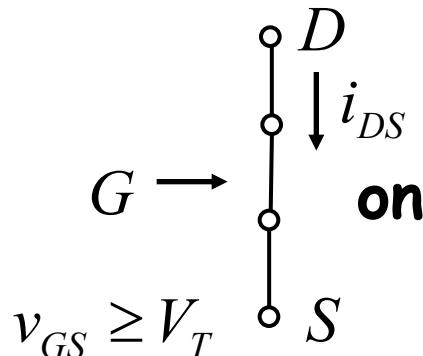
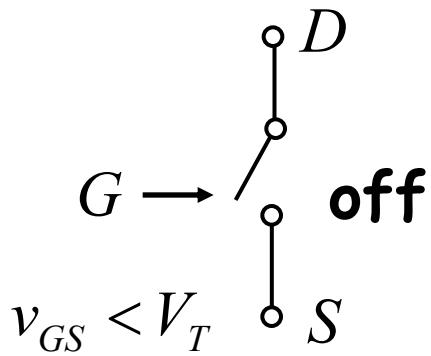
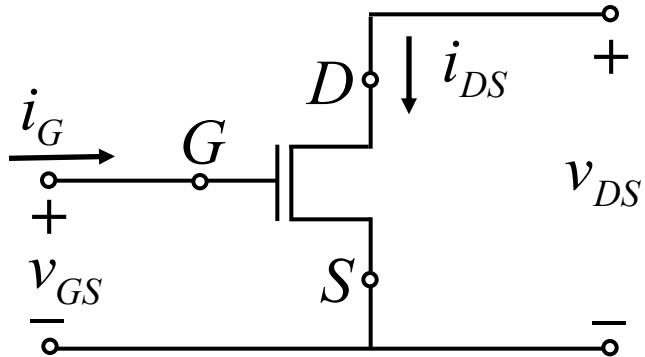
3 terminal lumped element
behaves like a switch

G : control terminal

D, S : behave in a symmetric manner (for our needs)

The MOSFET Device

- Understand its operation by viewing it as a two-port element –



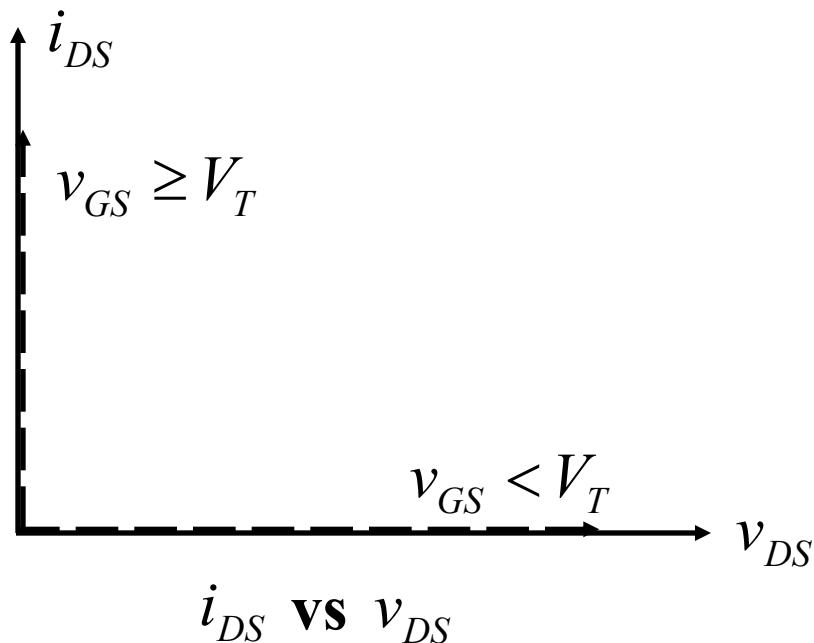
$V_T \approx 1V$ (or less) typically

“Switch” model (S model) of the MOSFET

The MOSFET Device

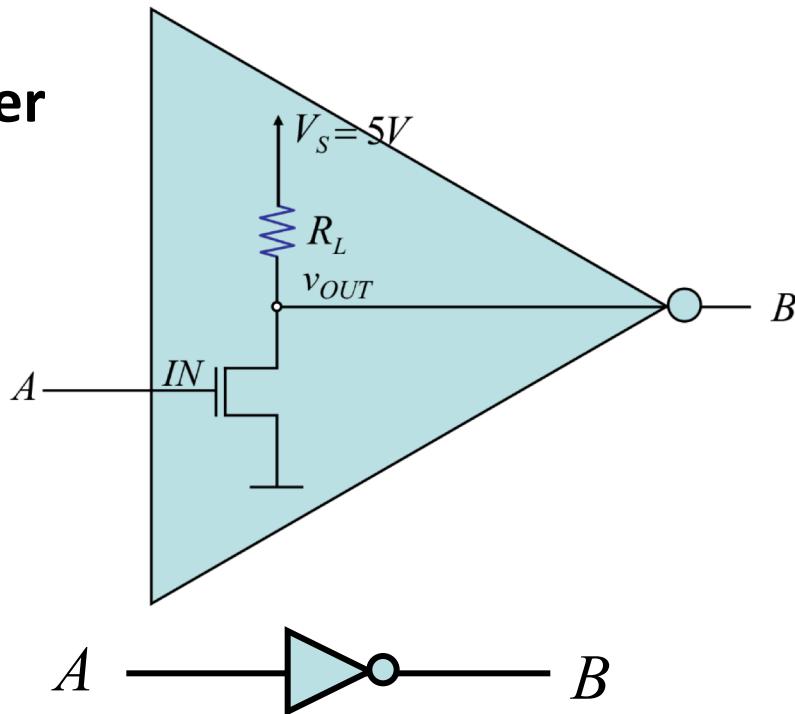
■ S model of the MOSFET: v - i characteristics

- For $v_{GS} < V_T \rightarrow i_{DS} = 0$ (open)
- For $v_{GS} \geq V_T \rightarrow v_{DS} = 0$ (closed)



The MOSFET Device

■ MOSFET Inverter

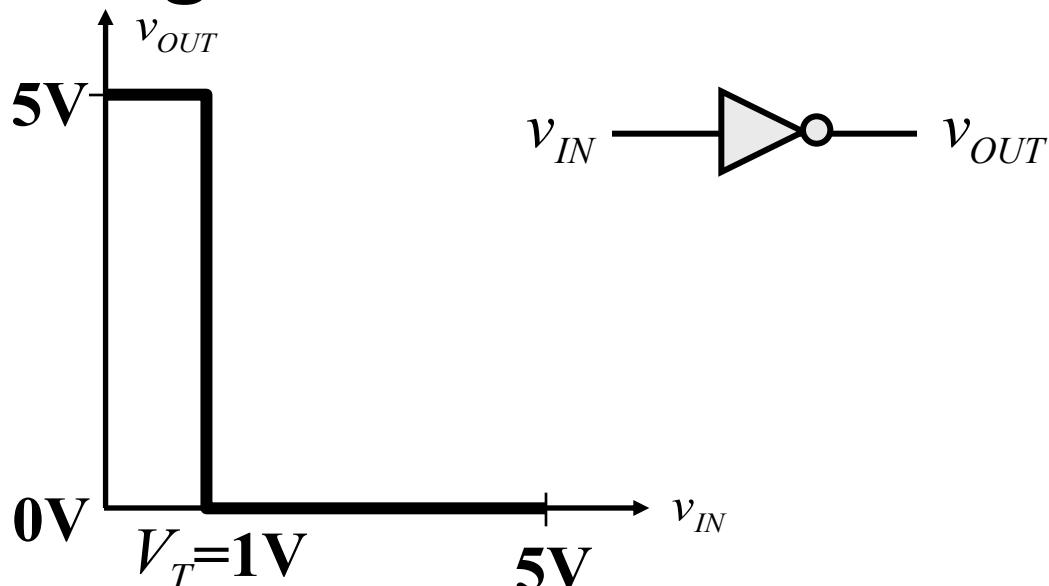


Note the power of abstraction.

The abstract inverter gate representation
hides the internal details such as power
supply connections, R_L , GND, etc.

(When we build digital circuits, the
↑ and ↓ are common across all gates!)

Example: Voltage Transfer Characteristics



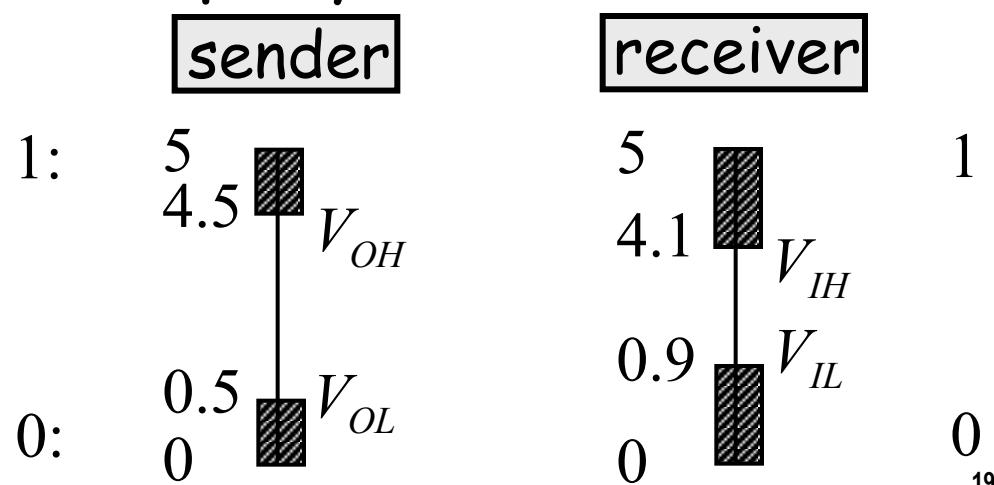
My laptop desires gates that satisfy the static discipline with voltage thresholds. Does our inverter qualify?

$$V_{OL} = 0.5V$$

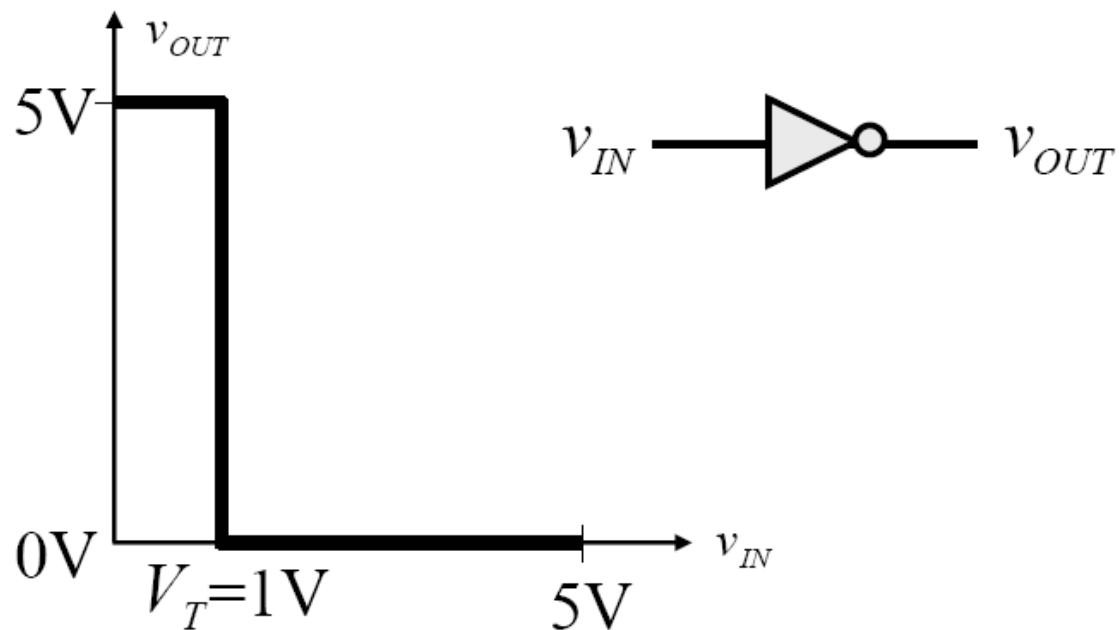
$$V_{OH} = 4.5V$$

$$V_{IL} = 0.9V$$

$$V_{IH} = 4.1V$$



Example: Voltage Transfer Characteristics



■ Example 6.4: Does this case satisfy static discipline?

$$V_{OH} = 4V, \quad V_{OL} = 1V, \quad V_{IH} = 3.5V, \quad V_{IL} = 1.5V$$

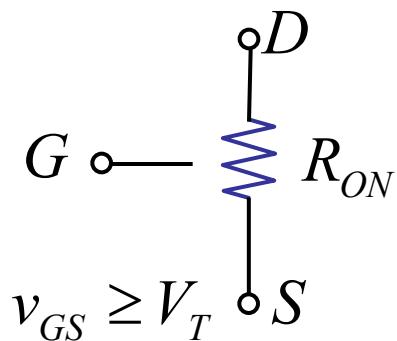
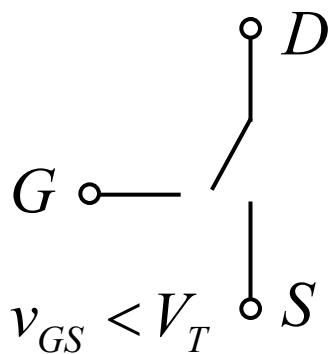
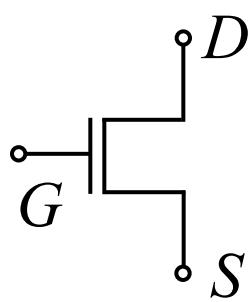
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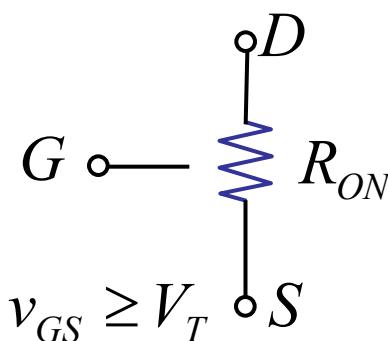
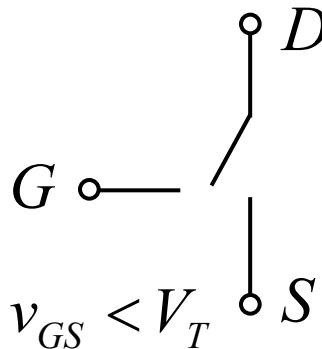
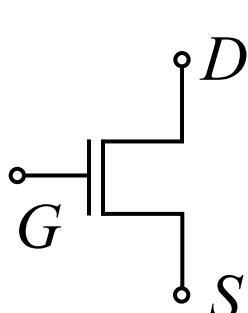
Switch resistor (SR) model of MOSFET

- ...more accurate MOS model

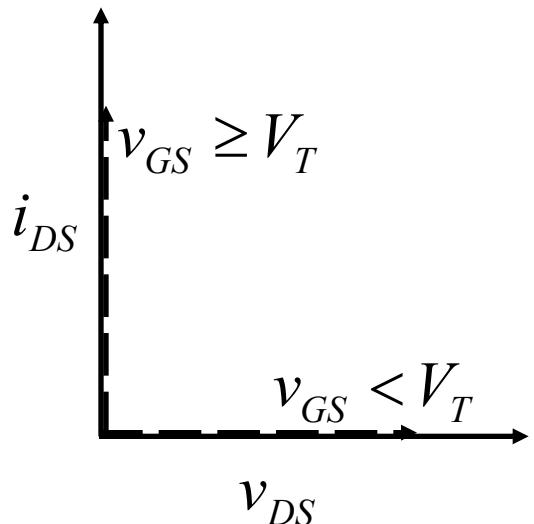


e.g. $R_{ON} = 5K\Omega$

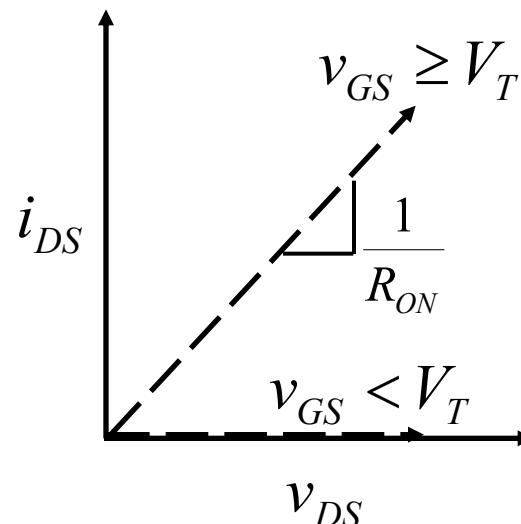
Switch resistor (SR) model of MOSFET



MOSFET
S model

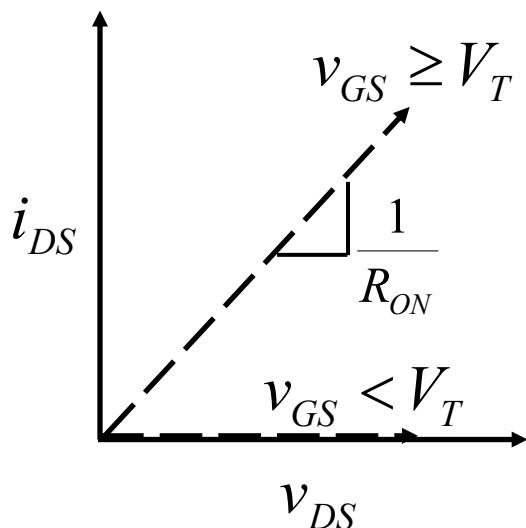


MOSFET
SR model



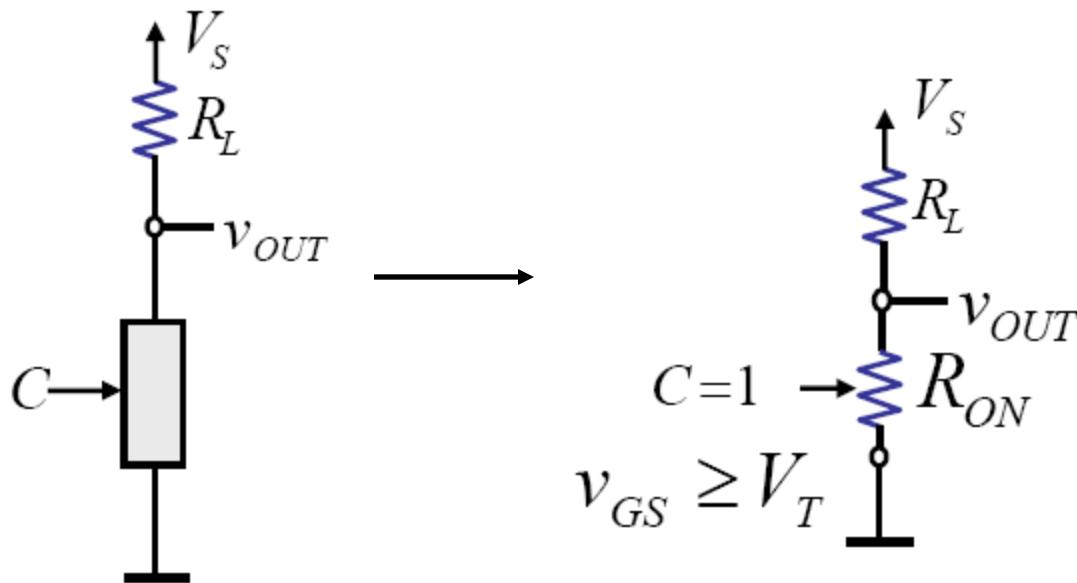
Switch resistor (SR) model of MOSFET

- SR model of the MOSFET: v - i characteristics
 - For $v_{GS} < V_T \rightarrow i_{DS} = 0$ (open)
 - For $v_{GS} \geq V_T \rightarrow i_{DS} = v_{DS}/R_{on}$ (closed with R_{on})
- S model is a special case of SR model with $R_{on} \rightarrow 0$.



Switch resistor (SR) model of MOSFET

■ MOSFET Inverter: Revisited



Choose R_L , R_{ON} , V_S such that:

$$v_{OUT} = \frac{V_S R_{ON}}{R_{ON} + R_L} \leq V_{OL}$$

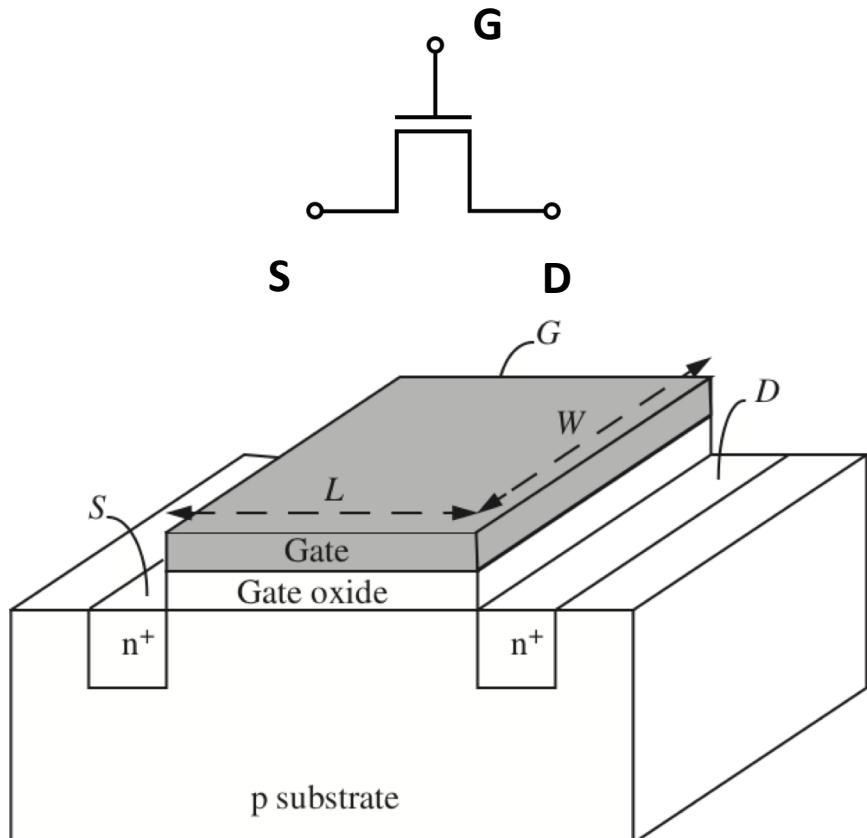
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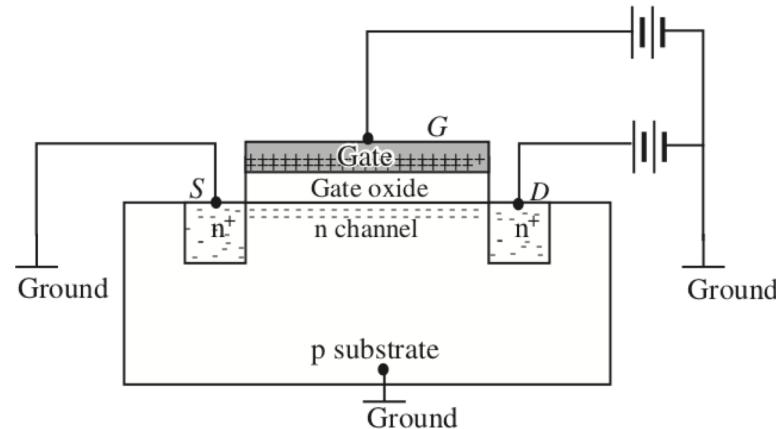
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Physical Structure of MOSFET

- Three dimensional view of n-channel MOSFET (NMOS)



MOSFET operation when a positive gate voltage is applied.



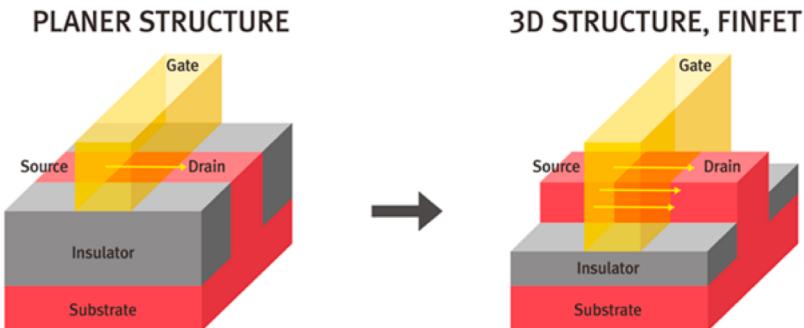
$$R_{ON} = R_n \cdot (L/W)$$

(R_n : resistance per square of NMOS in on state)

Physical Structure of MOSFET

■ A \$400M lawsuit

- US Patent #6885055
“Double-gate FinFET device and fabricating method thereof”
(이중-게이트 FinFET 소자 및 그 제조방법)
- Invented by Prof. Jong Ho LEE @ SNU ECE
- Bulk FinFET technology



전자신문 | etnews

“핀펫 특허 침해한 삼성 4400억원 배상하라” 美배심원 평결

발행일 : 2018.06.16



<이종호 서울대학교 교수.>

삼성전자가 반도체 특허침해로 한국과학기술원(KAIST)에 4억달러(약 4400억 원)를 물어줘야 한다는 미국 배심원단 평결이 나왔다.

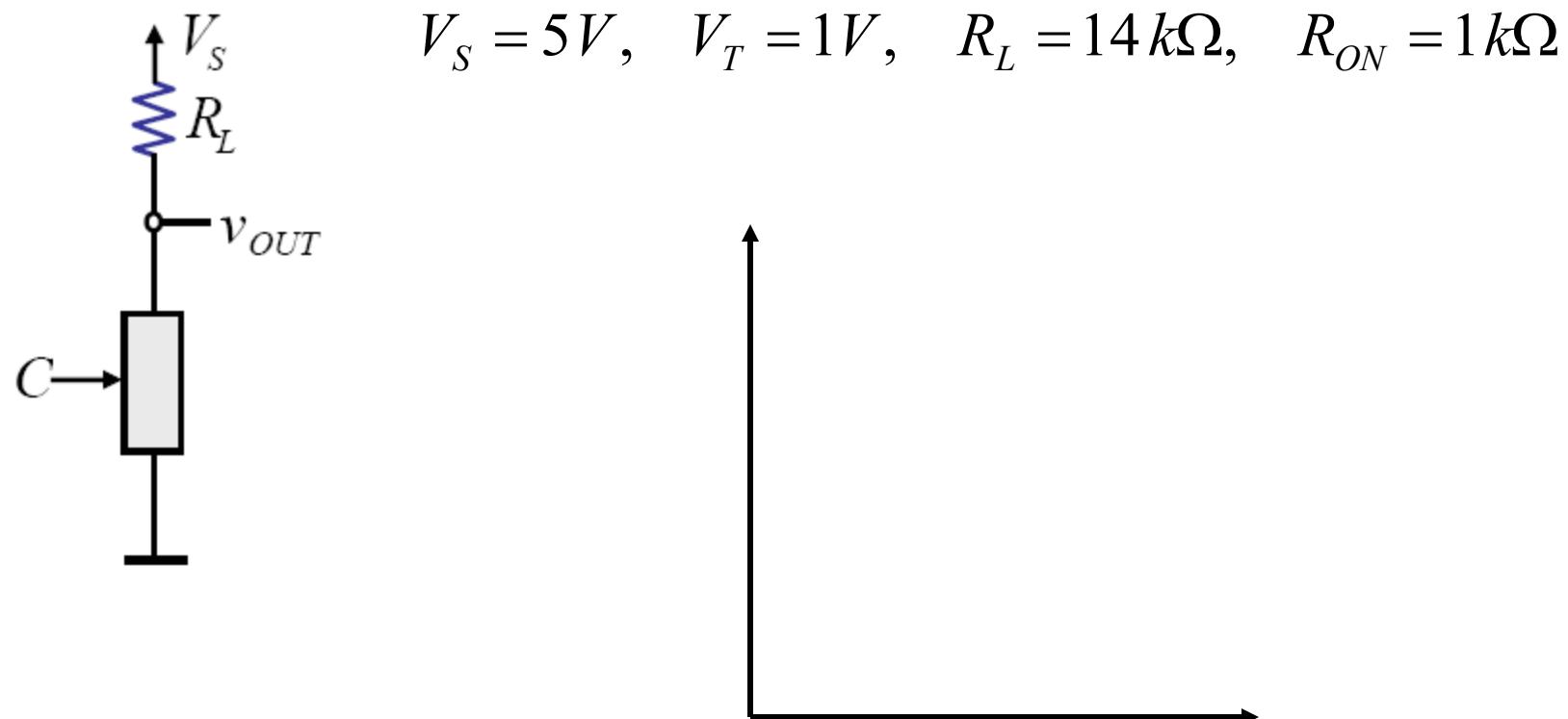
블룸버그는 15일 미국 텍사스 동부지법 1심 배심원단이 이 같은 결론을 내렸다고 보도했다. 문제가 된 기술은 '핀펫(FinFET)'이다. 반도체 칩을 소형화하기 위한 3차원(D) 트랜지스터 설계 구조를 의미한다. 이종호 서울대 전기·정보공학부 교수가 2001년 발명해 2003년 미국에서 특허를 출원했다.

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Inverter Characteristics: SR Model



Example: Switching Analysis of Inverter

- Example 6.5: Determine W/L for correct inverter operation

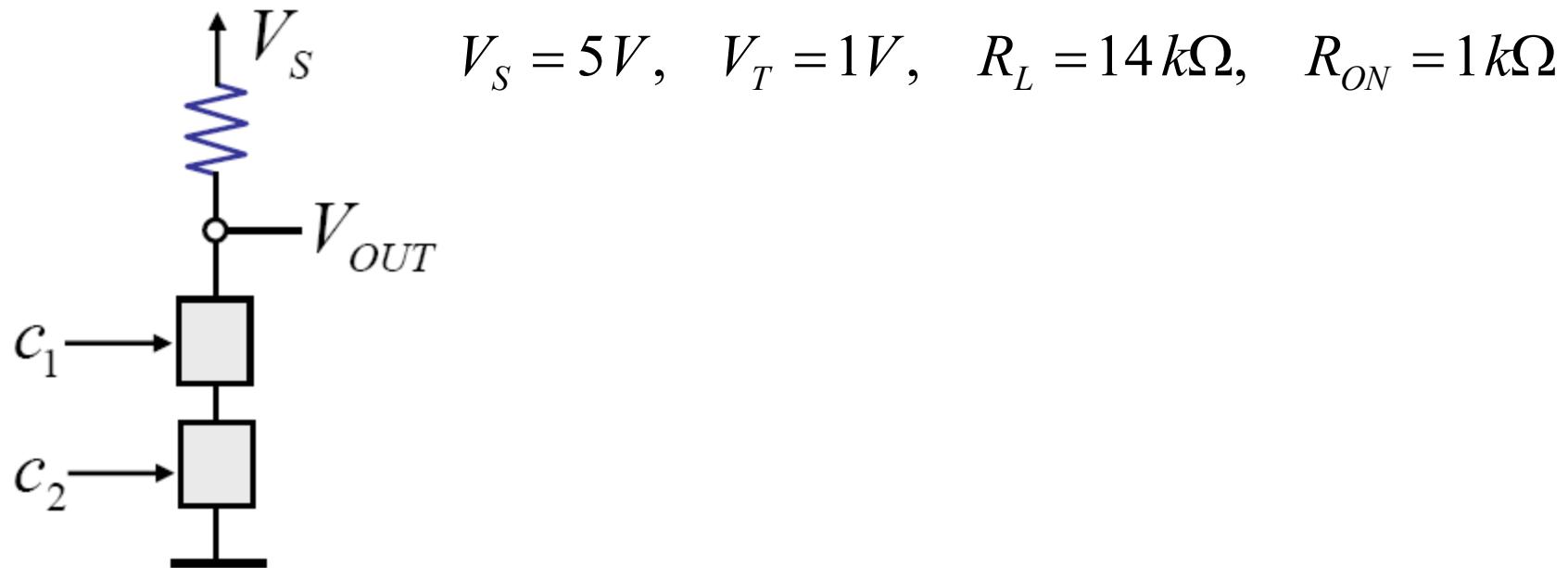
$$V_S = 5V, \quad V_T = 1V, \quad R_L = 10k\Omega, \quad R_n = 5k\Omega$$

Example: Design an Inverter

- Example 6.6: To satisfy the following static discipline redesign the inverter.

$$\begin{aligned}V_{OH} &= 4.5V, & V_{OL} &= 0.2V, & V_{IH} &= 4V, & V_{IL} &= 0.2V \\V_S &= 5V, & V_T &= 1V, & R_L &= 10\text{ k}\Omega, & R_n &= 5\text{ k}\Omega\end{aligned}$$

Static Analysis of NAND Gate: SR Model

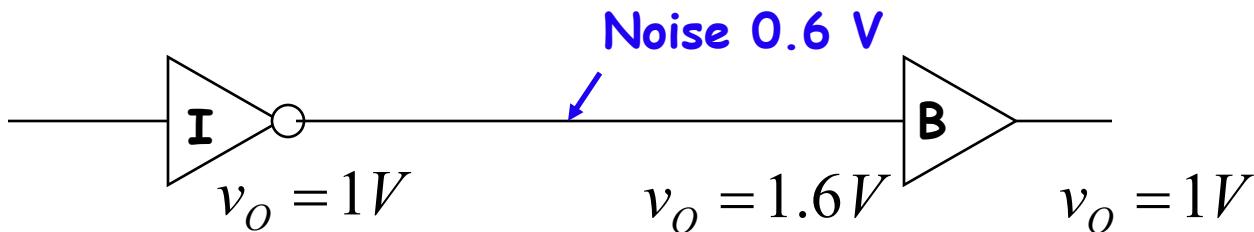


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Signal Restoration and Gain

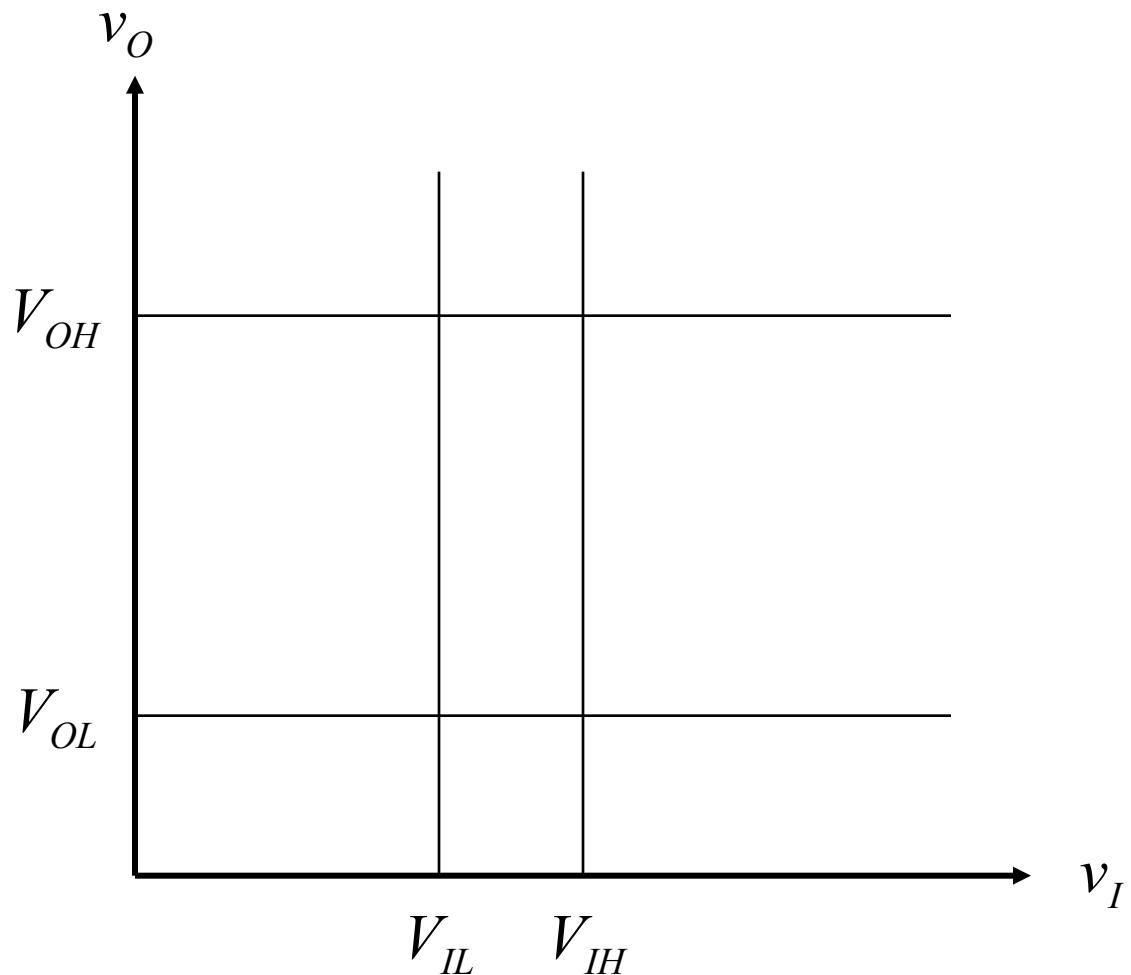


- Buffer restores the signal level (example)

$$V_{IL} = 2V, \quad V_{IH} = 3V, \quad V_{OL} = 1V, \quad V_{OH} = 4V$$

$$\text{Gain} = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}}$$

Buffer Voltage Transfer Characteristics (VTC)



Inverter Voltage Transfer Characteristics (VTC)

