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Energy and Power in Digital Circuits

Lecture 14
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Outline

Textbook: 11.1, 11.2, 11.3, 11.5

- **Power and Energy Relations for Simple RC Curcuit**
- Average Power in an RC Circuit
- Power Dissipation in Logic Gates
- CMOS Logic

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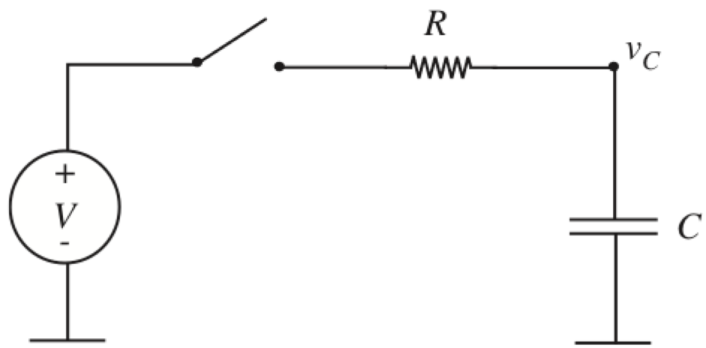
Power/Energy for Simple RC Circuit



- **Power delivered to a two-terminal element at any given instant of time *t***

$$p(t) = v(t)i(t)$$

  - *i(t)* is positive if the current enters into (+) terminal of the element
  - e.g., if both *v(t)* and *i(t)* are positive:
    - A resistor dissipates energy.
    - A capacitor stores energy.

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Power/Energy for Simple RC Circuit

- **Energy supplied by the voltage source over an interval of time 0 → T:**

$$w = \int_0^T p(t)dt.$$

  - Example: if $p(t) = (V^2/R)*e^{-t/RC}$, total energy supplied over time t=0 → ∞:

$$w = \int_{t=0}^{t=\infty} \frac{V^2}{R} e^{\frac{-t}{RC}} dt$$

$$= -\frac{V^2}{R} RC e^{\frac{-t}{RC}} \Big|_{t=0}^{t=\infty}$$

$$= CV^2.$$

    - Half of the energy dissipated by resistor; the other half stored in capacitor ($\frac{1}{2}CV^2$).

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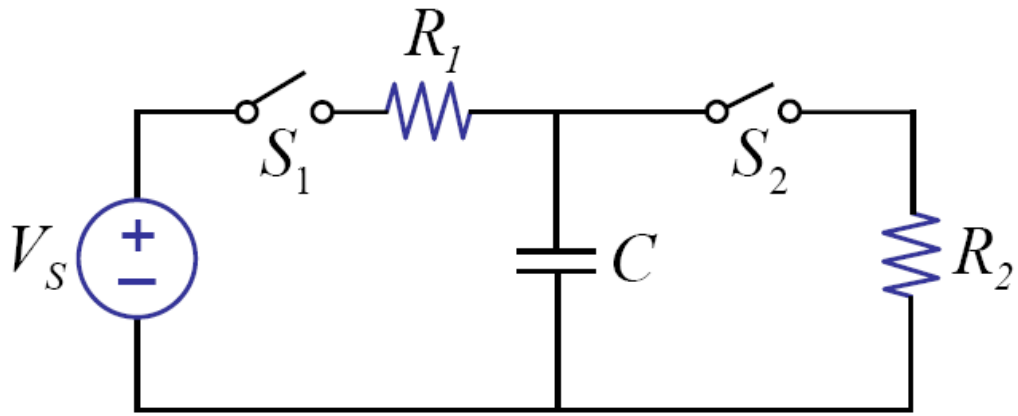
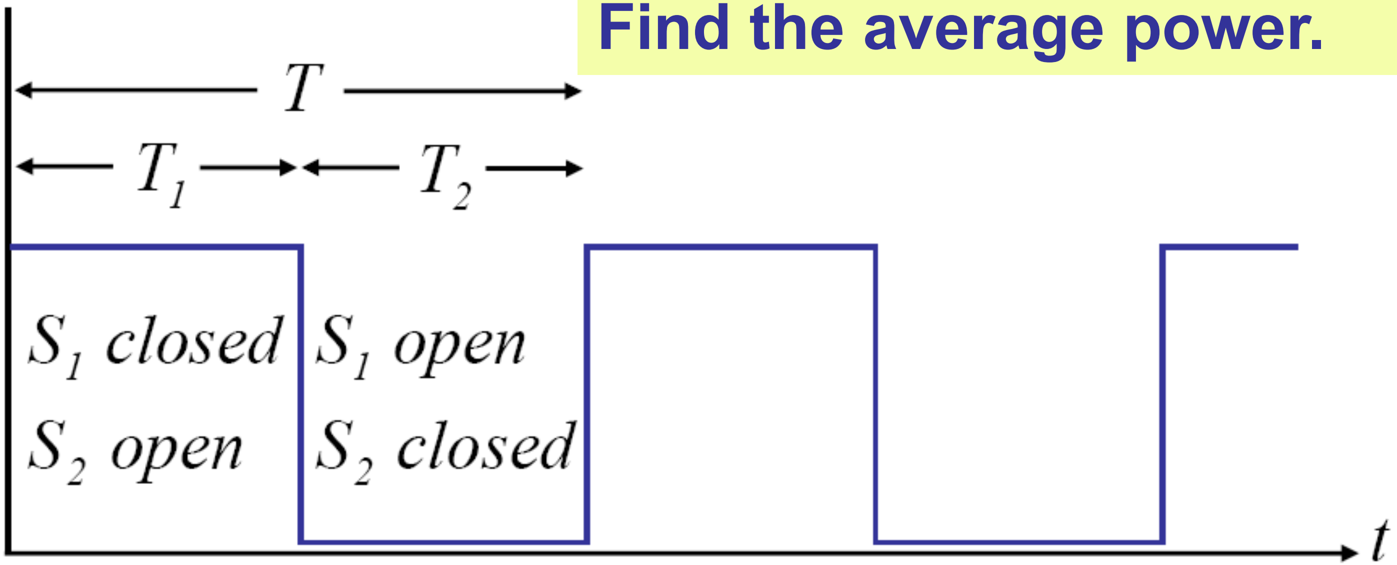
RC Circuit with a Switch



Find energy dissipated in each cycle
Find the average power.



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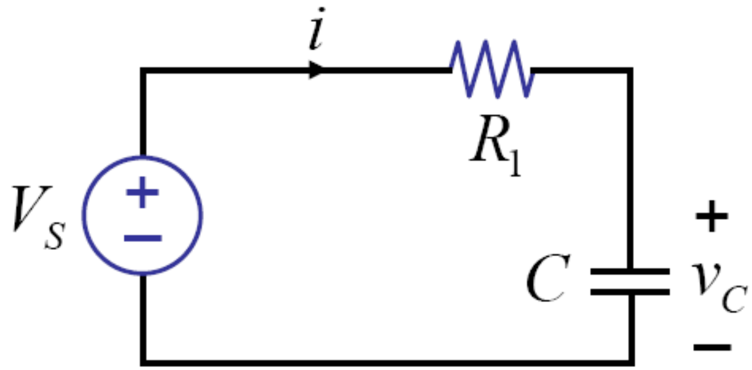
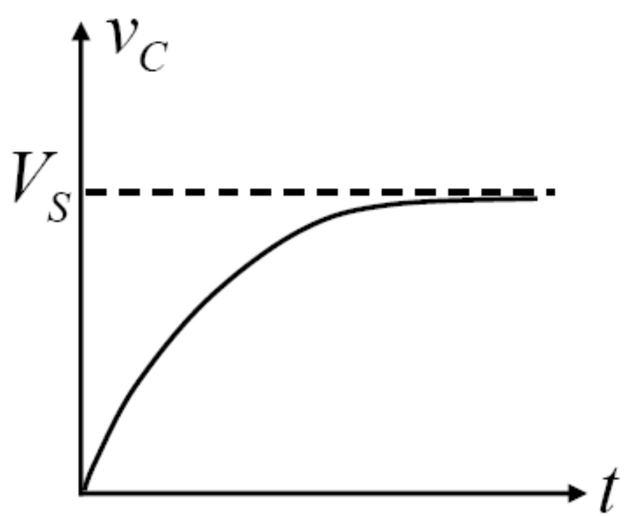
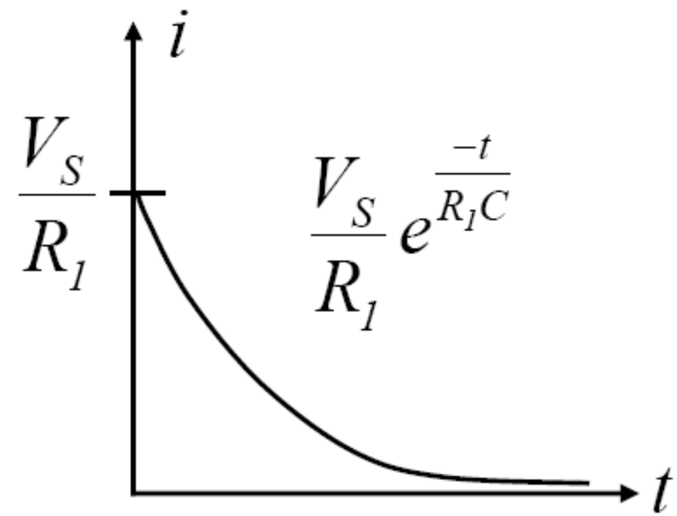
RC Circuit with a Switch

- **During T1**



assume
$v_C = 0$ at $t = 0$





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RC Circuit with a Switch

- **Energy Consumption: Total energy provided by the source during T1**

$$E = \int_0^{T_1} V_S i \, dt = \int_0^{T_1} V_S \frac{V_S}{R_1} e^{-\frac{t}{R_1 C}} dt = C V_S^2 (1 - e^{-\frac{T_1}{R_1 C}})$$

$$\approx C V_S^2 \quad if \quad T_1 >> R_1 C$$

- **Energy stored in the capacitor:** $$E_C = \frac{1}{2} C V_S^2$$

- **Energy dissipated in the resistor:** $$E_1 = \frac{1}{2} C V_S^2$$
  - Independent of R

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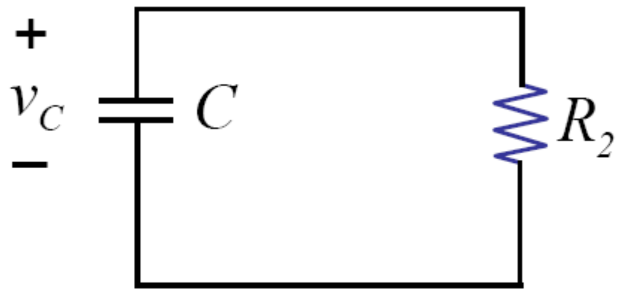
RC Circuit with a Switch

- **During T2**



Initially, $v_C = V_S$ (recall $T_1 >> R_1C$)

If we assume $T_2 >> R_2C$

Capacitor energy is fully discharged =
Energy dissipated by the resister: $E_2 = \frac{1}{2}CV_S^2$
- (again) independent of R

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Putting Together

- **Energy dissipated in each cycle**

$$E = E_1 + E_2 = CV_s^2$$

  - assuming that capacitor is fully charged and discharged during the period.

- **Average power**

$$\overline{P} = \frac{E}{T} = CV_s^2 f$$

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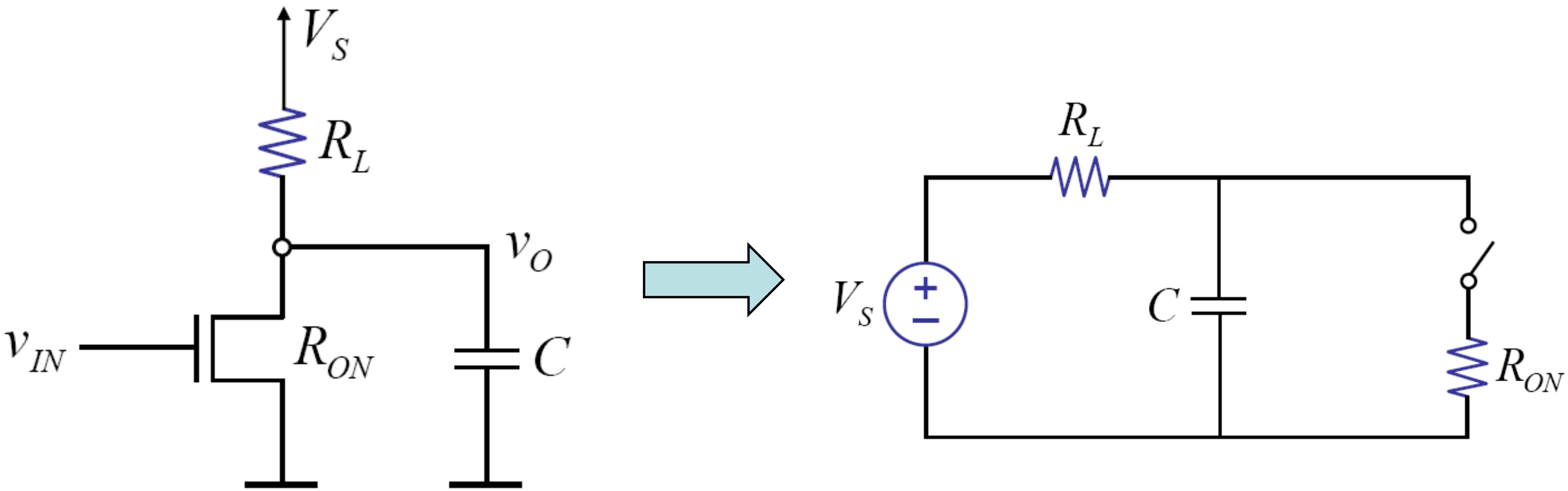
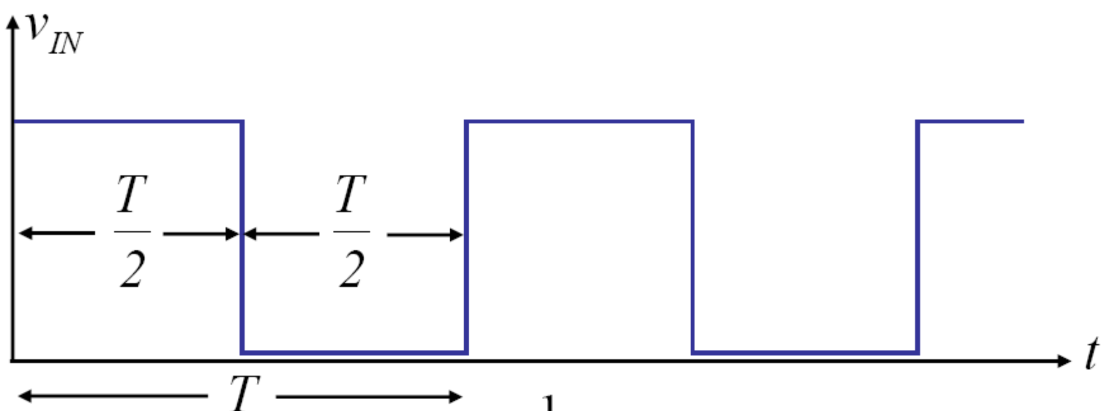
Power Dissipation of Inverter





$$T = \frac{1}{f}$$

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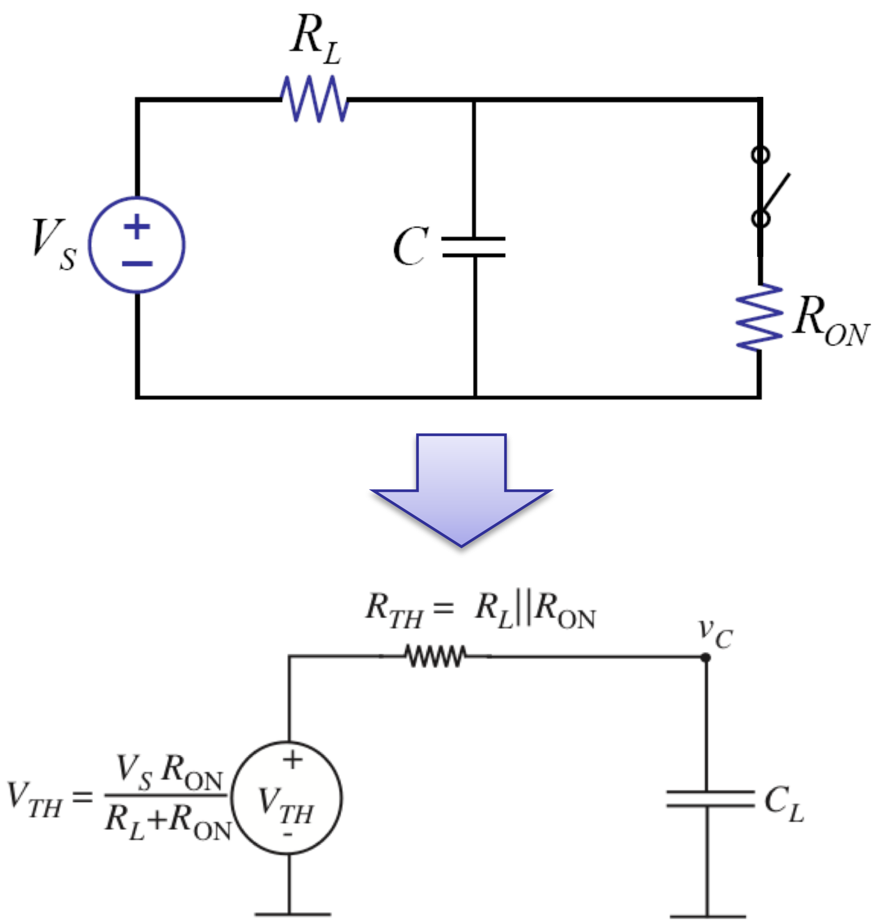
Power Dissipation of Inverter

- **During input is high**



Assuming initial voltage on capacitor is 0:

$$v_C = V_{TH} + (V_S - V_{TH}) e^{\frac{-t}{R_{TH} C_L}}$$

Thus, if T >> $R_{TH}C_L$, the energy consumption w_1

$$w_1 = \frac{V_S^2}{R_L + R_{ON}} T_1 + \frac{V_S^2 R_L^2 C_L}{2(R_L + R_{ON})^2}.$$

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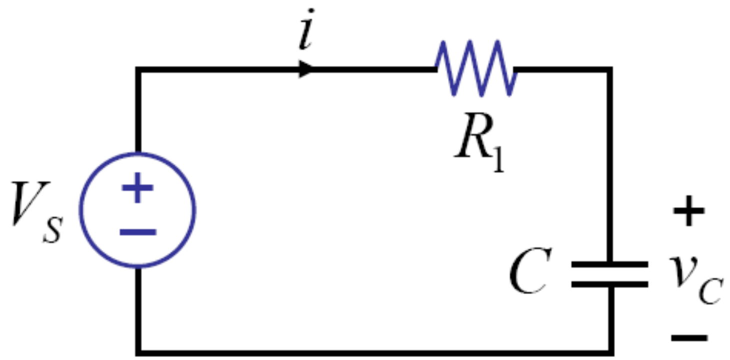
Power Dissipation of Inverter

- **During input is low**



Assuming initial voltage on capacitor is V_{TH} and final voltage of V_S:

$$v_C = V_{TH} + (V_S - V_{TH})\left(1 - e^{\frac{-t}{R_L C_L}}\right)$$

Thus, if T >> $R_L C_L$, the energy consumption w_2

$$w_2 = \frac{V_S^2 R_L^2 C_L}{2(R_L + R_{ON})^2}.$$

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Power Dissipation of Inverter

- **Average power = static power + dynamic power**
  - Static power: independent of the frequency
    - Power loss due to the static or continuous current drawn from the power supply
  - Dynamic power: dependent on the frequency
    - Power loss due to switching currents to charge and discharge capacitors

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Power Dissipation of Inverter

- **Average Power**

$$\overline{P} = \frac{V_S{}^2}{2(R_L + R_{ON})} + CV_S{}^2 f \frac{R_L{}^2}{(R_L + R_{ON})^2} \xrightarrow{R_L >> R_{ON}} \frac{V_S{}^2}{2R_L} + CV_S{}^2 f$$

Static power + dynamic power

✓ Static power: Independent of the switching frequency.

✓ Dynamic power: related to switching capacitor

$$\frac{P_{static}}{P_{dynamic}} = \frac{R_L + R_{ON}}{R_L} \times \frac{T}{2R_L C_L}$$

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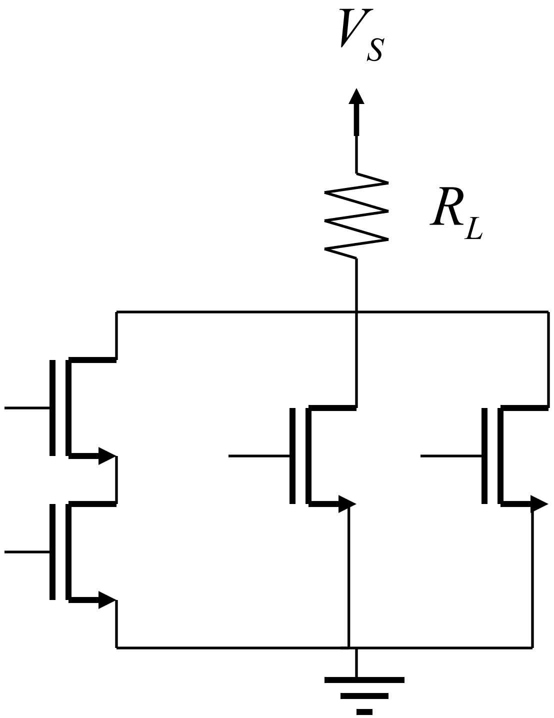
Worst Static Power Dissipation

- **Example 11.1**

$$R_L = 100k\Omega, \qquad R_{ON} = 10k\Omega$$



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Dynamic vs. Static Power

- **Example**

a chip with 10^6 gates clocking at 100 MHZ

$$C = 1\,fF$$
$$R_L = 10\,k\Omega$$
$$f = 100 \times 10^6$$
$$V_S = 5V$$

$$\frac{P_{static}}{P_{dynamic}} = \frac{R_L + R_{ON}}{R_L} \times \frac{T}{2R_L C_L}$$

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Power Minimization

- **Dynamic power**
  - Reduce the supply voltage (5V -> 1.5V)
    - Change the voltage on need
  - Reduce the capacitance
  - Reduce the frequency
    - Turn off clock when not in use

- **Static power**
  - CMOS logic

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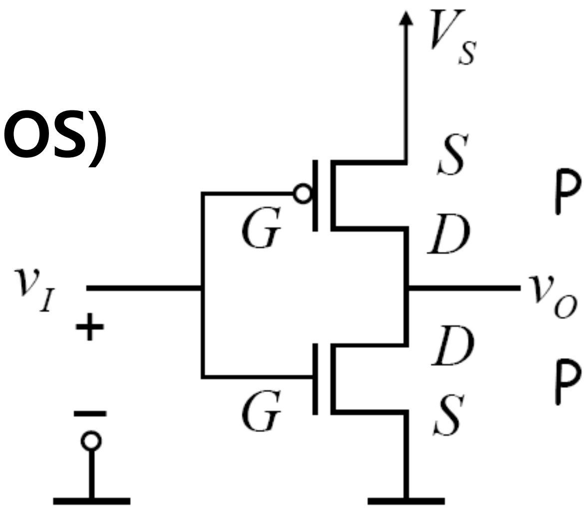
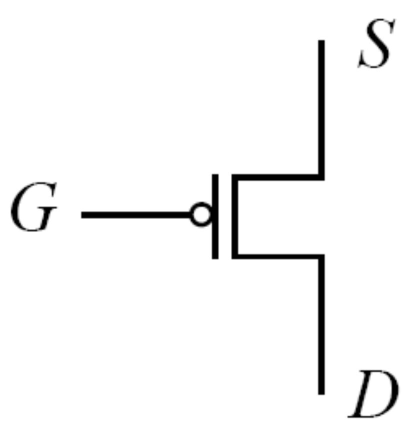
CMOS Logic
(Complementary MOS)



PU = pull up

PD = pull down

PMOS



on when $v_{GS} \leq V_{TP}$

off when $v_{GS} > V_{TP}$

e.g. $V_{TP} = \text{-}1V$

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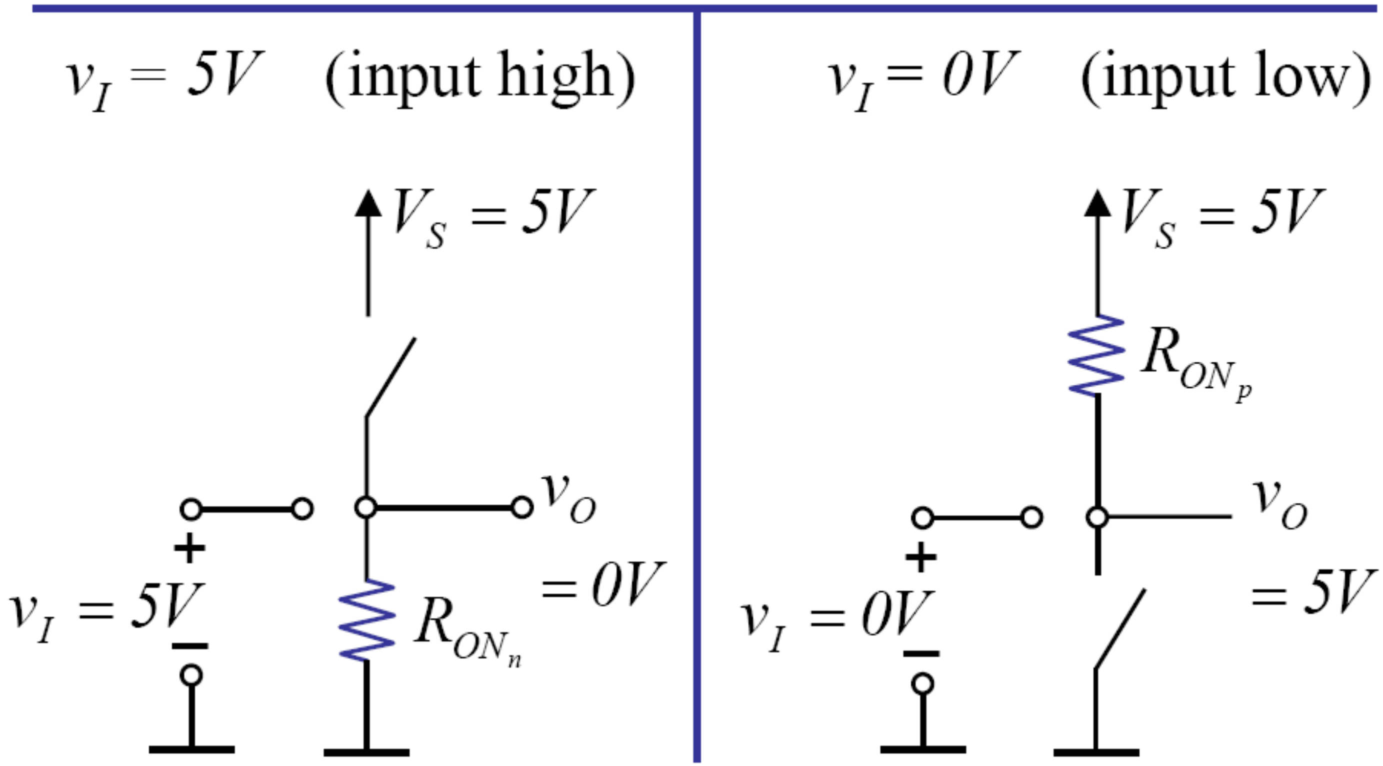
CMOS Inverter



No static power!

- No direct path from the supply to ground

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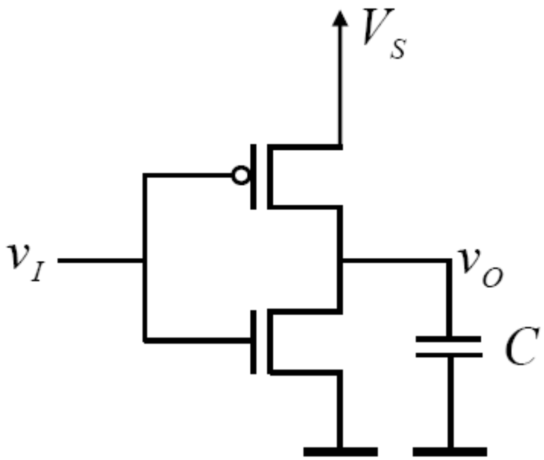
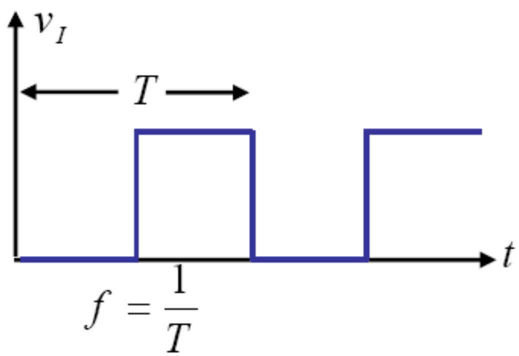
Dynamic Power of CMOS





$$\overline{P} = CV_S^2 f$$

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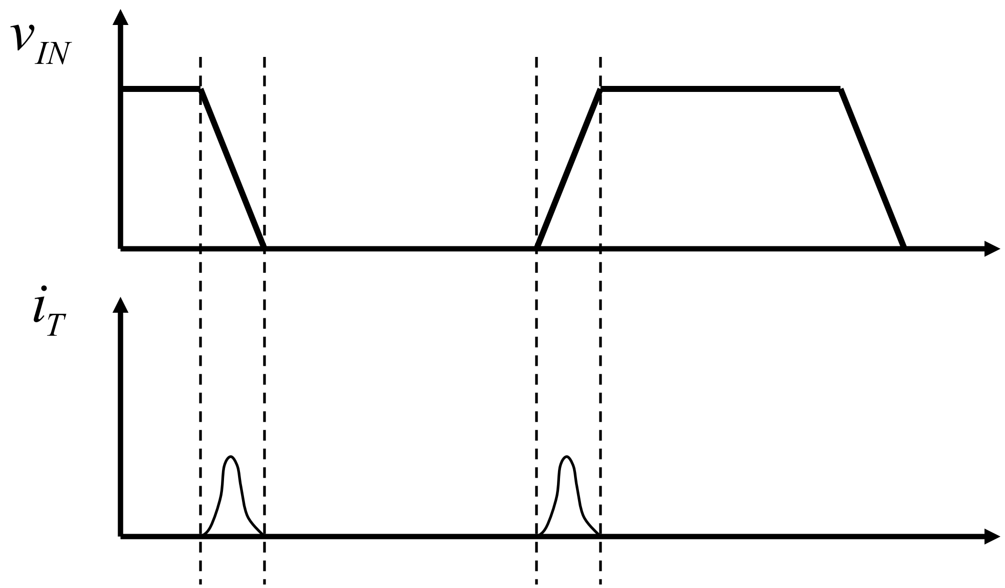
Static Power of CMOS

- Leakage power
- Transient current



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Examples

- Example 11.6: Processor SA27E
  - # of gates = 3M, 25% activity

$$C_L = 30\,fF, \quad V_S = 1.5V, \quad f = 425MHz$$

$$P_{dynamic} = (Fraction\ switching) \times (\#\ gates) \times fC_L V_S^2$$

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Examples

- **Exercise: Estimate the power of the following processor**
  - \# of gates = 25M, 25% activity

$$C_L = 1fF, \quad V_S = 1.5V, \quad f = 3GHz$$

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Summary

- **Total power = static power + dynamic power**
- **CMOS does not exhibit static loss**
- **Dynamic power**

$$P_{dynamic} = (Fraction\ switching) \times (\#\ gates) \times fC_L V_S^2$$

  - Reduce the supply voltage
  - Reduce the switching activities
  - Turn off the logic not in use (clock gating)