하드웨어 시스템 설계 6주차 실습 보고서

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Goal: Implement a simple sequenctial logic (1-sec checker)

Code:

sw2led.v

```
module sw2led(
    input [7:0] SW,
    output [7:0] LD
    );

    assign LD = SW;

endmodule
```

sw2led.xdc

```
set_property PACKAGE_PIN F22 [get_ports {SW[0]}];
set_property PACKAGE_PIN G22 [get_ports {SW[1]}];
set_property PACKAGE_PIN H22 [get_ports {SW[2]}];
set_property PACKAGE_PIN F21 [get_ports {SW[3]}];
set_property PACKAGE_PIN H19 [get_ports {SW[4]}];
set_property PACKAGE_PIN H18 [get_ports {SW[5]}];
set_property PACKAGE_PIN H17 [get_ports {SW[6]}];
```

```
set_property PACKAGE_PIN M15 [get_ports {SW[7]}];
set_property IOSTANDARD LVCMOS25 [get_ports -of_objects [get_iobanks 35]];

set_property PACKAGE_PIN T22 [get_ports {LD[0]}];
set_property PACKAGE_PIN T21 [get_ports {LD[1]}];
set_property PACKAGE_PIN U22 [get_ports {LD[2]}];
set_property PACKAGE_PIN U21 [get_ports {LD[3]}];
set_property PACKAGE_PIN V22 [get_ports {LD[4]}];
set_property PACKAGE_PIN W22 [get_ports {LD[5]}];
set_property PACKAGE_PIN U19 [get_ports {LD[6]}];
set_property PACKAGE_PIN U14 [get_ports {LD[7]}];
set_property IOSTANDARD LVCMOS33 [get_ports -of_objects [get_iobanks 33]];
set_property IOSTANDARD LVCMOS25 [get_ports -of_objects [get_iobanks 34]];
```

sec_checker.v

```
module sec_checker(
    input gclk,
    input rst,
    output [7:0] LD
    );

    reg[26:0] cnt;
    reg[7:0] LD_r;

    assign LD = LD_r;
```

```
    always @(posedge gclk) begin
        if(rst == 1) begin
            cnt <= 27'd100000000;
            LD_r <= 0;
        end
        else if(cnt == 0) begin
            cnt <= 27'd100000000;
            LD_r <= LD_r + 1;
        end
        else begin
            cnt <= cnt - 1;
        end
    end
endmodule
```

sec_checker.xdc

```
set_property PACKAGE_PIN Y9 [get_ports {gclk}];
set_property PACKAGE_PIN P16 [get_ports {rst}];
set_property IOSTANDARD LVCMOS33 [get_ports -of_objects [get_iobanks 13]];

set_property PACKAGE_PIN T22 [get_ports {LD[0]}];
set_property PACKAGE_PIN T21 [get_ports {LD[1]}];
set_property PACKAGE_PIN U22 [get_ports {LD[2]}];
set_property PACKAGE_PIN U21 [get_ports {LD[3]}];
```

```
set_property PACKAGE_PIN V22 [get_ports {LD[4]}];

set_property PACKAGE_PIN W22 [get_ports {LD[5]}];

set_property PACKAGE_PIN U19 [get_ports {LD[6]}];

set_property PACKAGE_PIN U14 [get_ports {LD[7]}];

set_property IOSTANDARD LVCMOS33 [get_ports -of_objects [get_iobanks 33]];

set_property IOSTANDARD LVCMOS25 [get_ports -of_objects [get_iobanks 34]];
```

Discussion:

gclk = 100MHz, 즉 1 초에 1 억번 진동하므로 down-counter 를 1 억으로 설정해주었고, center_pushbutton 을 reset 으로 사용하여 down-counter 와 up-counter 를 리셋하게 구현하였습니다.