### Lab. 01

Logic Design Lab.
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### **Contents**

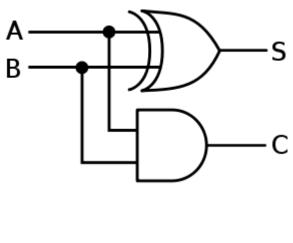
### What you will learn:

- Combinational / Sequential logic circuit
- Soldering / Prototyping
- Schematic Design
- Hardware Description Language (Verilog)
- Hardware Simulation
- Field-programmable Gate Array (FPGA) Programming

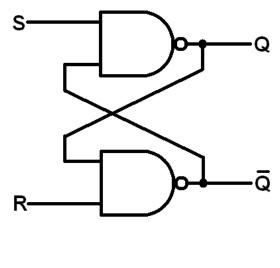
### Final Project

#### Practice Guideline

### Combinational and sequential logic circuit



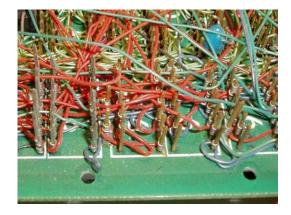




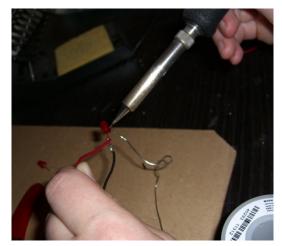
<SR Latch>

### Soldering and prototyping

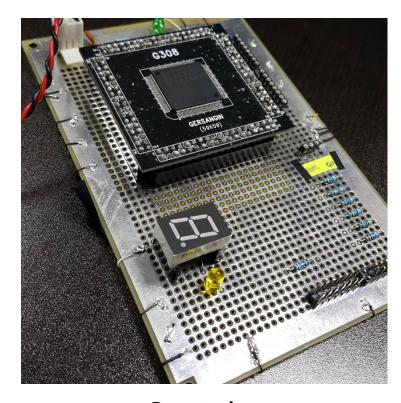
Wire wrapping







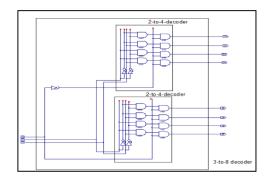




**Prototyping** 

### Computer Aided Design

#### **Schematic Design**

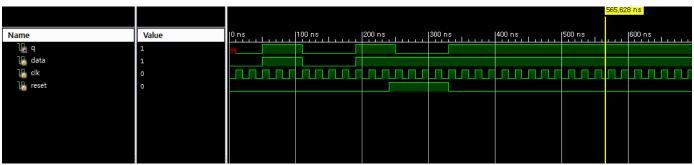


#### **Hardware Description Language**

```
module seq_test_module(data, clk, reset, q);
  input data, clk, reset;
  output q;
  reg q;

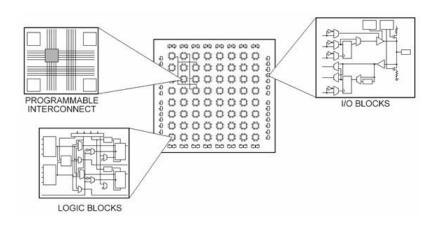
always @ (posedge clk)
  begin
    if (reset == 1)
        q <= 0;
    else
        q <= data;
  end
endmodule</pre>
```





**Hardware Simulation** 

Field Programmable Gate Array (FPGA)
 Programming

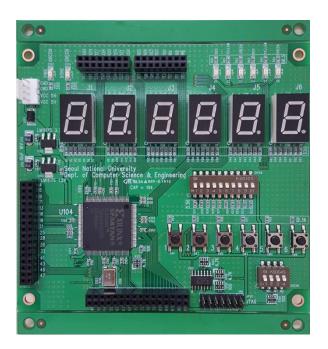




# Final Project

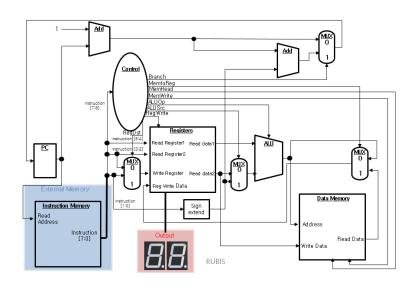
## Final Project

### You will be given:



<Custom-made logic design board>

### You will have to make:

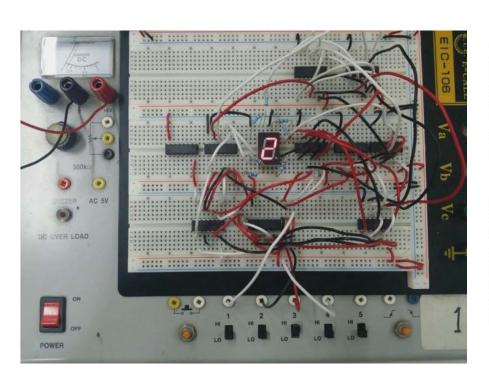


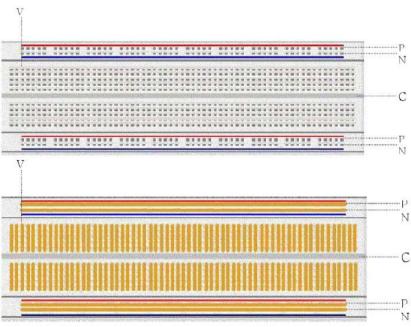
<Microprocessor>

## Practice Guideline

### Breadboard

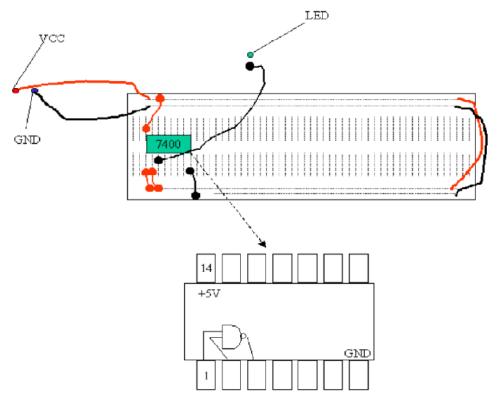
#### Breadboard





## Breadboard (Continued)

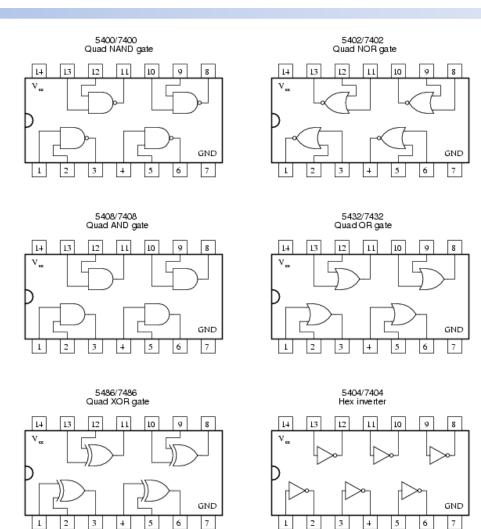
### Implementation guide



✓ A circuit using 7400 Quad 2-Input NAND gate is constructed on the bread board

## Logic Gates

### Logic Gates



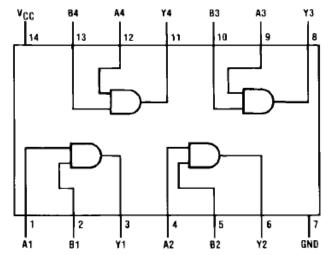
### Practice with a breadboard

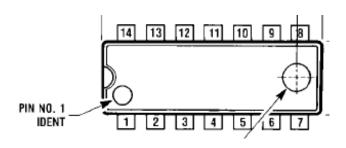
#### 2-Input AND Gate (7408)

$$Y = A \cdot B$$

Inputs		Output
Α	В	Υ
0	0	0
0	1	0
1	0	0
1	1	1

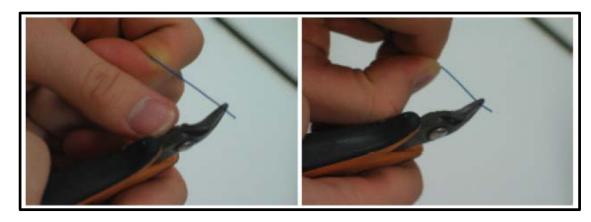
#### **Connection Diagram**





### Tools

### Bead Nipper



Ripping off coating

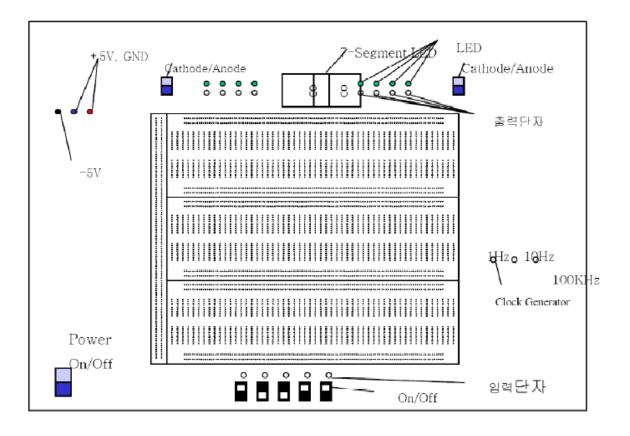
### Extracting chips

- To extract IC chips, use IC Chip extractor.
- Never extract chips using your hand



### Lab Unit

#### Lab Unit



## **Power Supply**

- Set current and voltage
  - Maximum allowed current
  - Supplied voltage
- Always supply 5V.



## Questions