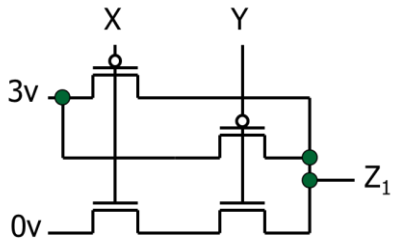
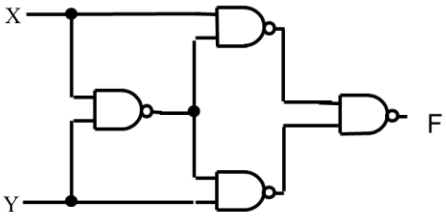
Logic design, mid-term, Oct. 31, 2012. 11am-noon

1. How can you express Z1 in a Boolean expression of inputs X and Y? Here, 3V is high voltage (TRUE) and 0V is low voltage (FALSE). (10p)



2. Represent output F in terms of Boolean expression. Then check whether F is equivalent to a certain logic gate of two inputs X and Y. (15p)



3. Use a Boolean cube to minimize the function F(A,B,C) = Σm(3,5,6,7). (15p)

4. Explain function1 in the Verilog code below. (15p)

```
module function1 (out, a, b);
  input          a, b;
  output         out;
  reg            out;
  always @(a or b) begin
     #6 out = a ^ b;
  end
endmodule
```

5. F(A,B,C) = Σm(0,2,6,7). Implement function F by using 4:1 MUX. Also, draw the internal logic of 4:1 MUX. (20p)

6. Design a 4-bit adder/subtractor system that carries out A+B and A-B. For instance, the 4 bits of B are denoted by B3, B2, B1, and B0, where B3 is MSB and B0 is LSB. Use modules of 1-bit full adders and 2:1 MUXs. That is, the internal logic of a full adder and a MUX need not be drawn. Note that 2s complement is used for -B. Inputs are 4 bits of A, B, B', Control bit (0: ADD, 1: SUBTRACT). Outputs are 4 bits of S (sum) and Overflow bit. (25p)