

Logic Design

Midterm Exam

Autumn 2014

2014/10/21

07:00 P.M. – 08:15 P.M.

Total: 135 points

Read Me First

1. Cheating on exam is a serious matter. If caught, you will get an “F” for the course.
(부정 행위 시에는 **F** 학점으로 처리됨.)
2. Some questions have several subproblems. Make sure that you put all the answers for the subproblems in one place on your answer sheet.
(답은 읽기 쉽게 깨끗하게 작성 하고 한 문제에 해당 하는 답은 반드시 한 곳에 모아서 작성 할 것.)

PROBLEM 1. [10]

There may be more than one minimum product-of-sums form for a given Boolean expression. Demonstrate this by drawing a four-variable Karnaugh map that has two different minimum product-of-sums forms for the same Boolean expression, each with the same number of product terms with the same number of literals.

PROBLEM 2. [12]

Decide if the following statement is true or false. If your answer is false, *argue* why the statement is not true. (If the answer is false but you didn't provide enough argument to justify your answer, you will get no point.) If your answer is true, explain why it is true.

- (a) [4] Any Boolean function expressed in sum of products form can be implemented using demultiplexors only.
- (b) [4] Tri-state gates are useful in building glitch-free circuits.
- (c) [4] A 1:2 decoder can be implemented using 2 transmission gates + some inverters.

PROBLEM 3. [10]

Fill in the blank with the correct answer.

- (a) [5] If you were to build a 64:1 mux from 4:1 muxes, you would need ___ 4:1 muxes.
- (b) [5] In implementing two-input two-stack AOI gate, x normally open switches and x normally closed switches are required. The smallest x is _____.

PROBLEM 4. [10]

- (a) [5] Given $X(A, B, C, D, E) = \sum m(1, 3, 4, 6, 10, 11, 13, 14, 18, 25)$ and $Y(A, B, C, D, E) = \sum m(1, 2, 4, 8, 9, 10, 13, 16, 17, 18, 25, 26, 29)$, find the minterm expansion of XY .
- (b) [5] Given $X(A, B, C, D, E) = \prod M(1, 3, 4, 6, 10, 11, 13, 14, 18, 25)$ and $Y(A, B, C, D, E) = \prod M(1, 2, 4, 8, 9, 10, 13, 16, 17, 18, 25, 26, 29)$, find the maxterm expansion of XY .

PROBLEM 5. [20]

The truth table for a 1-bit half subtractor computing $D(\text{ifference}) = A - B$ with BL (borrow from left) is given as follows (where (A, B) are inputs, and (D, BL) are outputs):

A	B	D	BL
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

- (a) [5] Show a truth table for a 1-bit full subtractor with two data inputs (A, B), a borrow from the right input (BR), a borrow request to the left output (BL), and a difference output (D).
- (b) [5] Find a minimum product of sums for BL.
- (c) [10] Show how your design of a 1-bit full subtractor can be cascaded to form a 4-bit binary subtractor. Demonstrate a proper working of your subtractor using $A = 0101$ and $B = 0011$.

PROBLEM 6. [10]

- (a) [5] Implement $F(A, B, C) = m_0 + m_2 + m_6 + m_7$ using a 4:1 multiplexer.
- (b) [5] Implement the two-input XOR function using a two-input two-stack AOI gate. (We assume that complemented input variables are available for free.)

PROBLEM 7. [10]

R-S latches are said to have a race condition. Explain what the race condition is in general, and describe when the race condition occurs in the R-S latch. Assume that the R-S latch is implemented by using cross-coupled NOR gates.

PROBLEM 8. [18]

- (a) [10] Prove that $F(x_1, x_2, \dots, x_n, 0, 1, +, \bullet)^D = F(x_1', x_2', \dots, x_n', 0, 1, +, \bullet)$.
- (b) [8] A self-dual logic function is a function F such that $F = F^D$. Argue if there exists a **two-input** logic function which is self-dual. (Note that x, y, x', y' are not strictly two-input logic functions. Logic functions with explicitly two inputs such as xy and $x+y'$ are considered strictly two-input logic functions.)

PROBLEM 9. [15]

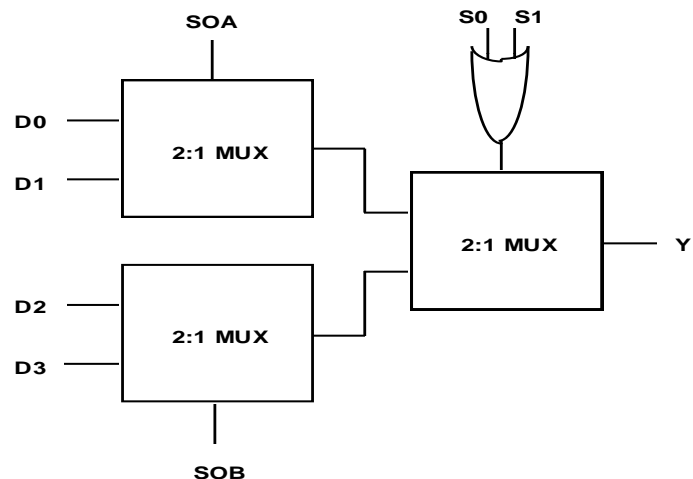
Fill in the following table. Assume that f is a function of three variables.

	Maxterm expansion of f	Minterm expansion of f'	Maxterm expansion of f'
$f = \sum m(3, 4, 5, 6, 7)$	(a) [5]	(b) [5]	(c) [5]

PROBLEM 10. [12]

You were asked to implement different functions using the following modified 4:1 mux. Show that how $D0$, $D1$, $D2$, $D3$, SOA , SOB , $S0$ and $S1$ should be configured to implement the following functions:

- (a) [6] A two-input (A , B) NAND gate when $S0 = A$ and $SOB = B$
- (b) [6] $Y = AB + AC + BC$ when $S0 = A$ and $SOB = B$

**PROBLEM 11. [8]**

Find the minimized product-of-sums for the following functions:

- (a) [4] $X(A, B, C, D) = \sum m(1, 3, 5, 7, 9) + \sum d(6, 12, 13)$
- (b) [4] $Y(A, B, C, D) = \sum m(1, 7, 11, 13) + \sum d(0, 5, 10, 15)$