Logic Design

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Professor

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Course Information

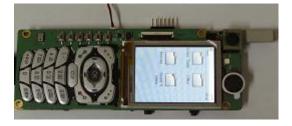
- Class Meeting Times: Tue/Thur 3:30pm 4:45pm
- Lab. Sessions: Tue 7:00pm 8:50pm
- Office Hour: Tue 12:30 1:30pm at 301-409 (Lunch will be served by appointment)
 - come to me pretty often
- Textbook: Contemporary Logic Design, 2nd Edition: Randy H. Katz and Gaetano Borriello
- Contact:
 - Chang-Gun Lee (cglee@snu.ac.kr, 880-1862, 010-6549-5605)
 - TA: WonJae Jang (<u>ta@rubis.snu.ac.kr</u>)
 - Course Website: http://rubis.snu.ac.kr
- Grading (Tentative)
 - Active participation: 10%
 - Homework & Projects: 30%
 - Midterm: 30%
 - Final: 30%

Course Philosophy

- Digital Logic Design is the base for many digital systems
 - Digital watch
 - DVD players
 - Cell Phones
 - Computers







- Students will be trained with
 - How to make digital systems from simple gates
 - How to optimize the design
 - How to validate your design
 - How to design digital systems just like SW programming

Topics

- CMOS basics
- Simple Gates (AND, OR, NOT, NAND, NOR)
- Combinational Logic Design
- Sequential Logic Design
- Hardware Description Language

Before We Start Passive vs. Active Learning

- After 2 weeks, we tend to remember
- Passive learning
 - 10% of what we read
 - 20% of what we hear
 - 30% of what we see (picture)
 - 50% of what we hear and see
- Active learning
 - 70% of what we say
 - 90% of what we say and do

Everybody! be an Active Learner

- recall prior material
- answer a question (say a lot!)
- guess the solution first (even guessing wrong will help you to remember the right approach)
- raise questions
- think of application
- imagine that you were the professor and think about how you would give a test on the subject material so that key concepts and results will be checked
- summarize a lecture, a set of homework or a lab in your own words concisely

An Active Learner will become an Independent Researcher and Engineer

Engineering Ethics

• Something to say....