In Lab:

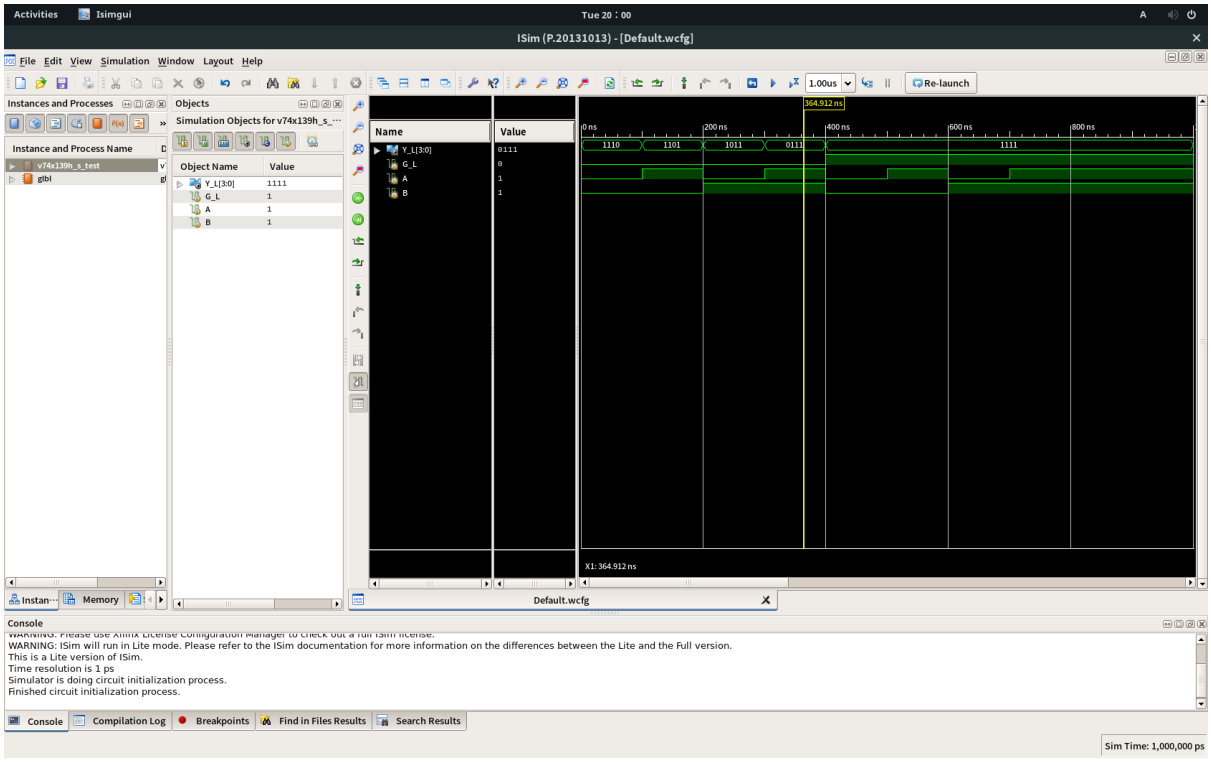
1. Structural description을 이용해 half 74x139를 디자인하고 실행해보았다.

코드:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:       19:55:07 04/03/2018
// Design Name:
// Module Name:       v74x139h_s
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module v74x139h_s(
      input G_L,
      input A,
```

```
    input B,
    output [3:0] Y_L
    );

        wire N_A, N_B, G;

        not T1(G, G_L);
        not T2(N_A, A);
        not T3(N_B, B);

        nand T4(Y_L[0], G, N_A, N_B);
        nand T5(Y_L[1], G, A, N_B);
        nand T6(Y_L[2], G, N_A, B);
        nand T7(Y_L[3], G, A, B);

endmodule
```

사진:


Activities
Isimgui
Tue 20 : 00
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Objects
Simulation Objects for v74x139h_s_...
Instance and Process Name
v74x139h_s_test
glbl
Object Name
Value
Y_L[3:0]
1111
G_L
1
A
1
B
1
Name
Value
Y_L[3:0]
0111
G_L
0
A
1
B
1
364.912 ns
0 ns
200 ns
400 ns
600 ns
800 ns
1110
1101
1011
0111
1111
X1: 364.912 ns
Memory
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps

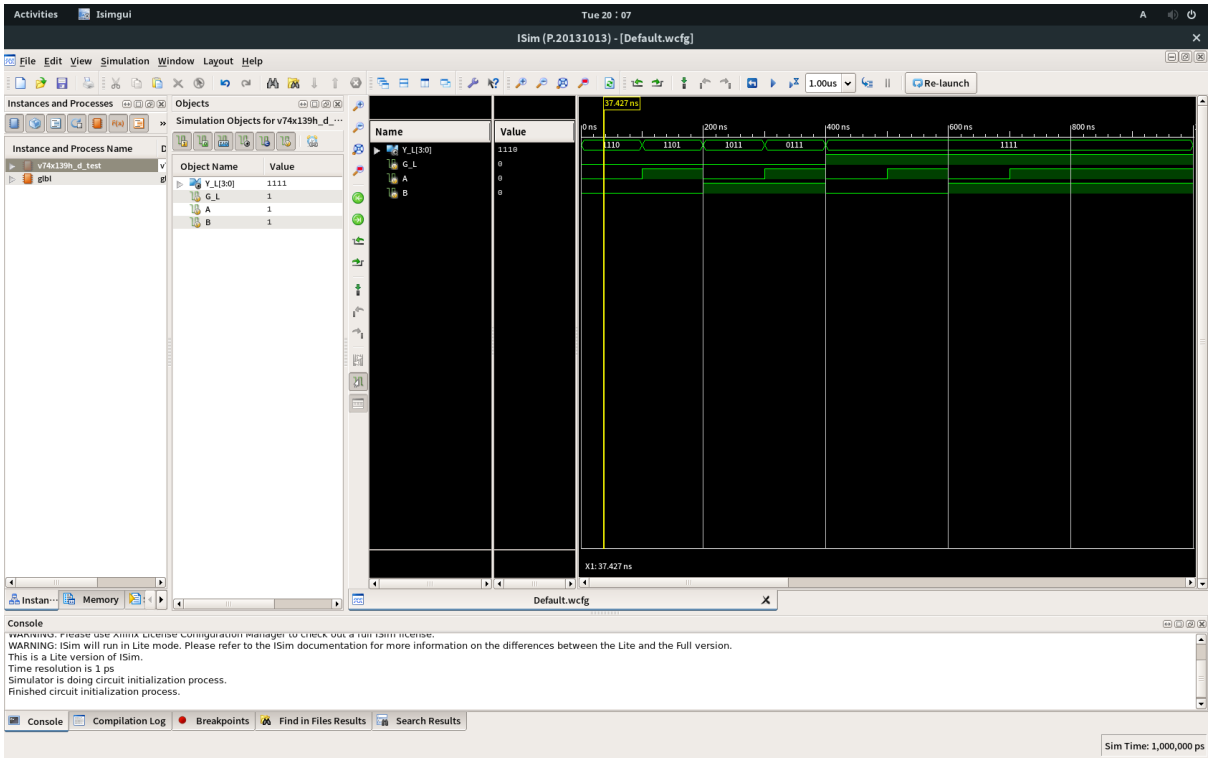
2. Data flow description을 이용해 half 74x139를 디자인하고 실행해보았다.

코드:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:       20:02:45 04/03/2018
// Design Name:
// Module Name:       v74x139h_d
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module v74x139h_d(
      input G_L,
      input A,
      input B,
```

```
    output [3:0] Y_L
    );

        wire [1:0] sel;
        wire [3:0] out;

        assign sel = {B, A};
        assign Y_L = ~out;

        assign out = (sel == 2'b00 && G_L == 1'b0) ? 4'b0001 :
                                                     (sel == 2'b01 && G_L == 1'b0) ? 4'b0010 :
                                                     (sel == 2'b10 && G_L == 1'b0) ? 4'b0100 :
                                                     (sel == 2'b11 && G_L == 1'b0) ? 4'b1000 :
                                                     4'b0000;

endmodule
```

사진:


Activities
Isimgui
Tue 20 : 07
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Instance and Process Name
v74x139h_d_test
glbl
Objects
Simulation Objects for v74x139h_d_...
Object Name
Value
Y_L[3:0]
1111
G_L
1
A
1
B
1
Name
Value
Y_L[3:0]
1110
G_L
0
A
0
B
0
37.427 ns
0 ns
200 ns
400 ns
600 ns
800 ns
1110
1101
1011
0111
1111
X1: 37.427 ns
Memory
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps

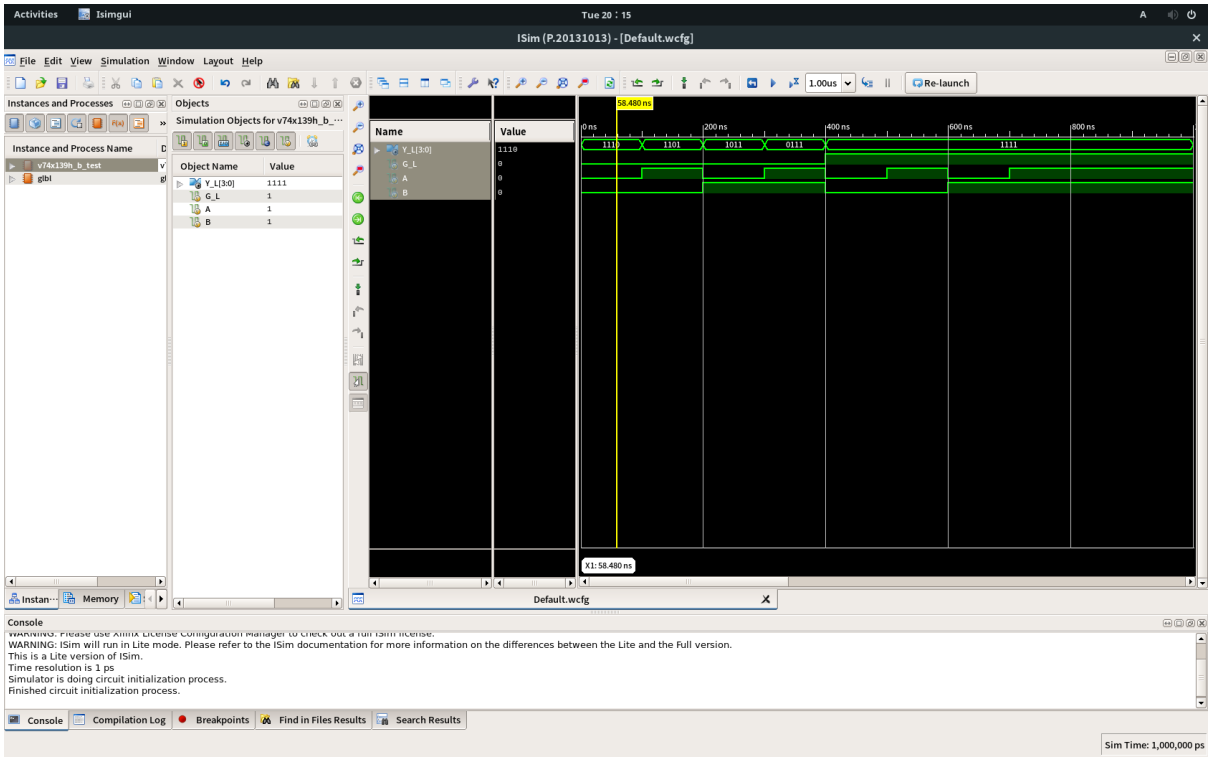
3. Behavioral description을 이용해 half 74x139를 디자인하고 실행해보았다.

코드:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:       20:09:31 04/03/2018
// Design Name:
// Module Name:       v74x139h_b
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module v74x139h_b(
      input G_L,
      input A,
      input B,
```

```
    output [3:0] Y_L
    );

        wire [1:0] sel;
        reg [3:0] out;

        assign sel = {B, A};
        assign Y_L = ~out;

        always@(G_L or sel)
            begin
                if (G_L == 1'b0)
                    begin
                        case(sel)
                            2'b00 : out = 4'b0001;
                            2'b01 : out = 4'b0010;
                            2'b10 : out = 4'b0100;
                            2'b11 : out = 4'b1000;
                        endcase
                    end
                else
                    begin
                        out = 4'b0000;
                    end
            end
endmodule
```

사진:


Activities
Isimgui
Tue 20 : 15
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Objects
Simulation Objects for v74x139h_b_...
Instance and Process Name
v74x139h_b_test
glbl
Object Name
Value
Y_L[3:0]
1111
G_L
1
A
1
B
1
Name
Value
Y_L[3:0]
1110
G_L
0
A
0
B
0
58.480 ns
0 ns
200 ns
400 ns
600 ns
800 ns
1110
1101
1011
0111
1111
X1: 58.480 ns
Default.wcfg
Console
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps

부록 1. half 74x139의 테스트코드: 세 종류 모두 동일한 테스트코드 사용

```
`timescale 1ns / 1ps


////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:     19:56:26 04/03/2018
// Design Name:     v74x139h_s
// Module Name:     /csehome/pistolstar1797/v74x139/v74x139h_s_test.v
// Project Name:    v74x139
// Target Device:
// Tool versions:
// Description:
//
// Verilog Test Fixture created by ISE for module: v74x139h_s
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////////////


module v74x139h_s_test;
```

```
// Inputs
reg G_L;
reg A;
reg B;

// Outputs
wire [3:0] Y_L;

// Instantiate the Unit Under Test (UUT)
v74x139h_s uut (
	.G_L(G_L),
	.A(A),
	.B(B),
	.Y_L(Y_L)
);

initial begin
	// Initialize Inputs
	G_L = 0;
	A = 0;
	B = 0;

	// Wait 100 ns for global reset to finish
	#100;
```

```
        // Add stimulus here
        G_L = 0;
        A = 1;
        B = 0;

        #100 G_L = 0; A = 0; B = 1;

        #100 G_L = 0; A = 1; B = 1;

        #100 G_L = 1; A = 0; B = 0;

        #100 G_L = 1; A = 1; B = 0;

        #100 G_L = 1; A = 0; B = 1;

        #100 G_L = 1; A = 1; B = 1;

    end

endmodule
```

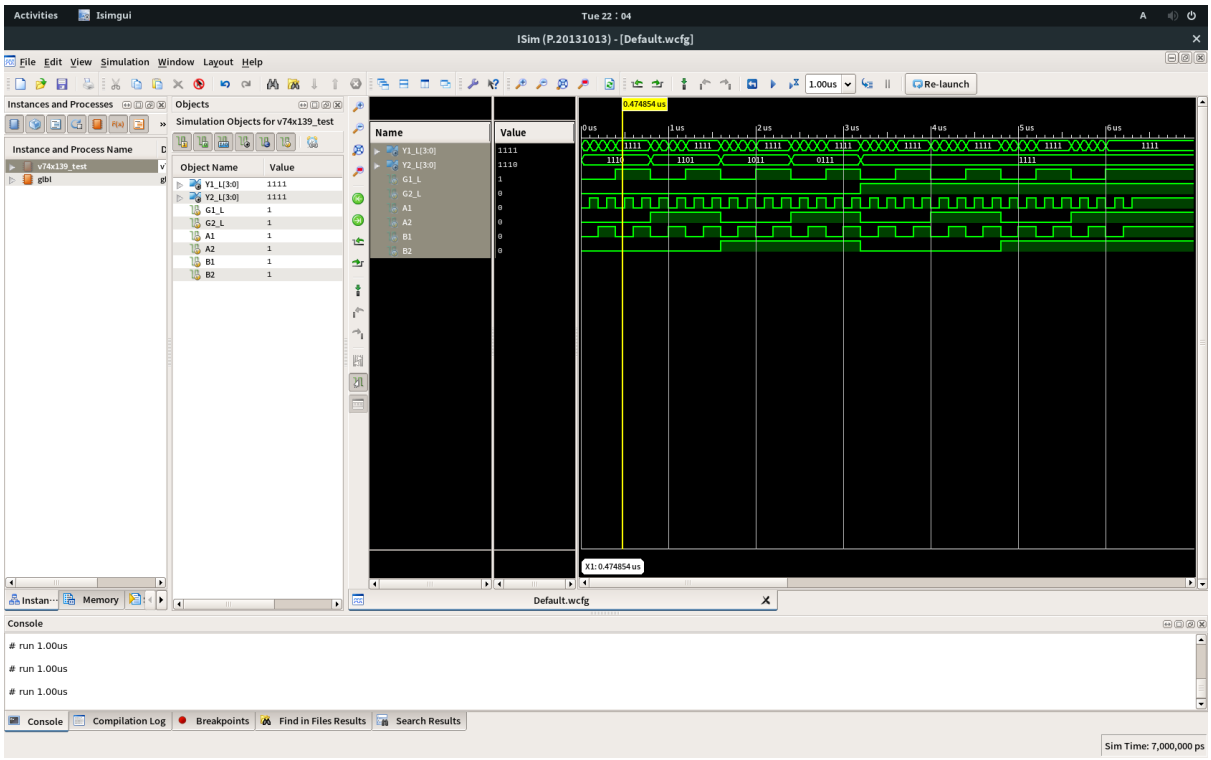
4. half 74x139 두개를 이용해 74x139를 디자인하고 실행해보았다.

코드:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:       20:18:47 04/03/2018
// Design Name:
// Module Name:       v74x139
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module v74x139(
      input G1_L,
      input G2_L,
      input A1,
```

```
    input A2,
    input B1,
    input B2,
    output [3:0] Y1_L,
    output [3:0] Y2_L
    );

        v74x139h_b T1(.G_L(G1_L), .A(A1), .B(B1), .Y_L(Y1_L));
        v74x139h_b T2(.G_L(G2_L), .A(A2), .B(B2), .Y_L(Y2_L));

endmodule
```

사진:



부록 2. 74x139 의 테스트코드: for 문이 작동하는 줄 모르고 2^6 줄을 일일이 손으로 작성함

```
`timescale 1ns / 1ps


////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:     20:24:45 04/03/2018
// Design Name:     v74x139
// Module Name:     /csehome/pistolstar1797/v74x139/v74x139_test.v
// Project Name:    v74x139
// Target Device:
// Tool versions:
// Description:
//
// Verilog Test Fixture created by ISE for module: v74x139
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////////////


module v74x139_test;
```

```
// Inputs
reg G1_L;
reg G2_L;
reg A1;
reg A2;
reg B1;
reg B2;

// Outputs
wire [3:0] Y1_L;
wire [3:0] Y2_L;

// Instantiate the Unit Under Test (UUT)
v74x139 uut (
        .G1_L(G1_L),
        .G2_L(G2_L),
        .A1(A1),
        .A2(A2),
        .B1(B1),
        .B2(B2),
        .Y1_L(Y1_L),
        .Y2_L(Y2_L)
);

initial begin
```

```
// Initialize Inputs
G1_L = 0;
G2_L = 0;
A1 = 0;
A2 = 0;
B1 = 0;
B2 = 0;

// Wait 100 ns for global reset to finish
#100;

// Add stimulus here
G1_L = 0;
G2_L = 0;
A1 = 1;
A2 = 0;
B1 = 0;
B2 = 0;

#100 G1_L = 0; G2_L = 0; A1 = 0;  A2 = 0; B1 = 1; B2 = 0;

#100 G1_L = 0; G2_L = 0; A1 = 1;  A2 = 0; B1 = 1; B2 = 0;

#100 G1_L = 1; G2_L = 0; A1 = 0;  A2 = 0; B1 = 0; B2 = 0;

#100 G1_L = 1; G2_L = 0; A1 = 1;  A2 = 0; B1 = 0; B2 = 0;
```

#100 G1_L = 1; G2_L = 0; A1 = 0; A2 = 0; B1 = 1; B2 = 0;

#100 G1_L = 1; G2_L = 0; A1 = 1; A2 = 0; B1 = 1; B2 = 0;

#100 G1_L = 0; G2_L = 0; A1 = 0; A2 = 1; B1 = 0; B2 = 0;

#100 G1_L = 0; G2_L = 0; A1 = 1; A2 = 1; B1 = 0; B2 = 0;

#100 G1_L = 0; G2_L = 0; A1 = 0; A2 = 1; B1 = 1; B2 = 0;

#100 G1_L = 0; G2_L = 0; A1 = 1; A2 = 1; B1 = 1; B2 = 0;

#100 G1_L = 1; G2_L = 0; A1 = 0; A2 = 1; B1 = 0; B2 = 0;

#100 G1_L = 1; G2_L = 0; A1 = 1; A2 = 1; B1 = 0; B2 = 0;

#100 G1_L = 1; G2_L = 0; A1 = 0; A2 = 1; B1 = 1; B2 = 0;

#100 G1_L = 1; G2_L = 0; A1 = 1; A2 = 1; B1 = 1; B2 = 0;

#100 G1_L = 0; G2_L = 0; A1 = 0; A2 = 0; B1 = 0; B2 = 1;

#100 G1_L = 0; G2_L = 0; A1 = 1; A2 = 0; B1 = 0; B2 = 1;

#100 G1_L = 0; G2_L = 0; A1 = 0; A2 = 0; B1 = 1; B2 = 1;

#100 G1_L = 0; G2_L = 0; A1 = 1; A2 = 0; B1 = 1; B2 = 1;

#100 G1_L = 1; G2_L = 0; A1 = 0; A2 = 0; B1 = 0; B2 = 1;

#100 G1_L = 1; G2_L = 0; A1 = 1; A2 = 0; B1 = 0; B2 = 1;

#100 G1_L = 1; G2_L = 0; A1 = 0; A2 = 0; B1 = 1; B2 = 1;

#100 G1_L = 1; G2_L = 0; A1 = 1; A2 = 0; B1 = 1; B2 = 1;

#100 G1_L = 0; G2_L = 0; A1 = 0; A2 = 1; B1 = 0; B2 = 1;

#100 G1_L = 0; G2_L = 0; A1 = 1; A2 = 1; B1 = 0; B2 = 1;

#100 G1_L = 0; G2_L = 0; A1 = 0; A2 = 1; B1 = 1; B2 = 1;

#100 G1_L = 0; G2_L = 0; A1 = 1; A2 = 1; B1 = 1; B2 = 1;

#100 G1_L = 1; G2_L = 0; A1 = 0; A2 = 1; B1 = 0; B2 = 1;

#100 G1_L = 1; G2_L = 0; A1 = 1; A2 = 1; B1 = 0; B2 = 1;

#100 G1_L = 1; G2_L = 0; A1 = 0; A2 = 1; B1 = 1; B2 = 1;

#100 G1_L = 1; G2_L = 0; A1 = 1; A2 = 1; B1 = 1; B2 = 1;

#100 G1_L = 0; G2_L = 1; A1 = 0; A2 = 0; B1 = 0; B2 = 0;

#100 G1_L = 0; G2_L = 1; A1 = 1; A2 = 0; B1 = 0; B2 = 0;

#100 G1_L = 0; G2_L = 1; A1 = 0; A2 = 0; B1 = 1; B2 = 0;

#100 G1_L = 0; G2_L = 1; A1 = 1; A2 = 0; B1 = 1; B2 = 0;

#100 G1_L = 1; G2_L = 1; A1 = 0; A2 = 0; B1 = 0; B2 = 0;

#100 G1_L = 1; G2_L = 1; A1 = 1; A2 = 0; B1 = 0; B2 = 0;

#100 G1_L = 1; G2_L = 1; A1 = 0; A2 = 0; B1 = 1; B2 = 0;

#100 G1_L = 1; G2_L = 1; A1 = 1; A2 = 0; B1 = 1; B2 = 0;

#100 G1_L = 0; G2_L = 1; A1 = 0; A2 = 1; B1 = 0; B2 = 0;

#100 G1_L = 0; G2_L = 1; A1 = 1; A2 = 1; B1 = 0; B2 = 0;

#100 G1_L = 0; G2_L = 1; A1 = 0; A2 = 1; B1 = 1; B2 = 0;

#100 G1_L = 0; G2_L = 1; A1 = 1; A2 = 1; B1 = 1; B2 = 0;

#100 G1_L = 1; G2_L = 1; A1 = 0; A2 = 1; B1 = 0; B2 = 0;

#100 G1_L = 1; G2_L = 1; A1 = 1; A2 = 1; B1 = 0; B2 = 0;

#100 G1_L = 1; G2_L = 1; A1 = 0; A2 = 1; B1 = 1; B2 = 0;

#100 G1_L = 1; G2_L = 1; A1 = 1; A2 = 1; B1 = 1; B2 = 0;

#100 G1_L = 0; G2_L = 1; A1 = 0; A2 = 0; B1 = 0; B2 = 1;

#100 G1_L = 0; G2_L = 1; A1 = 1; A2 = 0; B1 = 0; B2 = 1;

#100 G1_L = 0; G2_L = 1; A1 = 0; A2 = 0; B1 = 1; B2 = 1;

#100 G1_L = 0; G2_L = 1; A1 = 1; A2 = 0; B1 = 1; B2 = 1;

#100 G1_L = 1; G2_L = 1; A1 = 0; A2 = 0; B1 = 0; B2 = 1;

#100 G1_L = 1; G2_L = 1; A1 = 1; A2 = 0; B1 = 0; B2 = 1;

#100 G1_L = 1; G2_L = 1; A1 = 0; A2 = 0; B1 = 1; B2 = 1;

#100 G1_L = 1; G2_L = 1; A1 = 1; A2 = 0; B1 = 1; B2 = 1;

#100 G1_L = 0; G2_L = 1; A1 = 0; A2 = 1; B1 = 0; B2 = 1;

#100 G1_L = 0; G2_L = 1; A1 = 1; A2 = 1; B1 = 0; B2 = 1;

```
        #100 G1_L = 0; G2_L = 1; A1 = 0;  A2 = 1; B1 = 1; B2 = 1;

        #100 G1_L = 0; G2_L = 1; A1 = 1;  A2 = 1; B1 = 1; B2 = 1;

        #100 G1_L = 1; G2_L = 1; A1 = 0;  A2 = 1; B1 = 0; B2 = 1;

        #100 G1_L = 1; G2_L = 1; A1 = 1;  A2 = 1; B1 = 0; B2 = 1;

        #100 G1_L = 1; G2_L = 1; A1 = 0;  A2 = 1; B1 = 1; B2 = 1;

        #100 G1_L = 1; G2_L = 1; A1 = 1;  A2 = 1; B1 = 1; B2 = 1;

    end

endmodule
```

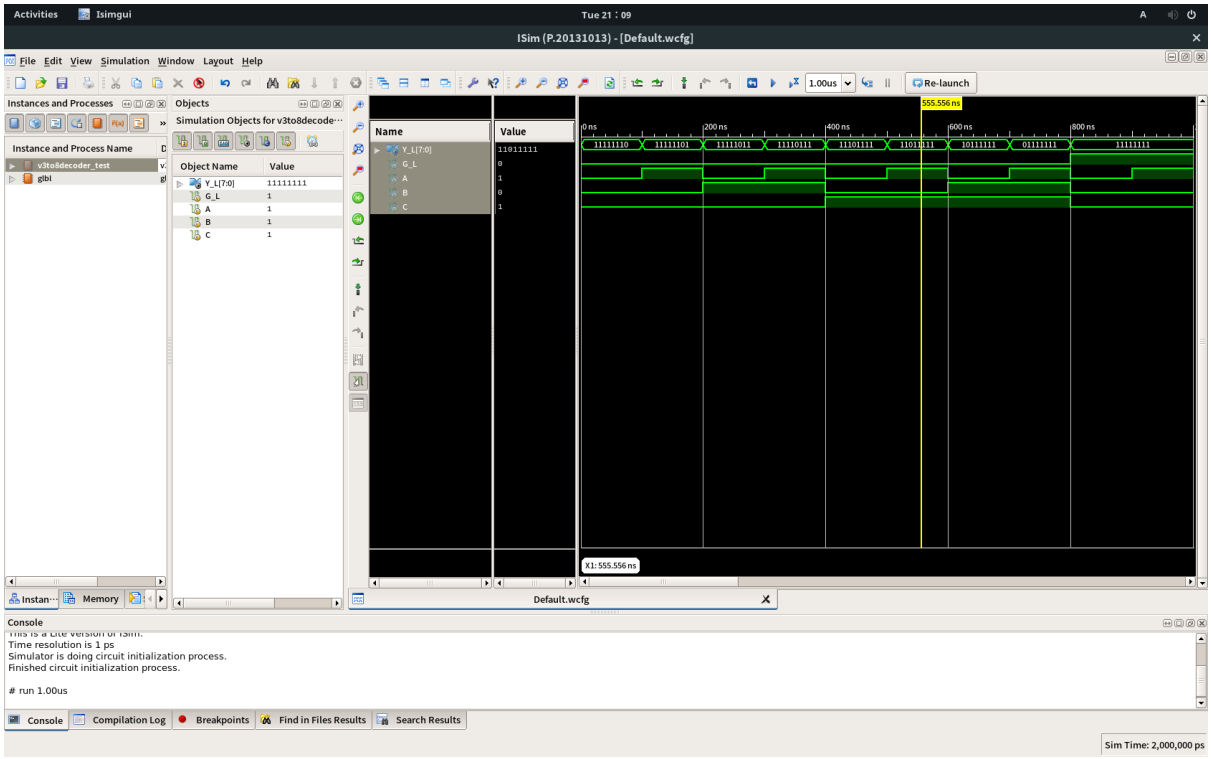
5. half 74x139 (2-to-4 decoder)를 응용하여 3-to-8 decoder를 디자인하고 실행해보았다.

코드:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:       20:55:17 04/03/2018
// Design Name:
// Module Name:       v3to8decoder
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module v3to8decoder(
      input G_L,
      input A,
      input B,
```

```
    input C,
    output [7:0] Y_L
    );

        wire [3:0] out1;
        wire [3:0] out2;

        assign Y_L[3:0] = out1;
        assign Y_L[7:4] = out2;

        v74x139h_b T1(.G_L(G_L | C), .A(A), .B(B), .Y_L(out1));
        v74x139h_b T2(.G_L(G_L | ~C), .A(A), .B(B), .Y_L(out2));

endmodule
```

사진:



부록 3. 3-to-8 decoder 의 테스트코드:

```
`timescale 1ns / 1ps


////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:     20:56:07 04/03/2018
// Design Name:     v3to8decoder
// Module Name:     /csehome/pistolstar1797/v74x139/v3to8decoder_test.v
// Project Name:    v74x139
// Target Device:
// Tool versions:
// Description:
//
// Verilog Test Fixture created by ISE for module: v3to8decoder
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////////////


module v3to8decoder_test;
```

```
// Inputs
reg G_L;
reg A;
reg B;
reg C;

// Outputs
wire [7:0] Y_L;

// Instantiate the Unit Under Test (UUT)
v3to8decoder uut (
        .G_L(G_L),
        .A(A),
        .B(B),
        .C(C),
        .Y_L(Y_L)
);

initial begin
        // Initialize Inputs
        G_L = 0;
        A = 0;
        B = 0;
        C = 0;
```

```
// Wait 100 ns for global reset to finish
#100;

// Add stimulus here
G_L = 0;
A = 1;
B = 0;
C = 0;

#100 G_L = 0; A = 0;       B = 1; C = 0;

#100 G_L = 0; A = 1;       B = 1; C = 0;

#100 G_L = 0; A = 0;       B = 0; C = 1;

#100 G_L = 0; A = 1;       B = 0; C = 1;

#100 G_L = 0; A = 0;       B = 1; C = 1;

#100 G_L = 0; A = 1;       B = 1; C = 1;

#100 G_L = 1; A = 0;       B = 0; C = 0;

#100 G_L = 1; A = 1;       B = 0; C = 0;

#100 G_L = 1; A = 0;       B = 1; C = 0;
```

```
        #100 G_L = 1; A = 1;       B = 1; C = 0;

        #100 G_L = 1; A = 0;       B = 0; C = 1;

        #100 G_L = 1; A = 1;       B = 0; C = 1;

        #100 G_L = 1; A = 0;       B = 1; C = 1;

        #100 G_L = 1; A = 1;       B = 1; C = 1;

    end

endmodule
```

Homework:

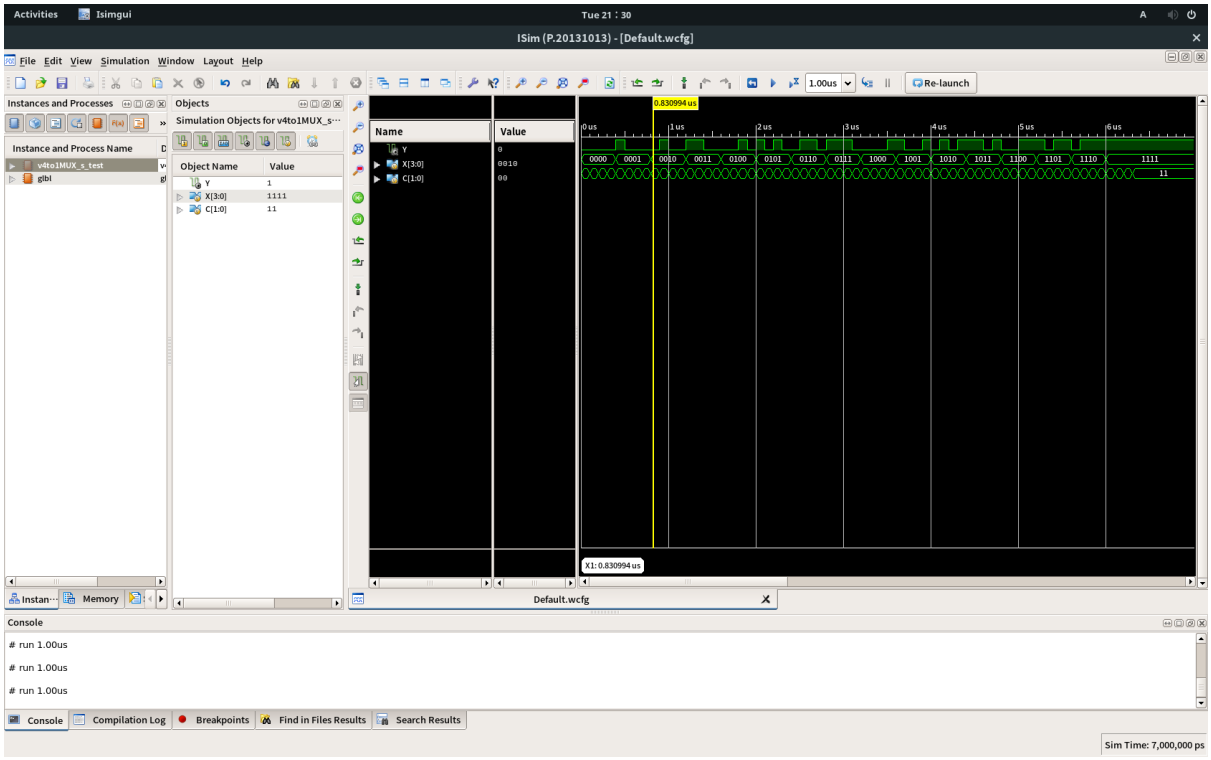
1. Structural description을 이용해 4-to-1 MUX를 디자인하고 실행해보았다.

코드:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:       21:13:14 04/03/2018
// Design Name:
// Module Name:       v4to1MUX_s
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module v4to1MUX_s(
      input [3:0] X,
            input [1:0] C,
```

```
    output Y
    );
        wire [3:0] T;
        wire [1:0] N_C;

        not (N_C[0], C[0]);
        not (N_C[1], C[1]);

        and (T[0], X[0], N_C[1], N_C[0]);
        and (T[1], X[1], N_C[1], C[0]);
        and (T[2], X[2], C[1], N_C[0]);
        and (T[3], X[3], C[1], C[0]);

        or (Y, T[0], T[1], T[2], T[3]);


endmodule
```

사진:


Activities
Isimgui
Tue 21 : 30
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Objects
Simulation Objects for v4to1MUX_s···
Instance and Process Name
Object Name
Value
v4to1MUX_s_test
glbl
Y
X[3:0]
C[1:0]
1111
11
Name
Value
0.830994 us
X1: 0.830994 us
Default.wcfg
Console
run 1.00us
run 1.00us
run 1.00us
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 7,000,000 ps

2. Data flow description을 이용해 4-to-1 MUX를 디자인하고 실행해보았다.

코드:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:       21:33:23 04/03/2018
// Design Name:
// Module Name:       v4to1MUX_d
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module v4to1MUX_d(
      input [3:0] X,
      input [1:0] C,
      output Y
```

);

assign Y = (X[0] == 1 && C == 2'b00) ? 1'b1 :

(X[1] == 1 && C == 2'b01) ? 1'b1 :

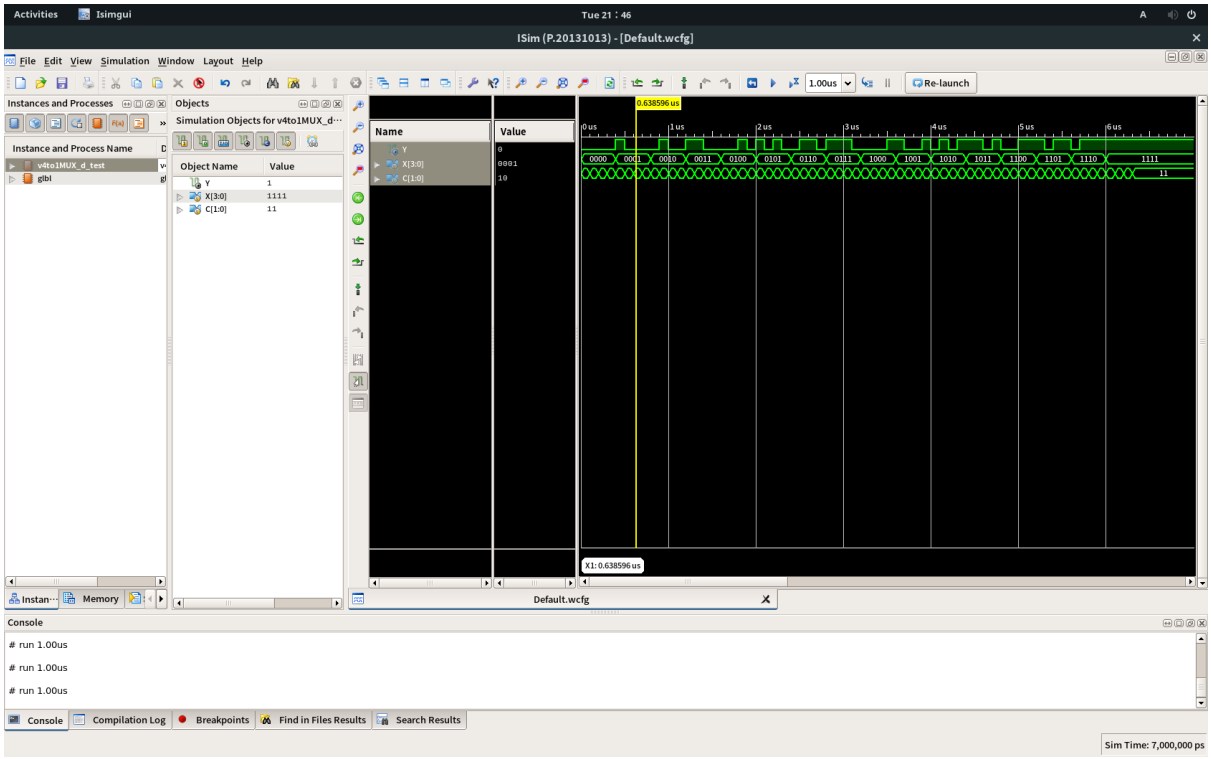
(X[2] == 1 && C == 2'b10) ? 1'b1 :

(X[3] == 1 && C == 2'b11) ? 1'b1 :

1'b0;

endmodule

사진:



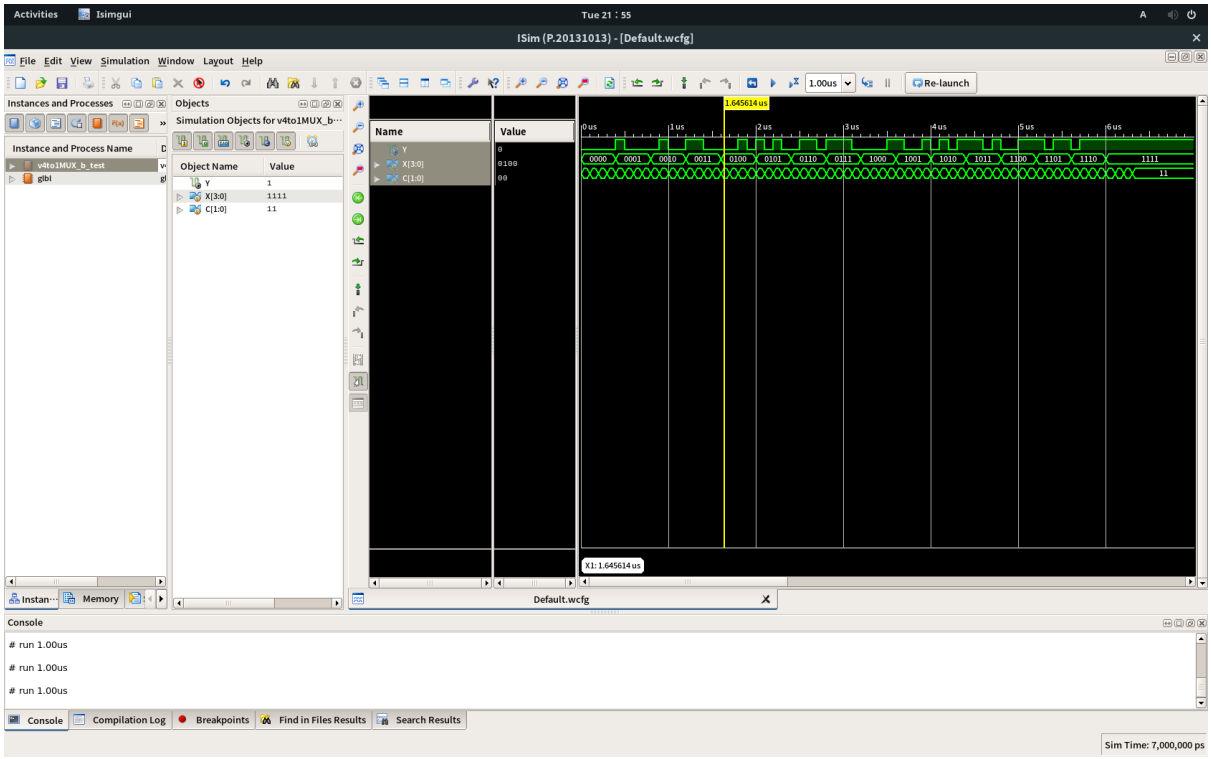
3. Behavioral description을 이용해 4-to-1 MUX를 디자인하고 실행해보았다.

코드:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:       21:47:40 04/03/2018
// Design Name:
// Module Name:       v4to1MUX_b
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module v4to1MUX_b(
      input [3:0] X,
      input [1:0] C,
      output Y
```

```
    );

        reg T;

        assign Y = T;

        always@(X or C)
            begin
                if(X[C]==1)
                    begin
                        T = 1'b1;
                    end
                else
                    begin
                        T = 1'b0;
                    end
            end

endmodule
```

사진:


Activities
Isimgui
Tue 21 : 55
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Objects
Simulation Objects for v4to1MUX_b
Instance and Process Name
v4to1MUX_b_test
glbl
Object Name
Value
Y
X[3:0]
C[1:0]
Name
Value
1.645614 us
0us
1us
2us
3us
4us
5us
6us
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
X1: 1.645614 us
Default.wcfg
Console
run 1.00us
run 1.00us
run 1.00us
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 7,000,000 ps

4. Structural description의 특징: Schematic diagram을 그대로 코드로 작성하는 방법

장점: schematic diagram을 안다면 틀릴 일이 없다.

단점: 게이트의 개수가 많아지면 코드가 길고 복잡해질 수 있다.

5. Data flow description의 특징: Truth table을 그대로 코드로 작성하는 방법

장점: truth table을 안다면 틀릴 일이 없다.

단점: 입/출력 값이 많아지면 코드가 기하급수적으로 길어진다.

6. Behavioral description의 특징: module이 무슨 기능을 하는지를 논리적으로 작성하는 방법

장점: 알고리즘을 잘 파악하고 있다면 짧고 효율적인 코드를 작성할 수 있다.

단점: 알고리즘을 제대로 파악하지 못하면 틀린 결과값을 출력하거나 코드가 산으로 갈 수 있다.