Vending Machine

TEAM VENDTECH

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Contents

- Implementation on FPGA
- Code
- FSM Diagram
- PCB Design

Hardware

- Nexys Artix 7 100t FPGA

```vhdl
5  entity vendingmachine is
6     Port(
7       clk_in  : in std_logic;
8       reset   : in std_logic;
9       AN_IN   : out std_logic_vector(7 downto 0);
10      LED_OUT : out std_logic_vector(6 downto 0);
11      SW2     : in std_logic_vector(2 downto 0);
12      SW3     : in std_logic_vector(1 downto 0);
13      SW4     : in std_logic;
14      LED_G, LED_R : out std_logic;
15      SW      : in std_logic_vector(2 downto 0)
16    );
17  end vendingmachine;
18
```

```vhdl
architecture Behavioral of vendingmachine is
    signal counter : integer range 0 to 100000 := 0;
    signal clk_out : std_logic := '0';
    constant DIVIDER_VALUE : integer := 100000;
    signal temp : integer range 0 to 9 := 0;

    type StateType is (Idle, item_select, Coin, Dispense);
    signal next_state : StateType := Idle;

begin
    -- Clock divider process
    process (clk_in, reset)
    begin
      if reset = '1' then
        counter <= 0;
        clk_out <= '0';
      elsif rising_edge(clk_in) then
        if counter = DIVIDER_VALUE then
          counter <= 0;
          clk_out <= not clk_out;
          if temp = 9 then
            temp <= 0;
          else
            temp <= temp + 1;
          end if;
        else
          counter <= counter + 1;
        end if;
      end if;
    end process;
```

```vhdl
49
50        -- State transition process
51    process (SW)
52    begin
53      if SW = "001" then
54        next_state <= Idle;
55      elsif SW = "010" then
56        next_state <= item_select;
57      elsif SW = "100" then
58        next_state <= Coin;
59      elsif SW = "111" then
60        next_state <= Dispense;
61      else
62        next_state <= Idle;
63      end if;
64    end process;
65
```

```vhdl
66    -- Item selection display process
67    process (SW2, temp)
68    begin
69      if next_state = item_select then
70        if SW2 = "000" then
71          -- Display Fanta
72          if temp = 0 then
73      AN_IN <= "01111111";
74      LED_OUT <= "0001110"; -- F
75  elsif temp = 1 then
76      AN_IN <= "10111111";
77      LED_OUT <= "0001000"; -- A
78  elsif temp = 2 then
79      AN_IN <= "11011111";
80      LED_OUT <= "0101011"; -- n
81  elsif temp = 3 then
82      AN_IN <= "11101111";
83      LED_OUT <= "0000111"; -- T
84      elsif temp = 4 then
85      AN_IN <= "11110111";
86      LED_OUT <= "0001000"; -- A
87  elsif temp = 5 then
88      AN_IN <= "11111110";
89      LED_OUT <= "0011001"; -- 4
90  else
91      AN_IN <= "11111111";
92      LED_OUT <= "1111111"; -- all segments off
93  end if;
```

```vhdl
201    elsif next_state = Dispense then
202      if SW4 = '1' then
203        if SW2 = "000" then --Fanta 4
204          if SW3 = "01" then --2
205            AN_IN <= "11111101";
206            LED_OUT <= "0100100"; --2 (red)
207            elsif SW3 = "00" then --1
208            AN_IN <= "11111101";
209            LED_OUT <= "0110000"; --3 (red)
210          elsif SW3 = "10" then --3
211            AN_IN <= "11111101";
212            LED_OUT <= "1001111"; --1 (red)
213          elsif SW3 = "11" then --4
214            AN_IN <= "11111101";
215            LED_OUT <= "1000000"; -- 0 (green)
216          else
217            AN_IN <= "11111111";
218            LED_OUT <= "1111111";
219          end if;
```

```vhdl
begin
    if next_state = Dispense then
        if SW4 = '1' then
            if SW2 = "000" then
                if SW3 = "00" then
                    LED_G <= '0';
                    LED_R <= '1';
                elsif SW3 = "01" then
                    LED_G <= '0';
                    LED_R <= '1';
                elsif SW3 = "10" then
                    LED_G <= '0';
                    LED_R <= '1';
                elsif SW3 = "11" then
                    LED_G <= '1';
                    LED_R <= '0';
                else
                    LED_G <= '1';
                    LED_R <= '1';
                end if;
```
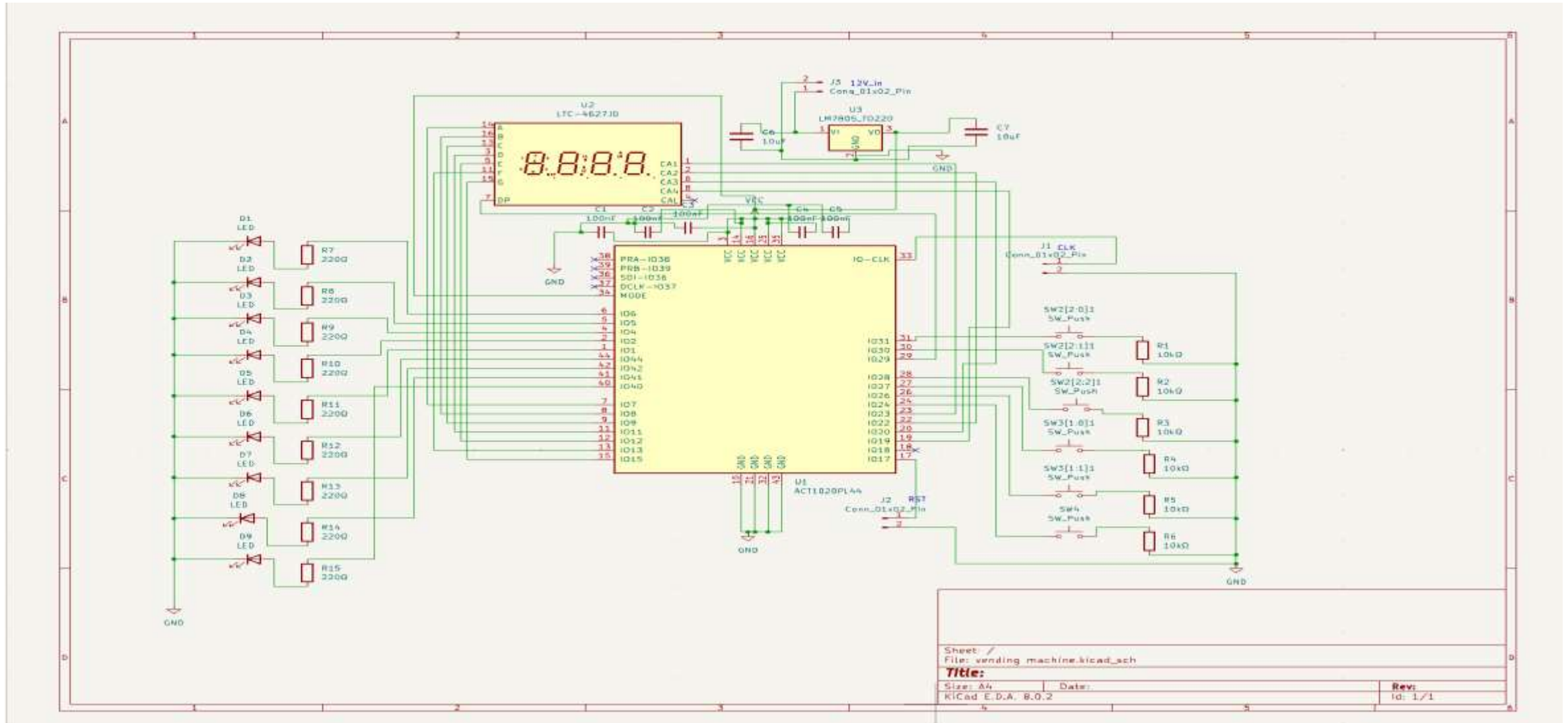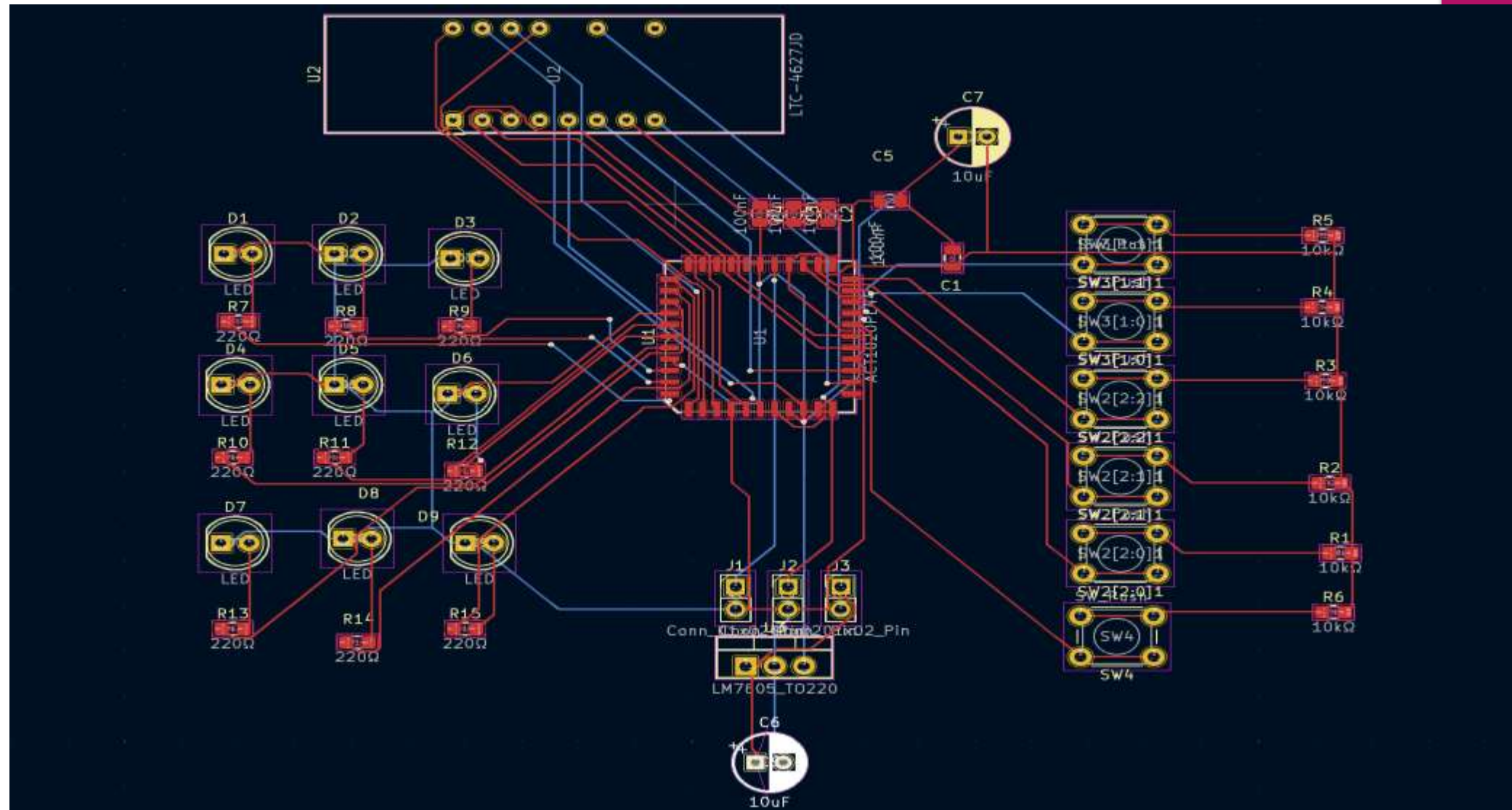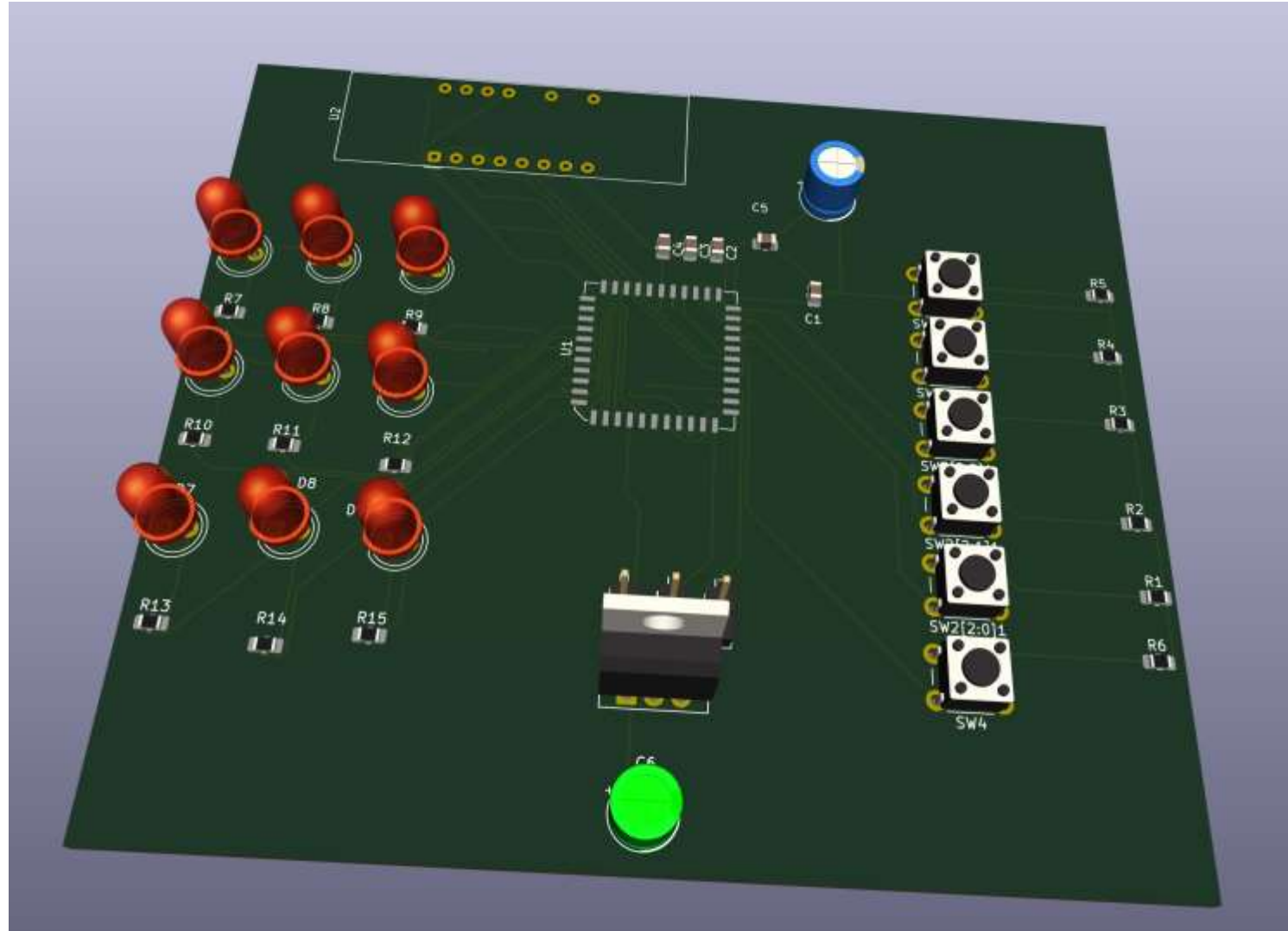
Finite State Model Diagram
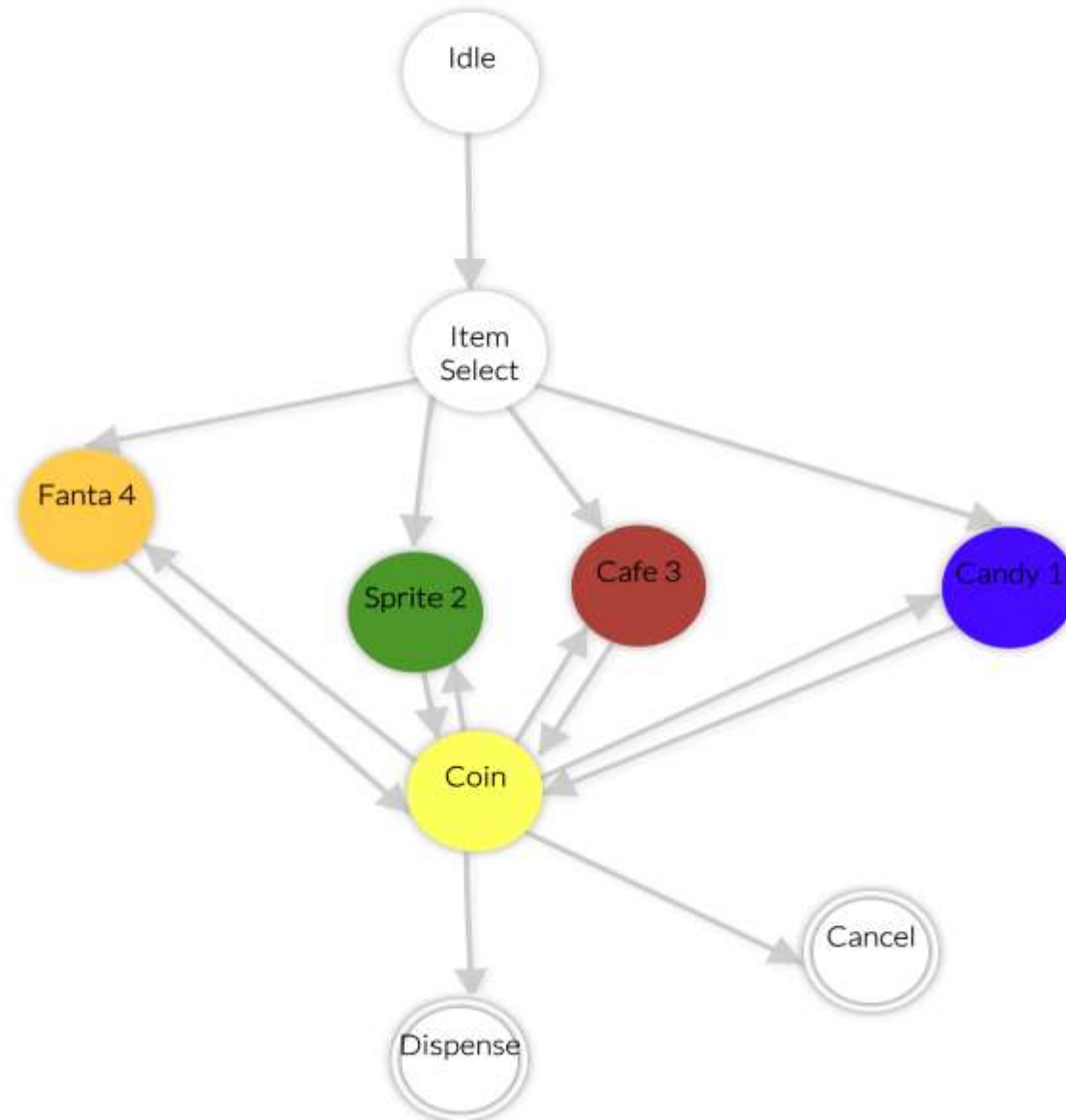
Schematic Design

PCB Board

3D View of PCB Board

THANK YOU