

June 1993 Revised April 2005

74LVX373

Low Voltage Octal Transparent Latch with 3-STATE Outputs

General Description

The LVX373 consists of eight latches with 3-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable $(\overline{\text{OE}})$ is LOW. When $\overline{\text{OE}}$ is HIGH, the bus output is in the high impedance state. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

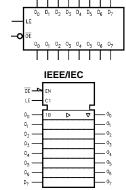
- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Ordering Code:

Order Number Package Number			Package Description
	74LVX373M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
	74LVX373SJ M20D		Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
	74LVX373MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code. Pb-Free package per JEDED J-STD-020B.

Logic Symbols



Connection Diagram



Pin Descriptions

Pin Names	Description
D ₀ -D ₇	Data Inputs
LE	Latch Enable Input
ŌĒ	Output Enable Input
O ₀ -O ₇	3-STATE Latch Outputs

Truth Table

	Inputs							
LE	OE	D _n	O _n					
Х	Н	Х	Z					
Н	L	L	L					
Н	L	Н	Н					
L	L	X	O ₀					

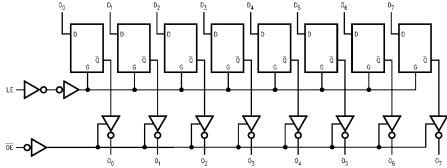
- H = HIGH Voltage Level
- L = LOW Voltage Level
- Z = High Impedance X = Immaterial
- O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Functional Description

The LVX373 contains eight D-type latches with 3-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the $D_{\rm n}$ inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transparent of the transparent of the D inputs a setup time preceding the HIGH-to-LOW transparent of the transparent of the

sition of LE. The 3-STATE standard outputs are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the standard outputs are in the 2-state mode. When \overline{OE} is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

0 ns/V to 100 ns/V

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC}) -0.5V to +7.0V

DC Input Diode Current (I_{IK})

 $\begin{array}{lll} \text{V}_{\text{I}} = -0.5 \text{V} & -20 \text{ mA} \\ \\ \text{DC Input Voltage (V}_{\text{I}}) & -0.5 \text{V to 7V} \end{array}$

DC Output Diode Current (I_{OK})

$$\begin{split} \text{V}_{\text{O}} &= -0.5 \text{V} & -20 \text{ mA} \\ \text{V}_{\text{O}} &= \text{V}_{\text{CC}} + 0.5 \text{V} & +20 \text{ mA} \end{split}$$

DC Output Voltage (V_O) -0.5V to $V_{CC} + 0.5V$

DC Output Source

or Sink Current (I_O) ± 25 mA

DC V_{CC} or Ground Current

 $\begin{array}{cc} (I_{CC} \ or \ I_{GND}) & \pm 75 \ mA \\ \\ Storage \ Temperature \ (T_{STG}) & -65 ^{\circ}C \ to +150 ^{\circ}C \end{array}$

Power Dissipation 180 mW

Recommended Operating Conditions (Note 2)

Input Rise and Fall Time (Δt/ΔV)

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V _{cc}	T _A = +25°C		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions		
Cymbol	i arameter	• 66	Min Typ		Max	Min	Max	Oilita	Conditions	
V _{IH}	HIGH Level	2.0	1.5			1.5				
	Input Voltage	3.0	2.0			2.0		V		
		3.6	2.4			2.4				
V _{IL}	LOW Level	2.0			0.5		0.5			
	Input Voltage	3.0			0.8		0.8	V		
		3.6			0.8		0.8			
V _{OH}	HIGH Level	2.0	1.9	2.0		1.9			$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu\text{A}$ $I_{OH} = -50 \mu\text{A}$ $I_{OH} = -4 \text{ mA}$	
	Output Voltage	3.0	2.9	3.0		2.9		V	I _{OH} = -50 μA	
		3.0	2.58			2.48			$I_{OH} = -4 \text{ mA}$	
V _{OL}	LOW Level	2.0		0.0	0.1		0.1		$V_{IN} = V_{IH} \text{ or } V_{IL} I_{OL} = 50 \mu\text{A}$	
	Output Voltage	3.0		0.0	0.1		0.1	V	$I_{OL} = 50 \mu A$	
		3.0			0.36		0.44		I _{OL} = 4 mA	
loz	3-STATE Output	3.6			±0.25		±2.5	μΑ	$V_{IN} = V_{IH}$ or V_{IL}	
	Off-State Current								V _{OUT} = V _{CC} or GND	
I _{IN}	Input Leakage Current	3.6			±0.1		±1.0	μΑ	V _{IN} = 5.5V or GND	
I _{CC}	Quiescent Supply Current	3.6			4.0		40.0	μΑ	V _{IN} = V _{CC} or GND	

Noise Characteristics (Note 3)

Symbol	Parameter	V _{CC} T _A = 2		25°C	Units	C _L (pF)	
-,			Тур	Limit			
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}		0.5	0.8	V	50	
V _{OLV}	Quiet Output Minimum Dynamic V _{OL} Minimum HIGH Level Dynamic Input Voltage Maximum LOW Level Dynamic Input Voltage		-0.5	-0.8	V	50	
V_{IHD}				2.0	V	50	
V_{ILD}				0.8	V	50	

Note 3: Input $t_r = t_f = 3$ ns.

AC Electrical Characteristics

Symbol	Parameter	V _{CC}	T _A = +25°C			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions	
Syllibol	Farameter	(V)	Min	Тур	Max	Min	Max	Units	Conditions	
t _{PLH}	Propagation Delay Time	2.7		7.7	15.0	1.0	18.5		C _L = 15 pF	
t _{PHL}	D _n to O _n	<u> </u>		10.2	18.5	1.0	22.0	ns	C _L = 50 pF	
		3.3 ± 0.3		6.0	9.7	1.0	11.5	115	C _L = 15 pF	
				8.5	13.2	1.0	15.0		C _L = 50 pF	
t _{PLH}	Propagation Delay Time	2.7		7.5	14.5	1.0	17.5		C _L = 15 pF	
t _{PHL}	LE to O _n	<u> </u>		10.0	18.0	1.0	21.0	ns	C _L = 50 pF	
		3.3 ± 0.3		5.8	9.3	1.0	11.0	115	C _L = 15 pF	
		<u> </u>		8.3	12.8	1.0	14.5		C _L = 50 pF	
t _{PZL}	3-STATE Output	2.7		7.7	15.0	1.0	18.5		$C_L = 15 \text{ pF}, R_L = 1 \text{ k}\Omega$	
t _{PZH}	Enable Time			10.2	18.5	1.0	22.0	ns	$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$	
		3.3 ± 0.3		6.0	9.7	1.0	11.5	ns	$C_L = 15 \text{ pF}, R_L = 1 \text{ k}\Omega$	
		<u> </u>		8.5	13.2	1.0	15.0		$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$	
t _{PLZ}	3-STATE Output	2.7		9.8	18.0	1.0	21.0	ns	$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$	
t _{PHZ}	Disable Time	3.3 ± 0.3		8.2	12.8	1.0	14.5	115	$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$	
t _W	LE Pulse Width, HIGH	2.7	6.5			7.5		ns		
		3.3 ± 0.3	5.0			5.0		115		
t _S	Setup Time, D _n to LE	2.7	6.0			6.0		ns		
		3.3 ± 0.3	4.0			4.0		115		
t _H	Hold Time, D _n to LE	2.7	1.0			1.0		ns		
		3.3 ± 0.3	1.0			1.0		115		
toslh	Output to Output Skew	2.7			1.5		1.5	ns	C _L = 50 pF	
toshl	(Note 4)	3.3			1.5		1.5	115		

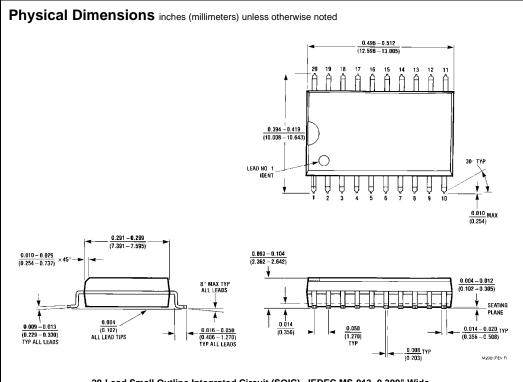
Note 4: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter		T _A = +25°C		T _A = -40°0	Units	
Cymbol		Min	Тур	Max	Min	Max	Oilita
C _{IN}	Input Capacitance		4	10		10	pF
C _{OUT}	Output Capacitance		6				pF
C _{PD}	Power Dissipation		27				pF
	Capacitance (Note 5)						

Note 5: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

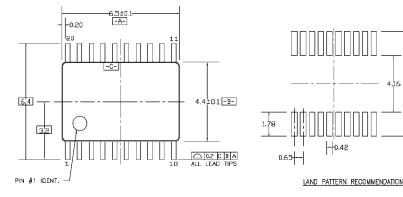
Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{|N} + I_{CC}}{8 \text{ (per Latch)}}$

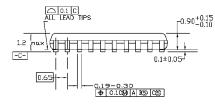


20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 2.6±0.10 0.40 TYP --A-5.01 TYP 5.3±0.10 9.27 TYP 7.8 -B-3.9 0.2 C B A ALL LEAD TIPS 10 PIN #1 IDENT.-0.6 TYP 1.27 TYP -LAND PATTERN RECOMMENDATION ALL LEAD TIPS SEE DETAIL A 0.1 C 2.1 MAX. 1.8±0.1 0.15±0.05 0.15-0.25 -1.27 TYP 0.35-0.51 **♦** 0.12 **⋈** C A DIMENSIONS ARE IN MILLIMETERS GAGE PLANE 0.25 NOTES: A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998. B. DIMENSIONS ARE IN MILLIMETERS. C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. 0.60±0.15-SEATING PLANE 1.25 -M20DRevB1 DETAIL A Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)







12.00*

R0.09min

GAGE PLANE

SEE DETAIL A

DIMENSIONS ARE IN MILLIMETERS

NOTES:

MTC20REVD1

- A. CONFORMS TO JEDEC REGISTRATION MD-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M. 1982.

IND TOLLOWINGS FER ANSI THEOM, 1962.

DETAIL A

-0.6±0.:

R0.09min

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20

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