

# Piyush Tulsidas Itankar

[in/pitankar](https://in/pitankar), [github/pitankar](https://github.com/pitankar), [www.linkedin.com/company/pitankar](https://www.linkedin.com/company/pitankar), [pitankar.com](https://www.pitankar.com)  
✉: [pitankar@gmail.com](mailto:pitankar@gmail.com), ☎: +918197611671

## experience

### Intel Tech India Pvt. Ltd

2015-Now

[System Validation Engineer (RF) : Since June 18] - Responsible for RF chain analysis and **development** of software required to tweak the RF parameters externally using **C** and **Python**. Responsibilities include studying the Bluetooth RF chain behavior for the ISM frequency band, **calibrating and programming RF peripheral registers** to ensure compliance with Bluetooth specification.

[Software Development Engineer: Nov 17 - Jun 18] - **Led** a team of college graduates to **design and develop GUI extension** for a debugging tool (in **Python and PyQt**) that could allow establishing a control path to the Bluetooth controller via the 'Host control Interface' protocol over USB, UART and Socket (for Virtual Platforms) interfaces. The tool enables discretely controlling the Bluetooth activities to be able to reproduce bugs and do code testing on real hardware. Responsibilities included cracking the **architecture of the pre-existing parts of the the software, designing data-structure and interfaces to tap the transaction flow over the hardware interfaces, handle the asynchronous command and event handling, modular and scalable modules, development of GUI in PyQt, mentoring, task assignment, follow-up and delivery of the tool.**

[Software Development Engineer: Dec 16 - Oct 17] - **Developed and delivered UEFI drivers** for Bluetooth Stack (in **C**). Responsible for working under a tech lead to design and deliver Vendor configuration driver which would **download Firmware** to Bluetooth controller as part of boot up, **Keyboard and Mouse report mode drivers** and **FTDI driver** for triggering a custom hardware for **latency measurement of wireless transactions** of click events.

[Software Development Engineer: June 16 - Nov 16] - Worked in team of Six under a Systems Architect to **develop and deliver the A2DP** (Audio profile for classic Bluetooth) profile (in **C**) to Zephyr open source IoT project.

[Intern: Firmware Engineering : 2015-2016] - Worked with GNSS firmware development group. Responsibilities included delivering on the development tasks assigned as part of which have **developed a memory manager** (in **C**) that **handled memory allocation for a 2kB space, designed and developed a math library** (in **C**) to **compute distance between two points over the surface of Earth**, bring up of pre-silicon development **virtual platforms, static analysis of firmware to compute memory and time requirement** for on chip memory design requirements.

## projects

[C, ASM]: RTOS for ARM: [github/pitankar/arm-rtos](https://github.com/pitankar/arm-rtos)

2016 - Now

[Verilog]: MIPS 32 Bit CPU Design on Altera DE1-Soc: [github/pitankar/mips-cpu](https://github.com/pitankar/mips-cpu)

2016 - Now

[Verilog]: Hardware Designs for Lattice iCE40 FPGA: [github/pitankar/FPGA-Designs](https://github.com/pitankar/FPGA-Designs)

2016 - Now

[C]: Symmetric Variable Key Cryptography: [github/pitankar/vaken-cli](https://github.com/pitankar/vaken-cli)

2014 - Now

[C]: Character driver for linux kernel: [github/pitankar/Driver](https://github.com/pitankar/Driver)

2014 - 2015

## education

### [Embedded Systems] School of Information Sciences, Manipal University

2014-2016

Master of Science in Technology (Embedded Systems). Research in Embedded Hardware-Software co-design with focus on design trade-offs. Thesis on Development of firmware components for GNSS Hardware, involves **firmware component design, development, static analysis, code optimization (for ARM CPU) and study of usefulness of virtual platforms in embedded development.**

### [Electrical Engineering] G.H. Rasoni College of Engineering, Nagpur University

2009-2013

Bachelor's in Electrical Engineering. Focus on Analog and Digital Circuit design. Worked on exploring the **Usability and applicability of Super-capacitors for Regenerative braking in Electric Vehicle** as part of final year project. Shortlisted for Motorola Scholar Awards 2013. Filed for patent <sup>1</sup>

## articles

FPGA development Flow: [medium/pulse/fpga-from-ground-up-piyush-itankar/](https://medium.com/pulse/fpga-from-ground-up-piyush-itankar/)

FPGA Internals: [medium/pulse/fpga-how-looks-inside-luts-piyush-itankar/](https://medium.com/pulse/fpga-how-looks-inside-luts-piyush-itankar/)

## arsenal

**Linux Drivers, C, GDB, OpenOCD, Verilog, Valgrind, splint, Python, ARM (Cortex M3, M4), FPGA, Shell Scripting, Git, Gerrit, JIRA.**

## interests

**C, Linux, ARM, FPGA** based solution/system design and development.

<sup>1</sup>Application No.2007/MUM/2013 A (In Progress). Page 36672 of OFFICIAL JOURNAL OF THE PATENT OFFICE (Issue No: 22/2015). Journal: <http://tinyurl.com/issue-no-22-2015>