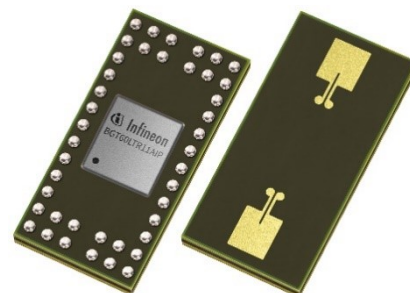


# BGT60LTR11(B)AIP

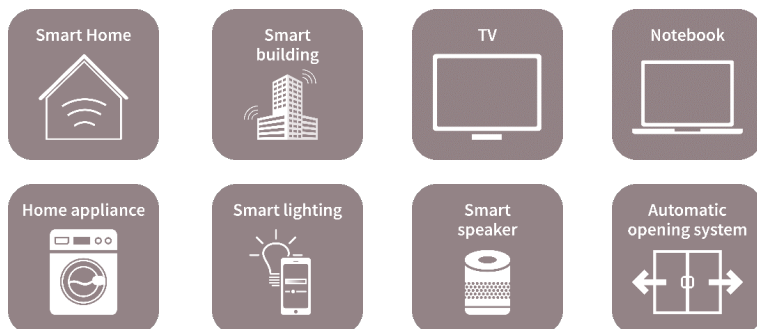
## Low power 60 GHz Doppler radar sensor with antennas in package

### Features

- 60 GHz transceiver MMIC with one transmitter and one receiver unit
- Antennas in package (AIP)
- Pulsed mode of operation for low power consumption
- Full autonomous mode
  - Integrated detector for motion and direction of movement
  - 15 configurable thresholds for target detection range
  - 16 configurations for detection status hold time
  - 4 configurable operation frequencies
  - 4 configurable pulse repetition rates
- High performance enabled from Infineon's BiCMOS technology
  - Fully integrated low phase noise VCO and PLL
  - Switchable prescaler with selectable sub-MHz frequencies
  - Medium power amplifier with configurable output power and integrated power detector
  - Homodyne low noise quadrature receiver
  - Low noise variable gain baseband amplifiers
  - Fully ESD protected device



### Potential applications and use-cases



### Description

The BGT60LTR11(B)AIP is a fully integrated millimeter wave Doppler motion sensor with antenna in package. The version BGT60LTR11AIP operates in the frequency band from 61 GHz to 61.5 GHz, while the version BGT60LTR11BAIP operates in the frequency band from 60.5 GHz to 61 GHz.

Both sensors detect the motion as well as the direction of a moving target. Both support the following two operation modes: autonomous and serial peripheral interface (SPI) mode.

- Autonomous mode: the sensor configuration parameters, detection threshold and hold time are set via external resistors; the pulse repetition rate and the operation frequency are set via hardware preset pins
- SPI mode: it allows the SPI connection to a microcontroller for more real time sensor configurations, that can be written in the internal registers through SPI

These different operation modes can be selected via hardware preset pins. For more detailed information, please refer to AN625.

**Description**

The BGT60LTR11(B)AIP integrates a medium power amplifier with configurable/adjustable output power, which can be controlled via SPI. The transmitted power is monitored by an integrated power detector. The packaged monolithic microwave integrated circuit (MMIC) features integrated broad-beam antennas for maximum area coverage.

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## 1 Electrical characteristics

## 1 Electrical characteristics

## 1.1 Absolute maximum ratings

Table 1 Absolute maximum ratings

$T_{OP} = -20^{\circ}\text{C} \dots 85^{\circ}\text{C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{DD}$	-0.3	–	1.9	V	
Voltage applied to non-RF I/O pins	$V_{DC,I/O}$	-0.3	–	$V_{DD}+0.3$	V	
Total power dissipation	$P_{DISS}$	–	–	300	mW	
Storage temperature range	$T_{STG}$	-40	–	150	$^{\circ}\text{C}$	
Operational temperature range	$T_{OP}$	-20	–	+85	$^{\circ}\text{C}$	Temperature at package soldering point
Thermal resistance of package	$R_{th,P}$	–	67	–	K/W	Represents bulk silicon to solder balls

**Attention:** Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and lifetime. Functionality of the device might not be given under these conditions.

## 1.2 ESD integrity

Table 2 ESD integrity

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
ESD robustness HBM	$V_{ESD-HBM}$	-1	–	1	kV	All pins
ESD robustness CDM	$V_{ESD-CDM}$	-500	–	500	V	All pins

**1 Electrical characteristics**
**1.3 Power supply**
**Table 3 Power supply electrical characteristics**
 $T_{OP} = -20^{\circ}\text{C} \dots 85^{\circ}\text{C}$ 

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{DD}$	1.45	1.5	1.6	V	
Current consumption in pulse-on phase	$I_{Pulse\_ON}$	–	128	–	mA	
Current consumption in pulse-off phase	$I_{Pulse\_OFF}$	–	0.8	–	mA	
Pulsed mode average power consumption	$P_{5/2000}$	–	2.3	–	mW	Duty cycle of 5/2000 us
	$P_{5/1000}$	–	3.4	–	mW	Duty cycle of 5/1000 us
	$P_{5/500}$	–	5.6	–	mW	Duty cycle of 5/500 us
	$P_{5/250}$	–	10.3	–	mW	Duty cycle of 5/250 us

**1.4 System parameters**
**Table 4 PLL parameters**
 $T_{OP} = -20^{\circ}\text{C} \dots 85^{\circ}\text{C}$ 

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{DD}$	1.45	1.5	1.6	V	
Transmitted frequency (BGT60LTR11AIP)	$f_{TX}$	61	61.25	61.5	GHz	$V_{tune} = V_{CPOUTPLL}$
Transmitted frequency (BGT60LTR11BAIP)	$f_{TX\_B}$	60.5	60.75	61	GHz	$V_{tune} = V_{CPOUTPLL}$
Output power (EIRP)	$P_{TX}$	–	+10	–	dBm	
Spurious emission < 40 GHz (EIRP)	$P_{SPUR1}$	–	–	-42	dBm	FCC 15.209
Spurious emission > 40 GHz and < 57 GHz (EIRP)	$P_{SPUR2}$	–	–	-20	dBm	ETSI EN 305 550
Spurious emission > 64 GHz and < 78 GHz (EIRP)	$P_{SPUR3}$	–	–	-20	dBm	ETSI EN 305 550
Spurious emission > 78 GHz (EIRP)	$P_{SPUR4}$	–	–	-30	dBm	ETSI EN 305 550
Frequency drift vs temperature	$\Delta f/\Delta T$	–	-10	–	MHz/K	$T_{OP} = -20^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}$ ; $V_{DD} = 1.5 \text{ V}$ ; free running VCO

## 1 Electrical characteristics

### 1.5 PLL parameters

**Table 5** PLL parameters

$T_{OP} = -20^{\circ}\text{C} \dots 85^{\circ}\text{C}$ ,  $V_{DD} = 1.45 \text{ V} \dots 1.6 \text{ V}$ .

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
External crystal frequency	$f_{CRY}$	–	38.4	–	MHz	
PLL lock frequency (BGT60LTR11AIP) <sup>1)</sup>	$f_L$	61	–	61.5	GHz	
PLL lock frequency (BGT60LTR11BAIP) <sup>1)</sup>	$f_{L\_B}$	60.5	–	61	GHz	

1) Programmed through Reg5 (for more information refer to AN625). Keep a 25 MHz guard band each side from the band edge to avoid outside of ISM band emission.

**Warning:** Sensors operating in close vicinity at the same operating frequency can interfere!

### 1.6 Frequency divider

**Table 6** Frequency divider electrical characteristics

$T_{OP} = -20^{\circ}\text{C} \dots 85^{\circ}\text{C}$ ,  $V_{DD} = 1.45 \text{ V} \dots 1.6 \text{ V}$ , Freq = 61.25 GHz.

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Divider output frequency 1	$f_{DIV1}$	–	9.6	–	MHz	Selectable via SPI (divided by 4 from crystal oscillator)
Dividing factor 2	$D_{DIV1}$	–	$2^{14}$	–	–	Selectable via SPI
Dividing factor 3	$D_{DIV2}$	–	$2^{17}$	–	–	Selectable via SPI
Dividing factor 4	$D_{DIV3}$	–	$2^{21}$	–	–	Selectable via SPI
Divider output voltage range	$V_{DIV}$	0	–	$V_{DD}$	V	
External capacitive load	$C_{extLoad}$	–	–	15	pF	

**1 Electrical characteristics****1.7 Antenna characteristics****Table 7 Antenna in package specifications**

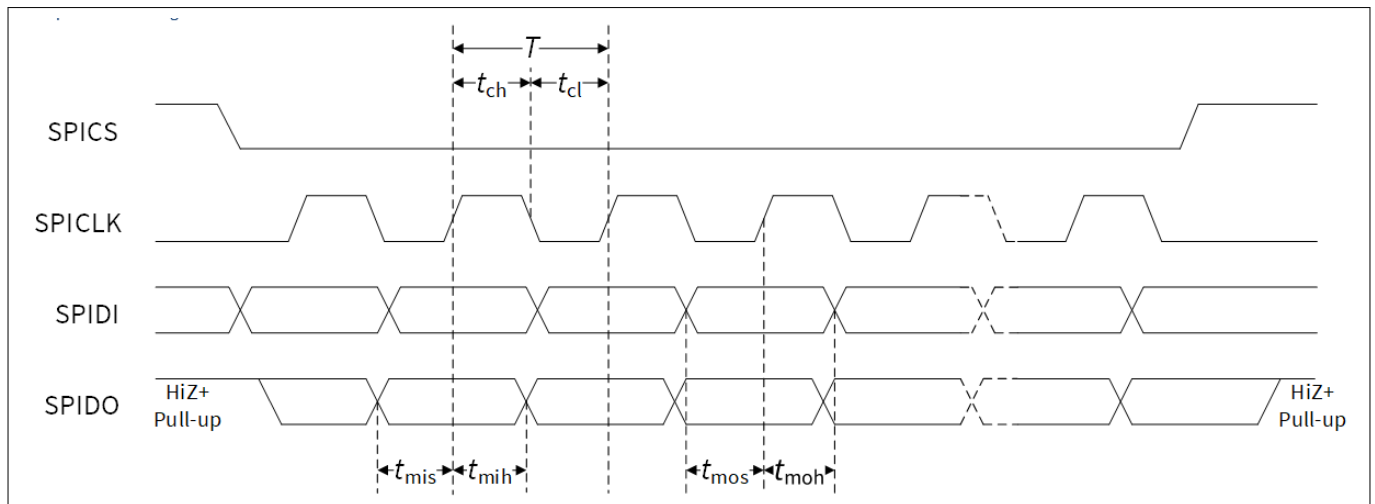
Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Operating frequency range	$f_{op}$	60.5	–	61.5	GHz	
Transmitter antenna gain	$G_{TX}$	–	6	–	dBi	@ Freq = 61.25 GHz
Receiver antenna gain	$G_{RX}$	–	6	–	dBi	@ Freq = 61.25 GHz
Horizontal -6dB beamwidth	$H_{-6dBbw}$	–	±50	–	deg	@ Freq = 61.25 GHz
Vertical -6dB beamwidth	$E_{-6dBbw}$	–	±70	–	deg	@ Freq = 61.25 GHz
Horizontal sidelobe suppression		–	12	–	dB	@ Freq = 61.25 GHz
Vertical sidelobe suppression		–	12	–	dB	@ Freq = 61.25 GHz
TX-RX isolation		–	35	–	dB	@ Freq = 61.25 GHz

## 2 SPI interface

## 2 SPI interface

### 2.1 SPI timing requirements

The BGT60LTR11(B)AIP is configured using a 4-wire SPI. It is used to configure the internal blocks of the BGT60LTR11(B)AIP chip registers. The main tasks are to set the mode of operation of the TX and/or RX chain and the baseband section. Communication with an external microcontroller is possible through the four dedicated pins SPIDI, SPIDO, SPICS and SPICLK. [Figure 1](#) demonstrates how the timing of the SPI behaves. The “working edge” is the rising edge of the clock SPICLK. The master application processor presents data for BGT60LTR11(B)AIP at the falling edge on SPIDI, while BGT60LTR11(B)AIP samples data at the rising edge. Read data is presented for the master on the rising edge on SPIDO. Asynchronous reset (SPIRSTN) must be de-asserted at least 10 ns before the falling edge of SPICLK. Refer to the application note AN625 for all details related to the SPI registers to control the MMIC.



**Figure 1** SPI timing diagram

**Table 8** SPI timing requirements

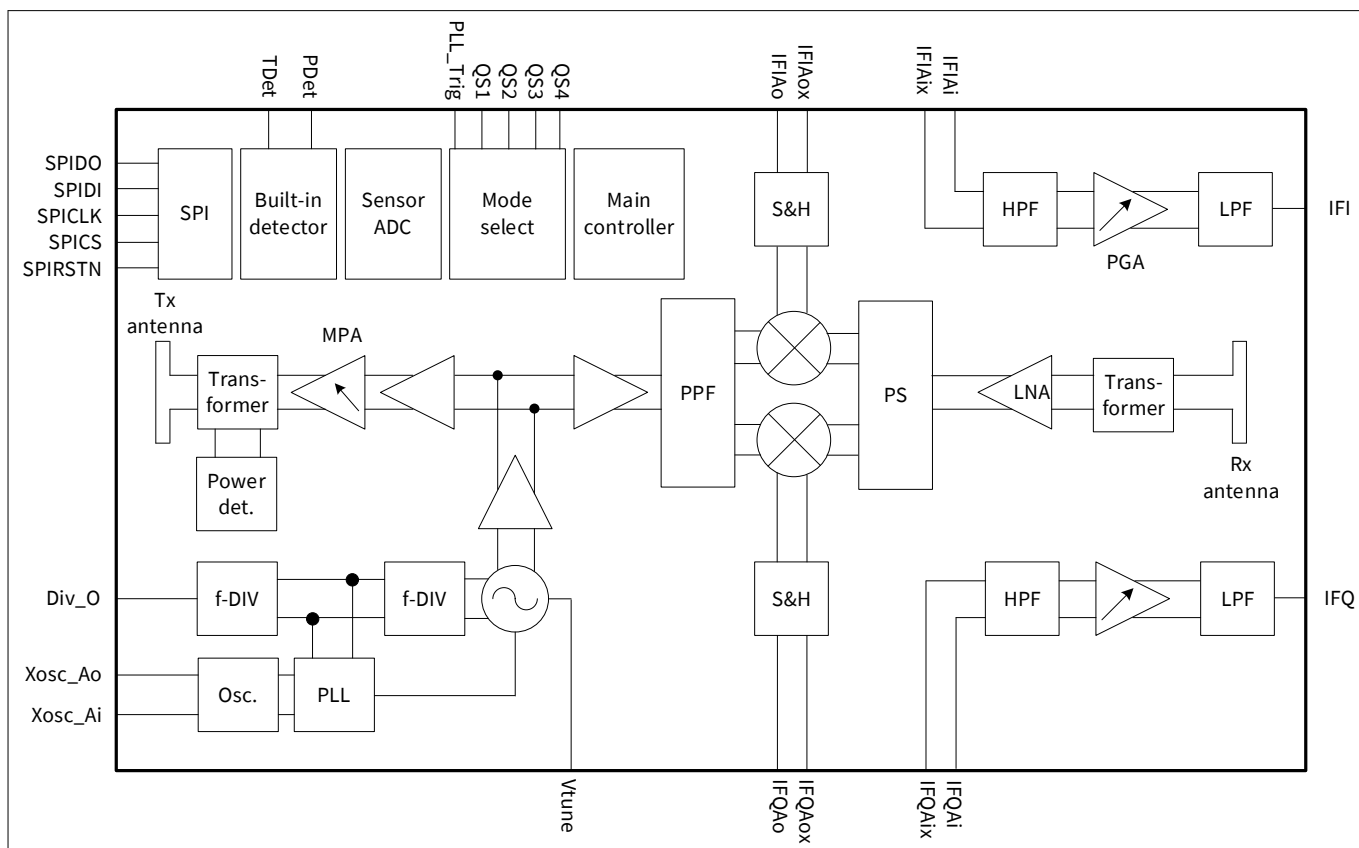
Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
SPI clock period	$T$	20	–	–	ns	50 MHz, with <1% clock jitter
Clock high time	$t_{ch}$	9	–	–	ns	
Clock low time	$t_{cl}$	9	–	–	ns	
Setup time SPIDI	$t_{mos}$	5	–	–	ns	
Hold time SPIDI	$t_{moh}$	5	–	–	ns	
Setup time SPIDO	$t_{mis}$	5	–	–	ns	
Hold time SPIDO	$t_{mih}$	4	–	–	ns	



### 3 Block diagram and pin description

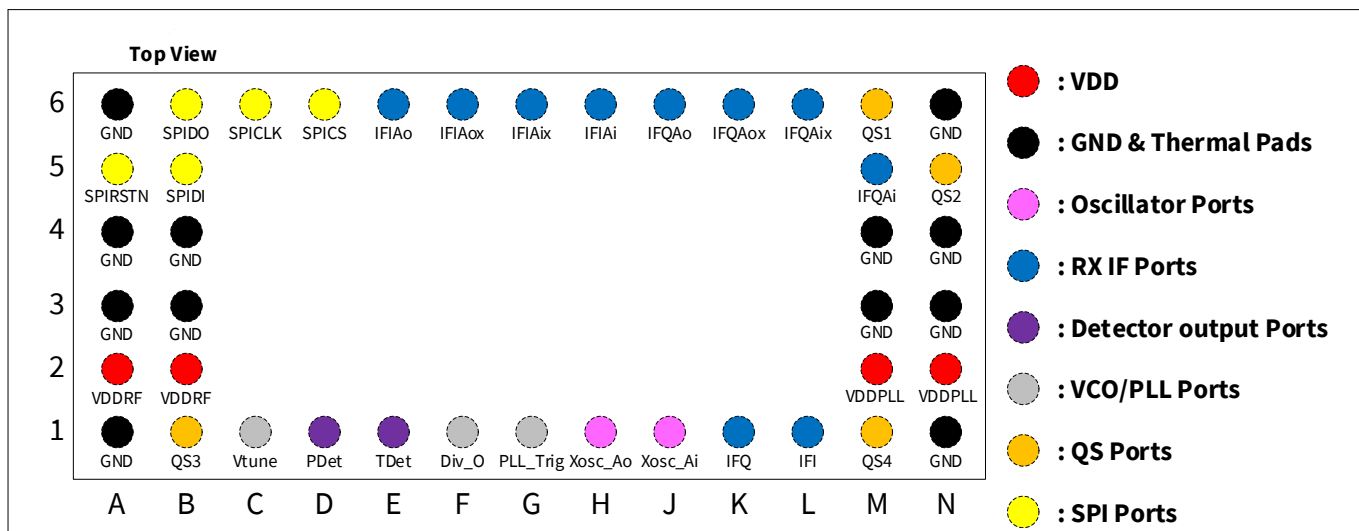
### 3 Block diagram and pin description

### 3.1 Block diagram



**Figure 2** **BGT60LTR11(B)AIP block diagram**

### 3.2 Pin out



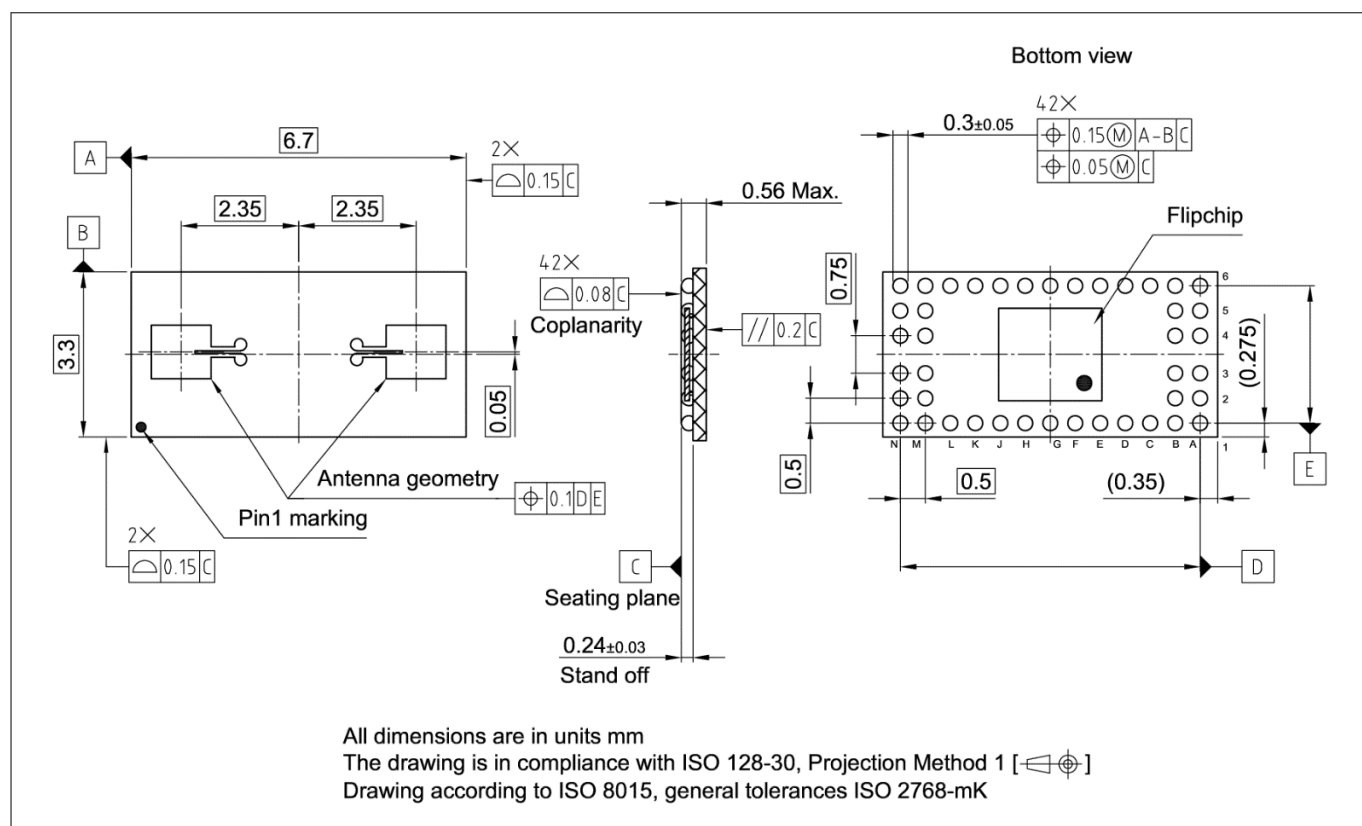
**Figure 3** **Pin out (top view)**

**3 Block diagram and pin description****3.3 Pin definition and function****Table 9 Pin definition and function**

Pin number	Name	Function
A1, N1, A3, B3, M3, N3, A4, B4, M4, N4, A6, N6	GND	Ground
A2, B2	VDDRF	DC supply of 1.5 V to internal RF circuitry
M2, N2	VDDPLL	DC supply of 1.5 V to internal PLL circuitry
M6	QS1	Quad state input 1 – voltage value
N5	QS2	Quad state input 2 or analog input to configure threshold
B1	QS3	Quad state input 3 or analog input to configure hold time
M1	QS4	Quad state input 4
A5	SPIRSTN	SPI reset, active low
B5	SPIDI	SPI data in
B6	SPIDO	SPI data out
C6	SPICLK	SPI clock
D6	SPICS	SPI chip select, active low
E6, F6	IFIAo, IFIAox	Complementary in phase down converter IF output
J6, K6	IFQAo, IFQAox	Complementary quadrature phase down converter IF output
G6, H6	IFIAix, IFIAi	Analog IF input PGA – complementary in phase
L6, M5	IFQAix, IFQAi	Analog IF input PGA – complementary quadrature phase
K1	IFQ	ABB output – Q Channel
L1	IFI	ABB output – I Channel
C1	Vtune	VCO tuning voltage
D1	PDet	Direction of movement detector output
E1	TDet	Motion detector output
F1	DIV_O	Frequency divider output
G1	PLL_Trig	“Advance mode” and “Basic mode” switch
H1	Xosc_Ao	Internal oscillator quartz node
J1	Xosc_Ai	Internal oscillator quartz node

#### 4 Package dimensions and footprint

## 4 Package dimensions and footprint



**Figure 4** Package outline. Top, side and bottom view of PG-UF2BGA-42-1

## Revision history

Document version	Date of release	Description of changes
V2.4	2021-10-11	Updated preliminary datasheet
V2.5	2021-11-05	First formal release version

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