WT59F164
Flash Memory Type
32-bit Microcontroller

Data Sheet

Rev. 1.022

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1. General Description

The WT59F164 is a high-performance 32-Bit Microcontroller. It incorporates the 32-bit RISC CPU operating up to 25 MHz, Flash memory up to 64K bytes and SRAM up to 8K bytes, and rich peripherals / interfaces such as ADC, I^2C, SPI, UART, PWM, H/W CEC, IR receiver, I^2S and USB.

The WT59F164 is suitable for a wide range of applications, such as wireless audio devices, A/V devices, automotive entertainment platform, gaming platform, LED lighting control, medical equipment, PC peripherals and applications where high-speed communication and USB device are required.

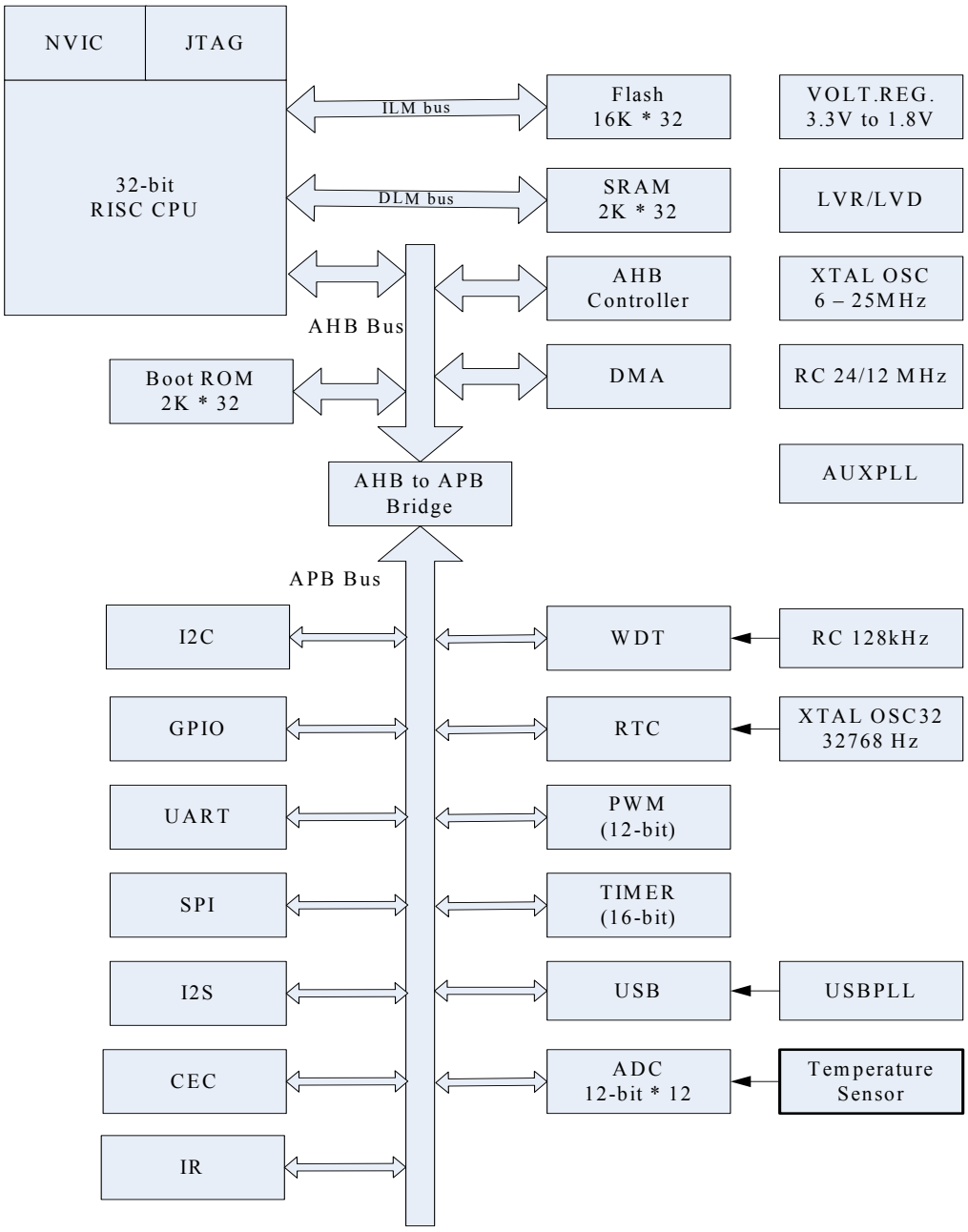
2. Features

The WT59F164 is an advanced 32-bit Microcontroller, and it also provides the following features.

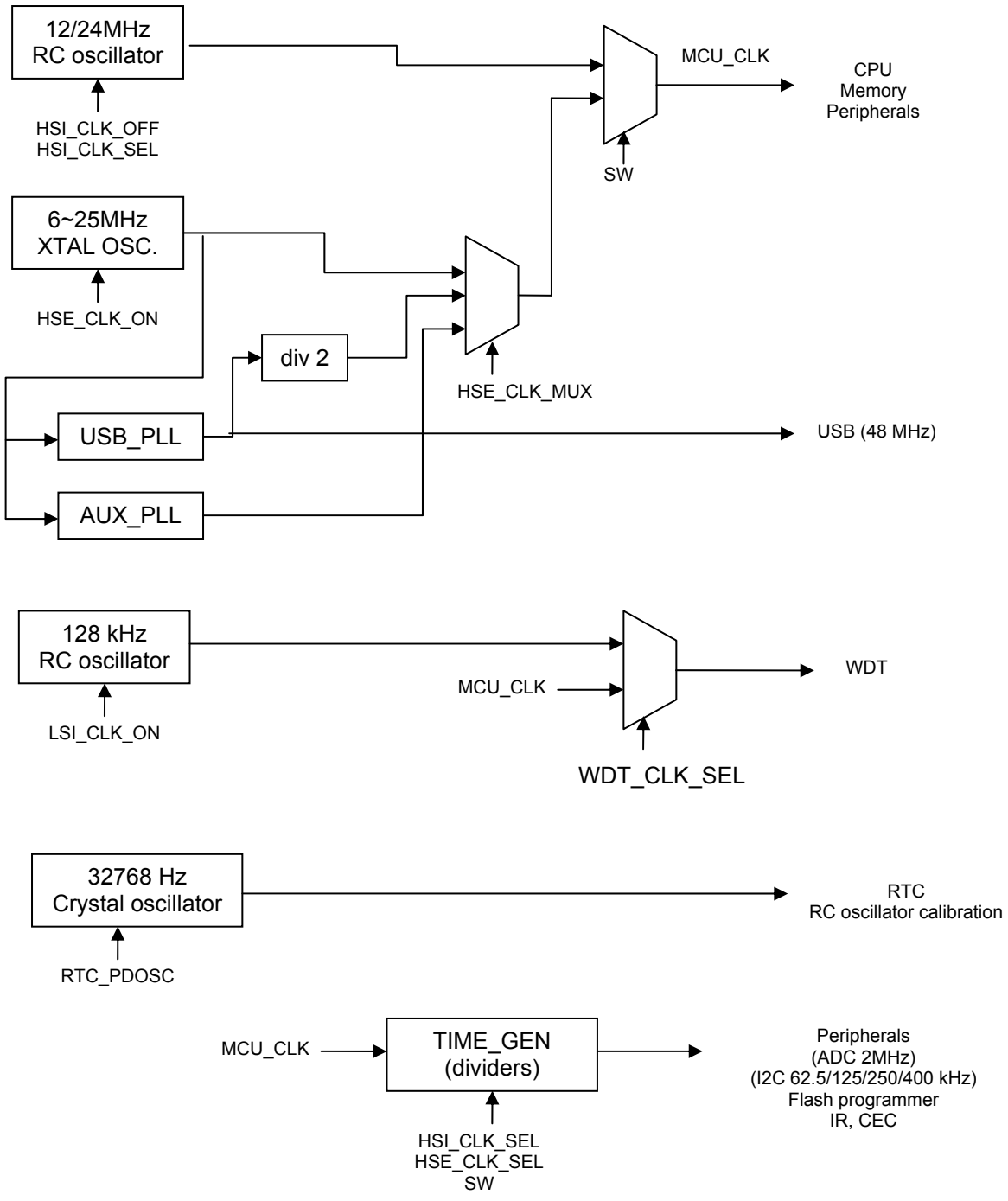
- Embedded 32-bit RISC CPU core
  - 1.3 DMIPS/MHz (Dhrystone 2.1) performance
  - Normal operating mode: 24.576 MHz, 24 MHz, 18.432 MHz, 12 MHz, and 6 MHz
  - Instruction execution time: Min. = 40ns @25 MHz (non-USB applications)
- Memory:
  - Flash memory: 64K bytes (16K * 32)
  - RAM: 8K bytes (2K * 32)
  - Boot ROM: 8K bytes (2K * 32), for USB online upgrade
- CPU clock source
  - Internal RC oscillator 12 MHz/24 MHz
  - External crystal oscillator 6 MHz ~25 MHz
  - Internal PLLs (generated by external crystal oscillator)
- Internal RC 128 kHz for WDT
- External crystal oscillator 32 kHz for RTC counter
- DMA: ADC, I^2C (*4), UART (*6), TIMER (*6), I^2S (*6), USB (*2), SPI (*4)
- Communication interface
  - 2 master/slave I^2C bus (SM bus) up to 400 kHz
  - 2 master/slave SPI up to 12 MHz@main frequency 24 MHz (main frequency/ 2)
  - 3 UARTs (UART0, UART1, UART2) up to 1.5 MHz@main frequency 24 MHz (main frequency/ 16)
  - 1 consumer electronics control (CEC) (with 16 bytes R/W buffer and auto-sending “ACK” bit)
  - 1 master/slave I^2S up to 48 kHz sampling rate, with 3 data input and 3 data output pins
  - 1 USB device controller supports isochronous transfer, which supports eight endpoints including:
    - Endpoint 0: Control transfer Endpoint
    - Endpoint 1~6: Interrupt/Volume transfer endpoint
    - Endpoint 7~8: Asynchronous transfer endpoint (supports DMA)
- Six 16-bit Timer (Timer 0 ~ Timer5) with IC/OC/OCN/PWM, Timer 4 without input and output pins
- Eight 12-bit PWM pins (PWM0 ~PWM7) output with adjustable frequency
- Hardware universal IR receiver with programmable digital filter for noise rejection
- Power on reset, 1-level low VDD reset (LVR), and 8-level low VDD detector (LVD)
- 12-channel 12-bit A/D converter (ADC0 ~ ADC11) with 12 selectable inputs (channel 11 is fixed for temperature sensor)
- Two built-in PLL circuits can use external crystal oscillator to produce a variety of frequencies for MCU and USB
- Temperature sensor (±3℃)

- Internal RC oscillator 12 MHz/24 MHz can be calibrated ±1% with 32 kHz crystal and ±3% without crystal
- Support two wires JTAG for ISP & ICE mode
- 47 programmable bi-directional I/O pins
- Read Out Protection
- Emulated E^2PROM
- Operating voltage range: 2.0V ~ 3.6V
- Operating temperature: -40℃ to +85℃
- ESD protection HBM > 4KV, MM > 400V
- Package type: LQFP64, LQFP48, QFN32

3. Block Diagram

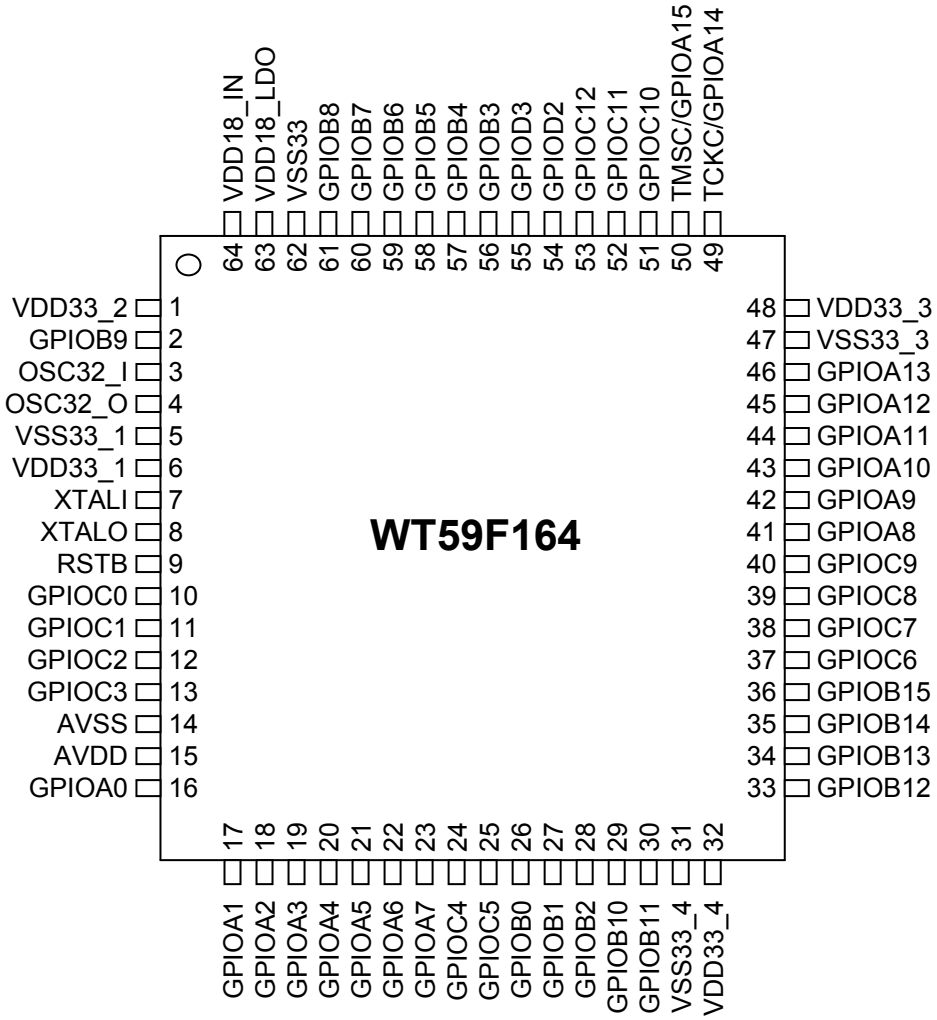


3.1 System Clock Tree



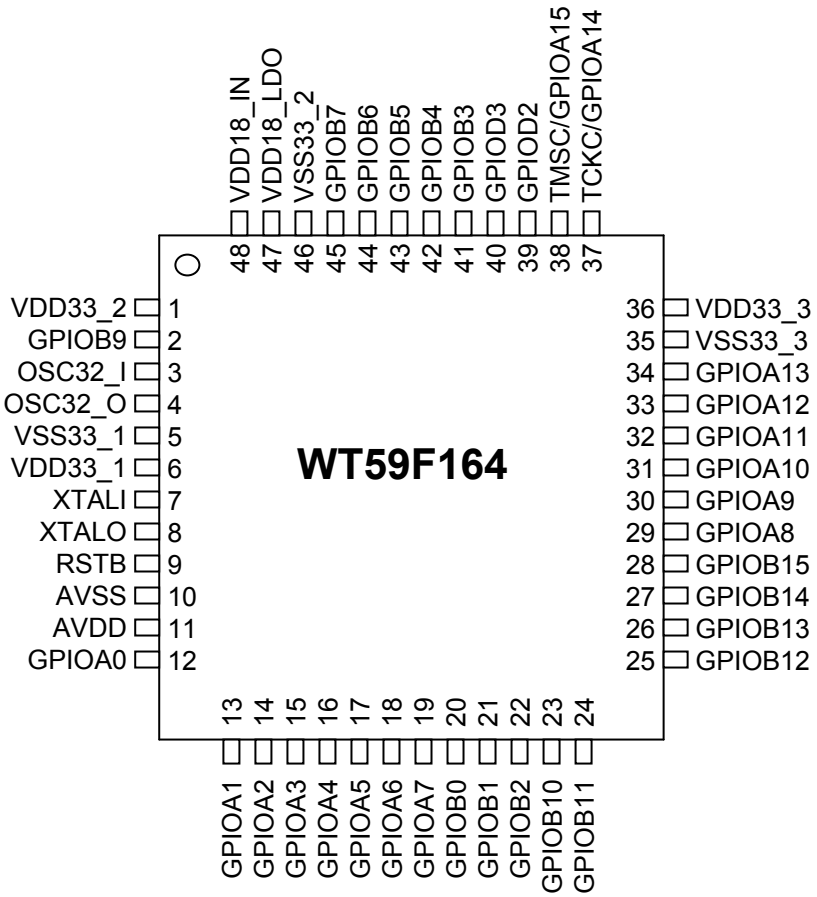
4. Pin Configuration

WT59F164-RG64AWT 64-Pin LQFP



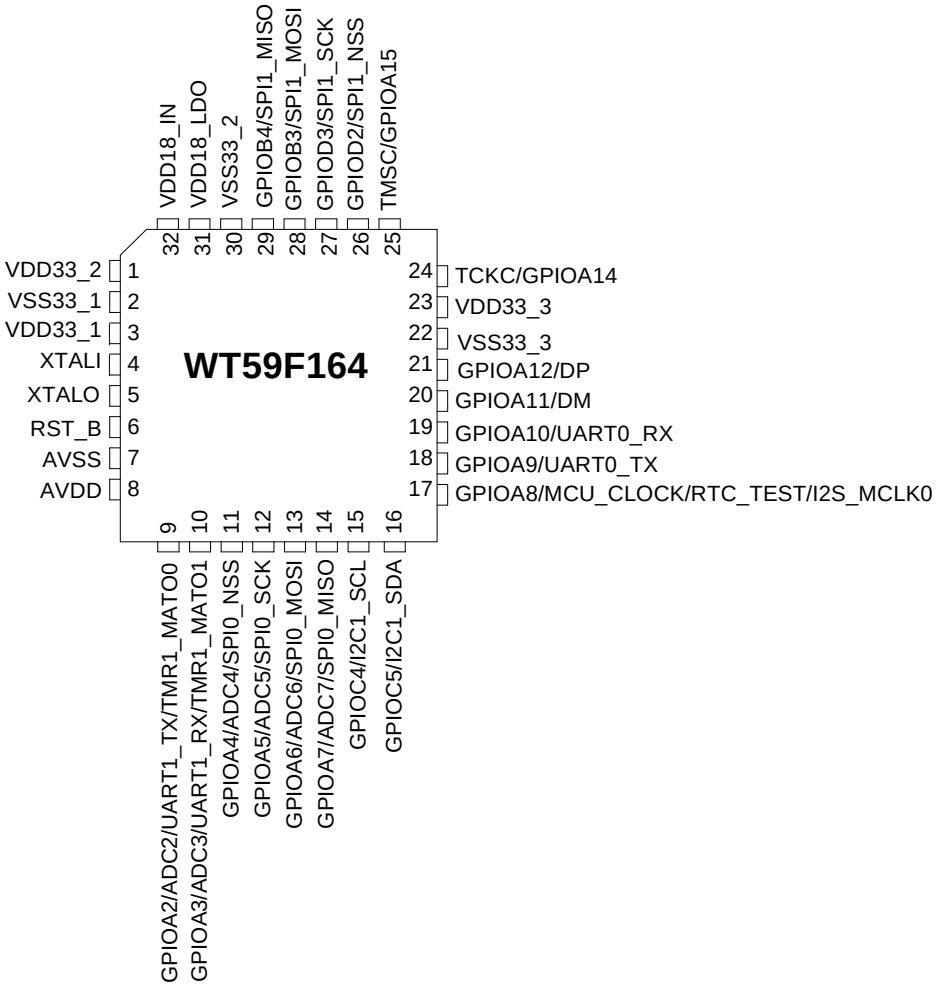
WT59F164 LQFP64 Package (7mm x 7mm x 1.4mm)

WT59F164-RG48AWT 48-Pin LQFP



WT59F164 LQFP48 Package (7mm x 7mm x 1.4mm)

WT59F164-UG32AWT 32-Pin QFN



WT59F164 QFN32 Package (5mm x 5mm x 0.75mm)

4.1 Pin Description

4.1.1 64-Pin LQFP, 48-Pin LQFP & 32-Pin QFN pin description

Pin Number			Pin Name		Primary Function	
RG64AWT	RG48AWT	QFN32		I/O	Description	Circuit Type
1	1	1	VDD33_2	P	3.3V Power	
2	2		GPIOB9/ PWM0/ TMR2_CAPI0	I/O	GPIOB9: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor input, input with internal pull-down resistor or input without internal pull-up/pull-down resistor PWM0: PWM0 output pin TMR2_CAPI0: External input pin 0 of Counter 2	A
3	3		OSC32_I	I	32.768 kHz XTAL oscillator input	
4	4		OSC32_O	O	32.768 kHz XTAL oscillator output	
5	5	2	VSS33_1	P	3.3V Ground	
6	6	3	VDD33_1	P	3.3V Power	
7	7	4	XTALI	I	18.432 MHz XTAL oscillator input (24.576 MHz/24 MHz/12 MHz/6 MHz)	
8	8	5	XTALO	O	18.432 MHz XTAL oscillator output (24.576 MHz/24 MHz/12 MHz/6 MHz)	
9	9	6	RST_B	I	Reset pin, active low	
10			GPIOC0/ ADC10/ TMR5_CAPI0	I/O	GPIOC0: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor ADC10: ADC input 10 TMR5_CAPI0: External input pin 0 of Counter 5	A
11			GPIOC1/ TMR5_CAPI1	I/O	GPIOC1: GPIO with programmable high current sink/source push-pull output, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor TMR5_CAPI1: External input pin 1 of Counter 5	A

Pin Number			Pin Name		Primary Function	
RG64A WT	RG48A WT	QFN32		I/O	Description	Circuit Type
12			GPIOC2/ TMR5_MATO0	I/O	GPIOC2: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor TMR5_MATO0: External output pin 0 of Counter 5	A
13			GPIOC3/ TMR5_MATO1	I/O	GPIOC3: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor TMR5_MATO1: External output pin 1 of Counter 5	A
14	10	7	AVSS	P	Analog Ground	
15	11	8	VREF+	I	ADC reference voltage input	
15	11	8	AVDD	P	Analog 3.3V Power	
16	12		GPIOA0/ ADC0/ TMR1_CAPI0	I/O	GPIOA0: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor ADC0: ADC input 0 TMR1_CAPI0: External input pin 0 of Counter 1	A
17	13		GPIOA1/ ADC1/ TMR1_CAPI1	I/O	GPIOA1: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor ADC1: ADC input 1 TMR1_CAPI1: External input pin 1 of Counter 1	A

Pin Number			Pin Name		Primary Function	
RG64AWT	RG48AWT	QFN32		I/O	Description	Circuit Type
18	14	9	GPIOA2/ ADC2/ UART1_TX/ TMR1_MATO0	I/O	GPIOA2: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor ADC2: ADC input 2 UART1_TX: Data Transmit pin of UART1 TMR1_MATO0: External output pin 0 of Counter 1	A
19	15	10	GPIOA3/ ADC3/ UART1_RX/ TMR1_MATO1	I/O	GPIOA3: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor ADC3: ADC input 3 UART1_RX: Data Receive pin of UART1 TMR1_MATO1: External output pin 1 of Counter 1	A
20	16	11	GPIOA4/ ADC4/ SPI0_NSS	I/O	GPIOA4: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor ADC4: ADC input 4 SPI0_NSS: NSS pin of SPI0	A
21	17	12	GPIOA5/ ADC5/ SPI0_SCK	I/O	GPIOA5: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor ADC5: ADC input 5 SPI0_SCK: SCK pin of SPI0	A
22	18	13	GPIOA6/ ADC6/ SPI0_MOSI	I/O	GPIOA6: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor ADC6: ADC input 3 SPI0_MOSI: MOSI pin of SPI0	A

Pin Number			Pin Name		Primary Function	
RG64AWT	RG48AWT	QFN32		I/O	Description	Circuit Type
23	19	14	GPIOA7/ ADC7/ SPI0_MISO	I/O	GPIOA7: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor ADC7: ADC input 7 SPI0_MISO: MISO pin of SPI0	A
24		15	GPIOC4/ I2C1_SCL	I/O	GPIOC4: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor I2C1_SCL: SCL pin of I²C1	A
25		16	GPIOC5/ I2C1_SDA	I/O	GPIOC5: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor I2C1_SDA: SDA pin of I²C1	A
26	20		GPIOB0/ ADC8/ PWM1	I/O	GPIOB0: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor ADC8: ADC input 8 PWM1: Output pin of PWM1	A
27	21		GPIOB1/ ADC9/ PWM2/ HDMI_CEC	I/O	GPIOB1: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor ADC9: ADC input 9 PWM2: Output pin of PWM2 HDMI_CEC: HDMI CEC pin	A

Pin Number			Pin Name		Primary Function	
RG64A WT	RG48A WT	QFN32		I/O	Description	Circuit Type
28	22		GPIOB2/ IR/ PWM3	I/O	GPIOB2: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor IR: IR pin PWM3: Output pin of PWM3	A
29	23		GPIOB10/ PWM4/ UART2_TX	I/O	GPIOB10: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor PWM4: Output pin of PWM4 UART2_TX: Data Transmit pin of UART2	A
30	24		GPIOB11/ PWM5/ UART2_RX	I/O	GPIOB11: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor PWM5: Output pin of PWM5 UART2_RX: Data Receive pin of UART2	A
31			VSS33_4	P	3.3V Ground	
32			VDD33_4	P	3.3V Power	
33	25		GPIOB12/ I2S_BCLK0/ TMR0_CAPI0	I/O	GPIOB12: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor I2S_BCLK0: BLCK pin of I^2S TMR0_CAPI0: External input pin 0 of Counter 0	A
34	26		GPIOB13/ I2S_LRCLK0/ TMR0_CAPI1	I/O	GPIOB13: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor I2S_LRCLK0: LRCLK pin of I^2S TMR0_CAPI1: External input pin 1 of Counter 0	A

Pin Number			Pin Name		Primary Function	
RG64AWT	RG48AWT	QFN32		I/O	Description	Circuit Type
35	27		GPIOB14/ I2S_DI0/ TMR0_MATO0	I/O	GPIOB14: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor I2S_DI0: DI0 pin of I^2S TMR0_MATO0: External output pin 0 of Counter 0	A
36	28		GPIOB15/ I2S_DO0/ TMR0_MATO1	I/O	GPIOB15: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor I2S_DO0: DO0 pin of I^2S TMR0_MATO1: External output pin 1 of Counter 0	A
37			GPIOC6/ I2S_DI1/ TMR3_CAPI0	I/O	GPIOC6: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor I2S_DI1: DI1 pin of I^2S TMR3_CAPI0: External input pin 0 of Counter 3	A
38			GPIOC7/ I2S_DO1/ TMR3_CAPI1	I/O	GPIOC7: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor I2S_DO1: DO1 pin of I^2S TMR3_CAPI0: External input pin 1 of Counter 3	A
39			GPIOC8/ I2S_DI2/ TMR3_MATO0	I/O	GPIOC8: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor I2S_DI2: DI2 pin of I^2S TMR3_MATO0: External output pin 0 of Counter 3	A

Pin Number			Pin Name		Primary Function	
RG64AWT	RG48AWT	QFN32		I/O	Description	Circuit Type
40			GPIOC9/ I2S_DO2/ TMR3_MATO1	I/O	GPIOC9: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor I2S_DO2: DO2 pin of I^2S TMR3_MATO0: External output pin 1 of Counter 3	A
41	29	17	GPIOA8/ MCU_CLOCK/ RTC_TEST/ I2S_MCLK0	I/O	GPIOA8: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor MCU_CLOCK: Output pin of MCU Clock RTC_TEST: Input pin of RTC Clock I2S_MCLK0: MCLK pin of I^2S	A
42	30	18	GPIOA9/ UART0_TX	I/O	GPIOA9: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor UART0_TX: Data Transmit pin of UART0	A
43	31	19	GPIOA10/ UART0_RX	I/O	GPIOA10: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor UART0_RX: Data Receive pin of UART0	A
44	32	20	GPIOA11/ DM	I/O	GPIOA11: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor DM: USB DM pin	A

Pin Number			Pin Name		Primary Function	
RG64AWT	RG48AWT	QFN32		I/O	Description	Circuit Type
45	33	21	GPIOA12/ DP	I/O	GPIOA12: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor DP: USB DP pin	A
46	34		GPIOA13/ PWM6	I/O	GPIOA13: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor PWM6: Output pin of PWM6	A
47	35	22	VSS33_3	P	3.3V Ground	
48	36	23	VDD33_3	P	3.3V Power	
49	37	24	TCKC/ GPIOA14	I/O	TCKC: TCKC pin of 2-wire JTAG GPIOA14: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor	A
50	38	25	TMSC/ GPIOA15	I/O	TCKC: TMSC pin of 2-wire of JTAG GPIOA15: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor	A
51			GPIOC10/ PWM7	I/O	GPIOC10: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor PWM7: Output pin of PWM7	A
52			GPIOC11	I/O	GPIOC11: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor	A

Pin Number			Pin Name		Primary Function	
RG64AWT	RG48AWT	QFN32		I/O	Description	Circuit Type
53			GPIOC12	I/O	GPIOC12: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor	A
54	39	26	GPIOD2/ SPI1_NSS	I/O	GPIOD2: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor SPI1_NSS: NSS pin of SPI1	A
55	40	27	GPIOD3/ SPI1_SCK	I/O	GPIOD3: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor SPI1_SCL: SCK pin of SPI1	A
56	41	28	GPIOB3/ SPI1_MOSI	I/O	GPIOB3: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor SPI1_MOSI: MOSI pin of SPI1	A
57	42	29	GPIOB4/ SPI1_MISO	I/O	GPIOB3: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor SPI1_MISO: MISO pin of SPI1	A
58	43		GPIOB5/ TMR2_CAPI1	I/O	GPIOB5: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor TMR2_CAPI1: External input pin 1 of Counter 2	A

Pin Number			Pin Name		Primary Function	
RG64A WT	RG48A WT	QFN32		I/O	Description	Circuit Type
59	44		GPIOB6/ I2C0_SCL/ TMR2_MATO0	I/O	GPIOB6: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor I2C0_SCL: SCL pin of I²C0 TMR2_MATO0: External output pin 0 of Counter 2	A
60	45		GPIOB7/ I2C0_SDA/ TMR2_MATO1	I/O	GPIOB7: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor I2C0_SDA: SDA pin of I²C0 TMR2_MATO1: External output pin 1 of Counter 2	A
61			GPIOB8	I/O	GPIOB8: GPIO with programmable high current sink/source push-pull, open drain output, input with internal pull-up resistor, input with internal pull-down resistor or input without internal pull-up/pull-down resistor	A
62	46	30	VSS33_2	P	3.3V Ground	
63	47	31	VDD18_LDO	P	1.8V LDO filter (connect to 4.7uF capacitor)/ 1.8V output	
64	48	32	VDD18_IN	P	1.8V power input	

Note: All I/O pins age floating on Reset status.

4.1.2 Package Type Reference

I/O Function \ Package Type	LQFP-64	LQFP-48	QFN-32
I^2S	3	1	0
I^2C	2	1	1
SPI	2	2	2
USB	1	1	1
UART	3	3	2
ADC	11	10	6
PWM	8	7	0
GPIO (shared with all pins with special functions)	47	33	19

4.2 Pin Summary

Explain each pin function in details.

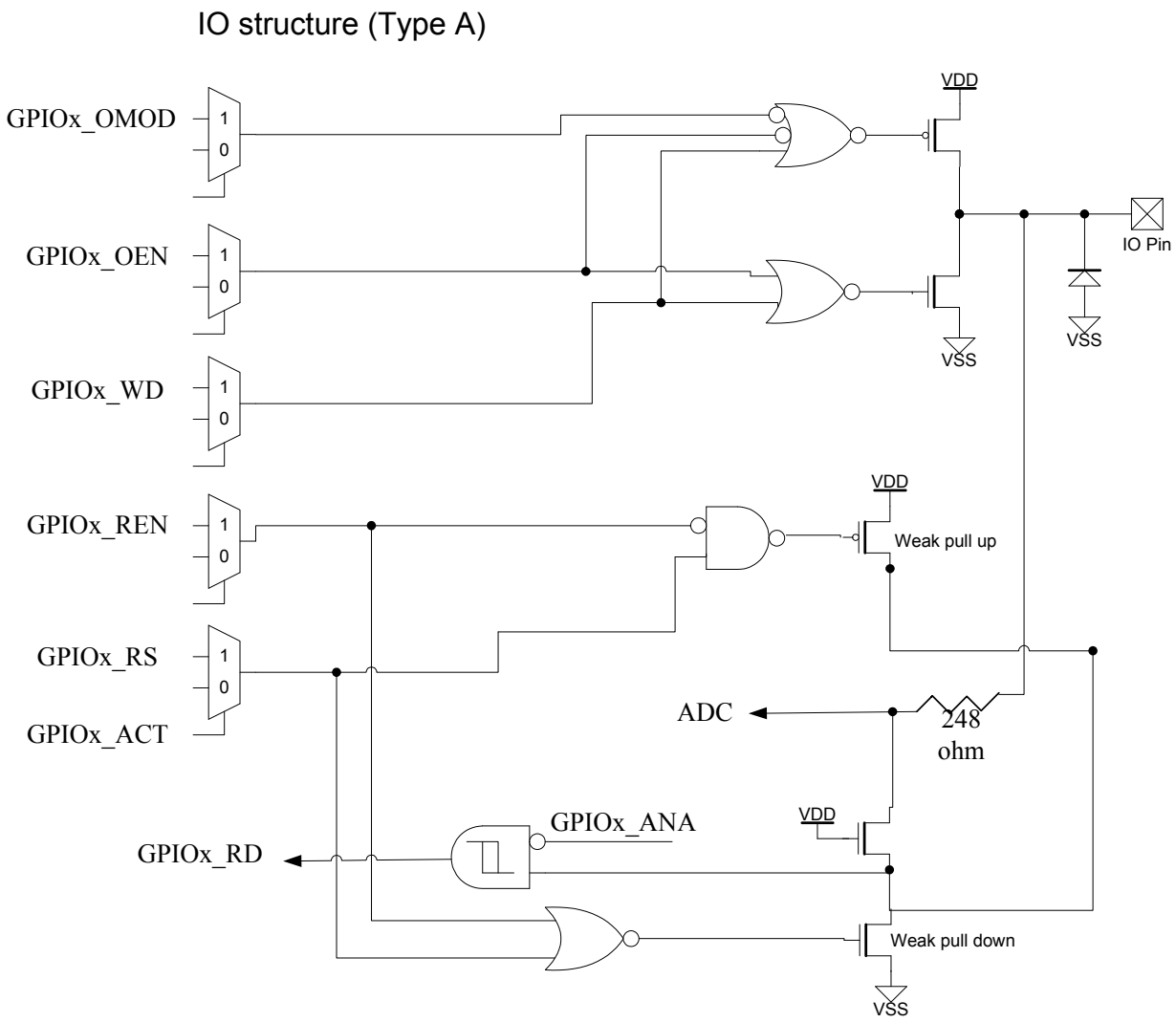
Pin Name	Type	Description
PORT		
GPIOA0 ~ GPIOA15	I/O	16-bit bidirectional general-purpose I/O port
GPIOB0 ~ GPIOB15	I/O	16-bit bidirectional general-purpose I/O port
GPIOC0 ~ GPIOC12	I/O	13-bit bidirectional general-purpose I/O port
GPIOD2 ~ GPIOD3	I/O	2-bit bidirectional general-purpose I/O port
Timer		
TMR0_MATO0	O	Timer/Counter 0 output
TMR0_MATO1	O	Timer/Counter 0 output
TMR0_CAPI0	I	Timer/Counter 0 external input
TMR0_CAPI1	I	Timer/Counter 0 external input
TMR1_MATO0	O	Timer/Counter 1 output
TMR1_MATO1	O	Timer/Counter 1 output
TMR1_CAPI0	I	Timer/Counter 1 external input
TMR1_CAPI1	I	Timer/Counter 1 external input
TMR2_MATO0	O	Timer/Counter 2 output
TMR2_MATO1	O	Timer/Counter 2 output
TMR2_CAPI0	I	Timer/Counter 2 external input
TMR2_CAPI1	I	Timer/Counter 2 external input
TMR3_MATO0	O	Timer/Counter 3 output
TMR3_MATO1	O	Timer/Counter 3 output
TMR3_CAPI0	I	Timer/Counter 3 external input
TMR3_CAPI1	I	Timer/Counter 3 external input
TMR5_MATO0	O	Timer/Counter 5 output
TMR5_MATO1	O	Timer/Counter 5 output
TMR5_CAPI0	I	Timer/Counter 5 external input
TMR5_CAPI1	I	Timer/Counter 5 external input
IR		
IR	I	IR receiver input
HDMI CEC		
HDMI_CEC	I/O	HDMI CEC pin
PWM		
PWM0	O	PWM 0 output
PWM1	O	PWM 1 output
PWM2	O	PWM 2 output
PWM3	O	PWM 3 output

Pin Name	Type	Description
PWM4	O	PWM 4 output
PWM5	O	PWM 5 output
PWM6	O	PWM 6 output
PWM7	O	PWM 7 output
UART		
UART0_RX	I	UART0 receive
UART0_TX	O	UART0 transmit
UART1_RX	I	UART1 receive
UART1_TX	O	UART1 transmit
UART2_RX	I	UART2 receive
UART2_TX	O	UART2 transmit
SPI		
SPI0_NSS	O	SPI0 enable
SPI0_SCK	I/O	SPI0 interface clock signal
SPI0_MOSI	I/O	SPI0 data pin MOSI (Master Output; Slave Input)
SPI0_MISO	I/O	SPI0 data pin MISO (Master Input; Slave Output)
SPI1_NSS	O	SPI1 enable
SPI1_SCK	I/O	SPI1 interface clock signal
SPI1_MOSI	I/O	SPI1 data pin MOSI (Master Output; Slave Input)
SPI1_MISO	I/O	SPI1 data pin MISO (Master Input; Slave Output)
ADC		
ADC0 ~ ADC10	I	11 Analog/Digital Input pins
I²C		
I2C0_SCL	I/O	I²C0 interface clock pin
I2C0_SDA	I/O	I²C0 interface data pin
I2C0_SCL	I/O	I²C1 interface clock pin
I2C0_SDA	I/O	I²C1 interface data pin
VCC & VSS		
VDD33_1~VDD33_4	P	3.3V power input
VSS33_1~ VSS33_4	P	3.3V ground
VDD18_LDO	P	1.8V power output & filter
VDD18_IN	P	1.8V power input
OSC		
XTALI	I	Main oscillator input
XTALO	O	Main oscillator output
OSC32_I	I	32.768 kHz oscillator input
OSC32_O	O	32.768 kHz oscillator output

Pin Name	Type	Description
RESET		
RST_B	I	CPU reset pin
ISP & ICE		
TCKC	I/O	2-wire JTAG ISP & ICE interface
TMSC	I/O	2-wire JTAG ISP & ICE interface

4.3 Port Structure

I/O Structure (Type A)



5. Normal Function

5.1 CPU

The WT59F164 has an embedded 32-bit RISC CPU with 1.3 DMIPS/MHz (Dhrystone 2.1) high-performance computing capacity. With 24-bit space addressable and 32-bit data access functions, the operating frequency can be up to 25 MHz.

WT59F164 CPU embedded sixteen 32-bit and two 64-bit General Purpose Register (GPR):

- 32-bit General Purpose Register: r0, r1, r2, r3, r4, r5, r6, r7, r8, r9, r10, r15, r28, r29, r30, r31
- 64-bit General Purpose Register: D0, D1

General Purpose Register (GPR) Table:

Register Name	32/16-bit (5)	16-bit (4)	16-bit (3)	Comments
r0	a0	h0	o0	
r1	a1	h1	o1	
r2	a2	h2	o2	
r3	a3	h3	o3	
r4	a4	h4	o4	
r5	a5	h5	o5	Implied register for beqs38 and bnes38
r6	s0	h6	o6	Saved by callee
r7	s1	h7	o7	Saved by callee
r8	s2	h8		Saved by callee
r9	s3	h9		Saved by callee
r10	s4	h10		Saved by callee
r15	ta			Temporary register for assembler Implied register for slt (s|i) 45, b[eq|ne]zs8
r28	fp			Frame pointer/Saved by callee
r29	gp			Global pointer
r30	lp			Link pointer
r31	sp			Stack pointer

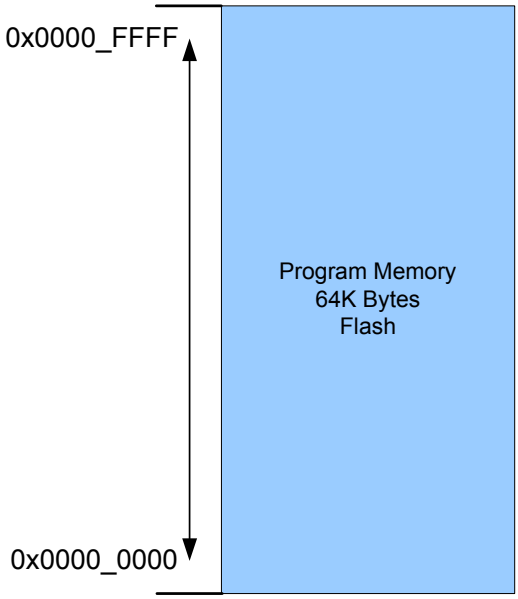
5.2 RAM

The WT59F164 consists of 8K bytes of SRAM accessed at CPU clock speed with no wait states. Its location is from 0x0010_0000 to 0x0010_1FFF.

5.3 Flash Memory

The WT59F164 consists of 64K bytes of embedded flash memory, which can be served as general Program memory or emulated E^2PROM (0x0000_0000 ~ 0x0000_FFFF) with features as below:

- Flash memory: 64K Bytes
- In-System Programming (ISP)
- Over 10 years Data Retention
- Read Out Protection and Code Encryption
- Emulated E^2PROM function



5.4 Boot ROM

8K Bytes of embedded Boot ROM is available for storing a boot code. After reset, the CPU will run the boot code for about 3.5ms, and then jump to user's program which is stored in the flash memory.

5.5 Memory Mapping

Memory Mapping Table

Index	Function	Description
0x0000_0000~0x0000_FFFF	64K Flash Memory	ILM Bus
0x0001_0000~0x000F_FFFF	Reserved	
0x0010_0000~0x0010_1FFF	8K SRAM	DLM Bus
0x0010_2000~0x001F_5BFF	Reserved	
0x001F_5C00~0x001F_5FFF	PWM0	APB Bus
0x001F_6000~0x001F_63FF	PWM1	
0x001F_6400~0x001F_67FF	Reserved	
0x001F_6800~0x001F_6BFF	GPIO A – D	
0x001F_6C00~0x001F_FFFF	Reserved	
0x0020_0000~0x0020_03FF	System Control	
0x0020_0400~0x0020_07FF	Flash Programmer	
0x0020_0800~0x0020_0BFF	WDT	
0x0020_0C00~0x0020_0FFF	Wake Up & Interrupt	
0x0020_1000~0x0020_13FF	RTC	
0x0020_1400~0x0020_17FF	CEC	
0x0020_1800~0x0020_1BFF	IR Receiver	
0x0020_1C00~0x0020_1FFF	Timer0	
0x0020_2000~0x0020_23FF	Timer1	
0x0020_2400~0x0020_27FF	Timer2	
0x0020_2800~0x0020_2BFF	Timer3	
0x0020_2C00~0x0020_2FFF	Timer4	
0x0020_3000~0x0020_33FF	Timer5	
0x0020_3400~0x0020_37FF	UART0	
0x0020_3800~0x0020_3BFF	UART1	
0x0020_3C00~0x0020_3FFF	UART2	
0x0020_4000~0x0020_43FF	Reserved	
0x0020_4400~0x0020_47FF	SPI0	
0x0020_4800~0x0020_4BFF	SPI1	
0x0020_4C00~0x0020_4FFF	Reserved	
0x0020_5000~0x0020_53FF	Reserved	
0x0020_5400~0x0020_57FF	I^2C0	
0x0020_5800~0x0020_5BFF	I^2C1	
0x0020_5C00~0x0020_63FF	Reserved	
0x0020_6400~0x0020_67FF	ADC	
0x0020_6800~0x0020_6BFF	Reserved	
0x0020_6C00~0x0020_6FFF	I^2S	
0x0020_7000~0x0020_77FF	Reserved	
0x0020_7800~0x0020_7BFF	USB	
0x0020_7C00~0x002F_FFFF	Reserved	

Index	Function	Description
0x0030_0000~0x0030_03FF	DMA	AHB Bus
0x0030_0400~0x003F_FFFF	Reserved	
0x0040_0000~0x0040_1FFF	Boot ROM	
0x0040_2000~0x00FF_FFFF	Reserved	Reserved Space

Note:

1. Refer to 5.7 "Reset" section for the initial value of SFR.

2. Other special function registers will be discussed in chapter 6.

5.6 In-System Programming (ISP)

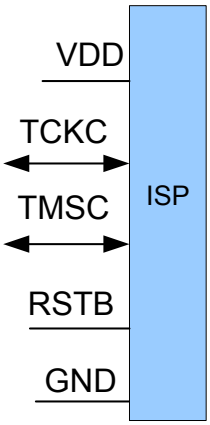
In-System Programming function allows users to perform programming on the target board directly without removing any components.

ISP interface adopts:

2-wire JTAG: VDD, GND (VSS), TCKC, TMSC, RSTB if the target board already has VDD power, then no need to connect VDD

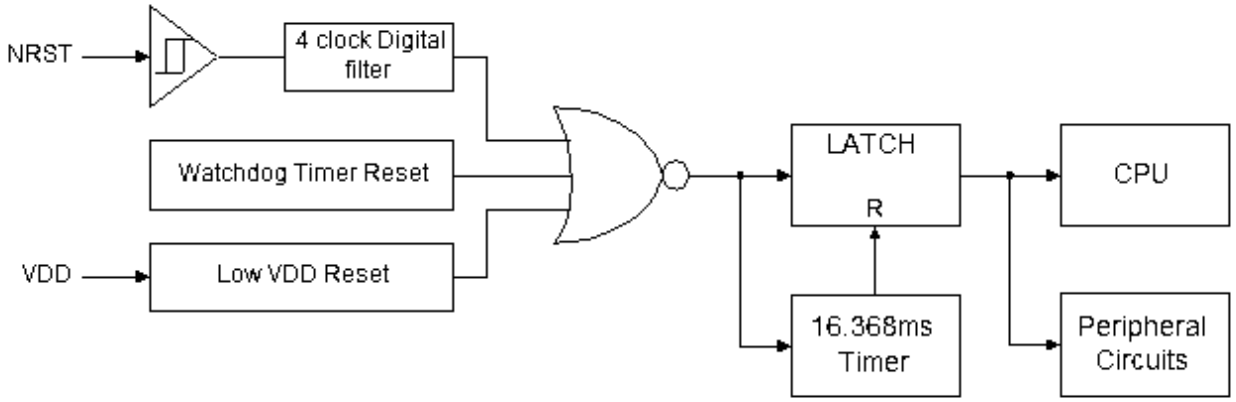
USB interface: by USB signal VDD, GND (VSS), DP, DM

The figure below illustrates pins of 2-wire JTAG ISP interface.



5.7 Reset

The WT59F164 has three reset generation sources: External NRST pin Reset, Low Voltage Reset, Watchdog Reset. All reset signals will last 16*12*1024* (OSC clock), awaiting system stable. During reset, almost all registers are set to their initial values. The figure below shows the block diagram of reset logic.



NRST

The NRST-Reset happens when there is a low level on the RSTB pin. (referring to the DC characteristics sections for more details.)

Low Voltage Reset (LVR)

The Low-VDD-Reset is generated when VDD18 is below 1.4V and last 1.5us. LVR can be disabled by register DIS_LVR.

Watchdog Timer Reset

The Watchdog-Timer-Reset happens when the watchdog timer is time out. The function can be disabled by program. Please refer to the Watchdog Timer section 6.9 for more details.

Reset Status

When above condition occurred, all registers are set to their initial values. GPR contents are described in the following text. XFR contents will be discussed in section 6.1.

The initial value of GPR after Reset (as shown below):

GPR	Initial Value
r0	0x0000_0000
r1	0x0000_0000
r2	0x0000_0000
r3	0x0000_0000

GPR	Initial Value
r4	0x0000_0000
r5	0x0000_0000
r6	0x0000_0000
r7	0x0000_0000
r8	0x0000_0000
r9	0x0000_0000
r10	0x0000_0000
r15	0x0000_0000
r28	0x0000_0000
r30	0x0000_0000
r31	0x0000_0000
D0	0x0000_0000_0000_0000
D1	0x0000_0000_0000_0000

Initial Load after Reset

In addition to the 64K of Flash ROM for storing program code, the WT59F164 includes additional 2K bytes of Flash ROM space (two Pages, Page 1K bytes each), called the Information Block, available to store some Register initial value. It is automatically loaded into the corresponding special register after reset with the relevant characteristics as follows:

- Initial load register:
  - CAL_LP18[2:0] (0x0020_0030 bit[6:4])
  - CALIBRATE18[2:0] (0x0020_0030 bit[2:0])
  - HSI_CLK_SEL (0x0020_002C bit[7])
  - HSI_COARSE_SEL[2:0] (0x0020_002C bit[6:4])
  - HSI_FINE_SEL[3:0] (0x0020_002C bit[3:0])
  - HSE_CLK_SEL[2:0] (0x0020_0000 bit[4:2])
  - HSEON (0x0020_0000 bit[1])
  - JTAG_EN (0x0020_0000 bit[2])
  - SW (0x0020_0000 bit[0])

- After reset 14.336ms, and read first bytes is AAH, then load flash information block data to register. The Information Block bytes are as follows:
  - 0x00[7:0]: check initial load magic word #AA (load enable)
  - 0x04[5:0]: {CAL_LP18[2:0], CALIBRATE18[2:0]}
  - 0x08[7:0]: {HSI_CLK_SEL, HSI_COARSE_SEL[2:0], HSI_FINE_SEL[3:0]}, the registers are loaded at about 20ms after reset.
  - 0x0C[3:0]: {HSE_CLK_SEL[2:0], HSEON}
  - 0x10[2,0]: {JTAG_EN, SW}, the registers are loaded at about 20ms after reset.
  - 0x200[7:0]: check flash protection magic word #AA (protection disable).

- We store factory calibration data on the second page of information block of flash, please don't modify them.
  - 0x400[7:0]: equals to 0xAA indicates the setting value has been stored
  - 0x404[5:0]: {CAL_LP18[2:0], CALIBRATE18[2:0]} (1.8V Regulator)

- 0x408[7:0]: {1'b0, HSI_COARSE_SEL[2:0], HSI_FINE_SEL[3:0]} (For 12 MHz RCOSC)
- 0x40C[7:0]: {1'b1, HSI_COARSE_SEL[2:0], HSI_FINE_SEL[3:0]} (For 24 MHz RCOSC)
- 0x414[11:0]: {TEMP_REF} (ADC value of temperature sensor output @ 25℃ & 3.3V)

➢ The following information words are reserved for future's USB ISP function, please don't use them but erase.

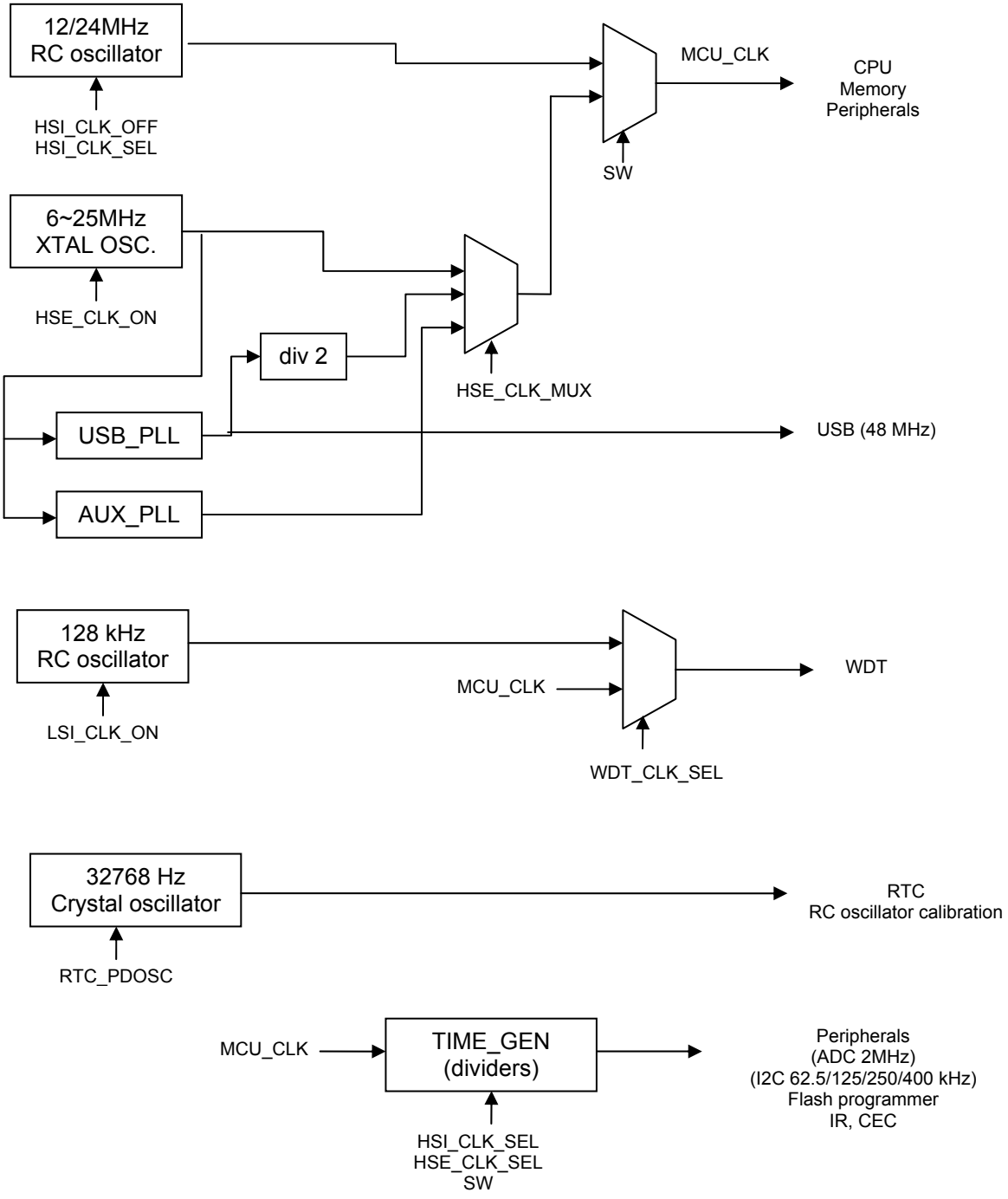
- 0x20[7:0]: Magic word of USB ISP (set 0x55AA33CC to enable USB ISP function)
- 0x24[15:0]: SYS_USBPLL_CTRL[15:0]
- 0x28[1:0]: HSE_CLK_MUX[1:0]
- 0x2C[31:0]: {USB ISP PID[15:0], USB ISP VID[15:0]}

5.8 System Clock and Clock Sources

The WT59F164 contains four clock sources: internal 12 MHz /24 MHz RC oscillator, 6 MHz ~ 25 MHz external crystal oscillator, external 32.768 kHz crystal oscillator, and internal 128 kHz RC oscillator. The WT59F164 also built-in two PLLs which can use External Crystal Oscillator to produce two different frequencies for USB or MCU illustrated as follows:

- Internal 12/24 MHz RC oscillator: In the default setting, MCU works in this Clock source. By setting Register SYS_OPTION1.HSI_CLK_SEL to switch12 MHz or 24 MHZ
- 6 MHz ~ 25 MHz external crystal oscillator: MCU can use Register SYS_CLOCK_SELECT.SW to switch working frequency from internal RC to external Crystal Oscillator. In the meantime, different clock sources can be generated by using Register SYS_USBPLL_CTRL & SYS_AUXPLL_CTRL, and Clock source of MCU can be selected by Register SYS_HSE_CLK_MUX.
- External 32.768 kHz crystal oscillator: provide for RTC Timer
- Internal 128 kHz RC oscillator: provide for Watchdog Timer (WDT)

System Clock Sources:



6. Enhanced Function

6.1 Special Function Register

Special Function Register (SFR) locates from 0x001F_5C00 ~ 0x0030_03FF.

Special Function Register Table:

Address	Function
0x001F_5C00~0x001F_5FFF	Pulse Width Modulation Register 0 (PWM0)
0x001F_6000~0x001F_63FF	Pulse Width Modulation Register 1 (PWM1)
0x001F_6800~0x001F_6BFF	General-purpose I/O Port Register and Multi-function Register (GPIO A-D)
0x0020_0000~0x0020_03FF	System Register and Low Voltage Detection & Reset Register (System Control)
0x0020_0400~0x0020_07FF	Emulated E^{2}PROM Register (Flash Programmer)
0x0020_0800~0x0020_0BFF	Watchdog Timer Register (WDT)
0x0020_0C00~0x0020_0FFF	Wakeup & Interrupt Register (Wake Up & Interrupt)
0x0020_1000~0x0020_13FF	Real-Time Clock Register (RTC)
0x0020_1400~0x0020_17FF	HDMI CEC Control Register (CEC)
0x0020_1800~0x0020_1BFF	IR Register (IR Receiver)
0x0020_1C00~0x0020_1FFF	Timer/Counter Register 0 (Timer0)
0x0020_2000~0x0020_23FF	Timer/Counter Register 1 (Timer1)
0x0020_2400~0x0020_27FF	Timer/Counter Register 2 (Timer2)
0x0020_2800~0x0020_2BFF	Timer/Counter Register 3 (Timer3)
0x0020_2C00~0x0020_2FFF	Timer/Counter Register 4 (Timer4)
0x0020_3000~0x0020_33FF	Timer/Counter Register 5 (Timer5)
0x0020_3400~0x0020_37FF	Universal Asynchronous Receiver-Transmitter 0 (UART0)
0x0020_3800~0x0020_3BFF	Universal Asynchronous Receiver-Transmitter 1 (UART1)
0x0020_3C00~0x0020_3FFF	Universal Asynchronous Receiver-Transmitter 2 (UART2)
0x0020_4400~0x0020_47FF	SPI Serial Port Interface Register 0 (SPI0)
0x0020_4800~0x0020_4BFF	SPI Serial Port Interface Register 1 (SPI1)
0x0020_5400~0x0020_57FF	I²C Serial Port Interface Register 0 (I^{2}C0)
0x0020_5800~0x0020_5BFF	I²C Serial Port Interface Register 1 (I^{2}C1)
0x0020_6400~0x0020_67FF	12-bit Analog/Digital Converter Register (ADC)
0x0020_6C00~0x0020_6FFF	I^{2}S Serial Port Interface Register (I^{2}S)
0x0020_7800~0x0020_7BFF	USB Serial Port Interface Register (USB)
0x0030_0000~0x0030_03FF	Direct Memory Access Register (DMA)

When the Reset status which is mentioned in section 5.7 occurred, the default value of external function register after reset is listed below:

Register Name	Address	Reset Default (Hex)	Index Section
Pulse Width Modulation Register 0 (PWM0) 0x001F_5C00~0x001F_5FFF			
PWM0_CTL	0x001F_5C00	0x0000_0000	6.7
PWM0_BASE_CLK	0x001F_5C04	0x0000_0000	6.7
PWM0_PWM0_CLK	0x001F_5C08	0x0000_0000	6.7

Register Name	Address	Reset Default (Hex)	Index Section
PWM0_PWM1_CLK	0x001F_5C0C	0x0000_0000	6.7
PWM0_PWM2_CLK	0x001F_5C10	0x0000_0000	6.7
PWM0_PWM3_CLK	0x001F_5C14	0x0000_0000	6.7
PWM0_PWM0_DUTY	0x001F_5C18	0x0000_0200	6.7
PWM0_PWM1_DUTY	0x001F_5C1C	0x0000_0200	6.7
PWM0_PWM2_DUTY	0x001F_5C20	0x0000_0200	6.7
PWM0_PWM3_DUTY	0x001F_5C24	0x0000_0200	6.7
PWM0_PWM0_PERIOD	0x001F_5C28	0x0000_03FF	6.7
PWM0_PWM1_PERIOD	0x001F_5C2C	0x0000_03FF	6.7
PWM0_PWM2_PERIOD	0x001F_5C30	0x0000_03FF	6.7
PWM0_PWM3_PERIOD	0x001F_5C34	0x0000_03FF	6.7
Pulse Width Modulation Register 1 (PWM1) 0x001F_6000~0x001F_63FF			
PWM1_CTL	0x001F_6000	0x0000_0000	6.7
PWM1_BASE_CLK	0x001F_6004	0x0000_0000	6.7
PWM1_PWM0_CLK	0x001F_6008	0x0000_0000	6.7
PWM1_PWM1_CLK	0x001F_600C	0x0000_0000	6.7
PWM1_PWM2_CLK	0x001F_6010	0x0000_0000	6.7
PWM1_PWM3_CLK	0x001F_6014	0x0000_0000	6.7
PWM1_PWM0_DUTY	0x001F_6018	0x0000_0200	6.7
PWM1_PWM1_DUTY	0x001F_601C	0x0000_0200	6.7
PWM1_PWM2_DUTY	0x001F_6020	0x0000_0200	6.7
PWM1_PWM3_DUTY	0x001F_6024	0x0000_0200	6.7
PWM1_PWM0_PERIOD	0x001F_6028	0x0000_03FF	6.7
PWM1_PWM1_PERIOD	0x001F_602C	0x0000_03FF	6.7
PWM1_PWM2_PERIOD	0x001F_6030	0x0000_03FF	6.7
PWM1_PWM3_PERIOD	0x001F_6034	0x0000_03FF	6.7
General-purpose I/O Port Register and Multi-function Register (GPIO A – D) 0x001F_6800~0x001F_6BFF			
GPIOA_ACT	0x001F_6800	0x0000_3FFF	6.3
GPIOA_OEN	0x001F_6804	0x0000_FFFF	6.3
GPIOA_OMOD	0x001F_6808	0x0000_0000	6.3
GPIOA_IN_DATA	0x001F_680C		6.3
GPIOA_OUT_DATA	0x001F_6810	0x0000_0000	6.3
GPIOA_REN	0x001F_6814	0x0000_3FFF	6.3
GPIOA_RS	0x001F_6818	0x0000_0000	6.3
GPIOA_BR	0x001F_681C		6.3
GPIOA_BS	0x001F_6820		6.3
GPIOA_ANA	0x001F_6824	0x0000_0000	6.3
GPIOB_ACT	0x001F_6880	0x0000_FFFF	6.3
GPIOB_OEN	0x001F_6884	0x0000_FFFF	6.3
GPIOB_OMOD	0x001F_6888	0x0000_0000	6.3
GPIOB_IN_DATA	0x001F_688C		6.3

Register Name	Address	Reset Default (Hex)	Index Section
GPIOB_OUT_DATA	0x001F_6890	0x0000_0000	6.3
GPIOB_REN	0x001F_6894	0x0000_FF1F	6.3
GPIOB_RS	0x001F_6898	0x0000_00C0	6.3
GPIOB_BR	0x001F_689C		6.3
GPIOB_BS	0x001F_68A0		6.3
GPIOB_ANA	0x001F_68A4	0x0000_0000	6.3
GPIOC_ACT	0x001F_6900	0x0000_1FFF	6.3
GPIOC_OEN	0x001F_6904	0x0000_1FFF	6.3
GPIOC_OMOD	0x001F_6908	0x0000_0000	6.3
GPIOC_IN_DATA	0x001F_690C		6.3
GPIOC_OUT_DATA	0x001F_6910	0x0000_0000	6.3
GPIOC_REN	0x001F_6914	0x0000_1FFF	6.3
GPIOC_RS	0x001F_6918	0x0000_0000	6.3
GPIOC_BR	0x001F_691C		6.3
GPIOC_BS	0x001F_6920		6.3
GPIOC_ANA	0x001F_6924	0x0000_0000	6.3
GPIOD_ACT	0x001F_6980	0x0000_000C	6.3
GPIOD_OEN	0x001F_6984	0x0000_000C	6.3
GPIOD_OMOD	0x001F_6988	0x0000_0000	6.3
GPIOD_IN_DATA	0x001F_698C		6.3
GPIOD_OUT_DATA	0x001F_6990	0x0000_0000	6.3
GPIOD_REN	0x001F_6994	0x0000_000C	6.3
GPIOD_RS	0x001F_6998	0x0000_0000	6.3
GPIOD_BR	0x001F_699C		6.3
GPIOD_BS	0x001F_69A0		6.3
GPIOD_ANA	0x001F_69A4		6.3
System Register and Low Voltage Detection & Reset Register (System Control) 0x0020_0000~0x0020_03FF			
SYS_OPTION1	0x0020_0000	0x0000_000C	6.2
SYS_CLOCK_SELECT	0x0020_0004	0x0000_0004	6.2
SYS_RC_COUNTER	0x0020_0008		6.8
SYS_RST	0x0020_000C	0x0000_0000	6.2
SYS_CLOCK_DISABLE1	0x0020_0010	0x0000_0000	6.2
SYS_CLOCK_DISABLE2	0x0020_0014	0x0000_0000	6.2
SYS_RTC_CTL	0x0020_0018	0x0000_0000	6.2
SYS_OPTION2	0x0020_0020	0x0000_0003	6.2
SYS_OPTION3	0x0020_0024	0x0000_0010	6.2
SYS_RES2	0x0020_0028		6.2
SYS_CALIBRATE_RC_FREQ	0x0020_002C	0x0000_0040	6.8
SYS_CALIBRATE_VD18	0x0020_0030	0x0000_0034	6.2
SYS_USBPLL_CTRL	0x0020_0034	0x0000_ADA7	6.2
SYS_AUXPLL_CTRL	0x0020_0038	0x0000_E380	6.2

Register Name	Address	Reset Default (Hex)	Index Section
SYS_HSE_CLK_MUX	0x0020_003C	0x0000_0000	6.2
Emulated E^{2}PROM Register (Flash Programmer) 0x0020_0400~0x0020_07FF			
EER_EN0	0x0020_0400	0x0000_0000	6.21
EER_EN1	0x0020_0404	0x0000_0000	6.21
EER_ADDR	0x0020_0408	0x0000_0000	6.21
EER_CTL	0x0020_040C	0x0000_0008	6.21
EER_W_DATA	0x0020_0410	0x0000_0000	6.21
EER_WAKEUP_ENABLE	0x0020_0414	0x0000_0001	6.21
EER_R_DATA	0x0020_0418		6.21
EER_WAKEUP_ENABLE_EXT	0x0020_041C	0x0000_0001	6.21
EER_W_DATA0	0x0020_0420	0x0000_0000	6.21
EER_W_DATA1	0x0020_0424	0x0000_0000	6.21
EER_W_DATA2	0x0020_0428	0x0000_0000	6.21
EER_W_DATA3	0x0020_042C	0x0000_0000	6.21
EER_W_DATA4	0x0020_0430	0x0000_0000	6.21
EER_W_DATA5	0x0020_0434	0x0000_0000	6.21
EER_W_DATA6	0x0020_0438	0x0000_0000	6.21
EER_W_DATA7	0x0020_043C	0x0000_0000	6.21
EER_ADDR_EXT	0x0020_0440	0x0000_0000	6.21
EER_CTL_EXT	0x0020_0444	0x0000_0008	6.21
Watchdog Timer Register (WDT) 0x0020_0800~0x0020_0BFF			
WDT_CTL	0x0020_0800	0x0000_0000	6.9
WDT_RST	0x0020_0804	0x0000_0000	6.9
WDT_DET	0x0020_0808	0x0000_0000	6.9
Wakeup & Interrupt Register (Wake Up & Interrupt) 0x0020_0C00~0x0020_0FFF			
WK_MISC	0x0020_0C00	0x0000_0000	6.6
WK_GPIOA	0x0020_0C04	0x0000_0000	6.6
WK_GPIOB	0x0020_0C08	0x0000_0000	6.6
WK_GPIOC	0x0020_0C0C	0x0000_0000	6.6
WK_GPIOD	0x0020_0C10	0x0000_0000	6.6
TOGGLE_MISC	0x0020_0C18		6.6
TOGGLE_GPIOA	0x0020_0C1C		6.6
TOGGLE_GPIOB	0x0020_0C20		6.6
TOGGLE_GPIOC	0x0020_0C24		6.6
TOGGLE_GPIOD	0x0020_0C28		6.6
TOGGLE_CLR_ALL_INT	0x0020_0C30		6.6
INT0_0_ENABLE	0x0020_0D00	0x0000_0000	6.4
INT0_1_ENABLE	0x0020_0D04	0x0000_0000	6.4
INT1_0_ENABLE	0x0020_0D08	0x0000_0000	6.4
INT1_1_ENABLE	0x0020_0D0C	0x0000_0000	6.4
INT0_0_FLAG	0x0020_0D10		6.4
INT0_1_FLAG	0x0020_0D14		6.4

Register Name	Address	Reset Default (Hex)	Index Section
INT1_0_FLAG	0x0020_0D18		6.4
INT1_1_FLAG	0x0020_0D1C		6.4
Real-Time Clock Register (RTC) 0x0020_1000~0x0020_13FF			
RTC_SEC	0x0020_1000	0x0000_0000	6.10
RTC_MIN	0x0020_1004	0x0000_0000	6.10
RTC_HOUR	0x0020_1008	0x0000_0000	6.10
RTC_DAY	0x0020_100C	0x0000_0001	6.10
RTC_WEEK	0x0020_1010	0x0000_0000	6.10
RTC_MONTH	0x0020_1014	0x0000_0001	6.10
RTC_YEAR	0x0020_1018	0x0000_0000	6.10
RTC_BACKUP1	0x0020_1020	0x0000_0000	6.10
RTC_BACKUP2	0x0020_1024	0x0000_0000	6.10
RTC_BACKUP3	0x0020_1028	0x0000_0000	6.10
RTC_BACKUP4	0x0020_102C	0x0000_0000	6.10
RTC_AMP	0x0020_1030	0x0000_0000	6.10
RTC_CAL	0x0020_1034	0x0000_0000	6.10
RTC_PARAMETER	0x0020_1038	0x0000_0009	6.10
RTC_MISC	0x0020_103C	0x0000_0062	6.10
HDMI CEC Control Register (CEC) 0x0020_1400~0x0020_17FF			
CEC_TX_ADDR	0x0020_1400	0x0000_00FF	6.15
CEC_TX_DATA1	0x0020_1404	0x0000_00FF	6.15
CEC_TX_DATA2	0x0020_1408	0x0000_00FF	6.15
CEC_TX_DATA3	0x0020_140C	0x0000_00FF	6.15
CEC_TX_DATA4	0x0020_1410	0x0000_00FF	6.15
CEC_TX_DATA5	0x0020_1414	0x0000_00FF	6.15
CEC_TX_DATA6	0x0020_1418	0x0000_00FF	6.15
CEC_TX_DATA7	0x0020_141C	0x0000_00FF	6.15
CEC_TX_DATA8	0x0020_1420	0x0000_00FF	6.15
CEC_TX_DATA9	0x0020_1424	0x0000_00FF	6.15
CEC_TX_DATA10	0x0020_1428	0x0000_00FF	6.15
CEC_TX_DATA11	0x0020_142C	0x0000_00FF	6.15
CEC_TX_DATA12	0x0020_1430	0x0000_00FF	6.15
CEC_TX_DATA13	0x0020_1434	0x0000_00FF	6.15
CEC_TX_DATA14	0x0020_1438	0x0000_00FF	6.15
CEC_TX_DATA15	0x0020_143C	0x0000_00FF	6.15
CEC_RX_ADDR	0x0020_1400		6.15
CEC_RX_DATA1	0x0020_1404		6.15
CEC_RX_DATA2	0x0020_1408		6.15
CEC_RX_DATA3	0x0020_140C		6.15
CEC_RX_DATA4	0x0020_1410		6.15
CEC_RX_DATA5	0x0020_1414		6.15
CEC_RX_DATA6	0x0020_1418		6.15

Register Name	Address	Reset Default (Hex)	Index Section
CEC_RX_DATA7	0x0020_141C		6.15
CEC_RX_DATA8	0x0020_1420		6.15
CEC_RX_DATA9	0x0020_1424		6.15
CEC_RX_DATA10	0x0020_1428		6.15
CEC_RX_DATA11	0x0020_142C		6.15
CEC_RX_DATA12	0x0020_1430		6.15
CEC_RX_DATA13	0x0020_1434		6.15
CEC_RX_DATA14	0x0020_1438		6.15
CEC_RX_DATA15	0x0020_143C		6.15
CEC_CTL	0x0020_1440	0x0000_0000	6.15
CEC_INIT	0x0020_1444	0x0000_0010	6.15
CEC_RETRY_CNT	0x0020_1448	0x0000_0000	6.15
CEC_FREE_CNT	0x0020_144C	0x0000_0046	6.15
CEC_FREE_TM	0x0020_1450	0x0000_0008	6.15
CEC_FREE_RESULT	0x0020_1454		6.15
CEC_RX_LEN	0x0020_1460		6.15
CEC_ACK_STA	0x0020_1464	0x0000_0002	6.15
CEC_ADR2	0x0020_1468	0x0000_00F0	6.15
CEC_BIT_STA	0x0020_1470		6.15
CEC_INT	0x0020_1478		6.15
CEC_INT_CLR	0x0020_147C	0x0000_0000	6.15
IR Register (IR Receiver) 0x0020_1800~0x0020_1BFF			
IR_CTL	0x0020_1800	0x0000_0000	6.16
IR_STATUS	0x0020_1804		6.16
IR_COUNT	0x0020_1808		6.16
IR_FILTER	0x0020_180C	0x0000_0000	6.16
Timer/Counter Register 0 (Timer0) 0x0020_1C00~0x0020_1FFF			
TIMER0_CTL	0x0020_1C00	0x0000_0000	6.11
TIMER0_COUNT	0x0020_1C04	0x0000_0000	6.11
TIMER0_PSCL	0x0020_1C08	0x0000_0000	6.11
TIMER0_PCNT	0x0020_1C0C	0x0000_0000	6.11
TIMER0_CCTL	0x0020_1C10	0x0000_0000	6.11
TIMER0_CICTL	0x0020_1C14	0x0000_0000	6.11
TIMER0_MCTL	0x0020_1C18	0x0000_0000	6.11
TIMER0_MOCTL	0x0020_1C1C	0x0000_0000	6.11
TIMER0_MAT0A	0x0020_1C30	0x0000_0000	6.11
TIMER0_MAT0B	0x0020_1C34	0x0000_0000	6.11
TIMER0_MAT1A	0x0020_1C38	0x0000_0000	6.11
TIMER0_MAT1B	0x0020_1C3C	0x0000_0000	6.11
TIMER0_IF_OF	0x0020_1C40	0x0000_0000	6.11
TIMER0_INT_EN	0x0020_1C44	0x0000_0000	6.11
TIMER0_DMA_FLAG	0x0020_1C48	0x0000_0000	6.11

Register Name	Address	Reset Default (Hex)	Index Section
TIMER0_DMA_EN	0x0020_1C4C	0x0000_0000	6.11
Timer/Counter Register 1 (Timer1) 0x0020_2000~0x0020_23FF			
TIMER1_CTL	0x0020_2000	0x0000_0000	6.11
TIMER1_COUNT	0x0020_2004	0x0000_0000	6.11
TIMER1_PSCL	0x0020_2008	0x0000_0000	6.11
TIMER1_PCNT	0x0020_200C	0x0000_0000	6.11
TIMER1_CCTL	0x0020_2010	0x0000_0000	6.11
TIMER1_CICTL	0x0020_2014	0x0000_0000	6.11
TIMER1_MCTL	0x0020_2018	0x0000_0000	6.11
TIMER1_MOCTL	0x0020_201C	0x0000_0000	6.11
TIMER1_MAT0A	0x0020_2030	0x0000_0000	6.11
TIMER1_MAT0B	0x0020_2034	0x0000_0000	6.11
TIMER1_MAT1A	0x0020_2038	0x0000_0000	6.11
TIMER1_MAT1B	0x0020_203C	0x0000_0000	6.11
TIMER1_IF_OF	0x0020_2040	0x0000_0000	6.11
TIMER1_INT_EN	0x0020_2044	0x0000_0000	6.11
TIMER1_DMA_FLAG	0x0020_2048	0x0000_0000	6.11
TIMER1_DMA_EN	0x0020_204C	0x0000_0000	6.11
Timer/Counter Register 2 (Timer2) 0x0020_2400~0x0020_27FF			
TIMER2_CTL	0x0020_2400	0x0000_0000	6.11
TIMER2_COUNT	0x0020_2404	0x0000_0000	6.11
TIMER2_PSCL	0x0020_2408	0x0000_0000	6.11
TIMER2_PCNT	0x0020_240C	0x0000_0000	6.11
TIMER2_CCTL	0x0020_2410	0x0000_0000	6.11
TIMER2_CICTL	0x0020_2414	0x0000_0000	6.11
TIMER2_MCTL	0x0020_2418	0x0000_0000	6.11
TIMER2_MOCTL	0x0020_241C	0x0000_0000	6.11
TIMER2_MAT0A	0x0020_2430	0x0000_0000	6.11
TIMER2_MAT0B	0x0020_2434	0x0000_0000	6.11
TIMER2_MAT1A	0x0020_2438	0x0000_0000	6.11
TIMER2_MAT1B	0x0020_243C	0x0000_0000	6.11
TIMER2_IF_OF	0x0020_2440	0x0000_0000	6.11
TIMER2_INT_EN	0x0020_2444	0x0000_0000	6.11
TIMER2_DMA_FLAG	0x0020_2448	0x0000_0000	6.11
TIMER2_DMA_EN	0x0020_244C	0x0000_0000	6.11
Timer/Counter Register 3 (Timer3) 0x0020_2800~0x0020_2BFF			
TIMER3_CTL	0x0020_2800	0x0000_0000	6.11
TIMER3_COUNT	0x0020_2804	0x0000_0000	6.11
TIMER3_PSCL	0x0020_2808	0x0000_0000	6.11
TIMER3_PCNT	0x0020_280C	0x0000_0000	6.11
TIMER3_CCTL	0x0020_2810	0x0000_0000	6.11
TIMER3_CICTL	0x0020_2814	0x0000_0000	6.11

Register Name	Address	Reset Default (Hex)	Index Section
TIMER3_MCTL	0x0020_2818	0x0000_0000	6.11
TIMER3_MOCTL	0x0020_281C	0x0000_0000	6.11
TIMER3_MAT0A	0x0020_2830	0x0000_0000	6.11
TIMER3_MAT0B	0x0020_2834	0x0000_0000	6.11
TIMER3_MAT1A	0x0020_2438	0x0000_0000	6.11
TIMER3_MAT1B	0x0020_283C	0x0000_0000	6.11
TIMER3_IF_OF	0x0020_2840	0x0000_0000	6.11
TIMER3_INT_EN	0x0020_2844	0x0000_0000	6.11
TIMER3_DMA_FLAG	0x0020_2848	0x0000_0000	6.11
TIMER3_DMA_EN	0x0020_284C	0x0000_0000	6.11
Timer/Counter Register 4 (Timer4) 0x0020_2C00~0x0020_2FFF			
TIMER4_CTL	0x0020_2C00	0x0000_0000	6.11
TIMER4_COUNT	0x0020_2C04	0x0000_0000	6.11
TIMER4_PSCL	0x0020_2C08	0x0000_0000	6.11
TIMER4_PCNT	0x0020_2C0C	0x0000_0000	6.11
TIMER4_CCTL	0x0020_2C10	0x0000_0000	6.11
TIMER4_CICTL	0x0020_2C14	0x0000_0000	6.11
TIMER4_MCTL	0x0020_2C18	0x0000_0000	6.11
TIMER4_MOCTL	0x0020_2C1C	0x0000_0000	6.11
TIMER4_MAT0A	0x0020_2C30	0x0000_0000	6.11
TIMER4_MAT0B	0x0020_2C34	0x0000_0000	6.11
TIMER4_MAT1A	0x0020_2C38	0x0000_0000	6.11
TIMER4_MAT1B	0x0020_2C3C	0x0000_0000	6.11
TIMER4_IF_OF	0x0020_2C40	0x0000_0000	6.11
TIMER4_INT_EN	0x0020_2C44	0x0000_0000	6.11
TIMER4_DMA_FLAG	0x0020_2C48	0x0000_0000	6.11
TIMER4_DMA_EN	0x0020_2C4C	0x0000_0000	6.11
Timer/Counter Register 5 (Timer5) 0x0020_3000~0x0020_33FF			
TIMER5_CTL	0x0020_3000	0x0000_0000	6.11
TIMER5_COUNT	0x0020_3004	0x0000_0000	6.11
TIMER5_PSCL	0x0020_3008	0x0000_0000	6.11
TIMER5_PCNT	0x0020_300C	0x0000_0000	6.11
TIMER5_CCTL	0x0020_3010	0x0000_0000	6.11
TIMER5_CICTL	0x0020_3014	0x0000_0000	6.11
TIMER5_MCTL	0x0020_3018	0x0000_0000	6.11
TIMER5_MOCTL	0x0020_301C	0x0000_0000	6.11
TIMER5_MAT0A	0x0020_3030	0x0000_0000	6.11
TIMER5_MAT0B	0x0020_3034	0x0000_0000	6.11
TIMER5_MAT1A	0x0020_3038	0x0000_0000	6.11
TIMER5_MAT1B	0x0020_303C	0x0000_0000	6.11
TIMER5_IF_OF	0x0020_3040	0x0000_0000	6.11
TIMER5_INT_EN	0x0020_3044	0x0000_0000	6.11

Register Name	Address	Reset Default (Hex)	Index Section
TIMER5_DMA_FLAG	0x0020_3048	0x0000_0000	6.11
TIMER5_DMA_EN	0x0020_304C	0x0000_0000	6.11
Universal Asynchronous Receiver-Transmitter 0 (UART0) 0x0020_3400~0x0020_37FF			
UART0_SET_CTL	0x0020_3400	0x0000_0000	6.5
UART0_INT_CTL	0x0020_3404	0x0000_0000	6.5
UART0_STATUS	0x0020_3408	0x0000_0000	6.5
UART0_TX_DATA	0x0020_340C		6.5
UART0_RX_DATA	0x0020_3410		6.5
UART0_BAUDRATE	0x0020_3414	0x0000_0000	6.5
UART0_BREAK	0x0020_3418	0x0000_0000	6.5
Universal Asynchronous Receiver-Transmitter 1 (UART1) 0x0020_3800~0x0020_3BFF			
UART1_SET_CTL	0x0020_3800	0x0000_0000	6.5
UART1_INT_CTL	0x0020_3804	0x0000_0000	6.5
UART1_STATUS	0x0020_3808	0x0000_0000	6.5
UART1_TX_DATA	0x0020_380C		6.5
UART1_RX_DATA	0x0020_3810		6.5
UART1_BAUDRATE	0x0020_3814	0x0000_0000	6.5
UART1_BREAK	0x0020_3818	0x0000_0000	6.5
Universal Asynchronous Receiver-Transmitter 2 (UART2) 0x0020_3C00~0x0020_3FFF			
UART2_SET_CTL	0x0020_3C00	0x0000_0000	6.5
UART2_INT_CTL	0x0020_3C04	0x0000_0000	6.5
UART2_STATUS	0x0020_3C08	0x0000_0000	6.5
UART2_TX_DATA	0x0020_3C0C		6.5
UART2_RX_DATA	0x0020_3C10		6.5
UART2_BAUDRATE	0x0020_3C14	0x0000_0000	6.5
UART2_BREAK	0x0020_3C18	0x0000_0000	6.5
SPI Serial Port Interface Register 0 (SPI0) 0x0020_4400~0x0020_47FF			
SPI0_CR1	0x0020_4400	0x0000_0001	6.13
SPI0_CR2	0x0020_4404	0x0000_0000	6.13
SPI0_IER	0x0020_4408	0x0000_0000	6.13
SPI0_ISR	0x0020_440C	0x0001_0001	6.13
SPI0_TDR	0x0020_4410	0x0000_0000	6.13
SPI0_RDR	0x0020_4414	0x0000_0000	6.13
SPI Serial Port Interface Register 1 (SPI1) 0x0020_4800~0x0020_4BFF			
SPI1_CR1	0x0020_4800	0x0000_0001	6.13
SPI1_CR2	0x0020_4804	0x0000_0000	6.13
SPI1_IER	0x0020_4808	0x0000_0000	6.13
SPI1_ISR	0x0020_480C	0x0001_0001	6.13
SPI1_TDR	0x0020_4810	0x0000_0000	6.13
SPI1_RDR	0x0020_4814	0x0000_0000	6.13
I²C Serial Port Interface Register 0 (I^2C0) 0x0020_5400~0x0020_57FF			
IIC0_CTL	0x0020_5400	0x0000_0020	6.12

Register Name	Address	Reset Default (Hex)	Index Section
IIC0_STATUS	0x0020_5404		6.12
IIC0_MI2CDSLV	0x0020_5408	0x0000_0000	6.12
IIC0_TX_BUFFER	0x0020_540C	0x0000_00FF	6.12
IIC0_RX_BUFFER	0x0020_5410		6.12
IIC0_SLAVE_ADDR	0x0020_5414	0x0000_0000	6.12
IIC0_EXTEN_CTL	0x0020_5418	0x0000_0000	6.12
I²C Serial Port Interface Register 1 (I²C1) 0x0020_5800~0x0020_5BFF			
IIC1_CTL	0x0020_5800	0x0000_0020	6.12
IIC1_STATUS	0x0020_5804		6.12
IIC1_MI2CDSLV	0x0020_5808	0x0000_0000	6.12
IIC1_TX_BUFFER	0x0020_580C	0x0000_00FF	6.12
IIC1_RX_BUFFER	0x0020_5810		6.12
IIC1_SLAVE_ADDR	0x0020_5814	0x0000_0000	6.12
IIC1_EXTEN_CTL	0x0020_5818	0x0000_0000	6.12
12-bit Analog/Digital Converter Register (ADC) 0x0020_6400~0x0020_67FF			
ADC_CTL	0x0020_6400	0x0000_0000	6.14
ADC_DATA	0x0020_6404		6.14
ADC_EOC	0x0020_6408	0x0000_0000	6.14
ADC_OPTION	0x0020_640C	0x0000_0000	6.14
ADC_WAKEUP_VOLTAGE	0x0020_6410	0x0000_0800	6.14
ADC_EN_CH	0x0020_6418	0x0000_0000	6.14
I²S Serial Port Interface Register (I²S) 0x0020_6C00~0x0020_6FFF			
I2S_CLK_CFG	0x0020_6C00	0x0000_2851	6.17
I2S_CFG	0x0020_6C04	0x0000_0000	6.17
I2S_CTRL	0x0020_6C08	0x0000_0000	6.17
I2S_TX_STAT	0x0020_6C0C	0x0050_5050	6.17
I2S_RX_STAT	0x0020_6C10	0x0010_1010	6.17
I2S_TX0_BUF	0x0020_6C20		6.17
I2S_TX1_BUF	0x0020_6C24		6.17
I2S_TX2_BUF	0x0020_6C28		6.17
I2S_RX0_BUF	0x0020_6C30		6.17
I2S_RX1_BUF	0x0020_6C34		6.17
I2S_RX2_BUF	0x0020_6C38		6.17
USB Serial Port Interface Register (USB) 0x0020_7800~0x0020_7BFF			
FADDR	0x0020_7800	0x0000_0000	6.19
USBFI	0x0020_7804	0x0000_0000	6.19
USBFIE	0x0020_7808	0x0000_0000	6.19
SIEI	0x0020_780C	0x0000_0000	6.19
EPINDEX	0x0020_7814	0x0000_0000	6.19
EPCON	0x0020_7818	0x0000_0025	6.19
TXDAT	0x0020_7820		6.19
TXCON	0x0020_7824	0x0000_0000	6.19

Register Name	Address	Reset Default (Hex)	Index Section
TXFLG	0x0020_7828	0x0000_0008	6.19
TXCNT	0x0020_782C	0x0000_0000	6.19
TXSTAT	0x0020_7830	0x0000_0000	6.19
USBFI_CLR	0x0020_7840	0x0000_0000	6.19
USBFI2	0x0020_7844	0x0000_0000	6.19
USBFIE2	0x0020_7848	0x0000_0000	6.19
REP	0x0020_784C	0x0000_0000	6.19
TXEN	0x0020_7850	0x0000_0000	6.19
RXDAT	0x0020_7860		6.19
RXCON	0x0020_7864	0x0000_0000	6.19
RXFLG	0x0020_7868	0x0000_0008	6.19
RXCNT	0x0020_786C	0x0000_0000	6.19
RXSTAT	0x0020_7870	0x0000_0000	6.19
EP7_CON	0x0020_7880	0x0000_0000	6.19
EP7_STAT	0x0020_7884	0x0000_0000	6.19
EP7_BASE	0x0020_7888	0x0000_0000	6.19
EP7_LIMIT	0x0020_788C	0x0000_0100	6.19
EP7_W_BYTE	0x0020_7890		6.19
EP8_CON	0x0020_78A0	0x0000_0000	6.19
EP8_STAT	0x0020_78A4	0x0000_0800	6.19
EP8_BASE	0x0020_78A8	0x0000_0100	6.19
EP8_LIMIT	0x0020_78AC	0x0000_0100	6.19
EP8_R_BYTE	0x0020_78B0		6.19
FRAME	0x0020_78C0	0x0000_0000	6.19
Direct Memory Access Register (DMA)	**0x0030_0000~0x0030_03FF**		
DMA_BUSY_STATUS	0x0030_0004		6.18
DMA_INT_STATUS	0x0030_0008		6.18
DMA_INT_CLR	0x0030_000C	0x0000_0000	6.18
DMA_SADDR0	0x0030_0010	0x0000_0000	6.18
DMA_SADDR1	0x0030_0020	0x0000_0000	6.18
DMA_SADDR2	0x0030_0030	0x0000_0000	6.18
DMA_SADDR3	0x0030_0040	0x0000_0000	6.18
DMA_SADDR4	0x0030_0050	0x0000_0000	6.18
DMA_SADDR5	0x0030_0060	0x0000_0000	6.18
DMA_SADDR6	0x0030_0070	0x0000_0000	6.18
DMA_DADDR0	0x0030_0014	0x0000_0000	6.18
DMA_DADDR1	0x0030_0024	0x0000_0000	6.18
DMA_DADDR2	0x0030_0034	0x0000_0000	6.18
DMA_DADDR3	0x0030_0044	0x0000_0000	6.18
DMA_DADDR4	0x0030_0054	0x0000_0000	6.18
DMA_DADDR5	0x0030_0064	0x0000_0000	6.18
DMA_DADDR6	0x0030_0074	0x0000_0000	6.18

Register Name	Address	Reset Default (Hex)	Index Section
DMA_LENGTH0	0x0030_0018	0x0000_0000	6.18
DMA_LENGTH1	0x0030_0028	0x0000_0000	6.18
DMA_LENGTH2	0x0030_0038	0x0000_0000	6.18
DMA_LENGTH3	0x0030_0048	0x0000_0000	6.18
DMA_LENGTH4	0x0030_0058	0x0000_0000	6.18
DMA_LENGTH5	0x0030_0068	0x0000_0000	6.18
DMA_LENGTH6	0x0030_0078	0x0000_0000	6.18
DMA_CONFIG0	0x0030_001C	0x0000_0000	6.18
DMA_CONFIG1	0x0030_002C	0x0000_0000	6.18
DMA_CONFIG2	0x0030_003C	0x0000_0000	6.18
DMA_CONFIG3	0x0030_004C	0x0000_0000	6.18
DMA_CONFIG4	0x0030_005C	0x0000_0000	6.18
DMA_CONFIG5	0x0030_006C	0x0000_0000	6.18
DMA_CONFIG6	0x0030_007C	0x0000_0000	6.18

6.2 System Setting Register

System Setting Register can control the system related function such as: Clock Source, Peripheral Function Reset, Internal RC Calibration, and Internal 1.8V Voltage Calibration exc. With 15 registers as follows:

Register Name	Address	Reset Default (Hex)	Description
System Register and Low Voltage Detection & Reset Register (System Control) 0x0020_0000~0x0020_03FF			
SYS_OPTION1	0x0020_0000	0x0000_000C	Internal RC & external crystal oscillator related setting
SYS_CLOCK_SELECT	0x0020_0004	0x0000_0004	MCU clock source switch & special I/O setting
SYS_RC_COUNTER	0x0020_0008		Internal RC to 32.768 kHz counting value
SYS_RST	0x0020_000C	0x0000_0000	Hardware peripheral reset setting
SYS_CLOCK_DISABLE1	0x0020_0010	0x0000_0000	Hardware peripheral clock power down setting
SYS_CLOCK_DISABLE2	0x0020_0014	0x0000_0000	Hardware peripheral clock power down setting
SYS_RTC_CTL	0x0020_0018	0x0000_0000	RTC control
SYS_OPTION2	0x0020_0020	0x0000_0003	Internal low-speed RC enable, LDO and temperature sensor setting
SYS_OPTION3	0x0020_0024	0x0000_0010	LVD setting
SYS_RES2	0x0020_0028		LVD flag
SYS_CALIBRATE_RC_FREQ	0x0020_002C	0x0000_0040	Internal high-speed RC setting & calibration
SYS_CALIBRATE_VD18	0x0020_0030	0x0000_0034	Internal 1.8V voltage calibration
SYS_USBPLL_CTRL	0x0020_0034	0x0000_ADA7	USB PLL setting
SYS_AUXPLL_CTRL	0x0020_0038	0x0000_E380	AUX PLL setting
SYS_HSE_CLK_MUX	0x0020_003C	0x0000_0000	MCU clock source selection

System Control Register 0 SYS_OPTION1 (Address: 0x0020_0000) Reset Value: 0x0000_000C

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	R/W
Name	Reserved							OSC_OFF
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	OSC_OFF2	MCU_OFF	XTAL_OFF	HSE_CLK_SEL[2:0]			HSEON	HSIOFF

Bit Number	Bit Mnemonic	Description
31-9	Reserved	-
8	OSC_OFF	Internal high-speed RC Oscillator Power down mode setting 1: Internal RC Oscillator enters Power down mode, meanwhile System Clock stops, signals wake up MCU to MCU work after 256 RC OSC clocks 0: Normal mode (default) When this bit is set, MCU follows command "standby 2" to enter Power down mode
7	OSC_OFF2	Internal High-speed RC Oscillator Power down mode setting (OSC bias ON) 1: Internal RC Oscillator enters Power down mode, meanwhile System Clock stops, signals wake up MCU to MCU work after 32 RC OSC clocks 0: Normal mode (default)
6	MCU_OFF	System Clock power down mode setting 1: Turn off System Clock, meanwhile Internal RC or External Crystal Oscillator turn on, signals wake up MCU to MCU work after 4 system clocks 0: Normal mode (default)
5	XTAL_OFF	External High-speed Crystal Oscillator Power down mode setting 1: External Crystal Oscillator enters Power down mode, meanwhile System Clock stops, signals wake up MCU to MCU work after 65K clocks 0: Normal mode (default)
4-2	HSE_CLK_SEL[2:0]	External High-speed Crystal Oscillator Clock selection, this value must be set precisely, or it will influence the speed of low-speed peripherals (ADC, I^2C, E^2PROM, IR, or CEC) 000: 18 MHz 001: 6 MHz 010: 12 MHz 011: 24 MHz (default) 1xx: 36 MHz
1	HSEON	External High-speed Crystal Oscillator enable setting 1: Enable High-speed External Crystal Oscillator 0: Disable High-speed External Crystal Oscillator (default)
0	HSIOFF	Internal High-speed RC Oscillator disable setting 1 : Disable high-speed internal RC oscillator 0 : Enable high-speed internal RC oscillator (default)

-: unimplemented.

System Clock Select Register SYS_CLOCK_SELECT

(Address: 0x0020_0004) **Reset Value: 0x0000_0004**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	-	R/W	R/W	R/W
Name	Reserved	UART2_PPEN	UART1_PPEN	UART0_PPEN	Reserved	JTAG_EN	EN_WDTOSC	SW

Bit Number	Bit Mnemonic	Description
31-7	Reserved	-
6	UART2_PPEN	UART2 Output pin Push-Pull mode setting 1: UART2 Output pin is Push-Pull 0: UART2 Output pin is Open-Drain (default)
5	UART1_PPEN	UART1 Output pin Push-Pull mode setting 1: UART1 Output pin is Push-Pull 0: UART1 Output pin is Open-Drain (default)
4	UART0_PPEN	UART0 Output pin Push-Pull mode setting 1: UART0 Output pin is Push-Pull 0: UART0 Output pin is Open-Drain (default)
6	Reserved	-
2	JTAG_EN	Enable JTAG pins 1: Enable JTAG pin, set GPIOA[15:14] as JTAG pins (default) 0: Disable JTAG pin
1	EN_WDTOSC	Internal 128K RC Oscillator Clock (Clock) Output enable setting 1: Enable Internal 128K RC Oscillator Clock Output, set “1” to output RC 128K_clk to PA[13] 0: Disable Internal 128K RC Oscillator Clock Output (default)
0	SW	System Clock source switch 1 : Select External high-speed Crystal Oscillator as system clock source 0 : Select Internal high-speed RC Oscillator as system clock source (default)

-: unimplemented.

Internal RC Calibration Register SYS_RC_COUNTER

(Address: 0x0020_0008) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	R	R
Name	Reserved						RC_CALIBRATE[9:8]	
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	RC_CALIBRATE[7:0]							

Bit Number	Bit Mnemonic	Description
31-10	Reserved	-
9-0	RC_CALIBRATE[9:0]	RC counter calibrate with external 32.768 kHz clock (with two rising-edge counter value of 32.768 kHz)

-: unimplemented.

System Peripheral Reset Setting Register SYS_RST

(Address: 0x0020_000C) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved		USBRST	IRRST	I2SRST	CECRST	PWM1RST	PWM0RST
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	WDTRST	Reserved	UART2RST	UART1RST	UART0RST	I2C1RST	I2C0RST	SPI1RST
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	SPI0RST	TIM5RST	TIM4RST	TIM3RST	TIM2RST	TIM1RST	TIM0RST	ADCRST
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved						IOPTRST	DMARST

Bit Number	Bit Mnemonic	Description
31-30	Reserved	-
29	USBRST	USB function reset setting 1: USB reset
28	IRRST	IR function reset setting 1: IR receiver reset
27	I2SRST	I^2S function reset setting 1: I^2S reset
26	CECRST	CEC function reset setting 1: CEC reset
25	PWM1RST	PWM1 function reset setting 1: PWM1 reset
24	PWM0RST	PWM0 function reset setting 1: PWM0 reset
23	WDTRST	WDT function reset setting 1: WDTRST reset
22	Reserved	-
21	UART2RST	UART2 function reset setting 1: UART2 reset
20	UART1RST	UART1 function reset setting 1: UART1 reset
19	UART0RST	UART0 function reset setting 1: UART0 reset
18	I2C1RST	I^2C1 function reset setting 1: I^2C1 reset
17	I2C0RST	I^2C0 function reset setting 1: I^2C0 reset
16	SPI1RST	SPI1 function reset setting 1: SPI1 reset

Bit Number	Bit Mnemonic	Description
15	SPI0RST	SPI0 function reset setting 1: SPI0 reset
14	TIM5RST	TIMER5 function reset setting 1: TIMER5 reset
13	TIM4RST	TIMER4 function reset setting 1: TIMER4 reset
12	TIM3RST	TIMER3 function Reset setting 1: TIMER3 reset
11	TIM2RST	TIMER2 function Reset setting 1: TIMER2 reset
10	TIM1RST	TIMER1 function Reset setting 1: TIMER1 reset
9	TIM0RST	TIMER0 function Reset setting 1: TIMER0 reset
8	ADCRST	ADC function Reset setting 1: ADC reset
7-2	Reserved	-
1	IOPTRST	I/O function Reset setting 1: I/O (GPIOA~GPIOE) reset
0	DMARST	DMA function Reset setting 1: DMA reset

-: unimplemented.

System Function Clock Disable Setting Register 1 SYS_CLOCK_DISABLE1

(Address: 0x0020_0010) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved		USB_CK_DIS	IR_CK_DIS	I2S_CK_DIS	CEC_CK_DIS	PWM1_CK_DIS	PWM0_CK_DIS
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	WDT_CK_DIS	Reserved	UART2_CK_DIS	UART1_CK_DIS	UART0_CK_DIS	I2C1_CK_DIS	I2C0_CK_DIS	SPI1_CK_DIS
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	SPI0_CK_DIS	TIM5_CK_DIS	TIM4_CK_DIS	TIM3_CK_DIS	TIM2_CK_DIS	TIM1_CK_DIS	TIM0_CK_DIS	ADC_CK_DIS
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R/W	-
Name	Reserved						IOPT_CK_DIS	Reserved

Bit Number	Bit Mnemonic	Description
31-30	Reserved	-
29	USB_CK_DIS	USB Clock disable setting 1: Disable USB Clock
28	IR_CK_DIS	IR Clock disable setting 1: Disable IR Clock
27	I2S_CK_DIS	I^2S Clock disable setting 1: Disable I^2S Clock
26	CEC_CK_DIS	CEC Clock disable setting 1: Disable CEC Clock

Bit Number	Bit Mnemonic	Description
25	PWM1_CK_DIS	PWM1 Clock disable setting 1: Disable PWM1 Clock
24	PWM0_CK_DIS	PWM0 Clock disable setting 1: Disable PWM0 Clock
23	WDT_CK_DIS	WDT Clock disable setting 1: Disable WDT Clock
22	Reserved	-
21	UART2_CK_DIS	UART2 Clock disable setting 1: Disable UART2 Clock
20	UART1_CK_DIS	UART1 Clock disable setting 1: Disable UART1 Clock
19	UART0_CK_DIS	UART0 Clock disable setting 1: Disable UART0 Clock
18	I2C1_CK_DIS	I^2C1 Clock disable setting 1: Disable I^2C1 Clock
17	I2C0_CK_DIS	I^2C0 Clock disable setting 1: Disable I^2C0 Clock
16	SPI1_CK_DIS	SPI1 Clock disable setting 1: Disable SPI1 Clock
15	SPI0_CK_DIS	SPI0 Clock disable setting 1: Disable SPI0 Clock
14	TIM5_CK_DIS	TIMER5 Clock disable setting 1: Disable TIMER5 Clock
13	TIM4_CK_DIS	TIMER4 Clock disable setting 1: Disable TIMER4 Clock
12	TIM3_CK_DIS	TIMER3 Clock disable setting 1: Disable TIMER3 Clock
11	TIM2_CK_DIS	TIMER2 Clock disable setting 1: Disable TIMER2 Clock
10	TIM1_CK_DIS	TIMER1 Clock disable setting 1: Disable TIMER1 Clock
9	TIM0_CK_DIS	TIMER0 Clock disable setting 1: Disable TIMER0 Clock
8	ADC_CK_DIS	ADC Clock disable setting 1: Disable ADC Clock
7-2	Reserved	-
1	IOPT_CK_DIS	I/O Clock disable setting 1: Disable I/O (GPIOA~GPIOE) Clock
0	Reserved	-

-: unimplemented.

System Function Clock Disable Setting Register 2 SYS_CLOCK_DISABLE2

(Address: 0x0020_0014) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	-	R/W
Name	Reserved							DMA_CK_DIS

Bit Number	Bit Mnemonic	Description
31-1	Reserved	-
0	DMA_CK_DIS	DMA Clock Disable setting 1: Disable DMA Clock

-: unimplemented.

Real-Time Clock (RTC) Control Register SYS_RTC_CTL

(Address: 0x0020_0018) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R/W	R/W	R/W	-	-	-	W
Name	RTC_1S	RTC_CS	RTC_EN	RTC_RESET	Reserved			CLR_RTC_1S

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	RTC_1S	RTC 1-second Event Flag 1: RTC 1-second event occurs
6	RTC_CS	RTC WR/RD enable setting 1: enable RTC WR/RD 0: disable RTC WR/RD (default)
5	RTC_EN	RTC enable setting 1: enable RTC 0: disable RTC (default)
4	RTC_RESET	RTC Reset setting 1: RTC Reset (must be set as 0 to leave Reset status)
3-1	Reserved	-
0	CLR_RTC_1S	RTC 1-second Event Interrupt Clear 1: clear RTC_1S event Interrupt

-: unimplemented.

System Control Register 2 SYS_OPTION2 (Address: 0x0020_0020) Reset Value: 0x0000_0003

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	R/W	R/W	-	R/W	R/W
Name	Reserved			LDO_OFF[1:0]		Reserved	LSION	TS_PD

Bit Number	Bit Mnemonic	Description
31-5	Reserved	-
4	LDO_OFF1	LDO power down mode setting 1: LDO enter power down mode
3	LDO_OFF0	LDO Power down mode setting Register (at SUSPEND status) 1: While MCU enters SUSPEND mode, LDO enters Power Down mode
2	Reserved	-
1	LSION	Internal low-speed (128 kHz) RC oscillator enable setting 1: Enable internal low-speed (128 kHz) RC oscillator (default) 0: Disable internal low-speed (128 kHz) RC oscillator
0	TS_PD	Internal temperature sensor power down mode setting 1: Internal temperature sensor enters power down mode (default)

-: unimplemented.

System Control Register 3 SYS_OPTION3 (Address: 0x0020_0024) Reset Value: 0x0000_0010

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved						EN_MCUCLK_O[2:1]	
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	EN_MCUCLK_O[0]	EN_32KCLK_I	EN_32KCLK_O	LVD_LEVEL[2:0]			LVRON	LVDON

Bit Number	Bit Mnemonic	Description
31-10	Reserved	-

Bit Number	Bit Mnemonic	Description
9-7	EN_MCUCLK_O[2:0]	MCU clock output selection (from GPIOA[8] Output) 001: Enable MCU clock output to GPIOA[8] 011: Enable MCU clock div 2 output to GPIOA[8] 101: Enable AUX_PLL clock output to GPIOA[8] 111: Enable USB_PLL clock output to GPIOA[8] xx0: Disable MCU Clock output to GPIOA[8] (default)
6	EN_32KCLK_I	(testing purpose) 1: Set GPIOA[8] as 32K clock source
5	EN_32KCLK_O	(testing purpose) 1: 32K clock output to GPIOA[8]
4-2	LVD_LEVEL[2:0]	Low Voltage Detection (LVD) Voltage Detection setting (auto reset by POR) LVD Detection Voltage = 2.2 + 0.1* LVD_LEVEL[2:0]
1	LVRON	Low Voltage Reset (LVR) enable 1: Enable low voltage reset 0: Disable low voltage reset (default)
0	LVDON	Low Voltage Detection (LVD) enable setting 1: Enable Low Voltage Detection 0: Disable Low Voltage Detection (default)

-: unimplemented.

Low Voltage Detection Status Register SYS_RES2 (Address: 0x0020_0028) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	-	R
Name	Reserved							LVDF

Bit Number	Bit Mnemonic	Description
31-1	Reserved	-
0	LVDF	Low Voltage Detection (LVD) status flag 1: Low voltage detected

-: unimplemented.

System RC Calibration Register SYS_CALIBRATE_RC_FREQ

(Address: 0x0020_002C) Reset Value: 0x0000_0040

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	HSI_CLK_SEL	HSI_COARSE_SEL[2:0]			HSI_FINE_SEL[3:0]			

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	HSI_CLK_SEL	High-speed internal RC oscillator clock output frequency selection 1: 24 MHz 0: 12 MHz (default)
6-4	HSI_COARSE_SEL[2:0]	Coarse adjustment of high-speed internal RC oscillator 001: 16-unit current (8%) 010: 32-unit current (16%) 011: 48-unit current (24%) 100: 64-unit current (32%) (default) 101: 80-unit current (40%) 110: 96-unit current (48%) 111: 112-unit current (56%)
3-0	HSI_FINE_SEL[3:0]	Fine adjustment of high-speed internal RC oscillator 0000: 0-unit current (0%) (default) 0001: 1-unit current (0.5%) 0010: 2-unit current (1%) 0011: 3-unit current (1.5%) 0100: 4-unit current (2%) 0101: 5-unit current (2.5%) 0110: 6-unit current (3%) 0111: 7-unit current (3.5%) 1000: 8-unit current (4%) 1001: 9-unit current (4.5%) 1010: 10-unit current (5%) 1011: 11-unit current (5.5%) 1100: 12-unit current (6%) 1101: 13-unit current (6.5%) 1110: 14-unit current (7%) 1111: 15-unit current (7.5%)

-: unimplemented.

System 1.8V Calibration Register SYS_CALIBRATE_VD18

(Address: 0x0020_0030) Reset Value: 0x0000_0034

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	-	R/W	R/W	R/W
Name	Reserved	CAL_LP18[2:0]			Reserved	CALIBRATE18[2:0]		

Bit Number	Bit Mnemonic	Description
31-7	Reserved	-
6-4	CAL_LP18[2:0]	The adjuster of V1.8 Output Voltage during suspend mode when VDD = 3.3V, VD18: 000: 1.392V 001: 1.496V 010: 1.601V 011: 1.706V (default) 100: 1.810V 101: 1.941V 110: 2.071V 111: 2.200V
3	Reserved	-
2-0	CALIBRATE18[2:0]	The adjuster of V1.8 Output Voltage in Normal mode when VDD = 3.3V, VD18: 000: 1.675V 001: 1.705V 010: 1.736V 011: 1.768V 100: 1.803V (default) 101: 1.839V 110: 1.878V 111: 1.918V

-: unimplemented.

USB PLL Control Register SYS_USBPLL_CTRL

(Address: 0x0020_0034) **Reset Value: 0x0000_ADA7**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	USB_PLL_PD	USB_PLL_SEL[1:0]		USB_PLL_DIVN1[4:0]				
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	USB_PLL_MUL1[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15	USB_PLL_PD	USB PLL Power Down mode setting 1: USB PLL enters Power Down (default)
14-13	USB_PLL_SEL[1:0]	The output selector of the PLL, can work together with USB_PLL_DIVN1 & USB_PLL_MUL1 to proceed PLL Clock Output setting (swap 0 and 3 of A version)
12-8	USB_PLL_DIVN1[4:0]	The pre-divider of the reference clock input, can work together with USB_PLL_SEL & USB_PLL_MUL1 to proceed PLL Clock Output setting
7-0	USB_PLL_MUL1[7:0]	PLL feedback multiplier of the pre-divider, can work together with USB_PLL_DIVN1 & USB_PLL_SEL to proceed PLL Clock Output setting f(PLL) = (f(XTAL) *(MUL1+1))/((DIVN1+1)*(2<<SEL))

-: unimplemented.

AUX PLL Control Register SYS_AUXPLL_CTRL

(Address: 0x0020_0038) Reset Value: 0x0000_E380

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	AUX_PLL_PD	AUX_PLL_SEL[1:0]		AUX_PLL_DIVN1[4:0]				
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	AUX_PLL_MUL1[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15	AUX_PLL_PD	AUX PLL Power Down mode setting 1: AUX PLL enters Power Down (default)
14-13	AUX_PLL_SEL[1:0]	The Output selector of the PLL, can work together with AUX_PLL_DIVN1 & AUX_PLL_MUL1 to proceed PLL Clock Output setting (swap 0 and 3 of A version)
12-8	AUX_PLL_DIVN1[4:0]	The pre-divider of the reference clock input, can work together with AUX_PLL_SEL & AUX_PLL_MUL1 to proceed PLL Clock Output setting
7-0	AUX_PLL_MUL1[7:0]	PLL feedback multiplier of the pre-divider setting, can work together with AUX_PLL_DIVN1 & AUX_PLL_SEL to proceed PLL Clock Output setting f(PLL) = (f(XTAL)*(MUL1+1))/((DIVN1+1)*(2<<SEL))

-: unimplemented.

External High-speed Frequency Selection Register SYS_HSE_CLK_MUX

(Address: 0x0020_003C) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved						HSE_CLK_MUX[1:0]	

Bit Number	Bit Mnemonic	Description
31-2	Reserved	-
1-0	HSE_CLK_MUX[1:0]	External high-speed Clock selection 00: External high-speed crystal oscillator (default) 01: Reserved (same as External high-speed crystal oscillator) 10: AUX PLL 11: USB_PLL_div_2 **Note: Since there is no glitch-free clock switch, user should change this register under HIS mode (SW = 0)**

-: unimplemented.

6.3 I/O Port

6.3.1 Features

- 47 programmable I/Os, contains: GPIOA[15:0], GPIOB[15:0], GPIOC[12:0], GPIOD[3:2]
- Some I/O with special functions (such as ADC and PWM exc.), can be configured by Special Function Register
- Each port bit of the General Purpose I/O (GPIO) Ports, can be individually configured by software in several modes:
  - Input floating
  - Input pull-up
  - Input pull-down
  - Output open-drain
  - Output push-pull
  - Analog I/O
- Each I/O has Internal Pull-Up/Pull-Down resistor, can be configured as On or Off by Special Function Register GPIOx_REN & GPIOx_RS
- During and just after reset, the alternate functions are not active and the I/O ports are configured in Input Floating mode.
  The JTAG pins are in output pull-down after reset:
  PA15: TMSC in PD
  PA14: TCKC in PD
- Can be operated by special register GPIOx_BR and GPIOx_BS. If both GPIOx_BR and GPIOx_BS are set, GPIOx_BS has priority.
- When configured as Output of Internal special function such as SPI Clock, it requires setting the corresponding GPIOx_ACT bit as 0.

6.3.2 Register

WT59F164 I/O related registers are classified into four categories as below:

- GPIOx_ACT: configure I/O as general-purpose Output / Input I/O or special function I/O
- GPIOx_OEN: Control Output/Input Register, can configure I/O as Output or Input. If the corresponding GPIOx_OEN bit = 0, this I/O is configured as output.
- GPIOx_OMOD: Output Mode Setting Register, is configured to set I/O as push-pull or open drain type.
- GPIOx_IN_DATA: Data Read Register, reading I/O data by this register
- GPIOx_OUT_DATA: Data Output Register, setting I/O Output by this register
- GPIOx_REN: Internal Pull-Up Resistor Enable Register, can configure if I/O is with pull-up or pull-down resistor (selected by GPIOx_RS). If the corresponding GPIOx_REN bit = 0, then this bit is with internal pull-up or pull-down resistor.
- GPIOx_RS: Internal Pull-Up or Pull-Down resistor selection Register. If I/O ports configure pull-up/pull-down Resistor Enable Register (GPIOx_REN), the Register is allowed to configure I/O as pull-up or pull-down resistor. If the corresponding GPIOx_RS bit = 0, then this I/O is with internal pull-down; Vice versa, if the corresponding GPIOx_RS bit = 1, then this I/O is with internal pull-up.
- GPIOx_BR: Bit Clear Register. When configured as Output port (by GPIOx_OEN) and the corresponding GPIOx_BR bit = 1, then the mapping I/O is configured as Low level Output; if the corresponding bit = 0, then the corrdesponding I/O Output remains unchanged.
- GPIOx_BS: Bit Setting Register. When configured as Output port (by GPIOx_OEN) and the corresponding GPIOx_BS bit = 1, then the mapping I/O is configured as High level Output; if the corresponding bit = 0, the corresponding I/O output remains unchanged.
- GPIOx_ANA: Digital input buffer enable setting

- I/O configuration reference Table:

I/O Type	GPIOx_REN	GPIOx_RS	GPIOx_OEN	GPIOx_OMOD	GPIOx_ANA
Input floating	1	x	1	x	0
Input pull-up resistor	0	1	1	x	0
Input pull-down resistor	0	0	1	x	0
Output open-drain	1	x	0	1	x
Output push-pull	1	x	0	0	x
Analog I/O	1	x	1	x	1

Register Name	Address	Reset Default (Hex)	Primary Function
General-purpose I/O port Register and Multi-function Register (GPIO A – D) 0x001F_6800~0x001F_6BFF			
GPIOA_ACT	0x001F_6800	0x0000_3FFF	GPIOA function setting
GPIOA_OEN	0x001F_6804	0x0000_FFFF	GPIOA output/input setting
GPIOA_OMOD	0x001F_6808	0x0000_0000	GPIOA output setting
GPIOA_IN_DATA	0x001F_680C		GPIOA read data
GPIOA_OUT_DATA	0x001F_6810	0x0000_0000	GPIOA output data
GPIOA_REN	0x001F_6814	0x0000_3FFF	GPIOA pull-up/pull-down resister enable setting
GPIOA_RS	0x001F_6818	0x0000_0000	GPIOA pull-up/pull-down resistor selection
GPIOA_BR	0x001F_681C		GPIOA output bit setting
GPIOA_BS	0x001F_6820		GPIOA output bit clear
GPIOA_ANA	0x001F_6824	0x0000_0000	GPIOA digital input buffer setting
GPIOB_ACT	0x001F_6880	0x0000_FFFF	GPIOB function setting
GPIOB_OEN	0x001F_6884	0x0000_FFFF	GPIOB output/input setting
GPIOB_OMOD	0x001F_6888	0x0000_0000	GPIOB output mode setting
GPIOB_IN_DATA	0x001F_688C		GPIOB read data
GPIOB_OUT_DATA	0x001F_6890	0x0000_0000	GPIOB output data
GPIOB_REN	0x001F_6894	0x0000_FF1F	GPIOB pull-up/pull-down resistor enable setting
GPIOB_RS	0x001F_6898	0x0000_00C0	GPIOB pull-up/pull-down resistor selection
GPIOB_BR	0x001F_689C		GPIOB output bit setting
GPIOB_BS	0x001F_68A0		GPIOB output bit clear
GPIOB_ANA	0x001F_68A4	0x0000_0000	GPIOB digital input buffer setting
GPIOC_ACT	0x001F_6900	0x0000_1FFF	GPIOC function setting
GPIOC_OEN	0x001F_6904	0x0000_1FFF	GPIOC output/input setting
GPIOC_OMOD	0x001F_6908	0x0000_0000	GPIOC output mode setting
GPIOC_IN_DATA	0x001F_690C		GPIOC read data
GPIOC_OUT_DATA	0x001F_6910	0x0000_0000	GPIOC output data
GPIOC_REN	0x001F_6914	0x0000_1FFF	GPIOC pull-up/pull-down resistor enable setting
GPIOC_RS	0x001F_6918	0x0000_0000	GPIOC pull-up/pull-down selection
GPIOC_BR	0x001F_691C		GPIOC output bit setting
GPIOC_BS	0x001F_6920		GPIOC output bit clear
GPIOC_ANA	0x001F_6924	0x0000_0000	GPIOC digital input buffer setting

Register Name	Address	Reset Default (Hex)	Primary Function
GPIOD_ACT	0x001F_6980	0x0000_000C	GPIOD function setting
GPIOD_OEN	0x001F_6984	0x0000_000C	GPIOD output/input setting
GPIOD_OMOD	0x001F_6988	0x0000_0000	GPIOD output mode setting
GPIOD_IN_DATA	0x001F_698C		GPIOD read data
GPIOD_OUT_DATA	0x001F_6990	0x0000_0000	GPIOD output data
GPIOD_REN	0x001F_6994	0x0000_000C	GPIOD pull-up/pull-down resistor enable setting
GPIOD_RS	0x001F_6998	0x0000_0000	GPIOD pull-up/pull-down resistor selection
GPIOD_BR	0x001F_699C		GPIOD output bit setting
GPIOD_BS	0x001F_69A0		GPIOD output bit clear
GPIOD_ANA	0x001F_69A4		GPIOD digital input buffer setting

General-purpose I/O Port A Control Register GPIOA_ACT

(Address: 0x001F_6800) **Reset Value: 0x0000_3FFF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_ACT[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_ACT[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	GPIOA_ACT[15:0]	General-purpose I/O port A control register 1: configure GPIOA[x] as general-purpose function (default) 0: configure GPIOA[x] as special function The port GPIOA14 and GPIOA15 are enabled as special function (JTAG) by default

-: unimplemented.

General-purpose I/O Port A Output Enable Register GPIOA_OEN

(Address: 0x001F_6804) **Reset Value: 0x0000_FFFF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_OEN[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_OEN[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	GPIOA_OEN[15:0]	General-purpose I/O port A output/input setting 1: GPIOA[x] as input (default) 0: GPIOA[x] as output

-: unimplemented.

General-purpose I/O Port A Output mode Register GPIOA_OMOD

(Address: 0x001F_6808) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_OMOD[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_OMOD[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	GPIOA_OMOD[15:0]	General-purpose I/O port A output type setting 1 : GPIOA[x] output type is open-drain 0: GPIOA[x] output type is push-pull (default)

-: unimplemented.

General-purpose I/O Port A Data Read Register GPIOA_IN_DATA

(Address: 0x001F_680C) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R	R	R	R	R	R	R	R
Name	GPIOA_IN_DATA[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	GPIOA_IN_DATA[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	GPIOA_IN_DATA[15:0]	General-purpose I/O port A input data

-: unimplemented.

General-purpose I/O Port A Data Output Register GPIOA_OUT_DATA

(Address: 0x001F_6810) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	GPIOA_OUT_DATA[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	GPIOA_OUT_DATA [7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	GPIOA_OUT_DATA [15:0]	General-purpose I/O port A output data

-: unimplemented.

General-purpose I/O Port A Enable Internal Pull-Up/Pull-Down Control Register GPIOA_REN

(Address: 0x001F_6814) Reset Value: 0x0000_3FFF

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_REN[15:8]							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_REN[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	GPIOA_REN[15:0]	Enable general-purpose I/O port A with pull-up/pull-Down setting 1 : Disable GPIOA[x] (default) 0: Enable GPIOA[x] The port GPIOA[14] and GPIOA[15] are default pull-down after reset.

-: unimplemented.

General-purpose I/O Port A Internal Pull-Up/Pull-Down Resistor Selection Control Register GPIOA_RS
(Address: 0x001F_6818) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_RS[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_RS[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	GPIOA_RS[15:0]	I/O Port A with pull-up/pull-down setting 1 : GPIOA[x] select pull-up 0 : GPIOA[x] select pull-down (default)

-: unimplemented.

General-purpose I/O Port A Bit Clear Register GPIOA_BR
(Address: 0x001F_681C) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	GPIOA_BR[15:8]							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	GPIOA_BR[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	GPIOA_BR[15:0]	General-purpose I/O port A bit clear 1 : GPIOA[x] bit clear, output low level 0 : GPIOA[x] no action

-: unimplemented.

General-purpose I/O Port A Bit Setting Register GPIOA_BS

(Address: 0x001F_6820) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	GPIOA_BS[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	GPIOA_BS[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	GPIOA_BS[15:0]	General-purpose I/O port A bit setting 1 : GPIOA[x] bit setting, output high level 0 : GPIOA[x] no action

-: unimplemented.

General-purpose I/O Port A Digital Input Buffer Control Register GPIOA_ANA

(Address: 0x001F_6824) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_ANA[15:8]							

Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_ANA[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	GPIOA_ANA[15:0]	General-purpose I/O port A digital input buffer enable setting 1: Disable GPIOA[x] digital input buffer 0: Enable GPIOA[x] digital input buffer

-: unimplemented.

General-purpose I/O Port B Control Register GPIOB_ACT

(Address: 0x001F_6880) **Reset Value: 0x0000_FFFF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_ACT[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_ACT[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	GPIOB_ACT[15:0]	General-purpose I/O Port B Control Register 1: configure GPIOB[x] as general-purpose function (default) 0: configure GPIOB[x] as special function

-: unimplemented.

General-purpose I/O Port B Output Enable Register GPIOB_OEN

(Address: 0x001F_6884) **Reset Value: 0x0000_FFFF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_OEN[15:8]							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_OEN[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	GPIOB_OEN[15:0]	General-purpose I/O Port B Output / Input setting 1: GPIOB[x] is input (default) 0: GPIOB[x] is output

-: unimplemented.

General-purpose I/O Port B Output Mode Register GPIOB_OMOD

(Address: 0x001F_6888) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_OMOD[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_OMOD[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	GPIOB_OMOD[15:0]	General-purpose I/O port B output type setting 1 : GPIOB[x] output type is open-drain 0: GPIOB[x] output type is push-pull (default)

-: unimplemented.

General-purpose I/O Port B Data Read Register GPIOB_IN_DATA

(Address: 0x001F_688C) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R	R	R	R	R	R	R	R
Name	GPIOB_IN_DATA[15:8]							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	GPIOB_INT_DATA[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	GPIOB_IN_DATA[15:0]	General-purpose I/O port B input data

-: unimplemented.

General-purpose I/O Port B Data Output Register GPIOB_OUT_DATA

(Address: 0x001F_6890) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	GPIOB_OUT_DATA[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	GPIOB_OUT_DATA[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	GPIOB_OUT_DATA[15:0]	General-purpose I/O port B output data

-: unimplemented.

General-purpose I/O Port B Enable Internal Pull-Up/Pull-Down Resistor Control Register GPIOB_REN

(Address: 0x001F_6894) Reset Value: 0x0000_FF1F

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_REN[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_REN[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	GPIOB_REN[15:0]	Enable general-purpose I/O port B with pull-up/pull-down resistor setting 1 : disable GPIOB[x] (default) 0: enable GPIOB[x] The port GPIOB[5] is default pull-down after reset. The port GPIOA[6] and GPIOA[7] are default pull-up after reset.

-: unimplemented.

General-purpose I/O Port B Internal Pull-Up/Pull-Down Resistor Selection Control Register GPIOB_RS
(Address: 0x001F_6898) Reset Value: 0x0000_00C0

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_RS[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_RS[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	GPIOB_RS[15:0]	I/O port B pull-up/pull-down resistor setting 1 : GPIOB[x select pull-up resistor 0 : GPIOB[x] select pull-down resistor (default)

-: unimplemented.

General-purpose I/O Port B Bit Clear Register GPIOB_BR
(Address: 0x001F_689C) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	GPIOB_BR[15:8]							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	GPIOB_BR[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	GPIOB_BR[15:0]	General-purpose I/O port B bit clear 1: GPIOB[x] bit clear, output low level 0: GPIOB[x] no action

-: unimplemented.

General-purpose I/O Port B Bit Setting Register GPIOB_BS

(Address: 0x001F_68A0) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	GPIOB_BS[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	GPIOB_BS[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	GPIOB_BS[15:0]	General-purpose I/O port B bit setting 1 : GPIOB[x] bit setting, output high level 0 : GPIOB[x] no action

-: unimplemented.

General-purpose I/O Port B Digital Input Buffer Setting Register GPIOB_ANA

(Address: 0x001F_68A4) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_ANA[15:8]							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_ANA[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	GPIOB_ANA[15:0]	General-purpose I/O port B digital input buffer enable setting 1: disable GPIOB[x] digital input buffer 0: enable GPIOB[x] digital input buffer

-: unimplemented.

General-purpose I/O Port C Control Register GPIOC_ACT

(Address: 0x001F_6900) **Reset Value: 0x0000_1FFF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	R/W	R/W	R/W	R/W	R/W
Name	Reserved			GPIOC_ACT[12:8]				
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOC_ACT[7:0]							

Bit Number	Bit Mnemonic	Description
31-13	Reserved	-
12-0	GPIOC_ACT[12:0]	General-purpose I/O port C control register 1 : configure GPIOC[x] as general-purpose function (default) 0 : configure GPIOC[x] as special function

-: unimplemented.

General-purpose I/O Port C Output Enable Register GPIOC_OEN

(Address: 0x001F_6904) **Reset Value: 0x0000_1FFF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	R/W	R/W	R/W	R/W	R/W
Name	Reserved			GPIOC_OEN[12:8]				

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOC_OEN[7:0]							

Bit Number	Bit Mnemonic	Description
31-13	Reserved	-
12-0	GPIOC_OEN[12:0]	General-purpose I/O port C output/input setting 1: configure GPIOC[x] as input (default) 0: configure GPIOC[x] as output

-: unimplemented.

General-purpose I/O Port C Output Mode Register GPIOC_OMOD

(Address: 0x001F_6908) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	R/W	R/W	R/W	R/W	R/W
Name	Reserved			GPIOC_OMOD[12:8]				
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOC_OMOD[7:0]							

Bit Number	Bit Mnemonic	Description
31-13	Reserved	-
12-0	GPIOC_OMOD[12:0]	General-purpose I/O port C output type setting 1 : GPIOC[x] output type is open-drain 0: GPIOC[x] output type is push-pull (default)

-: unimplemented.

General-purpose I/O Port C Data Read Register GPIOC_IN_DATA

(Address: 0x001F_690C) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	R	R	R	R	R
Name	Reserved			GPIOC_IN_DATA[12:8]				

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	GPIOC_IN_DATA[7:0]							

Bit Number	Bit Mnemonic	Description
31-13	Reserved	-
12-0	GPIOC_IN_DATA[12:0]	General-purpose I/O port C input data

-: unimplemented.

General-purpose I/O Port C Data Output Register GPIOC_OUT_DATA
(Address: 0x001F_6910) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	W	W	W	W	W
Name	Reserved			GPIOC_OUT_DATA[12:8]				
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	GPIOC_OUT_DATA [7:0]							

Bit Number	Bit Mnemonic	Description
31-13	Reserved	-
12-0	GPIOC_OUT_DATA [12:0]	General-purpose I/O port C output data

-: unimplemented.

General-purpose I/O Port C Enable Internal Pull-Up/Pull-Down Resistor Control Register GPIOC_REN
(Address: 0x001F_6914) Reset Value: 0x0000_1FFF

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	R/W	R/W	R/W	R/W	R/W
Name	Reserved			GPIOC_REN[12:8]				
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOC_REN[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
12-0	GPIOC_REN[12:0]	Enable general-purpose I/O port C with pull-up/pull-down resistor setting 1 : Disable GPIOC[x] (default) 0: Enable GPIOC[x]

-: unimplemented.

General-purpose I/O Port C Internal Pull-Up/Pull-Down Resistor Selection Control Register GPIOC_RS

(Address: 0x001F_6918) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	R/W	R/W	R/W	R/W	R/W
Name	Reserved			GPIOC_RS[12:8]				
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOC_RS[7:0]							

Bit Number	Bit Mnemonic	Description
31-13	Reserved	-
12-0	GPIOC_RS[12:0]	I/O port C pull-up/pull-down resistor setting 1 : GPIOC[x] selection pull-up resistor 0 : GPIOC[x] selection pull-down resistor (default)

-: unimplemented.

General-purpose I/O Port C Bit Clear Register GPIOC_BR

(Address: 0x001F_691C) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	W	W	W	W	W
Name	Reserved			GPIOC_BR[12:8]				
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	GPIOC_BR[7:0]							

Bit Number	Bit Mnemonic	Description
31-13	Reserved	-
12-0	GPIOC_BR[12:0]	General-purpose I/O port C bit clear 1: GPIOC[x] bit clear, output low level 0: GPIOC[x] no action

-: unimplemented.

General-purpose I/O Port C Bit Setting Register

GPIOC_BS (Address: 0x001F_6920) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	W	W	W	W	W
Name	Reserved			GPIOC_BS[12:8]				
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	GPIOC_BS[7:0]							

Bit Number	Bit Mnemonic	Description
31-13	Reserved	-
12-0	GPIOC_BS[12:0]	General-purpose I/O port C bit setting 1 : GPIOC[x] bit setting, output high level 0 : GPIOC[x] no action

-: unimplemented.

General-purpose I/O Port C Digital Input Buffer Setting GPIOC_ANA

(Address: 0x001F_6924) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	R/W	R/W	R/W	R/W	R/W
Name	Reserved			GPIOC_ANA[12:8]				
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOC_ANA[7:0]							

Bit Number	Bit Mnemonic	Description
31-13	Reserved	-
12-0	GPIOC_ANA[12:0]	General-purpose I/O port C digital input buffer enable setting 1: Disable GPIOC[x] digital input buffer 0: Enable GPIOC[x] digital input buffer

-: unimplemented.

General-purpose I/O Port D Control Register GPIOD_ACT

(Address: 0x001F_6980) **Reset Value: 0x0000_000C**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	-	-
Name	Reserved				GPIOD_ACT[3:2]		Reserved	

Bit Number	Bit Mnemonic	Description
31-4	Reserved	-
3-2	GPIOD_ACT[3:2]	General-purpose I/O port D control register 1 : configure GPIOD[x] as general-purpose function (default) 0 : configure GPIOD[x] as special function
1-0	Reserved	-

-: unimplemented.

General-purpose I/O Port D Output Enable Register GPIOD_OEN

(Address: 0x001F_6984) **Reset Value: 0x0000_000C**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	-	-
Name	Reserved				GPIOD_OEN[3:2]		Reserved	

Bit Number	Bit Mnemonic	Description
31-4	Reserved	-
3-2	GPIOD_OEN[3:2]	General-purpose I/O port D output/input setting 1: configure GPIOD[x] as input (default) 0: configure GPIOD[x] as output
1-0	Reserved	-

-: unimplemented.

General-purpose I/O Port D Output Mode Register GPIOD_OMOD

(Address: 0x001F_6988) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	-	-
Name	Reserved				GPIOD_OMOD[3:2]		Reserved	

Bit Number	Bit Mnemonic	Description
31-4	Reserved	-
3-2	GPIOD_OMOD[3:2]	General-purpose I/O port D output type setting 1 : GPIOD[x] output type is open-drain 0 : GPIOD[x] output type is push-pull (default)
1-0	Reserved	-

-: unimplemented.

General-purpose I/O Port D Data Read Register GPIOD_IN_DATA

(Address: 0x001F_698C) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R	R	-	-
Name	Reserved				GPIOD_IN_DATA[3:2]		Reserved	

Bit Number	Bit Mnemonic	Description
31-4	Reserved	-
3-2	GPIOD_IN_DATA[3:2]	General-purpose I/O port D input data
1-0	Reserved	-

-: unimplemented.

General-purpose I/O Port D Data Output Register GPIOD_OUT_DATA

(Address: 0x001F_6990) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	W	W	-	-
Name	Reserved				GPIOD_OUT_DATA[3:2]		Reserved	

Bit Number	Bit Mnemonic	Description
31-4	Reserved	-
3-2	GPIOD_OUT_DATA[3:2]	General-purpose I/O port D output data
1-0	Reserved	-

-: unimplemented.

General-purpose I/O Port D Enable Internal Pull-Up/Pull-Down Resistor Control Register GPIOD_REN

(Address: 0x001F_6994) Reset Value: 0x0000_000C

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	-	-
Name	Reserved				GPIOD_REN[3:2]		Reserved	

Bit Number	Bit Mnemonic	Description
31-4	Reserved	-
3-2	GPIOD_REN[3:2]	Enable general-purpose I/O port D pull-up/pull-down resistor setting 1 : Disable GPIOD[x] pull-up/pull-down resistor (default) 0: Enable GPIOD[x] pull-up/pull-down resistor
1-0	Reserved	-

-: unimplemented.

General-purpose I/O Port D Internal Pull-Up/Pull-Down Resistor Selection Control Register GPIOD_RS
(Address: 0x001F_6998) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	-	-
Name	Reserved				GPIOD_RS[3:2]		Reserved	

Bit Number	Bit Mnemonic	Description
31-4	Reserved	-
3-2	GPIOD_RS[3:2]	I/O port D pull-up/pull-down resistor setting 1 : GPIOD[x] select pull-up resistor 0 : GPIOD[x] select pull-down resistor (default)
1-0	Reserved	-

-: unimplemented.

General-purpose I/O Port D Bit Clear Register GPIOD_BR
(Address: 0x001F_699C) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	W	W	-	-
Name	Reserved				GPIOD_BR[3:2]		Reserved	

Bit Number	Bit Mnemonic	Description
31-4	Reserved	-
3-2	GPIOD_BR[3:2]	General-purpose I/O port D bit clear 1: GPIOD[x] bit clear, output low level 0: GPIOD[x] no action
1-0	Reserved	-

-: unimplemented.

General-purpose I/O Port D Bit Setting Register GPIOD_BS

(Address: 0x001F_69A0) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	W	W	-	-
Name	Reserved				GPIOD_BS[3:2]		Reserved	

Bit Number	Bit Mnemonic	Description
31-4	Reserved	-
3-2	GPIOD_BS[3:2]	General-purpose I/O port D bit setting 1 : GPIOD[x] bit setting, output high level 0 : GPIOD[x] no action
1-0	Reserved	-

-: unimplemented.

General-purpose I/O Port D Digital Input Buffer Enable Setting Register GPIOD_ANA

(Address: 0x001F_69A4) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	-	-
Name	Reserved				GPIOD_ANA[3:2]		Reserved	

Bit Number	Bit Mnemonic	Description
31-4	Reserved	-
3-2	GPIOD_ANA[3:2]	General-purpose I/O port D digital input buffer enable setting 1: Disable GPIOD[x] digital input buffer 0: Enable GPIOD[x] digital input buffer
1-0	Reserved	-

-: unimplemented.

Note:
1. The port GPIOA[15] and GPIOA[14] work as JTAG interface instead of GPIO after power on reset. If you want to use these pin as GPIO pins, remember to set these pins as functional pin in your program.
2. The GPIOA[15] and GPIOA[14] are default input pull down. The other GPIO ports are default input floating.
3. In IC of A version, special register GPIOD_ANA is not initialized. User should write 0 to this register to be able to read pin status from register GPIOD_RD.

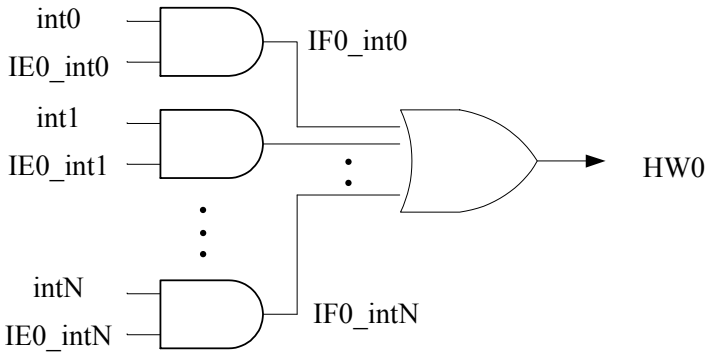
6.4 Interrupt

6.4.1 Features

The WT59F164 provides four hardware interrupt sources: INT0 (HW0), INT1 (HW1), INT2 (HW2) and INT3 (HW3).

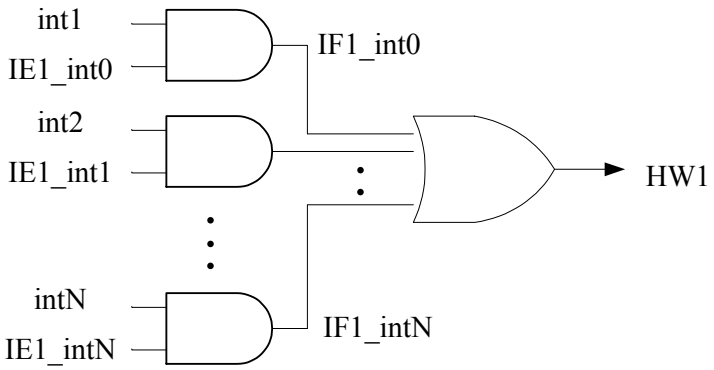
1. Thirteen peripherals interrupt sources are derived from INT0, as described below:
   (1) ADC Interrupt
   (2) I^2C Serial Port Interrupt
   (3) SPI Serial Port Interrupt
   (4) UART Receiver Interrupt
   (5) Timer/Counter Interrupt
   (6) I/O Port Input Toggle Interrupt
   (7) Watchdog Timer (WDT) Interrupt
   (8) Low Voltage Detection (LVD) Interrupt
   (9) I^2S Serial Port Interrupt
   (10) Direct Memory Access (DMA) Interrupt
   (11) HDMI CEC (CEC) Interrupt
   (12) IR Interrupt
   (13) Real-Time Clock (RTC) 1S Interrupt

   Each of these interrupt sources has its own enable control bit, and can be enabled or disabled by setting or clearing the corresponding bit Iex_XXX in the register INT0_0_ENABLE and INT0_1_ENABLE. When INT0 interrupt is generated, by judging the corresponding bit IF0_XXX in the register INT0_0_FLAG and INT0_1_FLAG can find out which function interrupt has occurred.



2. Same as INT0, thirteen peripheral interrupts sources are derived from INT1, as described below:
   (1) ADC Interrupt
   (2) I^2C Serial Port Interrupt
   (3) SPI Serial Port Interrupt
   (4) UART Receiver (UART) Interrupt
   (5) Timer/Counter (TIMER) Interrupt
   (6) I/O Port Input Toggle Interrupt
   (7) Watchdog Timer (WDT) Interrupt
   (8) Low Voltage Detection (LVD) Interrupt
   (9) I^2S Serial Port Interrupt
   (10) Direct Memory Access (DMA) Interrupt
   (11) HDMI CEC (CEC) Interrupt
   (12) IR Interrupt
   (13) Real-Time Clock (RTC) 1S Interrupt

Each of these interrupt sources has its own enable control bit, and can be enabled or disabled by setting or clearing the corresponding bit IE1_XXX in the register INT1_0_ENABLE and INT1_1_ENABLE. When INT1 Interrupt is generated, by judging the corresponding bit IF1_XXX in the register INT1_0_FLAG and INT1_1_FLAG can find out which function interrupt has occurred.

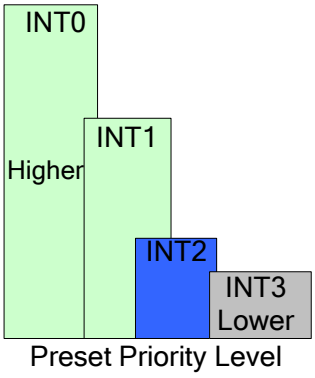


3. INT2 (HW2): INT2 interrupt is caused by USB SUSPEND, RESUME, RESET and SOF. Each interrupt can be enabled/disabled independently by programming register USBFIE2. When an INT2 interrupt is generated, by judging the register USBFI2 can find out which interrupt has occurred. Please refer to section 6.19 for more details on USB interrupt.

4. INT3 (HW3): INT3 interrupt is caused by USB Endpoint 0 ~ Endpoint 6. Each interrupt can be enabled/disabled independently by programming register USBFIE. When an INT3 interrupt is generated, by judging the register USBFI can find out which interrupt has occurred. Please refer to section 6.19 for more details on USB interrupt.

When an interrupt is generated, CPU will jump to interrupt vector from service routine. If multiple requests of different priority levels are received simultaneously, the request is serviced sequentially from INT0 to INT3. If interrupt flag bit is set, CPU will enter the interrupt processing again.

As illustrated below, the priority level of interrupt will be 「**INT0 > INT1 > INT2 > INT3**」.



6.4.2 Register

Register Name	Address	Reset Default (Hex)	Description
Wakeup & Interrupt Register (Wakeup & Interrupt) 0x0020_0C00~0x0020_0FFF			
INT0_0_ENABLE	0x0020_0D00	0x0000_0000	Interrupt 0 enable setting
INT0_1_ENABLE	0x0020_0D04	0x0000_0000	Interrupt 0 enable setting
INT1_0_ENABLE	0x0020_0D08	0x0000_0000	Interrupt 1 enable setting
INT1_1_ENABLE	0x0020_0D0C	0x0000_0000	Interrupt 1 enable setting
INT0_0_FLAG	0x0020_0D10		Interrupt 0 interrupt flag
INT0_1_FLAG	0x0020_0D14		Interrupt 0 interrupt flag
INT1_0_FLAG	0x0020_0D18		Interrupt 1 interrupt flag
INT1_1_FLAG	0x0020_0D1C		Interrupt 1 interrupt flag

Interrupt Enable Register INT0_0_ENABLE (Address: 0x0020_0D00) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IE0_ADC	IE0_I2C1	IE0_I2C0	IE0_SPI1	IE0_SPI0	Reserved	IE0_UART2	IE0_UART1
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IE0_UART0	IE0_TMR3	IE0_TMR2	IE0_TMR1	IE0_TMR0	IE0_IN_TOG	IE0_WDT	IE0_LVD

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15	IE0_ADC	INT0 ADC interrupt enable setting 1: Enable ADC interrupt generated by INT0 0: Disable ADC interrupt generated by INT0 (default)
14	IE0_I2C1	INT0 I^2C1 interrupt enable setting 1: Enable I^2C1 interrupt generated by INT0 0: Disable I^2C1 interrupt generated by INT0 (default)
13	IE0_I2C0	INT0 I^2C0 interrupt enable setting 1: Enable I^2C0 interrupt generated by INT0 0: Disable I^2C0 interrupt generated by INT0 (default)
12	IE0_SPI1	INT0 SPI1 interrupt enable setting 1: Enable SPI1 interrupt generated by INT0 0: Disable SPI1 interrupt generated by INT0 (default)
11	IE0_SPI0	INT0 SPI0 interrupt enable setting 1: Enable SPI0 interrupt generated by INT0 0: Disable SPI0 interrupt generated by INT0 (default)
10	Reserved	-

Bit Number	Bit Mnemonic	Description
9	IE0_UART2	INT0 UART2 interrupt enable setting 1: Enable UART2 interrupt generated by INT0 0: Disable UART2 interrupt generated by INT0 (default)
8	IE0_UART1	INT0 UART1 interrupt enable setting 1: Enable UART1 interrupt generated by INT0 0: Disable UART1 interrupt generated by INT0 (default)
7	IE0_UART0	INT0 UART0 interrupt enable setting 1: Enable UART0 interrupt generated by INT0 0: Disable UART0 interrupt generated by INT0 (default)
6	IE0_TMR3	INT0 TIMER3 interrupt enable setting 1: Enable Timer/Counter 3 interrupt generated by INT0 0: Disable Timer/Counter 3 interrupt generated by INT0 (default)
5	IE0_TMR2	INT0 TIMER2 interrupt enable setting 1: Enable Timer/Counter 2 interrupt generated by INT0 0: Disable Timer/Counter 2 interrupt generated by INT0 (default)
4	IE0_TMR1	INT0 TIMER1 interrupt enable setting 1: Enable Timer/Counter 1 interrupt generated by INT0 0: Disable Timer/Counter 1 interrupt generated by INT0 (default)
3	IE0_TMR0	INT0 TIMER0 interrupt enable setting 1: Enable Timer/Counter 0 interrupt generated by INT0 0: Disable Timer/Counter 0 interrupt generated by INT0 (default)
2	IE0_IN_TOG	INT0 I/O port toggle interrupt enable setting 1: Enable I/O port toggle interrupt generated by INT0 0: Disable I/O port toggle interrupt generated by INT0 (default)
1	IE0_WDT	INT0 WDT interrupt enable setting 1: Enable Watchdog Timer (WDT) Interrupt generated by INT0 0: Disable Watchdog Timer (WDT) Interrupt generated by INT0 (default)
0	IE0_LVD	INT0 LVD interrupt enable setting 1: Enable Low Voltage Detection (LVD) interrupt generated by INT0 0: Disable Low Voltage Detection (LVD) interrupt generated by INT0 (default)

-: unimplemented.

Interrupt Enable Register INT0_1_ENABLE
(Address: 0x0020_0D04) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	R/W	R/W	-	R/W	R/W	R/W	R/W
Name	Reserved	IE0_I2S_TX	IE0_I2S_RX	Reserved	IE0_DMA6	IE0_DMA5	IE0_DMA4	IE0_DMA3
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IE0_DMA2	IE0_DMA1	IE0_DMA0	IE0_TMR5	IE0_TMR4	IE0_CEC	IE0_IR	IE0_RTC

Bit Number	Bit Mnemonic	Description
31-15	Reserved	-
14	IE0_I2S_TX	INT0 I^2S transmit interrupt enable setting 1: Enable I^2S transmit data interrupt generated by INT0 0: Disable I^2S transmit data interrupt generated by INT0 (default)
13	IE0_I2S_RX	INT0 I^2S receive interrupt enable setting 1: Enable I^2S receive data interrupt generated by INT0 0: Disable I^2S receive data interrupt generated by INT0 (default)
12	Reserved	-
11	IE0_DMA6	INT0 DMA6 interrupt enable setting 1: Enable Direct Memory Access (DMA) 6 interrupt generated by INT0 0: Disable Direct Memory Access (DMA) 6 interrupt generated by INT0 (default)
10	IE0_DMA5	INT0 DMA5 interrupt enable setting 1: Enable Direct Memory Access (DMA) 5 interrupt generated by INT0 0: Disable Direct Memory Access (DMA) 5 interrupt generated by INT0 (default)
9	IE0_DMA4	INT0 DMA4 interrupt enable setting 1: Enable Direct Memory Access (DMA) 4 interrupt generated by INT0 0: Disable Direct Memory Access (DMA) 4 interrupt generated by INT0 (default)
8	IE0_DMA3	INT0 DMA3 interrupt enable setting 1: Enable Direct Memory Access (DMA) 3 interrupt generated by INT0 0: Disable Direct Memory Access (DMA) 3 interrupt generated by INT0 (default)
7	IE0_DMA2	INT0 DMA2 interrupt enable setting 1: Enable Direct Memory Access (DMA) 2 interrupt generated by INT0 0: Disable Direct Memory Access (DMA) 2 interrupt generated by INT0 (default)
6	IE0_DMA1	INT0 DMA1 interrupt Enable setting 1: Enable Direct Memory Access (DMA) 1 interrupt generated by INT0 0: Disable Direct Memory Access (DMA) 1 interrupt generated by INT0 (default)
5	IE0_DMA0	INT0 DMA0 interrupt enable setting 1: Enable Direct Memory Access (DMA) 0 interrupt generated by INT0 0: Disable Direct Memory Access (DMA) 0 interrupt generated by INT0 (default)
4	IE0_TMR5	INT0 TIMER5 interrupt enable setting 1: Enable Timer/Counter 5 interrupt generated by INT0 0: Disable Timer/Counter 5 interrupt generated by INT0 (default)
3	IE0_TMR4	INT0 TIMER4 interrupt enable setting 1: Enable Timer/Counter 4 interrupt generated by INT0 0: Disable Timer/Counter 4 interrupt generated by INT0 (default)
2	IE0_CEC	INT0 CEC interrupt enable setting 1: Enable HDMI CEC interrupt generated by INT0 0: Disable HDMI CEC interrupt generated by INT0 (default)
1	IE0_IR	INT0 IR interrupt enable setting 1: Enable IR interrupt generated by INT0 0: Disable IR interrupt generated by INT0 (default)

Bit Number	Bit Mnemonic	Description
0	IE0_RTC	INT0 RTC interrupt enable setting 1: Enable Real-Time Clock (RTC) interrupt generated by INT0 0: Disable Real-Time Clock (RTC) interrupt generated by INT0 (default)

-: unimplemented.

Interrupt Enable Register INT1_0_ENABLE
(Address: 0x0020_0D08) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IE1_ADC	IE1_I2C1	IE1_I2C0	IE1_SPI1	IE1_SPI0	Reserved	IE1_UART2	IE1_UART1
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IE1_UART0	IE1_TMR3	IE1_TMR2	IE1_TMR1	IE1_TMR0	IE1_IN_TOG	IE1_WDT	IE1_LVD

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15	IE1_ADC	INT1 ADC interrupt enable setting 1: Enable ADC interrupt generated by INT1 0: Disable ADC interrupt generated by INT1 (default)
14	IE1_I2C1	INT1 I^2C1 interrupt enable setting 1: Enable I^2C1 interrupt generated by INT1 0: Disable I^2C1 interrupt generated by INT1 (default)
13	IE1_I2C0	INT1 I^2C0 interrupt Enable setting 1: Enable I^2C0 Interrupt generated by INT1 0: Disable I^2C0 Interrupt generated by INT1 (default)
12	IE1_SPI1	INT1 SPI1 interrupt enable setting 1: Enable SPI1 interrupt generated by INT1 0: Disable SPI1 interrupt generated by INT1 (default)
11	IE1_SPI0	INT1 SPI0 interrupt enable setting 1: Enable SPI0 interrupt generated by INT1 0: Disable SPI0 interrupt generated by INT1 (default)
10	Reserved	-
9	IE1_UART2	INT1 UART2 interrupt enable setting 1: Enable UART2 interrupt generated by INT1 0: Disable UART2 interrupt generated by INT1 (default)
8	IE1_UART1	INT1 UART1 interrupt enable setting 1: Enable UART1 interrupt generated by INT1 0: Disable UART1 interrupt generated by INT1 (default)

Bit Number	Bit Mnemonic	Description
7	IE1_UART0	INT1 UART0 interrupt enable setting 1: Enable UART0 interrupt generated by INT1 0: Disable UART0 interrupt generated by INT1 (default)
6	IE1_TMR3	INT1 TIMER3 interrupt enable setting 1: Enable Timer/Counter 3 interrupt generated by INT1 0: Disable Timer/Counter 3 interrupt generated by INT1 (default)
5	IE1_TMR2	INT1 TIMER2 interrupt enable setting 1: Enable Timer/Counter 2 interrupt generated by INT1 0: Disable Timer/Counter 2 interrupt generated by INT1 (default)
4	IE1_TMR1	INT1 TIMER1 interrupt enable setting 1: Enable Timer/Counter 1 interrupt generated by INT1 0: Disable Timer/Counter 1 interrupt generated by INT1 (default)
3	IE1_TMR0	INT1 TIMER0 interrupt enable setting 1: Enable Timer/Counter 0 interrupt generated by INT1 0: Disable Timer/Counter 0 interrupt generated by INT1 (default)
2	IE1_IN_TOG	INT1 I/O port interrupt enable setting 1: Enable I/O Port Toggle interrupt generated by INT1 0: Disable I/O Port Toggle interrupt generated by INT1 (default)
1	IE1_WDT	INT1 WDT interrupt enable setting 1: Enable Watchdog Timer (WDT) Interrupt generated by INT1 0: Disable Watchdog Timer (WDT) Interrupt generated by INT1 (default)
0	IE1_LVD	INT1 LVD Interrupt enable setting 1: Enable Low Voltage Detection (LVD) interrupt generated by INT1 0: Disable Low Voltage Detection (LVD) interrupt generated by INT1 (default)

-: unimplemented.

Interrupt Enable Register INT1_1_ENABLE
(Address: 0x0020_0D0C) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	R/W	R/W	-	R/W	R/W	R/W	R/W
Name	Reserved	IE1_I2S_TX	IE1_I2S_RX	Reserved	IE1_DMA6	IE1_DMA5	IE1_DMA4	IE1_DMA3
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IE1_DMA2	IE1_DMA1	IE1_DMA0	IE1_TMR5	IE1_TMR4	IE1_CEC	IE1_IR	IE1_RTC

Bit Number	Bit Mnemonic	Description
31-15	Reserved	-

Bit Number	Bit Mnemonic	Description
14	IE1_I2S_TX	INT1 I^2S transmit interrupt enable setting 1: Enable I^2S transmit data interrupt generated by INT1 0: Disable I^2S transmit data interrupt generated by INT1 (default)
13	IE1_I2S_RX	INT1 I^2S receive interrupt enable setting 1: Enable I^2S receive data interrupt generated by INT1 0: Disable I^2S receive data interrupt generated by INT1 (default)
12	Reserved	-
11	IE1_DMA6	INT1 DMA6 interrupt enable setting 1: Enable Direct Memory Access (DMA) 6 interrupt generated by INT1 0: Disable Direct Memory Access (DMA) 6 interrupt generated by INT1 (default)
10	IE1_DMA5	INT1 DMA5 interrupt enable setting 1: Enable Direct Memory Access (DMA) 5 interrupt generated by INT1 0: Disable Direct Memory Access (DMA) 5 interrupt generated by INT1 (default)
9	IE1_DMA4	INT1 DMA4 interrupt enable setting 1: Enable Direct Memory Access (DMA) 4 interrupt generated by INT1 0: Disable Direct Memory Access (DMA) 4 interrupt generated by INT1 (default)
8	IE1_DMA3	INT1 DMA3 interrupt enable setting 1: Enable Direct Memory Access (DMA) 3 interrupt generated by INT1 0: Disable Direct Memory Access (DMA) 3 interrupt generated by INT1 (default)
7	IE1_DMA2	INT1 DMA2 interrupt enable setting 1: Enable Direct Memory Access (DMA) 2 interrupt generated by INT1 0: Disable Direct Memory Access (DMA) 2 interrupt generated by INT1 (default)
6	IE1_DMA1	INT1 DMA1 interrupt enable setting 1: Enable Direct Memory Access (DMA) 1 interrupt generated by INT1 0: Disable Direct Memory Access (DMA) 1 interrupt generated by INT1 (default)
5	IE1_DMA0	INT1 DMA0 interrupt enable setting 1: Enable Direct Memory Access (DMA) 0 interrupt generated by INT1 0: Disable Direct Memory Access (DMA) 0 interrupt generated by INT1 (default)
4	IE1_TMR5	INT1 TIMER5 interrupt enable setting 1: Enable Timer/Counter 5 interrupt generated by INT1 0: Disable Timer/Counter 5 interrupt generated by INT1 (default)
3	IE1_TMR4	INT1 TIMER4 interrupt enable setting 1: Enable Timer/Counter 4 interrupt generated by INT1 0: Disable Timer/Counter 4 interrupt generated by INT1 (default)

Bit Number	Bit Mnemonic	Description
2	IE1_CEC	INT1 CEC interrupt enable setting 1: Enable HDMI CEC interrupt generated by INT1 0: Disable HDMI CEC interrupt generated by INT1 (default)
1	IE1_IR	INT1 IR interrupt enable setting 1: Enable IR interrupt generated by INT1 0: Disable IR interrupt generated by INT1 (default)
0	IE1_RTC	INT1 RTC interrupt enable setting 1: Enable Real-Time Clock (RTC) interrupt generated by INT1 0: Disable Real-Time Clock (RTC) interrupt generated by INT1 (default)

-: unimplemented.

Interrupt Flag Register INT0_0_FLAG
(Address: 0x0020_0D10) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IF0_ADC	IF0_I2C1	IF0_I2C0	IF0_SPI1	IF0_SPI0	Reserved	IF0_UART2	IF0_UART1
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IF0_UART0	IF0_TMR3	IF0_TMR2	IF0_TMR1	IF0_TMR0	IF0_IN_TOG	IF0_WDT	IF0_LVD

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15	IF0_ADC	INT0 ADC interrupt event flag 1: ADC interrupt event occurred
14	IF0_I2C1	INT0 I2C1 interrupt event flag 1: I2C1 interrupt event occurred
13	IF0_I2C0	INT0 I^2C0 interrupt event flag 1: I^2C0 interrupt event occurred
12	IF0_SPI1	INT0 SPI1 interrupt event flag 1: SPI1 interrupt event occurred
11	IF0_SPI0	INT0 SPI0 interrupt event flag 1: SPI0 interrupt event occurred
10	Reserved	-
9	IF0_UART2	INT0 UART2 interrupt event flag 1: UART2 interrupt event occurred
8	IF0_UART1	INT0 UART1 interrupt event flag 1: UART1 interrupt event occurred
7	IF0_UART0	INT0 UART0 interrupt event flag 1: UART0 interrupt event occurred

Bit Number	Bit Mnemonic	Description
6	IF0_TMR3	INT0 TIMER3 interrupt event flag 1: TIMER3 interrupt event occurred
5	IF0_TMR2	INT0 TIMER2 interrupt event flag 1: TIMER2 interrupt event occurred
4	IF0_TMR1	INT0 TIMER1 interrupt event flag 1: TIMER1 interrupt event occurred
3	IF0_TMR0	INT0 TIMER0 interrupt event flag 1: TIMER0 interrupt event occurred
2	IF0_IN_TOG	INT0 I/O toggle interrupt event flag 1: I/O toggle interrupt event occurred
1	IF0_WDT	INT0 WDT interrupt event flag 1: Watchdog (WDT) interrupt event occurred
0	IF0_LVD	INT0 LVD interrupt event flag 1: LVD interrupt event occurred

-: unimplemented.

Interrupt Flag Register INT0_1_FLAG (Address: 0x0020_0D14) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	R/W	R/W	-	R/W	R/W	R/W	R/W
Name	Reserved	IF0_I2S_TX	IF0_I2S_RX	Reserved	IF0_DMA6	IF0_DMA5	IF0_DMA4	IF0_DMA3
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IF0_DMA2	IF0_DMA1	IF0_DMA0	IF0_TMR5	IF0_TMR4	IF0_CEC	IF0_IR	IF0_RTC

Bit Number	Bit Mnemonic	Description
31-15	Reserved	-
14	IF0_I2S_TX	INT0 I^2S transmit interrupt event flag 1: I^2S transmit data interrupt event occurred
13	IF0_I2S_RX	INT0 I^2S receive interrupt event flag 1: I^2S receive data interrupt event occurred
12	Reserved	-
11	IF0_DMA6	INT0 DMA6 interrupt event flag 1: DMA6 interrupt event occurred
10	IF0_DMA5	INT0 DMA5 interrupt event flag 1: DMA5 interrupt event occurred
9	IF0_DMA4	INT0 DMA4 interrupt event flag 1: DMA4 interrupt event occurred
8	IF0_DMA3	INT0 DMA3 interrupt event flag 1: DMA3 interrupt event occurred

Bit Number	Bit Mnemonic	Description
7	IF0_DMA2	INT0 DMA2 interrupt event flag 1: DMA2 interrupt event occurred
6	IF0_DMA1	INT0 DMA1 interrupt event flag 1: DMA1 interrupt event occurred
5	IF0_DMA0	INT0 DMA0 interrupt event flag 1: DMA0 interrupt event occurred
4	IF0_TMR5	INT0 TIMER5 interrupt event flag 1: TIMER5 Interrupt Event occurred
3	IF0_TMR4	INT0 TIMER4 interrupt event flag 1: TIMER4 interrupt event occurred
2	IF0_CEC	INT0 CEC interrupt event flag 1: CEC interrupt event occurred
1	IF0_IR	INT0 IR interrupt event flag 1: IR interrupt event occurred
0	IF0_RTC	INT0 RTC interrupt event flag 1: RTC interrupt event occurred

-: unimplemented.

Interrupt Flag Register INT1_0_FLAG (Address: 0x0020_0D18) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IF1_ADC	IF1_I2C1	IF1_I2C0	IF1_SPI1	IF1_SPI0	Reserved	IF1_UART2	IF1_UART1
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IF1_UART0	IF1_TMR3	IF1_TMR2	IF1_TMR1	IF1_TMR0	IF1_IN_TOG	IF1_WDT	IF1_LVD

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15	IF1_ADC	INT1 ADC interrupt event flag 1: ADC interrupt event occurred
14	IF1_I2C1	INT1 I^2C1 interrupt event flag 1: I^2C1 interrupt event occurred
13	IF1_I2C0	INT1 I^2C0 interrupt event flag 1: I^2C0 interrupt event occurred
12	IF1_SPI1	INT1 SPI1 interrupt event flag 1: SPI1 interrupt event occurred
11	IF1_SPI0	INT1 SPI0 interrupt event flag 1: SPI0 interrupt event occurred
10	Reserved	-

Bit Number	Bit Mnemonic	Description
9	IF1_UART2	INT1 UART2 interrupt event flag 1: UART2 interrupt event occurred
8	IF1_UART1	INT1 UART1 interrupt event flag 1: UART1 interrupt event occurred
7	IF1_UART0	INT1 UART0 interrupt event flag 1: UART0 interrupt event occurred
6	IF1_TMR3	INT1 TIMER3 interrupt event flag 1: TIMER3 interrupt event occurred
5	IF1_TMR2	INT1 TIMER2 interrupt event flag 1: TIMER2 Interrupt Event occurred
4	IF1_TMR1	INT1 TIMER1 interrupt event flag 1: TIMER1 interrupt event occurred
3	IF1_TMR0	INT1 TIMER0 interrupt event flag 1: TIMER0 interrupt event occurred
2	IF1_IN_TOG	INT1 I/O toggle interrupt event flag 1: I/O toggle interrupt event occurred
1	IF1_WDT	INT1 WDT interrupt event flag 1: Watchdog (WDT) interrupt event occurred
0	IF1_LVD	INT1 LVD interrupt event flag 1: LVD interrupt event occurred

-: unimplemented.

Interrupt Flag Register INT1_1_FLAG(Address: 0x0020_0D1C) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	R/W	R/W	-	R/W	R/W	R/W	R/W
Name	Reserved	IF1_I2S_TX	IF1_I2S_RX	Reserved	IF1_DMA6	IF1_DMA5	IF1_DMA4	IF1_DMA3
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IF1_DMA2	IF1_DMA1	IF1_DMA0	IF1_TMR5	IF1_TMR4	IF1_CEC	IF1_IR	IF1_RTC

Bit Number	Bit Mnemonic	Description
31-15	Reserved	-
14	IF1_I2S_TX	INT1 I^2S transmit interrupt event flag 1: I^2S transmit data interrupt event occurred
13	IF1_I2S_RX	INT1 I^2S receive interrupt event flag 1: I^2S receive data interrupt event occurred
12	Reserved	-
11	IF1_DMA6	INT1 DMA6 interrupt event flag 1: DMA6 interrupt event occurred

Bit Number	Bit Mnemonic	Description
10	IF1_DMA5	INT1 DMA5 interrupt event flag 1: DMA5 interrupt event occurred
9	IF1_DMA4	INT1 DMA4 interrupt event flag 1: DMA4 interrupt event occurred
8	IF1_DMA3	INT1 DMA3 interrupt event flag 1: DMA3 interrupt event occurred
7	IF1_DMA2	INT1 DMA2 interrupt event flag 1: DMA2 interrupt event occurred
6	IF1_DMA1	INT1 DMA1 interrupt event flag 1: DMA1 interrupt event occurred
5	IF1_DMA0	INT1 DMA1 interrupt event flag 1: DMA0 interrupt event occurred
4	IF1_TMR5	INT1 TIMER5 interrupt event flag 1: TIMER5 interrupt event occurred
3	IF1_TMR4	INT1 TIMER4 interrupt event flag 1: TIMER4 interrupt event occurred
2	IF1_CEC	INT1 CEC interrupt event flag 1: CEC interrupt event occurred
1	IF1_IR	INT1 IR interrupt event flag 1: IR interrupt event occurred
0	IF1_RTC	INT1 RTC interrupt event flag 1: RTC interrupt event occurred

-: unimplemented.

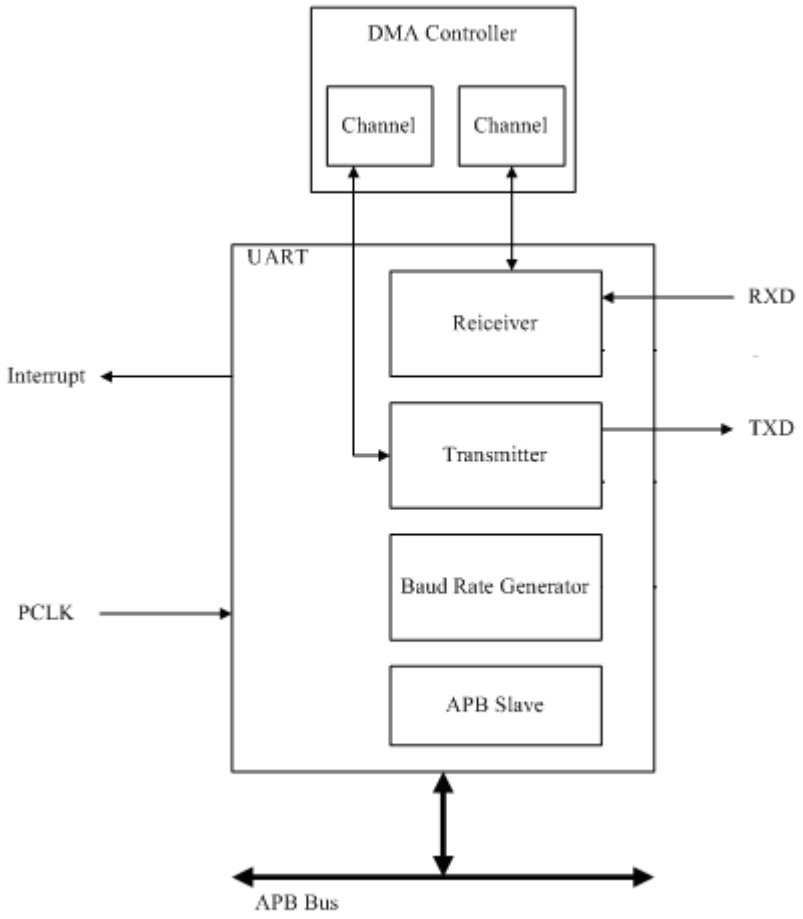
6.5 UART Receiver (UART)

6.5.1 Features

WT59F164 contains three Universal Asynchronous Receiver-Transmitters (UART0, UART1 and UART2), with features as below:

- Full duplex, asynchronous communications
- NRZ standard format
- Three UARTs, each with one baud rate generator
- Eight or nine bits data word length
- One Stop bit
- Separate enable/disable bits for transmitter or receiver
- Parity control
- With DMA function
- Transfer detection flags:
  - Receive data register full
  - Transmit data register empty
  - Transmit complete
- Four error detection flags
  - Overrun error
  - Frame error
  - Noise error
  - Parity error
- Interrupt sources:
  - Transmit data register empty
  - Transmit complete
  - Receive data register full
  - Break detection
  - Overrun error
  - Frame error
  - Noise error
  - Parity error
- Multi-processo communication – enter into mute mode if address match does not occur
- Wakeup from mute mode (by idle line detection or address mark detection)
- Two Receiver Wakeup modes: Address bit (MSB, 9th Bit), Idle line
- Send break
- Break detection length: 10/11/12/20/22/24 bit

6.5.2 Block Diagram

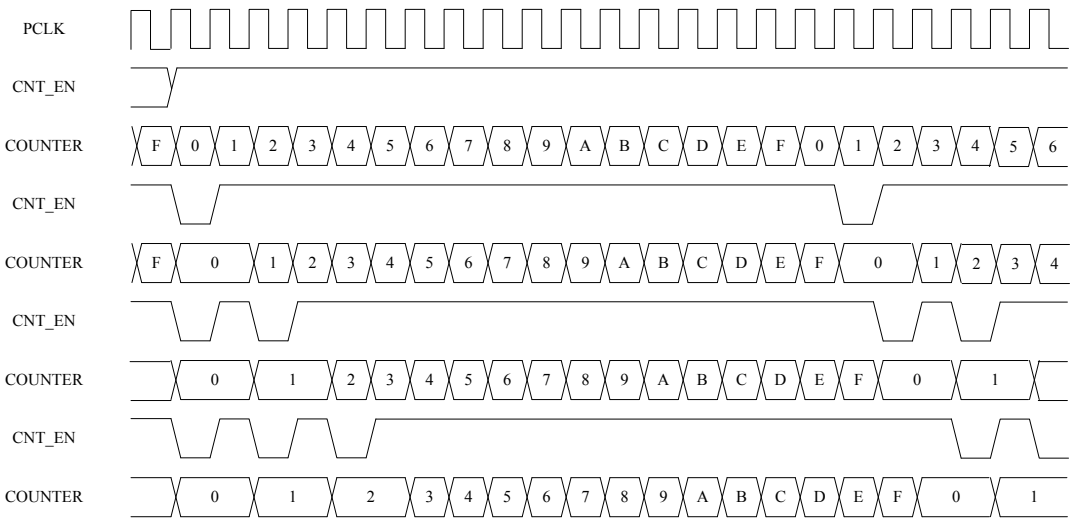


6.5.3 Baud Rate Generator

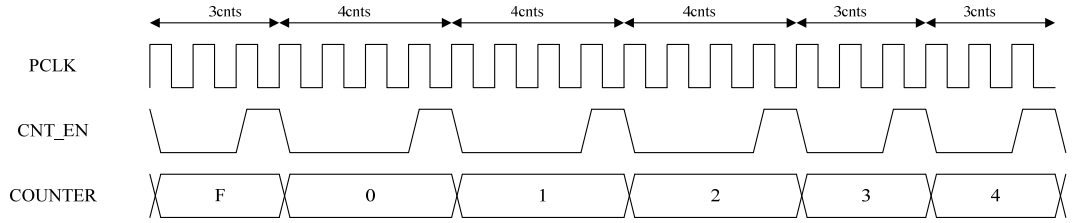
$$\text{Baud rate} = \frac{Pclk}{16*(Mantissa+\frac{Franction}{16})}$$

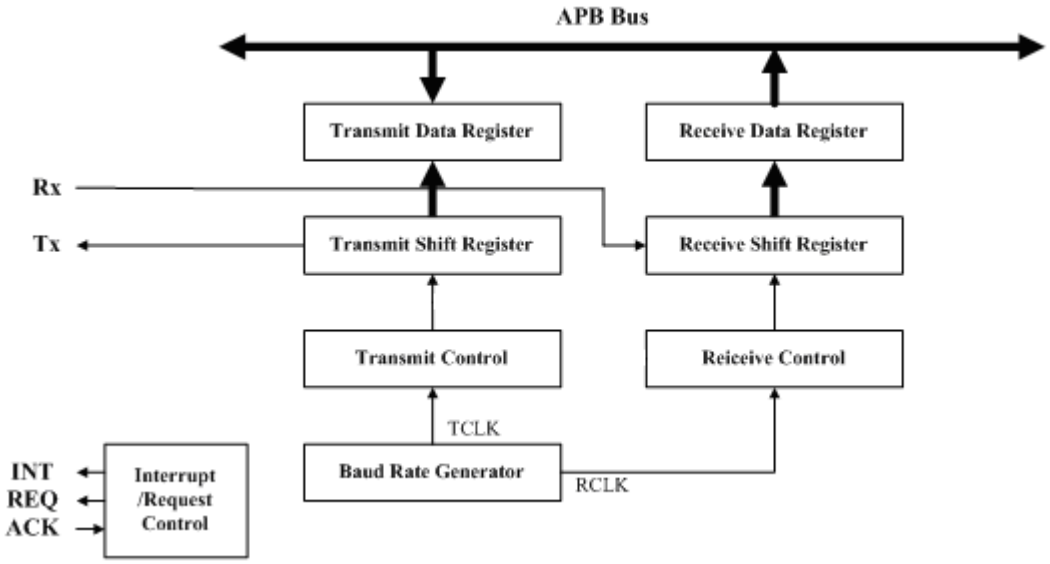
Ex: $\frac{Pclk}{16*(1+\frac{1}{16})}$, $\frac{Pclk}{16*(1+\frac{2}{16})}$, $\frac{Pclk}{16*(1+\frac{3}{16})}$

MCU Clock is Pclk.



Ex: $\frac{Pclk}{16*(3+\frac{3}{16})}$





6.5.4 UART Error

Overrun Error

When a data has received completely, if RXNE = 1, error occurred. In the meantime, data cannot be moved to UART Receive Buffer (UARTx_RXD) until RXNE = 1 data can be moved to UART Receive Buffer.

Noise Error

Noise detection from sampled data

Sampled value	NE status	Received bit value	Data validity
000	0	0	Valid
001	1	0	Not Valid
010	1	0	Not Valid
011	1	1	Not Valid
100	1	0	Not Valid

Noise detection from sampled data

Sampled value	NE status	Received bit value	Data validity
101	1	1	Not Valid
110	1	1	Not Valid
111	0	1	Valid

Framing Error

A framing error is detected when:
The stop bit is not recognized on reception at the expected time, following either a de-synchronization or excessive noise.

6.5.5 UART Special Register

Register Name	Address	Reset Default (Hex)	Description
UART Receiver Register 0 (UART0) 0x0020_3400~0x0020_37FF			
UART0_SET_CTL	0x0020_3400	0x0000_0000	UART0 function & mode setting
UART0_INT_CTL	0x0020_3404	0x0000_0000	UART0 interrupt enable
UART0_STATUS	0x0020_3408	0x0000_0000	UART0 status
UART0_TX_DATA	0x0020_340C		UART0 transmit data buffer
UART0_RX_DATA	0x0020_3410		UART0 receive data buffer
UART0_BAUDRATE	0x0020_3414	0x0000_0000	UART0 baud rate setting
UART0_BREAK	0x0020_3418	0x0000_0000	UART0 Break setting
UART Receiver Register 1 (UART1) 0x0020_3800~0x0020_3BFF			
UART1_SET_CTL	0x0020_3800	0x0000_0000	UART1 function & mode setting

Register Name	Address	Reset Default (Hex)	Description
UART1_INT_CTL	0x0020_3804	0x0000_0000	UART1 interrupt enable
UART1_STATUS	0x0020_3808	0x0000_0000	UART1 status
UART1_TX_DATA	0x0020_380C		UART1 transmit data buffer
UART1_RX_DATA	0x0020_3810		UART1 receive data buffer
UART1_BAUDRATE	0x0020_3814	0x0000_0000	UART1 baud rate setting
UART1_BREAK	0x0020_3818	0x0000_0000	UART1 break setting
UART Receiver Register 2 (UART2) 0x0020_3C00~0x0020_3FFF			
UART2_SET_CTL	0x0020_3C00	0x0000_0000	UART2 function & mode setting
UART2_INT_CTL	0x0020_3C04	0x0000_0000	UART2 interrupt enable
UART2_STATUS	0x0020_3C08	0x0000_0000	UART2 status
UART2_TX_DATA	0x0020_3C0C		UART2 transmit data buffer
UART2_RX_DATA	0x0020_3C10		UART2 receive data buffer
UART2_BAUDRATE	0x0020_3C14	0x0000_0000	UART2 baud rate setting
UART2_BREAK	0x0020_3C18	0x0000_0000	UART2 break setting

UART Control Register
UART0_SET_CTL (Address: 0x0020_3400)
UART1_SET_CTL (Address: 0x0020_3800)
UART2_SET_CTL (Address: 0x0020_3C00) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	WKAE_A	UE	TE	RE	M	DMAT	DMAR
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	RWU	WAKE	ADD[3:0]				PCE	PS

-: unimplemented.

Bit Number	Bit Mnemonic	Description
31-15	Reserved	-
14	WAKE_A	Address mark wakeup option 1: Receive data includes the address word 0: Receive data excludes the address word (default)
13	UE	UART enable setting 1: UART is enabled 0: UART is disabled (default)
12	TE	UART transmit enable setting 1: UART transmit is enabled 0: UART transmit is disabled (default)

Bit Number	Bit Mnemonic	Description
11	RE	UART receive enable setting 1: UART receive is enabled 0: UART receive is disabled (default)
10	M	UART word length setting 1: 9 data bits 0: 8 data bits (default)
9	DMAT	UART transmit DMA enable setting 1: Transmit DMA is enabled 0: Transmit DMA is disabled (default)
8	DMAR	UART receive DMA enable setting 1: Receive DMA is enabled 0: Receive DMA is disabled (default)
7	RWU	Receive wakeup setting 1: Receive in mute mode 0: Receive in active mode (default)
6	WAKE	Wakeup method setting in mute mode 1: Address mark wakeup (wakeup when received the same address of ADD[3:0] 0: Idle line wakeup (wakeup when receive Idle Frame) (default)
5-2	ADD[3:0]	USART node address setting
1	PCE	UART parity control enable setting 1: Parity is enabled 0: Parity is disabled (default)
0	PS	UART parity selection 1: Odd 0: Even (default)

-: unimplemented.

UART Interrupt Enable Register
UART0_INT_CTL (Address: 0x0020_3404)
UART1_INT_CTL (Address: 0x0020_3804)
UART2_INT_CTL (Address: 0x0020_3C04) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	R/W
Name	Reserved							IDLEIE
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	BDIE	TXEIE	TCIE	RXNEIE	EIE	Reserved		PEIE

Bit Number	Bit Mnemonic	Description
31-9	Reserved	-

Bit Number	Bit Mnemonic	Description
8	IDLEIE	UART IDLE interrupt enable setting 1: Enable UART IDLE interrupt (an interrupt is generated whenever UART0_STAT IDLE = 1) 0: Disable UART IDLE interrupt (default)
7	BDIE	UART BREAK detection interrupt enable setting 1: Enable UART BREAK detection interrupt (an interrupt is generated whenever UART0_STAT BD = 1) 0: Disable UART BREAK detection interrupt (default)
6	TXEIE	UART transmit interrupt enable setting 1: Enable UART transmit interrupt (an interrupt is generated whenever UART0_STAT TXE = 1) 0: Disable UART transmit interrupt (default)
5	TCIE	UART receive interrupt enable setting 1: Enable UART receive interrupt (an interrupt is generated whenever UART0_STAT TX = 1) 0: Disable UART receive interrupt (default)
4	RXNEIE	UART overrun error interrupt enable setting 1: Enable UART overrun error interrupt (an interrupt is generated whenever UART0_STAT ORE = 1) 0: Disable UART overrun error Interrupt (default)
3	EIE	UART error interrupt enable setting 1: Enable UART error interrupt (an interrupt is generated whenever UART0_STAT DMAR = 1, FE = 1, ORE = 1 or NE = 1) 0: Disable UART error interrupt (default)
2-1	Reserved	-
0	PEIE	UART parity error interrupt enable setting 1: Enable UART parity error interrupt (an interrupt is generated whenever UART0_STAT PE = 1) 0: Disable UART parity error interrupt (default)

-: unimplemented.

UART Status Register
UART0_STATUS (Address: 0x0020_3408)
UART1_STATUS (Address: 0x0020_3808)
UART2_STATUS (Address: 0x0020_3C08) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	R
Name	Reserved							IDLE
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R/W	R	R	R	R
Name	BD	TXE	TC	RXNE	ORE	NE	FE	PE

Bit Number	Bit Mnemonic	Description
31-9	Reserved	-
8	IDLE	IDLE LINE status flag 1: UART IDLE LINE is detected
7	BD	BREAK status flag 1: UART BREAK is detected
6	TXE	Transmit data register status flag 1: UART transmit data register (UART0_TXD) empty
5	TC	Transmission complete status flag 1: UART transmission is complete. Write 0 to this bit or write data to UART0_TXD will clear this bit
4	RXNE	Receive complete status flag 1: UART receive data complete, read receive data register (UART0_RXD) will clear this bit
3	ORE	Overrun error flag 1: UART overrun error, read receive data register (UART0_RXD) will clear this bit
2	NE	Noise error flag 1: UART noise is detected
1	FE	Frame error flag 1: UART frame error or break character is detected
0	PE	Parity error flag 1: UART parity error occurred

-: unimplemented.

UART Transmit Data Buffer
UART0_TX_DATA (Address: 0x0020_340C)
UART1_TX_DATA (Address: 0x0020_380C)
UART2_TX_DATA (Address: 0x0020_3C0C) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	R/W
Name	Reserved							TDR[8]
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	TDR[7:0]							

Bit Number	Bit Mnemonic	Description
31-9	Reserved	-
8-0	TDR[8:0]	UART transmit data buffer

-: unimplemented.

UART Receive Data Buffer
UART0_RX_DATA (Address: 0x0020_3410)
UART1_RX_DATA (Address: 0x0020_3810)
UART2_RX_DATA (Address: 0x0020_3C10) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	R/W
Name	Reserved							RDR[8]
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	RDR[7:0]							

Bit Number	Bit Mnemonic	Description
31-9	Reserved	-
8-0	RDR[8:0]	UART receive data buffer

-: unimplemented.

UART Baud Rate Setting Register
UART0_BAUDRATE (Address: 0x0020_3414)
UART1_BAUDRATE (Address: 0x0020_3814)
UART2_BAUDRATE (Address: 0x0020_3C14) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MANTISSA[11:4]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MANTISSA[3:0]				FRACTION[3:0]			

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-4	MANTISSA[11:0]	MANTISSA of UART baud rate generator (referring to 6.5.3 for baud rate planning)
3-0	FRACTION[3:0]	FRACTION of UART baud rate generator (referring to 6.5.3 for baud rate planning)

-: unimplemented.

UART BREAK Setting Register
UART0_BREAK (Address: 0x0020_3418)
UART1_BREAK (Address: 0x0020_3818)
UART2_BREAK (Address: 0x0020_3C18) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				SBK_EN	BKL	BKLD	STOP

Bit Number	Bit Mnemonic	Description
31-4	Reserved	-
3	SBK_EN	Transmit break character setting 1: Break character will be transmitted 0: No Break character is transmitted (default) If BKL = 1, SBK_EN is set by software and cleared by hardware If BKL = 0, SBK_EN is set and cleared by software
2	BKL	Break length setting and detection A: Send Break 1: Break character timing is controlled by hardware 0: Break character timing is controlled by software (default) Break character length = Start + M + n STOP B: Break detecting 1: BD = 1 when Break length = (Start + M + n STOP) 0: BD = 1 when Break length > (Start + M + n STOP) and a rising edge (default)
1	BKLD	Double Break length detection setting 1: Double Break length 0: Double Break length (default)
0	STOP	STOP bit length setting 1: STOP = 2 bits 0: STOP = 1 bit (default)

-: unimplemented.

6.6 Wakeup & I/O Toggle

6.6.1 Features

- Wakeup sources include: WDT, RTC 1S, LVD, ADC, IR, and GPIO
- All I/O can generate toggle by external rising-edge or falling-edge signal, and with Wakeup MCU function

6.6.2 Register

Register Name	Address	Reset Default (Hex)	Description
Wakeup & Interrupt Register 0x0020_0C00~0x0020_0FFF			
WK_MISC	0x0020_0C00	0x0000_0000	Peripheral wakeup enable setting
WK_GPIOA	0x0020_0C04	0x0000_0000	GPIOA wakeup enable setting
WK_GPIOB	0x0020_0C08	0x0000_0000	GPIOB wakeup enable setting
WK_GPIOC	0x0020_0C0C	0x0000_0000	GPIOC wakeup enable setting
WK_GPIOD	0x0020_0C10	0x0000_0000	GPIOD wakeup enable setting
TOGGLE_MISC	0x0020_0C18		Miscellaneous toggle status
TOGGLE_GPIOA	0x0020_0C1C		GPIOA toggle status
TOGGLE_GPIOB	0x0020_0C20		GPIOB toggle status
TOGGLE_GPIOC	0x0020_0C24		GPIOC toggle status
TOGGLE_GPIOD	0x0020_0C28		GPIOD toggle status
TOGGLE_CLR_ALL_INT	0x0020_0C30		Toggle status clear

Peripheral Wakeup Setting Register WK_MISC (Address: 0x0020_0C00) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	R/W	R/W	R/W	R/W	R/W
Name	Reserved			WDT_WAKE	RTC_1S_WAKE	LVD_WAKE	ADC_WAKE	IR_WAKE

Bit Number	Bit Mnemonic	Description
31-5	Reserved	-
4	WDT_WAKE	WDT wakeup enable setting 1: Enable WDT wakeup 0: Disable WDT wakeup (default)

Bit Number	Bit Mnemonic	Description
3	RTC_1S_WAKE	RTC 1-second wakeup enable setting 1: Enable RTC 1-second wakeup 0: Disable RTC 1-second wakeup (default)
2	LVD_WAKE	Low voltage detection wakeup setting 1: Enable LVD wakeup 0: Disable LVD wakeup (default)
1	ADC_WAKE	ADC complete wakeup setting 1: Enable ADC wakeup 0: Disable ADC wakeup (default)
0	IR_WAKE	IR Wakeup setting 1: Enable IR wakeup 0: Disable IR wakeup (default)

-: unimplemented.

GPIOA Wakeup Setting Register WK_GPIOA (Address: 0x0020_0C04) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	WK_GPIOA[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	WK_GPIOA[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	WK_GPIOA[15:0]	GPIOA[x] wakeup enable setting 1: Enable GPIOA[x] wakeup 0: Disable GPIOA[x] wakeup (default)

-: unimplemented.

GPIOB Wakeup Setting Register WK_GPIOB (Address: 0x0020_0C08) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	WK_GPIOB[15:8]							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	WK_GPIOB[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	WK_GPIOB[15:0]	GPIOB[x] wakeup enable setting 1: Enable GPIOB[x] wakeup 0: Disable GPIOB[x] wakeup (default)

-: unimplemented.

GPIOC Wakeup Setting Register WK_GPIOC (Address: 0x0020_0C0C) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	R/W	R/W	R/W	R/W	R/W
Name	Reserved			WK_GPIOC[12:8]				
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	WK_GPIOC[7:0]							

Bit Number	Bit Mnemonic	Description
31-13	Reserved	-
12-0	WK_GPIOC[12:0]	GPIOC[x] wakeup enable setting 1: Enable GPIOC[x] wakeup 0: Disable GPIOC[x] wakeup (default)

-: unimplemented.

GPIOD Wakeup setting Register WK_GPIOD (Address: 0x0020_0C10) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	-	-
Name	Reserved				WK_GPIOD [3:2]		Reserved	

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
3-2	WK_GPIOD[3:2]	GPIOD[x] wakeup enable setting 1: Enable GPIOD[x] wakeup 0: Disable GPIOD[x] wakeup (default)
1-0	Reserved	-

-: unimplemented.

Peripheral Toggle Status Register TOGGLE_MISC (Address: 0x0020_0C18) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	R	R	R	R	R	R
Name	Reserved		IN_TOG	WDT_EVT	RTC_1S_TOG	LVD_EVT	ADC_TOG	IR_TOG

Bit Number	Bit Mnemonic	Description
31-6	Reserved	-
5	IN_TOG	Toggle source status 1: Each toggle source toggled (including GPIO)
4	WDT_EVT	WDT toggle source status 1: WDT event
3	RTC_1S_TOG	RTC toggle source status 1: RTC 1S toggled
2	LVD_EVT	LVD toggle source status 1: LVD event
1	ADC_TOG	ADC toggle Source status 1: ADC toggled
0	IR_TOG	IR toggle Source status 1: IR toggled

-: unimplemented.

GPIOA Toggle Status Register TOGGLE_GPIOA (Address: 0x0020_0C1C) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R	R	R	R	R	R	R	R
Name	TOGGLE_GPIOA[15:8]							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	TOGGLE_GPIOA[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	TOGGLE_GPIOA[15:0]	GPIOA[x] toggle status 1: GPIOA[x] toggled

-: unimplemented.

GPIOB Toggle Status Register TOGGLE_GPIOB (Address: 0x0020_0C20) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R	R	R	R	R	R	R	R
Name	TOGGLE_GPIOB[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	TOGGLE_GPIOB[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	TOGGLE_GPIOB[15:0]	GPIOB[x] Toggle status 1: GPIOB[x] toggled

-: unimplemented.

GPIOC Toggle Status Register TOGGLE_GPIOC (Address: 0x0020_0C24) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	R	R	R	R	R
Name	Reserved			TOGGLE_GPIOC[12:8]				
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	TOGGLE_GPIOC[7:0]							

Bit Number	Bit Mnemonic	Description
31-13	Reserved	-

Bit Number	Bit Mnemonic	Description
12-0	TOGGLE_GPIOC[12:0]	GPIOC[x] toggle status 1: GPIOC[x] toggled

-: unimplemented.

GPIOD Toggle Status Register TOGGLE_GPIOD (Address: 0x0020_0C28) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R	R	-	-
Name	Reserved				TOGGLE_GPIOD[3:2]		Reserved	

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
3-2	TOGGLE_GPIOD[3:2]	GPIOD[x] toggle status 1: GPIOD[x] toggled
1-0	Reserved	-

-: unimplemented.

Toggle Status Clear Register TOGGLE_CLR_ALL_INT (Address: 0x0020_0C30) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	-	W
Name	Reserved							CLR_IN_TOG

Bit Number	Bit Mnemonic	Description
31-1	Reserved	-
0	CLR_IN_TOG	Toggle status clear setting 1: Clear all input toggle

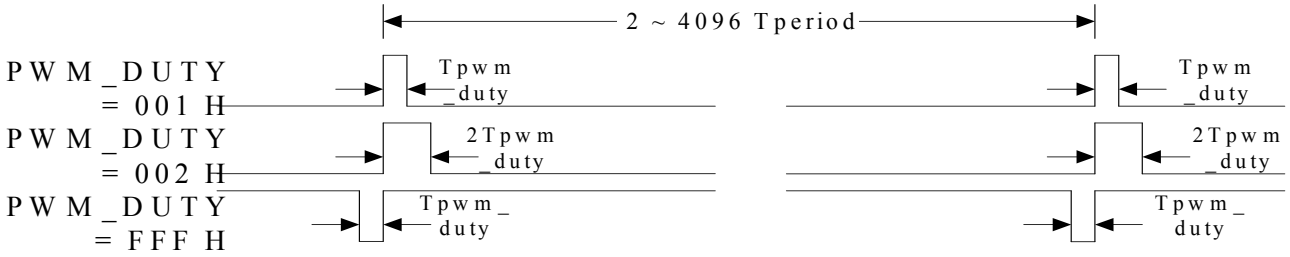
-: unimplemented.

6.7 Pulse Width Modulation (PWM)

6.7.1 Features

WT59F164 provides eight 12-bit precise Pulse Width Modulation modules to generate period and duty cycles.

- Clock source: MCU clock, can be configured as main frequency/1, 2, 3, or 12 by register PWMx_BASE_CLK
- With two special registers:
  PWM0_XXXX control PWM3~0 output
  PWM1_XXXX control PWM7~4 output
- Output frequency range:
  1.907 Hz ~ 6 MHz (at IRC 12 MHz)
  3.815 Hz ~ 12 MHz (at IRC 24 MHz)
- Duty range is from 0/4096 to 4095/4096



- If PWMx_PERIOD = 0, PWM[x] outputs high level

- If PWMx_PERIOD ≠ 0 and PWMx_DUTY = 0, PWM[x] outputs low level
- If PWMx_DUTY ＞ PWMx_PERIOD, PWM[x] outputs high level
- In normal mode:
  PWMx_PERIOD ≧ 1 and PWMx_DUTY ≧ 1
  PWMx_DUTY≦PWMx_PERIOD
- Configure if the corresponding PWM IO outputs PWM signal by PWM_EN[3:0]
  Example: MCU_CLOCK = 12 MHz and configure PWM[0]:
  If PWM0_BAS_CLK[1:0] = 0x03 => PWM Clock = 12 MHz/12 = 1 MHz
  PWM output frequency = 1 MHz/((PWM0_PWM0_CLK+1)*(PWM0_PWM0_PERIOD+1)), and then
  MAX frequency = 1 MHz/(1*2) = 500 kHz
  MIN frequency = 1 MHz/(128*4096) = 1.907 Hz

➢ The MAX and MIN frequency table while using internal RC oscillators:

PWM output frequency (Min/Max)	MCU Clock = 12 MHz	MCU Clock = 24 MHz
PWM_BAS_CLK = 00 (12 MHz/24 MHz)	22.89 Hz/6.0 MHz	45.78 Hz/12.0 MHz
PWM_BAS_CLK = 01 (6 MHz/12 MHz)	11.44 Hz/3.0 MHz	22.89 Hz/6.0 MHz
PWM_BAS_CLK = 10 (4 MHz/8 MHz)	7.63 Hz/2.0 MHz	15.26 Hz/4.0 MHz
PWM_BAS_CLK = 11 (1 MHz/2 MHz)	1.91 Hz/0.5 MHz	3.81 Hz/1.0 MHz

6.7.2 Register (PWM0)

Register Name	Address	Reset Default (Hex)	Description
Pulse Width Modulation Register 0 (PWM0)	**0x001F_5C00~0x001F_5FFF**		
PWM0_CTL	0x001F_5C00	0x0000_0000	PWM[3:0] enable setting
PWM0_BASE_CLK	0x001F_5C04	0x0000_0000	PWM[3:0] baseband setting
PWM0_PWM0_CLK	0x001F_5C08	0x0000_0000	PWM[0] clock setting
PWM0_PWM1_CLK	0x001F_5C0C	0x0000_0000	PWM[1] clock setting
PWM0_PWM2_CLK	0x001F_5C10	0x0000_0000	PWM[2] clock setting
PWM0_PWM3_CLK	0x001F_5C14	0x0000_0000	PWM[3] clock setting
PWM0_PWM0_DUTY	0x001F_5C18	0x0000_0200	PWM[0] duty setting
PWM0_PWM1_DUTY	0x001F_5C1C	0x0000_0200	PWM[1] duty setting
PWM0_PWM2_DUTY	0x001F_5C20	0x0000_0200	PWM[2] duty setting
PWM0_PWM3_DUTY	0x001F_5C24	0x0000_0200	PWM[3] duty setting
PWM0_PWM0_PERIOD	0x001F_5C28	0x0000_03FF	PWM[0] period setting
PWM0_PWM1_PERIOD	0x001F_5C2C	0x0000_03FF	PWM[1] period setting
PWM0_PWM2_PERIOD	0x001F_5C30	0x0000_03FF	PWM[2] period setting
PWM0_PWM3_PERIOD	0x001F_5C34	0x0000_03FF	PWM[3] period setting

PWM Control Register PWM0_CTL (Address: 0x0020_5C00) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	-	-	-
Name	PWM_EN[3:0]				Reserved			

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-4	PWM_EN[3:0]	PWM[x] enable setting 1: Enable PWM[x] (corresponding to PWM3 ~ PWM0 pin output) 0: Disable PWM[x] (corresponding to PWM3 ~ PWM0 pin output) (default)
1-0	Reserved	-

-: unimplemented.

PWM0 Main Frequency Control Register PWM0_BASE_CLK
(Address: 0x0020_5C04) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved						PWM_BAS_CLK[1:0]	

Bit Number	Bit Mnemonic	Description
31-2	Reserved	-
1-0	PWM_BAS_CLK[1:0]	PWM0 main frequency setting 00: MCU Clock (default) 01: MCU Clock/2 10: MCU Clock/3 11: MCU Clock/12

-: unimplemented.

PWM0 Frequency Control Register 0 PWM0_PWM0_CLK
(Address: 0x0020_5C08) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	PWM0_PWM0_CLK[6:0]						

Bit Number	Bit Mnemonic	Description
31-7	Reserved	-
6-0	PWM0_PWM0_CLK[6:0]	Frequency setting of PWM[0] output

PWM0 Frequency Control Register 1 PWM0_PWM1_CLK
(Address: 0x0020_5C0C) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	PWM0_PWM1_CLK[6:0]						

Bit Number	Bit Mnemonic	Description
31-7	Reserved	-
6-0	PWM0_PWM1_CLK[6:0]	Frequency setting of PWM[1] output

-: unimplemented.

PWM0 Frequency Control Register 2 PWM0_PWM2_CLK
(Address: 0x0020_5C10) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	PWM0_PWM2_CLK[6:0]						

Bit Number	Bit Mnemonic	Description
31-7	Reserved	-
6-0	PWM0_PWM2_CLK[6:0]	Frequency setting of PWM[2] output

-: unimplemented.

PWM0 Frequency Control Register 3 PWM0_PWM3_CLK
(Address: 0x0020_5C10) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	PWM0_PWM3_CLK[6:0]						

Bit Number	Bit Mnemonic	Description
31-7	Reserved	-
6-0	PWM0_PWM3_CLK[6:0]	Frequency setting of PWM[3] output

-: unimplemented.

PWM0 Duty Control Register 0 PWM0_PWM0_DUTY
(Address: 0x0020_5C18) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				PWM0_PWM0_DUTY[11:8]			
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM0_PWM0_DUTY[7:0]							

Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11-0	PWM0_PWM0_DUTY[11:0]	Duty setting of PWM[0] output

-: unimplemented.

PWM0 Duty Control Register 1 PWM0_PWM1_DUTY
(Address: 0x0020_5C1C) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				PWM0_PWM1_DUTY[11:8]			
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM0_PWM1_DUTY[7:0]							

Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11-0	PWM0_PWM1_DUTY[11:0]	Duty setting of PWM[1] output

-: unimplemented.

PWM0 Duty Control Register 2 PWM0_PWM2_DUTY
(Address: 0x0020_5C20) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				PWM0_PWM2_DUTY[11:8]			
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM0_PWM2_DUTY[7:0]							

Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11-0	PWM0_PWM2_DUTY[11:0]	Duty setting of PWM[2] output

-: unimplemented.

PWM0 Duty Control Register 3 PWM0_PWM3_DUTY
(Address: 0x0020_5C24) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				PWM0_PWM3_DUTY[11:8]			
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM3[7:0]							

Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11-0	PWM0_PWM3_DUTY[11:0]	Duty setting of PWM[3] output

-: unimplemented.

PWM0 Period Control Register 0
PWM0_PWM0_PERIOD (Address: 0x0020_5C28) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				PWM0_PWM0_PERIOD[11:8]			
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM0_PWM0_PERIOD[7:0]							

Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11-0	PWM0_PWM0_PERIOD[11:0]	Period setting of PWM[0] output

-: unimplemented.

PWM0 Period Control Register 1
PWM0_PWM1_PERIOD (Address: 0x0020_5C2C) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				PWM0_PWM1_PERIOD[11:8]			
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM0_PWM1_PERIOD[7:0]							

Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11-0	PWM0_PWM1_PERIOD[11:0]	Period setting of PWM[1] output

-: unimplemented.

PWM0 Period Control Register 2
PWM0_PWM2_PERIOD (Address: 0x0020_5C30) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Bit	-	-	-	-	-	-	-	-
Status	Reserved							
Name	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Bit	-	-	-	-	-	-	-	-
Status	Reserved							
Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Bit	-	-	-	-	R/W	R/W	R/W	R/W
Status	Reserved				PWM0_PWM2_PERIOD[11:8]			
Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Status	PWM0_PWM2_PERIOD[7:0]							

Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11-0	PMW0_PWM2_PERIOD[11:0]	Period setting of PWM[2] output

-: unimplemented.

PWM0 Period Control Register 3
PWM0_PWM3_PERIOD (Address: 0x0020_5C34) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				PWM0_PWM3_PERIOD[11:8]			

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM0_PWM3_PERIOD[7:0]							

Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11-0	PWM0_PWM3_PERIOD[11:0]	Period setting of PWM[3] output

-: unimplemented.

6.7.3 Register (PWM1)

Register Name	Address	Reset Default (Hex)	Description
Pulse Width Modulation Register 1(PWM1) 0x001F_6000~0x001F_63FF			
PWM1_CTL	0x001F_6000	0x0000_0000	PWM[7:4] enable setting
PWM1_BASE_CLK	0x001F_6004	0x0000_0000	PWM[7:4] baseband setting
PWM1_PWM0_CLK	0x001F_6008	0x0000_0000	PWM[4] clock setting
PWM1_PWM1_CLK	0x001F_600C	0x0000_0000	PWM[5] clock setting
PWM1_PWM2_CLK	0x001F_6010	0x0000_0000	PWM[6] clock setting
PWM1_PWM3_CLK	0x001F_6014	0x0000_0000	PWM[7] clock setting
PWM1_PWM0_DUTY	0x001F_6018	0x0000_0200	PWM[4] duty setting
PWM1_PWM1_DUTY	0x001F_601C	0x0000_0200	PWM[5] duty setting
PWM1_PWM2_DUTY	0x001F_6020	0x0000_0200	PWM[6] duty setting
PWM1_PWM3_DUTY	0x001F_6024	0x0000_0200	PWM[7] duty setting
PWM1_PWM0_PERIOD	0x001F_6028	0x0000_03FF	PWM[4] period setting
PWM1_PWM1_PERIOD	0x001F_602C	0x0000_03FF	PWM[5] period setting
PWM1_PWM2_PERIOD	0x001F_6030	0x0000_03FF	PWM[6] period setting
PWM1_PWM3_PERIOD	0x001F_6034	0x0000_03FF	PWM[7] period setting

PWM1 Control Register PWM1_CTL (Address: 0x0020_6000) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	-	-	-
Name	PWM_EN[3:0]				Reserved			

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-4	PWM_EN[3:0]	PWM[x] enable setting 1: Enable PWM[x] (corresponding to PWM7~PWM4 pin output) 0: Disable PWM[x] (corresponding to PWM7~PWM4 pin output) (default)
1-0	Reserved	-

-: unimplemented.

PWM1 Main Frequency Control Register PWM1_BASE_CLK
(Address: 0x0020_6004) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved						PWM_BAS_CLK[1:0]	

Bit Number	Bit Mnemonic	Description
31-2	Reserved	-
1-0	PWM_BAS_CLK[1:0]	PWM1 main frequency setting 00: MCU clock (default) 01: MCU clock/2 10: MCU clock/3 11: MCU clock/12

-: unimplemented.

PWM1 Frequency Setting Register 0 PWM1_PWM0_CLK
(Address: 0x0020_6008) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	PMW1_PWM0_CLK[6:0]						

Bit Number	Bit Mnemonic	Description
31-7	Reserved	-
6-0	PWM1_PWM0_CLK[6:0]	Frequency setting of PWM[4] output

-: unimplemented.

PWM1 Frequency Setting Register 1 PWM1_PWM1_CLK
(Address: 0x0020_600C) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	PWM1_PWM1_CLK[6:0]						

Bit Number	Bit Mnemonic	Description
31-7	Reserved	-
6-0	PWM1_PWM1_CLK[6:0]	Frequency setting of PWM[5] output

-: unimplemented.

PWM1 Frequency Setting Register 2 PWM1_PWM2_CLK
(Address: 0x0020_6010) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	PWM1_PWM2_CLK[6:0]						

Bit Number	Bit Mnemonic	Description
31-7	Reserved	-
6-0	PWM1_PWM2_CLK[6:0]	Frequency setting of PWM[6] output

-: unimplemented.

PWM1 Frequency Setting Register 3 PWM1_PWM3_CLK
(Address: 0x0020_6010) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	PWM1_PWM3_CLK[6:0]						

Bit Number	Bit Mnemonic	Description
31-7	Reserved	-
6-0	PWM1_PWM3_CLK[6:0]	Frequency setting of PWM[7] output

-: unimplemented.

PWM1 Duty Control Register 0 PWM0_PWM0_DUTY
(Address: 0x0020_6018) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				PWM1_PWM0_DUTY[11:8]			
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM1_PWM0_DUTY[7:0]							

Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11-0	PWM1_PWM0_DUTY[11:0]	Duty setting of PWM[4] output

-: unimplemented.

PWM1 Duty Control Register 1 PWM1_PWM1_DUTY
(Address: 0x0020_601C) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				PWM1_PWM1_DUTY[11:8]			
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM1_PWM1_DUTY[7:0]							

Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11-0	PWM1_PWM1_DUTY[11:0]	Duty setting of PWM[5] output

-: unimplemented.

PWM1 Duty Control Register 2 PWM1_PWM2_DUTY
(Address: 0x0020_6020) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				PWM1_PWM2_DUTY[11:8]			
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM1_PWM2_DUTY[7:0]							

Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11-0	PWM1_PWM2_DUTY[11:0]	Duty setting of PWM[6] output

-: unimplemented.

PWM1 Duty Control Register 3 PWM1_PWM3_DUTY
(Address: 0x0020_6024) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				PWM1_PWM3_DUTY[11:8]			
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM1_PWM3_DUTY[7:0]							

Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11-0	PWM1_PWM3_DUTY[11:0]	Duty setting of PWM[7] output

-: unimplemented.

PWM1 Period Control Register 0 PWM1_PWM0_PERIOD
(Address: 0x0020_6028) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				PWM1_PWM0_PERIOD[11:8]			
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM1_PWM0_PERIOD[7:0]							

Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11-0	PWM1_PWM0_PERIOD[11:0]	Period setting of PWM[4] output

-: unimplemented.

PWM1 Period Control Register 1 PWM1_PWM1_PERIOD
(Address: 0x0020_602C) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				PWM1_PWM1_PERIOD[11:8]			

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM1_PWM1_PERIOD[7:0]							

Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11-0	PWM1_PWM1_PERIOD[11:0]	Period setting of PWM[5] output

-: unimplemented.

PWM1 Period Register 2 PWM1_PWM2_PERIOD
(Address: 0x0020_6030) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				PWM1_PWM2_PERIOD[11:8]			
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM1_PWM2_PERIOD[7:0]							

Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11-0	PWM1_PWM2_PERIOD[11:0]	Period setting of PWM[6] output

-: unimplemented.

PWM1 Period Control Register 3 PWM1_PWM3_PERIOD
(Address: 0x0020_6034) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				PWM1_PWM3_PERIOD[11:8]			
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM1_PWM3_PERIOD[7:0]							

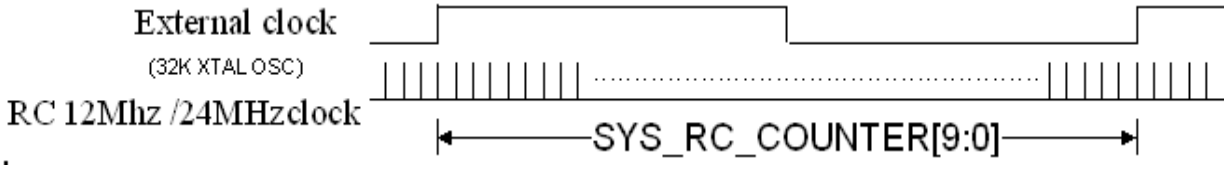
Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11-0	PWM1_PWM3_PERIOD[11:0]	Period setting of PWM[7] output

6.8 12 MHz RC Oscillator Calibration

6.8.1 Features

WT59F164 has a built-in 12/24 MHz RC oscillator to reduce the cost of external crystal oscillator. For more precise system clock, external crystal oscillator 12 MHz is available. In addition, it is a better choice to use 32.768 kHz (crystal oscillator) to calibrate internal RC 12 MHz oscillators (calibration can reach ±2% at -40℃ ~ +105℃). This section will introduce how to calibrate the Internal 12 MHz/24 MHz RC Oscillator by using 32.768 kHz.

- SYS_RC_COUNTER[9:0] counts with 32.768 kHz external Crystal Oscillator by Internal RC, which stores the counter value between two rising-edge of 32.768 kHz



- The table below indicates the SYS_RC_COUNTER[9:0] value which is close to 12MH when internal RC selects 12 MHz, and external 32K Crystal Oscillator selects 32.768 kHz, 50 kHz, and 100 kHz Crystal Oscillator frequency individually. The calibration is by setting the value of HSI_COARSE_SEL[2:0] and HSI_FINE_SEL[3:0] to have the value read from SYS_RC_COUNTER[9:0] close to the table below.

RCOSC = 12 MHz

	32 kHz	± 0.27%	50 kHz	± 0.42%	100 kHz	± 0.83%
SYS_RC_COUNTER[9:0]	366	11.993 MHz	239	11.950 MHz	119	11.900MHz
SYS_RC_COUNTER[9:0]	367	12.026 MHz	240	12.000 MHz	120	12.000 MHz
SYS_RC_COUNTER[9:0]	368	12.059 MHz	241	12.050 MHz	121	12.100 MHz

- The table below indicates the SYS_RC_COUNTER[9:0] value which is close to 24MH when internal RC selects 24 MHz, and external 32K Crystal Oscillator selects 32.768 kHz, 50 kHz, and 100 kHz Crystal Oscillator frequency individually. The calibration is by setting the value of HSI_COARSE_SEL[2:0] and HSI_FINE_SEL[3:0] to have the value read from SYS_RC_COUNTER[9:0] close to the table below.

RCOSC = 24 MHz

	32 kHz	± 0.14%	50 kHz	± 0.21%	100 kHz	± 0.83%
SYS_RC_COUNTER[9:0]	732	23.986 MHz	479	23.950 MHz	239	23.900 MHz
SYS_RC_COUNTER[9:0]	733	24.019 MHz	480	24.000 MHz	240	24.000 MHz
SYS_RC_COUNTER[9:0]	734	24.052 MHz	481	24.050 MHz	241	24.100 MHz

- The flash Information Block stores RC oscillator initial data and selects auto reload on reset. Please refer to section 5.7 for detailed information.

6.8.2 Register

Register Name	Address	Reset Default (Hex)	Description
System Register & Low Voltage Detection and Reset Register (System Control) 0x0020_0000~0x0020_03FF			
SYS_RC_COUNTER	0x0020_0008		Counts value with 32.768 kHz external clock by internal RC (storing the counter value between two rising edge of 32.768 kHz)
SYS_CALIBRATE_RC_FREQ	0x0020_002C	0x0000_0040	RC Oscillator frequency adjust

Internal RC Calibration Register SYS_RC_COUNTER

(Address: 0x0020_0008) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	R	R
Name	Reserved						SYS_RC_COUNTER[9:8]	
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	SYS_RC_COUNTER[7:0]							

Bit Number	Bit Mnemonic	Description
31-10	Reserved	-
9-0	SYS_RC_COUNTER[9:0]	Counts value with 32.768 kHz external clock by internal RC (storing the counter value between two rising edge of 32.768 kHz)

-: unimplemented.

System RC Control Register SYS_CALIBRATE_RC_FREQ

(Address: 0x0020_002C) Reset Value: 0x0000_0040

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	HSI_CLK_SEL	HSI_COARSE_SEL[2:0]			HSI_FINE_SEL[3:0]			

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	HSI_CLK_SEL	Internal high-speed RC oscillator frequency selection 1: 24 MHz 0: 12 MHz (default)
6-4	HSI_COARSE_SEL[2:0]	Internal high-speed RC oscillator coarse adjustment selection 001: 16-unit current (8%) 010: 32-unit current (16%) 011: 48-unit current (24%) 100: 64-unit current (32%) (default) 101: 80-unit current (40%) 110: 96-unit current (48%) 111: 112-unit current (56%)
3-0	HSI_FINE_SEL[3:0]	Internal high-speed RC oscillator fine adjustment selection 0000: 0-unit current (0%) (default) 0001: 1-unit current (0.5%) 0010: 2-unit current (1%) 0011: 3-unit current (1.5%) 0100: 4-unit current (2%) 0101: 5-unit current (2.5%) 0110: 6-unit current (3%) 0111: 7-unit current (3.5%) 1000: 8-unit current (4%) 1001: 9-unit current (4.5%) 1010: 10-unit current (5%) 1011: 11-unit current (5.5%) 1100: 12-unit current (6%) 1101: 13-unit current (6.5%) 1110: 14-unit current (7%) 1111: 15-unit current (7.5%)

-: unimplemented.

6.9 Watchdog Timer

6.9.1 Features

Watchdog Timer can be used to detect CPU failures, such as the software deadlock circles caused by noises, voltage disturbance, or power off. When an internal counter of the Watchdog Timer overflows, a reset signal will be generated then reset the CPU.

To prevent a reset occurred on Watchdog Timer, software can clear Watchdog Timer periodically (by setting register WDT_RST). When unpredictable reset occurred, user should check the WDT_RST_EVT bit to judge if the previous reset is occurred by Watchdog Timer.

- Clock Sources of Watchdog Timer: Internal 128 kHz or MCU main frequency
- Select MCU main frequency as clock source of Watchdog Timer, in the meantime MCU uses external Crystal Oscillator, the HSE_CLK_SEL must be set precisely to prevent abnormal on Watchdog Timer reset.
- Reset Time: 33 ms, 65 ms, 1S, 2S, or 8S
- The software can clear Watchdog Timer by writing register WDT_RST, WDT_DET or DIS_WDT (WDT is turned off). Otherwise, CPU will reset when times out
- When a Watchdog Reset occurred, WDT_DET_EVT = 1. Meanwhile software can clear WDT_DET_EVT by setting DIS_WDT = 1
- The WDT reset time of using Internal 24 MHz and 128 kHz

	MCU_24 MHz	RC_128 kHz
WDT_RST[2:0] = 000	1.048576s	1.024s
WDT_RST[2:0] = 001	65.536ms	64ms
WDT_RST[2:0] = 010	32.768ms	32ms
WDT_RST[2:0] = 011	2.097152s	2.048s
WDT_RST[2:0] = 1xx	8.23072s	8.128s

- WDT timer can be cleared by setting DIS_WDT = 0 and recount
- With WDT detection function. An interrupt is generated when WDT_DET[2:0] times out

6.9.2 Special Register

Register Name	Address	Reset Default (Hex)	Description
Watchdog Timer Register (WDT) 0x0020_0800~0x0020_0BFF			
WDT_CTL	0x0020_0800	0x0000_0000	WDT enable & interrupt setting
WDT_RST	0x0020_0804	0x0000_0000	WDT reset time setting
WDT_DET	0x0020_0808	0x0000_0000	WDT detection time adjustment

Watchdog Timer Control Register WDT_CTL (Address: 0x0020_0800) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	-	-	R
Name	DIS_WDT	WDT_CLK_SEL	WDT_INT_EN	WDT_INT_CLR	Reserved			WDT_RST_EVT

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	DIS_WDT	Watchdog Timer disable setting 1: Disable Watchdog Timer 0: Enable Watchdog Timer (default)
6	WDT_CLK_SEL	Watchdog Timer clock source selection 1: WDT clock source is internal 128 kHz RC oscillator (±20%) 0: WDT clock source is MCU clock (the calibration can reach ±2% if use internal RC) (default)
5	WDT_INT_EN	Watchdog Timer interrupt enable setting 1: Enable WDT interrupt 0: Disable WDT interrupt (default)
4	WDT_INT_CLR	WDT interrupt clear setting 1: clear interrupt
3-1	Reserved	-
0	WDT_RST_EVT	WDT reset event flag 1: WDT reset occurred (this bit is set by hardware automatically, and software is cleared by setting DIS_WDT)

-: unimplemented.

Watchdog Reset Time Setting Register WDT_RST
(Address: 0x0020_0804) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	R/W	R/W	R/W
Name	Reserved					WDT_RST[2:0]		

Bit Number	Bit Mnemonic	Description
31-3	Reserved	-
2-0	WDT_RST[2:0]	Watchdog reset time setting 1xx: Watchdog Reset Time = 8s 000: Watchdog Reset Time = 1s (default) 001: Watchdog Reset Time = 2s 010: Watchdog Reset Time = 33ms 011: Watchdog Reset Time = 65ms

-: unimplemented.

Watchdog Detection Time Setting Register WDT_DET
(Address: 0x0020_0808) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved						WDT_DET[1:0]	

Bit Number	Bit Mnemonic	Description
31-2	Reserved	-
1-0	WDT_DET[1:0]	Watchdog detection time setting 1x: Watchdog Detection Time = 5s 00: Watchdog Detection Time = 1s (default) 01: Watchdog Detection Time = 2s

-: unimplemented.

6.10 Real-Time Clock (RTC)

6.10.1 Features

Real-Time Clock is a precise clock. It is clocked by an external 32.768 kHz Crystal Oscillator and is configured to generate a time base of 1 second interrupt.

- Real-Time Clock source: external 32.768 kHz Crystal Oscillator
- With registers to store Second, Minute, Hour, Day, Week, Month, and Year BCD code
- With four backup registers (RTC_BACKUP1~4) to backup RTC time
- With Time Calibration function (by setting register RTC_CAL)

6.10.2 Special Register

Register Name	Address	Reset Default (Hex)	Description
Real Time Clock Register (RTC) 0x0020_1000~0x0020_13FF			
RTC_SEC	0x0020_1000	0x0000_0000	RTC Second BCD code
RTC_MIN	0x0020_1004	0x0000_0000	RTC Minute BCD code
RTC_HOUR	0x0020_1008	0x0000_0000	RTC Hour BCD code
RTC_DAY	0x0020_100C	0x0000_0001	RTC Day BCD code
RTC_WEEK	0x0020_1010	0x0000_0000	RTC Week BCD code
RTC_MONTH	0x0020_1014	0x0000_0001	RTC Month BCD code
RTC_YEAR	0x0020_1018	0x0000_0000	RTC Year BCD code
RTC_BACKUP1	0x0020_1020	0x0000_0000	RTC Backup
RTC_BACKUP2	0x0020_1024	0x0000_0000	RTC Backup
RTC_BACKUP3	0x0020_1028	0x0000_0000	RTC Backup
RTC_BACKUP4	0x0020_102C	0x0000_0000	RTC Backup
RTC_AMP	0x0020_1030	0x0000_0000	RTC start-up circuit current amplifier setting
RTC_CAL	0x0020_1034	0x0000_0000	RTC calibration setting
RTC_PARAMETER	0x0020_1038	0x0000_0009	RTC power and output frequency setting
RTC_MISC	0x0020_103C	0x0000_0062	RTC start-up circuit bias setting

Real Time Clock Second Register RTC_SEC (Address: 0x0020_1000) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	RTC_SEC[6:0]						

Bit Number	Bit Mnemonic	Description
31-7	Reserved	-
6-0	RTC_SEC[6:0]	Second coded in BCD, range is 0~59 RTC_SEC[6-4] represents 10 seconds RTC_SEC[3-0] represents seconds

-: unimplemented.

Real-Time Clock Minute Register RTC_MIN (Address: 0x0020_1004) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	RTC_MIN[6:0]						

Bit Number	Bit Mnemonic	Description
31-7	Reserved	-
6-0	RTC_MIN[6:0]	Minute coded in BCD, range is 0~59 RTC_MIN[6-4] represents 10 minutes RTC_MIN[3-0] represents minutes

-: unimplemented.

Real-Time Clock Hour Register RTC_HOUR (Address: 0x0020_1008) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved		RTC_HOUR[5:0]					

Bit Number	Bit Mnemonic	Description
31-6	Reserved	-
5-0	RTC_HOUR[5:0]	Hour coded in BCD, range is 0~23 RTC_HOUR[5-4] represents 10 hours RTC_HOUR[3-0] represents hours

-: unimplemented.

Real-Time Clock Day Register RTC_DAY (Address: 0x0020_100C) Reset Value: 0x0000_0001

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved		RTC_HOUR[5:0]					

Bit Number	Bit Mnemonic	Description
31-6	Reserved	-
5-0	RTC_DAY[5:0]	Day of month coded in BCD, range is 1~31 RTC_DAY[5-4] represents 10 days RTC_DAY[3-0] represents days

-: unimplemented.

Real-Time Clock Week Register RTC_WEEK (Address: 0x0020_1010) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	R/W	R/W	R/W
Name	Reserved					RTC_WEEK[2:0]		

Bit Number	Bit Mnemonic	Description
31-3	Reserved	-
2-0	RTC_WEEK[2:0]	Day of week 000: Sunday

Bit Number	Bit Mnemonic	Description
		001: Monday 010: Tuesday 011: Wednesday 100: Thursday 101: Friday 110: Saturday

-: unimplemented.

Real-Time Clock Month Register RTC_MONTH (Address: 0x0020_1014) Reset Value: 0x0000_0001

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	R/W	R/W	R/W
Name	Reserved					RTC_WEEK[2:0]		

Bit Number	Bit Mnemonic	Description
31-4	Reserved	-
3-0	RTC_MONTH[3:0]	Month 0001: January 0010: February 0011: March 0100: April 0101: May 0110: June 0111: July 1000: August 1001: September 1010: October 1011: November 1100: December

-: unimplemented.

Real-Time Clock Year Register RTC_YEAR (Address: 0x0020_1018) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	RTC_YEAR[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	RTC_YEAR[7:0]	Year coded in BCD, range is 0~99 RTC_YEAR[7-4] represents 10 years RTC_YEAR[3-0] represents years

-: unimplemented.

Real-Time Clock Backup Register 1 RTC_BACKUP1
(Address: 0x0020_1020) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	RTC_BAKUP1[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	RTC_BAKUP1[7:0]	RTC backup register 1

-: unimplemented.

Real-Time Clock Backup Register 2 RTC_BACKUP2
(Address: 0x0020_1024) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	RTC_BAKUP2[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	RTC_BAKUP2[7:0]	RTC backup register 2

-: unimplemented.

Real-Time Clock Backup Register 3 RTC_BACKUP3
(Address: 0x0020_1028) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	RTC_BAKUP3[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	RTC_BAKUP3[7:0]	RTC backup register 3

-: unimplemented.

Real-Time Clock Backup Register 4 RTC_BACKUP4
(Address: 0x0020_102C) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	RTC_BAKUP4[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	RTC_BAKUP4[7:0]	RTC backup register 4

-: unimplemented.

Real-Time Clock Current Amplifier Register RTC_AMP
(Address: 0x0020_1030) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				RTC_AMP[3:0]			

Bit Number	Bit Mnemonic	Description
31-4	Reserved	-
3-0	RTC_AMP[3:0]	RTC_AMP[3:2] enlarge the 2nd amplifier stage current RTC_AMP[1:0] enlarge the 1st amplifier stage current Current Amplifier: 11: four units 10: three units 01: two units 00: one unit

-: unimplemented.

Real-Time Clock Calibration Register RTC_CAL
(Address: 0x0020_1034) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	RTC_CA[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	RTC_CA[7:0]	RTC Calibration bits RTC_CA[7] = 1: add clocks; RTC_CA[7] = 0: skip clocks; RTC_CA[6:0]: number which add/skip clock within 128 minutes (add/skip 128 crystal clocks in one second of minute)

-: unimplemented.

Real-Time Clock Control Register 0 RTC_PARAMETER
(Address: 0x0020_1038) **Reset Value: 0x0000_0009**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	RTC_PDOSC	RTC_STOP	RTC_FAST	RTC_TEST	RTC_PDOSCSU	RTC_FS[2:0]		

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	RTC_PDOSC	32.768 kHz oscillator power down setting 1: 32.768 kHz oscillator power down (default) 0: 32.768 kHz oscillator enable
6	RTC_STOP	Stop RTC counting 1: Stop RTC counting 0: Enable RTC (default)
5	RTC_FAST	RTC fast mode setting 1: Fast mode for RTC test, it breaks the counter chain at DAY_CLOCK interrupt 0: Normal (default)
4	RTC_TEST	RTC Test mode setting 1: RTC clock source is GPIO (for test purpose) 0: RTC clock source is external 32.768 kHz (default)
3	RTC_PDOSCSU	32.768 kHz oscillator start up circuit power down setting 1: Power down 32.768 kHz oscillator start up circuit (when 32.768 kHz is stable, MCU can set this bit to reduce consumption) 0: Enable 32.768 kHz start up circuit (default)
2-0	RTC_FS[2:0]	Clock output frequency (RTC_SEC cumulative frequency) 000: no output 001: 0.25 Hz (default) 010: 1 Hz 011: 8 Hz

Bit Number	Bit Mnemonic	Description
		100: 64 Hz 101: 512 Hz 110: 1024 Hz 111: 32768 Hz

-: unimplemented.

Real-Time Clock Start Up Circuit Control Register RTC_MISC
(Address: 0x0020_103C) Reset Value: 0x0000_0062

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	-	R/W	R/W
Name	RTC_RX[3:0]				Reserved		RTC_DRV2	RTC_DRV1

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-4	RX[3:0]	RTC bias resistor setting 0000: 50K 0001: 300K 0010: 350K 0011: 400K 0100: 450K 0101: 500K 0110: 550K (default) 0111: 600K 1000: 650K 1001: 700K 1010: Reserved 1011: Reserved 11xx: 700K
3-2	Reserved	-
1	DRV2	Crystal oscillator bias current control 1: Default 0: Enlarge the crystal bias current If DRV2 = 1, Oscillator can oscillate fast, when crystal oscillate stably, MCU can program DRV2 = 0 to reduce power.
0	DRV1	Crystal oscillator driver gain control 1: Enlarge the gain of crystal driver 0: Default

-: unimplemented.

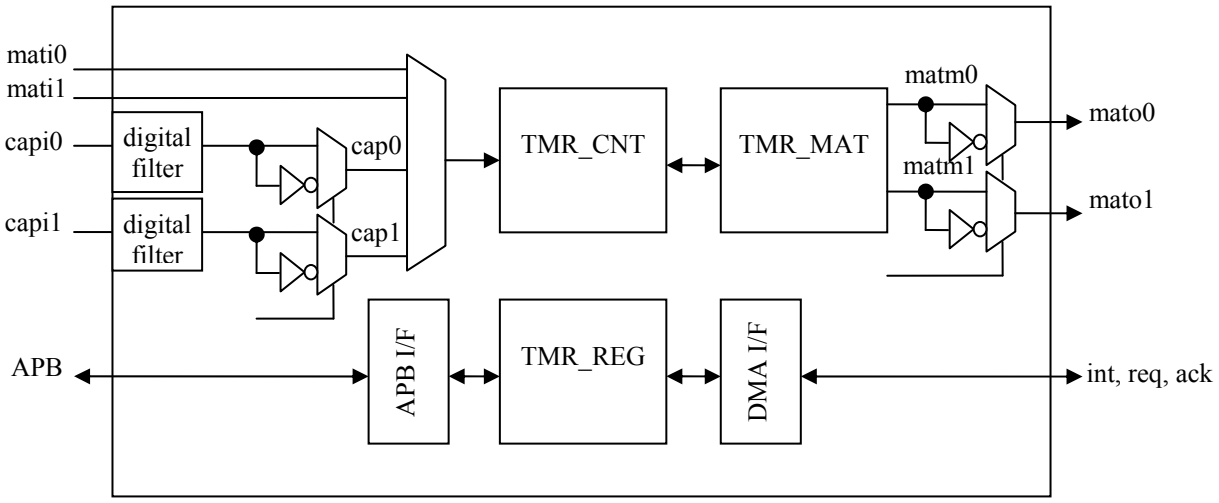
6.11 Timer/Counter

6.11.1 Features

The WT59F164 contains six 16-Bit Timer/Counters (Timer0 ~ Timer5). All six Timer/Counters can be configured as Timer or Counter. It also supports prescaler function and capture modes, and may be used for a variety of purposes, including measuring the pulse lengths of external signals or generating output waveforms (PWM) based on match registers. The timers can also generate interrupts or DMA requests as system requirements.

- A 16-Bit Timer/Counter with a programmable 16-Bit Prescaler
- Counter or Timer operation
- Two 16-Bit capture channels per timer, includes PWM input detection
- Synchronization circuit to control the timer with external signals and other timers
- Interrupt/DMA generation on the following events:
  - Input Capture
  - Output Match
- Four 16-Bit match registers that allow:
  - Continuous operation with optional interrupt generation on match
  - Stop timer on match with optional interrupt generation
  - Reset timer on match with optional interrupt generation
- Two external outputs corresponding to match registers, with the following capabilities:
  - Set low on match
  - Set high on match
  - Toggle on match
- The combination of paired match registers generates PWM output

TIMER



6.11.2 Timer/Counter Special Register

Register Name	Address	Reset Default (Hex)	Description
Timer/Counter Register 0(Timer0) 0x0020_1C00~0x0020_1FFF			
TIMER0_CTL	0x0020_1C00	0x0000_0000	Timer/Counter 0 enable & mode setting
TIMER0_COUNT	0x0020_1C04	0x0000_0000	Timer/Counter 0 counter value
TIMER0_PSCL	0x0020_1C08	0x0000_0000	Timer/Counter 0 prescaler setting
TIMER0_PCNT	0x0020_1C0C	0x0000_0000	Timer/Counter 0 prescaler value
TIMER0_CCTL	0x0020_1C10	0x0000_0000	Counter 0 catch setting
TIMER0_CICTL	0x0020_1C14	0x0000_0000	Counter 0 input setting
TIMER0_MCTL	0x0020_1C18	0x0000_0000	Timer/Counter 0 match control
TIMER0_MOCTL	0x0020_1C1C	0x0000_0000	Timer/Counter 0 match output control
TIMER0_MAT0A	0x0020_1C30	0x0000_0000	Timer/Counter 0 match setting
TIMER0_MAT0B	0x0020_1C34	0x0000_0000	Timer/Counter 0 match setting
TIMER0_MAT1A	0x0020_1C38	0x0000_0000	Timer/Counter 0 match setting
TIMER0_MAT1B	0x0020_1C3C	0x0000_0000	Timer/Counter 0 match setting
TIMER0_IF_OF	0x0020_1C40	0x0000_0000	Timer/Counter 0 interrupt & status flag
TIMER0_INT_EN	0x0020_1C44	0x0000_0000	Timer/Counter 0 interrupt enable setting
TIMER0_DMA_FLAG	0x0020_1C48	0x0000_0000	Timer/Counter 0 DMA status flag
TIMER0_DMA_EN	0x0020_1C4C	0x0000_0000	Timer/Counter 0 DMA enable setting
Timer/Counter Register 1(Timer1) 0x0020_2000~0x0020_23FF			
TIMER1_CTL	0x0020_2000	0x0000_0000	Timer/Counter 1 enable & mode setting
TIMER1_COUNT	0x0020_2004	0x0000_0000	Timer/Counter 1 counter
TIMER1_PSCL	0x0020_2008	0x0000_0000	Timer/Counter 1 prescaler setting
TIMER1_PCNT	0x0020_200C	0x0000_0000	Timer/Counter 1 prescaler value
TIMER1_CCTL	0x0020_2010	0x0000_0000	Counter 1 catch setting
TIMER1_CICTL	0x0020_2014	0x0000_0000	Counter 1 input setting
TIMER1_MCTL	0x0020_2018	0x0000_0000	Timer/Counter 1 match control
TIMER1_MOCTL	0x0020_201C	0x0000_0000	Timer/Counter 1 match output control
TIMER1_MAT0A	0x0020_2030	0x0000_0000	Timer/Counter 1 match setting
TIMER1_MAT0B	0x0020_2034	0x0000_0000	Timer/Counter 1 match setting
TIMER1_MAT1A	0x0020_2038	0x0000_0000	Timer/Counter 1 match setting
TIMER1_MAT1B	0x0020_203C	0x0000_0000	Timer/Counter 1 match setting
TIMER1_IF_OF	0x0020_2040	0x0000_0000	Timer/Counter 1 interrupt & status flag
TIMER1_INT_EN	0x0020_2044	0x0000_0000	Timer/Counter 1 interrupt enable setting
TIMER1_DMA_FLAG	0x0020_2048	0x0000_0000	Timer/Counter 1 DMA status flag
TIMER1_DMA_EN	0x0020_204C	0x0000_0000	Timer/Counter 1 DMA enable setting
Timer/Counter Register 2(Timer2) 0x0020_2400~0x0020_27FF			
TIMER2_CTL	0x0020_2400	0x0000_0000	Timer/Counter 2 enable & mode setting
TIMER2_COUNT	0x0020_2404	0x0000_0000	Timer/Counter 2 counter value
TIMER2_PSCL	0x0020_2408	0x0000_0000	Timer/Counter 2 prescaler setting
TIMER2_PCNT	0x0020_240C	0x0000_0000	Timer/Counter 2 prescaler value

Register Name	Address	Reset Default (Hex)	Description
TIMER2_CCTL	0x0020_2410	0x0000_0000	Counter 2 catch setting
TIMER2_CICTL	0x0020_2414	0x0000_0000	Counter 2 input setting
TIMER2_MCTL	0x0020_2418	0x0000_0000	Timer/Counter 2 match control
TIMER2_MOCTL	0x0020_241C	0x0000_0000	Timer/Counter 2 match output control
TIMER2_MAT0A	0x0020_2430	0x0000_0000	Timer/Counter 2 match setting
TIMER2_MAT0B	0x0020_2434	0x0000_0000	Timer/Counter 2 match setting
TIMER2_MAT1A	0x0020_2438	0x0000_0000	Timer/Counter 2 match setting
TIMER2_MAT1B	0x0020_243C	0x0000_0000	Timer/Counter 2 match setting
TIMER2_IF_OF	0x0020_2440	0x0000_0000	Timer/Counter 2 interrupt & status flag
TIMER2_INT_EN	0x0020_2444	0x0000_0000	Timer/Counter 2 interrupt enable setting
TIMER2_DMA_FLAG	0x0020_2448	0x0000_0000	Timer/Counter 2 DMA status flag
TIMER2_DMA_EN	0x0020_244C	0x0000_0000	Timer/Counter 2 DMA enable setting
Timer/Counter Register 3(Timer3) 0x0020_2800~0x0020_2BFF			
TIMER3_CTL	0x0020_2800	0x0000_0000	Timer/Counter 3 enable & mode setting
TIMER3_COUNT	0x0020_2804	0x0000_0000	Timer/Counter counter value
TIMER3_PSCL	0x0020_2808	0x0000_0000	Timer/Counter 3 prescaler setting
TIMER3_PCNT	0x0020_280C	0x0000_0000	Timer/Counter 3 prescaler value
TIMER3_CCTL	0x0020_2810	0x0000_0000	Counter 3 catch setting
TIMER3_CICTL	0x0020_2814	0x0000_0000	Counter 3 input setting
TIMER3_MCTL	0x0020_2818	0x0000_0000	Timer/Counter 3 match control
TIMER3_MOCTL	0x0020_281C	0x0000_0000	Timer/Counter 3 match output control
TIMER3_MAT0A	0x0020_2830	0x0000_0000	Timer/Counter 3 match setting
TIMER3_MAT0B	0x0020_2834	0x0000_0000	Timer/Counter 3 match setting
TIMER3_MAT1A	0x0020_2438	0x0000_0000	Timer/Counter 3 match setting
TIMER3_MAT1B	0x0020_283C	0x0000_0000	Timer/Counter 3 match setting
TIMER3_IF_OF	0x0020_2840	0x0000_0000	Timer/Counter 3 interrupt & status flag
TIMER3_INT_EN	0x0020_2844	0x0000_0000	Timer/Counter 3 interrupt enable setting
TIMER3_DMA_FLAG	0x0020_2848	0x0000_0000	Timer/Counter 3 DMA status flag
TIMER3_DMA_EN	0x0020_284C	0x0000_0000	Timer/Counter 3 DMA enable setting
Timer/Counter Register 4(Timer4) 0x0020_2C00~0x0020_2FFF			
TIMER4_CTL	0x0020_2C00	0x0000_0000	Timer/Counter 4 enable & mode setting
TIMER4_COUNT	0x0020_2C04	0x0000_0000	Timer/Counter 4 counter value
TIMER4_PSCL	0x0020_2C08	0x0000_0000	Timer/Counter 4 prescaler setting
TIMER4_PCNT	0x0020_2C0C	0x0000_0000	Timer/Counter 4 prescaler value
TIMER4_CCTL	0x0020_2C10	0x0000_0000	Counter 4 capture setting
TIMER4_CICTL	0x0020_2C14	0x0000_0000	Counter 4 input setting
TIMER4_MCTL	0x0020_2C18	0x0000_0000	Timer/Counter 4 match control
TIMER4_MOCTL	0x0020_2C1C	0x0000_0000	Timer/Counter 4 match output control
TIMER4_MAT0A	0x0020_2C30	0x0000_0000	Timer/Counter 4 match setting
TIMER4_MAT0B	0x0020_2C34	0x0000_0000	Timer/Counter 4 match setting
TIMER4_MAT1A	0x0020_2C38	0x0000_0000	Timer/Counter 4 match setting
TIMER4_MAT1B	0x0020_2C3C	0x0000_0000	Timer/Counter 4 match setting

Register Name	Address	Reset Default (Hex)	Description
TIMER4_IF_OF	0x0020_2C40	0x0000_0000	Timer/Counter 4 interrupt & status flag
TIMER4_INT_EN	0x0020_2C44	0x0000_0000	Timer/Counter 4 interrupt enable setting
TIMER4_DMA_FLAG	0x0020_2C48	0x0000_0000	Timer/Counter 4 DMA status flag
TIMER4_DMA_EN	0x0020_2C4C	0x0000_0000	Timer/Counter 4 DMA enable setting
Timer/Counter Register 5(Timer5) 0x0020_3000~0x0020_33FF			
TIMER5_CTL	0x0020_3000	0x0000_0000	Timer/Counter 5 enable & mode setting
TIMER5_COUNT	0x0020_3004	0x0000_0000	Timer/Counter 5 counter value
TIMER5_PSCL	0x0020_3008	0x0000_0000	Timer/Counter 5 prescaler setting
TIMER5_PCNT	0x0020_300C	0x0000_0000	Timer/Counter 5 prescaler value
TIMER5_CCTL	0x0020_3010	0x0000_0000	Counter 5 catch setting
TIMER5_CICTL	0x0020_3014	0x0000_0000	Counter 5 input setting
TIMER5_MCTL	0x0020_3018	0x0000_0000	Timer/Counter 5 match control
TIMER5_MOCTL	0x0020_301C	0x0000_0000	Timer/Counter 5 match output control
TIMER5_MAT0A	0x0020_3030	0x0000_0000	Timer/Counter 5 match setting
TIMER5_MAT0B	0x0020_3034	0x0000_0000	Timer/Counter 5 match setting
TIMER5_MAT1A	0x0020_3038	0x0000_0000	Timer/Counter 5 match setting
TIMER5_MAT1B	0x0020_303C	0x0000_0000	Timer/Counter 5 match setting
TIMER5_IF_OF	0x0020_3040	0x0000_0000	Timer/Counter 5 interrupt & status flag
TIMER5_INT_EN	0x0020_3044	0x0000_0000	Timer/Counter 5 interrupt enable setting
TIMER5_DMA_FLAG	0x0020_3048	0x0000_0000	Timer/Counter 5 DMA status flag
TIMER5_DMA_EN	0x0020_304C	0x0000_0000	Timer/Counter 5 DMA enable setting

Timer/Counter Control Register
TIMER0_CTL (Address: 0x0020_1C00)
TIMER1_CTL (Address: 0x0020_2000)
TIMER2_CTL (Address: 0x0020_2400)
TIMER3_CTL (Address: 0x0020_2800)
TIMER4_CTL (Address: 0x0020_2C00)
TIMER5_CTL (Address: 0x0020_3000) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	-	-	-	-	-	-	-
Name	TCTL_EN	Reserved						
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	TCTL_DE	TCTL_IOSW	TCTL_SEL[1:0]		TCTL_MODE[1:0]		TCTL_RST	TCTL_ST

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15	TCTL_EN	Timer/Counter enable setting 1: Timer/Counter enable 0: Timer/Counter disable (default)
14-8	Reserved	-
7	TCTL_DE	Timer/Counter debug enable setting 1: Timer/Counter operates normally during debug mode 0: Timer/Counter holds during debug mode (default)
6	TCTL_IOSW	I/O swap function setting 1: swap CAPIx/MATOx I/O definition and direction 0: no operation (default)
5-4	TCTL_SEL[1:0]	Counter input select 00: CAPI0 (default) 01: CAPI1 10: MATI0 (Last TIMER module's MATO output signal) 11: MATI1 (Last TIMER module's MATO output signal)
3-2	TCTL_MODE[1:0]	Timer/Counter mode setting 00: Timer (default) 01: rising edge counter 10: falling edge counter 11: both edges counter
1	TCTL_RST	Timer/Counter reset setting 1: setting counter reset
0	TCTL_ST	Timer/Counter start/stop setting 1: Timer/Counter starts 0: Timer/Counter stopped (default)

-: unimplemented.

Timer/Counter Count Register
TIMER0_COUNT (Address: 0x0020_1C04)
TIMER1_COUNT (Address: 0x0020_2004)
TIMER2_COUNT (Address: 0x0020_2404)
TIMER3_COUNT (Address: 0x0020_2804)
TIMER4_COUNT (Address: 0x0020_2C04)
TIMER5_COUNT (Address: 0x0020_3004) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	TCNT[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	TCNT [7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	TCNT [15:0]	timer counter, incremented every (PSCL + 1) of trigger source

-: unimplemented.

Timer/Counter Prescaler Register
TIMER0_PSCL (Address: 0x0020_1C08)
TIMER1_PSCL (Address: 0x0020_2008)
TIMER2_PSCL (Address: 0x0020_2408)
TIMER3_PSCL (Address: 0x0020_2808)
TIMER4_PSCL (Address: 0x0020_2C08)
TIMER5_PSCL (Address: 0x0020_3008) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PSCL[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PSCL [7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	PSCL [15:0]	Timer/Counter 0 Prescaler setting

-: unimplemented.

Timer/Counter Prescaler Counter Register
TIMER0_PCNT (Address: 0x0020_1C0C)
TIMER1_PCNT (Address: 0x0020_200C)
TIMER2_PCNT (Address: 0x0020_240C)
TIMER3_PCNT (Address: 0x0020_280C)
TIMER4_PCNT (Address: 0x0020_2C0C)
TIMER5_PCNT (Address: 0x0020_300C) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PCNT[15:8]							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PCNT [7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	PCNT [15:0]	Timer/Counter prescaler value

-: unimplemented.

Timer/Counter Catch Mode Control Register
TIMER0_CCTL (Address: 0x0020_1C10)
TIMER1_CCTL (Address: 0x0020_2010)
TIMER2_CCTL (Address: 0x0020_2410)
TIMER3_CCTL (Address: 0x0020_2810)
TIMER4_CCTL (Address: 0x0020_2C10)
TIMER5_CCTL (Address: 0x0020_3010) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				CCTL_CAPDF[1:0]		CCTL_C1SW	CCTL_C0SW
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				CCTL_CAP1F	CCTL_CAP1R	CCTL_CAP0F	CCTL_CAP0R

Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11-10	CCTL_CAPDF[1:0]	Digital filter setting for CAPI0 & CAPI1 00: no operation (default) 01: 2 clock 10: 4 clock 11: 8 clock
9	CCTL_C1SW	Invert CAPI1 setting 1: Invert CAPI1 for cap1
8	CCTL_C0SW	Invert CAPI0 setting 1: Invert CAPI0 for CAP0
3	CCTL_CAP1F	CAP1 falling edge enable setting 1: Capture enable on CAP1 falling edge (stored in TIMER_MAT1B_CAP1F[15:0])
2	CCTL_CAP1R	CAP1 rising edge enable setting 1: Capture enable of CAP1 rising edge (stored in TIMER_MAT1A_CAP1R[15:0])

Bit Number	Bit Mnemonic	Description
1	CCTL_CAP0F	CAP0 falling edge enable setting 1: Capture enable of CAP0 falling edge (stored in TIMER_MAT0B_CAP0F[15:0])
0	CCTL_CAP0R	CAP0 rising edge enable setting 1: Capture enable of CAP0 rising edge (stored in TIMER_MAT0A_CAP0R[15:0]

-: unimplemented.

Timer/Counter Counter Mode Control Register
TIMER0_CICTL (Address: 0x0020_1C14)
TIMER1_CICTL (Address: 0x0020_2014)
TIMER2_CICTL (Address: 0x0020_2414)
TIMER3_CICTL (Address: 0x0020_2814)
TIMER4_CICTL (Address: 0x0020_2C14)
TIMER5_CICTL (Address: 0x0020_3014) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				CICTL_C1ACTX[1:0]		CICTL_C0ACTX[1:0]	
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	CICTL_M1ACT[1:0]		CICTL_M0ACT[1:0]		CICTL_C1ACT[1:0]		CICTL_C0ACT[1:0]	

Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11-10	CICTL_C1ACTX[1:0]	CAPI1 Extend operation on counter 00: no action (default) 01: hold counter on CAPI1 low level 10: reset counter on CPAI1 falling edge 11: reserved
9-8	CICTL_C0ACTX[1:0]	CAPI0 Extend operation on counter 00: no action (default) 01: hold counter on CAPI0 low level 10: reset counter on CPAI0 falling edge 11: reserved
7-6	CICTL_M1ACT[1:0]	MATI1 operation on counter 00: no action (default) 01: hold counter on MATI1 high level 10: reset counter on MATI1 rising edge 11: trig counter (enable/disable switching) on MATI1 rising edge (Hardware will set TCTL_ST automatically)

Bit Number	Bit Mnemonic	Description
5-4	CICTL_M0ACT[1:0]	MATI0 operation on counter 00: no action (default) 01: hold counter on MATI0 high level 10: reset counter on MATI0 rising edge 11: trig counter (enable/disable switching) on MATI0 rising edge (Hardware will set TCTL_ST automatically)
3-2	CICTL_C1ACT[1:0]	CAPI1 operation on counter 00: no action (default) 01: hold counter on CAPI1 high level 10: reset counter on CPAI1 rising edge 11: trig counter (enable/disable switching) on CPAI1 rising edge (Hardware will set TCTL_ST automatically)
1-0	CICTL_C0ACT[1:0]	CAPI0 operation on counter 00: no action (default) 01: hold counter on CAPI0 high level 10: reset counter on CPAI0 rising edge 11: trig counter (enable/disable switching) on CPAI0 rising edge (Hardware will set TCTL_ST automatically)

-: unimplemented.

Timer/Counter MATCH Control Register
TIMER0_MCTL (Address: 0x0020_1C18)
TIMER1_MCTL (Address: 0x0020_2018)
TIMER2_MCTL (Address: 0x0020_2418)
TIMER3_MCTL (Address: 0x0020_2818)
TIMER4_MCTL (Address: 0x0020_2C18)
TIMER5_MCTL (Address: 0x0020_3018) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MCTL_M1MK[1:0]		MCTL_M0MK[1:0]		MCTL_MAT1	MCTL_MAT0	MCTL_M1SW	MCTL_M0SW
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MCTL_MAT1B[1:0]		MCTL_MAT1A[1:0]		MCTL_MAT0B[1:0]		MCTL_MAT0A[1:0]	

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-14	MCTL_M1MK[1:0]	MATM1 output mask selection 00: same as MAT1 (default) 01: reserved 10: clear MATM1 if CAP0 = 1 11: clear MATM1 if CAP1 = 1

Bit Number	Bit Mnemonic	Description
13-12	MCTL_M0MK[1:0]	MATM0 output mask selection 00: same as MAT0 (default) 01: reserved 10: clear MATM0 if CAP0 = 1 11: clear MATM0 if CAP1 = 1
11	MCTL_MAT1	MAT1 value (The control signal upon MATM1)
10	MCTL_MAT0	MAT0 value (The control signal upon MATM0)
9	MCTL_M1SW	MATM1 invert output setting 1: invert MATM1 for MATO1
8	MCTL_M0SW	MATM0 invert output setting 1: invert MATM0 for MATO0
7-6	MCTL_MAT1B[1:0]	MATCH control for MAT1B, when the Timer/Counter value equals to TIMERx_MAT1B[15:0]: 00: no operation (default) 01: clear the corresponding external MATO1 bit to 0 10: set the corresponding external MATO1 bit to 1 11: toggle the corresponding external MATO1 bit (0 ->1; 1 -> 0)
5-4	MCTL_MAT1A[1:0]	MATCH control for MAT1A, when the Timer/Counter value equals to IMERx_MAT1A[15:0]: 00: no operation (default) 01: clear the corresponding external MATO1 bit to 0 10: set the corresponding external MATO1 bit to 1 11: toggle the corresponding external MATO1 bit (0 -> 1; 1 -> 0)
3-2	MCTL_MAT0B[1:0]	MATCH control for MAT0B, when the Timer/Counter value equals to TIMERx_MAT0B[15:0]: 00: no operation (default) 01: clear the corresponding external MATO0 bit to 0 10: set the corresponding external MATO0 bit to 1 11: toggle the corresponding external MATO0 bit (0 ->1; 1 -> 0)
1-0	MCTL_MAT0A[1:0]	MATCH control for MAT0A, when the Timer/Counter value equals to TIMERx_MAT0A[15:0]: 00: no operation (default) 01: clear the corresponding external MATO0 bit to 0 10: set the corresponding external MATO0 bit to 1 11: toggle the corresponding external MATO0 bit (0 -> 1; 1 -> 0)

-: unimplemented.

Timer/Counter MATCH Output Control Register
TIMER0_MOCTL (Address: 0x0020_1C1C)
TIMER1_MOCTL (Address: 0x0020_201C)
TIMER2_MOCTL (Address: 0x0020_241C)
TIMER3_MOCTL (Address: 0x0020_281C)
TIMER4_MOCTL (Address: 0x0020_2C1C)
TIMER5_MOCTL (Address: 0x0020_301C) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MOCTL_M1BS	MOCTL_M1BR	MOCTL_M1AS	MOCTL_M1AR	MOCTL_M0BS	MOCTL_M0BR	MOCTL_M0AS	MOCTL_M0AR

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	MOCTL_M1BS	1: When Timer/Counter value equals to TIMERx_MAT1B[15:0], Timer/Counter stop counter (clear TCTL_ST)
6	MOCTL_M1BR	1: When Timer/Counter value equals to TIMERx_MAT1B[15:0], Timer/Counter value (TCNT[15:0]) will be cleared
5	MOCTL_M1AS	1: When Timer/Counter value equals to TIMERx_MAT1A[15:0], Timer/Counter stop counter (clear TCTL_ST)
4	MOCTL_M1AR	1: When Timer/Counter value equals to TIMERx_MAT1A[15:0], Timer/Counter value (TCNT[15:0]) will be cleared
3	MOCTL_M0BS	1: When Timer/Counter value equals to TIMERx_MAT0B[15:0], Timer/Counter stop counter (clear TCTL_ST)
2	MOCTL_M0BR	1: When Timer/Counter value equals to TIMERx_MAT0B[15:0], Timer/Counter value (TCNT[15:0]) will be cleared
1	MOCTL_M0AS	1: When Timer/Counter value equals to TIMERx_MAT0A[15:0], Timer/Counter stop counter (clear TCTL_ST)
0	MOCTL_M0AR	1: When Timer/Counter value equals to TIMERx_MAT0A[15:0], Timer/Counter value (TCNT[15:0]) will be cleared

-: unimplemented.

Timer/Counter MATCH/ CAP Register 0A
TIMER0_MAT0A (Address: 0x0020_1C30)
TIMER1_MAT0A (Address: 0x0020_2030)
TIMER2_MAT0A (Address: 0x0020_2430)
TIMER3_MAT0A (Address: 0x0020_2830)
TIMER4_MAT0A (Address: 0x0020_2C30)
TIMER5_MAT0A (Address: 0x0020_3030) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MAT0A(CAP0R)[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MAT0A(CAP0R) [7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	MAT0A(CAP0R) [15:0]	match MAT0A register for output match mode capture CAP0R register for input capture mode

-: unimplemented.

Timer/Counter MATCH/ CAP Register 0B
TIMER0_MAT0B (Address: 0x0020_1C34)
TIMER1_MAT0B (Address: 0x0020_2034)
TIMER2_MAT0B (Address: 0x0020_2434)
TIMER3_MAT0B (Address: 0x0020_2834)
TIMER4_MAT0B (Address: 0x0020_2C34)
TIMER5_MAT0B (Address: 0x0020_3034) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MAT0B(CAP0F)[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MAT0B(CAP0F)[7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	MAT0B(CAP0F) [15:0]	match MAT0B register for output MATCH mode capture CAP0F register for input CAPTURE mode

-: unimplemented.

Timer/Counter MATCH/ CAP Register 1A
TIMER0_MAT1A (Address: 0x0020_1C38)
TIMER1_MAT1A (Address: 0x0020_2038)
TIMER2_MAT1A (Address: 0x0020_2438)
TIMER3_MAT1A (Address: 0x0020_2838)
TIMER4_MAT1A (Address: 0x0020_2C38)
TIMER5_MAT1A (Address: 0x0020_3038) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MAT1A(CAP1R)[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MAT1A(CAP1R) [7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	MAT1A(CAP1R) [15:0]	match MAT1A register for output MATCH mode capture CAP1R register for input CAPTURE mode

-: unimplemented.

Timer/Counter MATCH/ CAP Register 1B
TIMER0_MAT1B (Address: 0x0020_1C3C)
TIMER1_MAT1B (Address: 0x0020_203C)
TIMER2_MAT1B (Address: 0x0020_243C)
TIMER3_MAT1B (Address: 0x0020_283C)
TIMER4_MAT1B (Address: 0x0020_2C3C)
TIMER5_MAT1B (Address: 0x0020_303C) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MAT1B(CAP1F)[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MAT1B(CAP1F) [7:0]							

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-0	MAT1B(CAP1F) [15:0]	match MAT1B register for output MATCH mode capture CAP1F register for input CAPTURE mode

-: unimplemented.

Timer/Counter Status/Interrupt Flag Register
TIMER0_IF_OF (Address: 0x0020_1C40)
TIMER1_IF_OF (Address: 0x0020_2040)
TIMER2_IF_OF (Address: 0x0020_2440)
TIMER3_IF_OF (Address: 0x0020_2840)
TIMER4_IF_OF (Address: 0x0020_2C40)
TIMER5_IF_OF (Address: 0x0020_3040) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	-	-	-	R/W	R/W	R/W	R/W
Name	OF_TCNT	Reserved			OF_CAP1F	OF_CAP1R	OF_CAP0F	OF_CAP0R
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IF_MAT1B	IF_MAT1A	IF_MAT0B	IF_MAT0A	IF_CAP1F	IF_CAP1R	IF_CAP0F	IF_CAP0R

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15	OF_TCNT	Timer/Counter overflow flag 1: TCNT[15:0] overflow occurs (from FFFFH to 0000H)
14-12	Reserved	-
11	OF_CAP1F	Timer/Counter capture overflow flag (the second capture interrupt occurs when the first capture interrupt hasn't been handled.) 1: CAP1F overflow occurs (write 1 to clear)
10	OF_CAP1R	Timer/Counter capture overflow flag (the second capture interrupt occurs when the first capture interrupt hasn't been handled.) 1: CAP1R overflow occurs (write 1 to clear)
9	OF_CAP0F	Timer/Counter capture overflow flag (the second capture interrupt occurs when the first capture interrupt hasn't been handled.) 1: CAP0F overflow occurs (write 1 to clear)
8	OF_CAP0R	Timer/Counter capture overflow flag (the second capture interrupt occurs when the first capture interrupt hasn't been handled.) 1: CAP0R overflow occurs (write 1 to clear)
7	IF_MAT1B	MAT1B interrupt event flag 1: MAT1B interrupt event occurred (write 1 to clear)
6	IF_MAT1A	MAT1A interrupt event flag 1: MAT1A interrupt event occurred (write 1 to clear)
5	IF_MAT0B	MAT0B interrupt event flag 1: MAT0B Interrupt Event occurred (write 1 to clear)
4	IF_MAT0A	MAT0A interrupt event flag 1: MAT0A interrupt event occurred (write 1 to clear)
3	IF_CAP1F	CAP1F interrupt event flag 1: CAP1F interrupt event occurred (write 1 to clear)
2	IF_CAP1R	CAP1R interrupt event flag 1: CAP1R interrupt event occurred (write 1 to clear)
1	IF_CAP0F	CAP0F interrupt event flag 1: CAP0F interrupt event occurred (write 1 to clear)
0	IF_CAP0R	CAP0R interrupt event flag 1: CAP0R interrupt event occurred (write 1 to clear)

-: unimplemented.

Timer/Counter Interrupt Enable Setting Register
TIMER0_INT_EN (Address: 0x0020_1C44)
TIMER1_INT_EN (Address: 0x0020_2044)
TIMER2_INT_EN (Address: 0x0020_2444)
TIMER3_INT_EN (Address: 0x0020_2844)
TIMER4_INT_EN (Address: 0x0020_2C44)
TIMER5_INT_EN (Address: 0x0020_3044) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IE_MAT1B	IE_MAT1A	IE_MAT0B	IE_MAT0A	IE_CAP1F	IE_CAP1R	IE_CAP0F	IE_CAP0R

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	IE_MAT1B	MAT1B interrupt enable setting 1: MAT1B interrupt enable 0: MAT1B interrupt disable (default)
6	IE_MAT1A	MAT1A interrupt enable setting 1: MAT1A interrupt enable 0: MAT1A interrupt disable (default)
5	IE_MAT0B	MAT0B interrupt enable setting 1: MAT0B interrupt enable 0: MAT0B interrupt disable (default)
4	IE_MAT0A	MAT0A interrupt enable setting 1: MAT0A interrupt enable 0: MAT0A interrupt disable (default)
3	IE_CAP1F	CAP1F interrupt enable setting 1: CAP1F interrupt enable 0: CAP1F interrupt disable (default)
2	IE_CAP1R	CAP1R interrupt enable setting 1: CAP1R interrupt enable 0: CAP1R interrupt disable (default)
1	IE_CAP0F	CAP0F interrupt enable setting 1: CAP0F interrupt enable 0: CAP0F interrupt disable (default)
0	IE_CAP0R	CAP0R interrupt enable setting 1: CAP0R interrupt enable 0: CAP0R interrupt disable (default)

-: unimplemented.

Timer/Counter DMA Event Flag Register
TIMER0_DMA_FLAG (Address: 0x0020_1C48)
TIMER1_DMA_FLAG (Address: 0x0020_2048)
TIMER2_DMA_FLAG (Address: 0x0020_2448)
TIMER3_DMA_FLAG (Address: 0x0020_2848)
TIMER4_DMA_FLAG (Address: 0x0020_2C48)
TIMER5_DMA_FLAG (Address: 0x0020_3048) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MAT1B_RF	MAT1A_RF	MAT0B_RF	MAT0A_RF	CAP1F_RF	CAP1R_RF	CAP0F_RF	CAP0R_RF

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	RF_MAT1B	MAT1B DMA event flag 1: DMA request flag for MAT1B (write 1 to clear)
6	RF_MAT1A	MAT1A DMA event flag 1: DMA request flag for MAT1A (write 1 to clear)
5	RF_MAT0B	MAT0B DMA event flag 1: DMA request flag for MAT0B (write 1 to clear)
4	RF_MAT0A	MAT0A DMA event flag 1: DMA request flag for MAT0A (write 1 to clear)
3	RF_CAP1F	CAP1F DMA event flag 1: DMA request flag for CAP1F (write 1 to clear)
2	RF_CAP1R	CAP1R DMA event flag 1: DMA request flag for CAP1R (write 1 to clear)
1	RF_CAP0F	CAP0F DMA event flag 1: DMA request flag for CAP0F (write 1 to clear)
0	RF_CAP0R	CAP0R DMA event flag 1: DMA request flag for CAP0R (write 1 to clear)

-: unimplemented.

Timer/Counter DMA Enable Setting Register
TIMER0_DMA_EN (Address: 0x0020_1C4C)
TIMER1_DMA_EN (Address: 0x0020_204C)
TIMER2_DMA_EN (Address: 0x0020_244C)
TIMER3_DMA_EN (Address: 0x0020_284C)
TIMER4_DMA_EN (Address: 0x0020_2C4C)
TIMER5_DMA_EN (Address: 0x0020_304C) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MAT1B_RE	MAT1A_RE	MAT0B_RE	MAT0A_RE	CAP1F_RE	CAP1R_RE	CAP0F_RE	CAP0R_RE

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	RE_MAT1B	MAT1B DMA enable setting 1: DMA request enable for MAT1B 0: MAT1B DMA is disabled (default)

Bit Number	Bit Mnemonic	Description
6	RE_MAT1A	MAT1A DMA enable setting 1: DMA request enable for MAT1A 0: MAT1A DMA is disabled (default)
5	RE_MAT0B	MAT0B DMA enable setting 1: DMA request enable for MAT0B 0: MAT0B DMA is disabled (default)
4	RE_MAT0A	MAT0A DMA enable setting 1: DMA request enable for MAT0A 0: MAT0A DMA is disabled (default)
3	RE_CAP1F	CAP1F DMA enable setting 1: DMA request enable for CAP1F 0: CAP1F DMA is disabled (default)
2	RE_CAP1R	CAP1R DMA enable setting 1: DMA request enable for CAP1R 0: CAP1R DMA is disabled (default)
1	RE_CAP0F	CAP0F DMA enable setting 1: DMA request enable for CAP0F 0: CAP0F DMA is disabled (default)
0	RE_CAP0R	CAP0R DMA enable setting 1: DMA request enable for CAP0R 0: CAP0R DMA is disabled (default)

-: unimplemented.

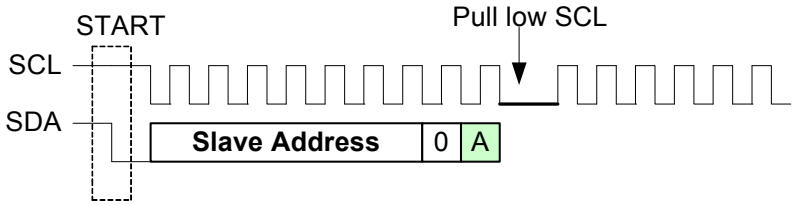
Note: All Interrupt Event Flag XXX_IF and all DMA Event Flag XXX_RF are cleared if TCTL_EN = 0.

6.12 I²C Serial Interface

6.12.1 Features

WT59F164 supports two I²C modules: I²C0 and I²C1

- I²C module use SCL (clock) and SDA (data) wires to connect with other I²C interfaces, the transmission is determined by the software programmed MI2C_CLK[1:0] in XFR, and is allowed to reach 400 Kbps (maximum).
- I²C module also provide Master/Slave mode, and it is set by register
- I²C SCL & SDA input pin with digital filter
- If the firmware processing time is slower than the time of I²C receiving 9 bits, then the firmware must set MI2C_WAIT enabling WT59F164 to pull SCL low after the 9th bit.

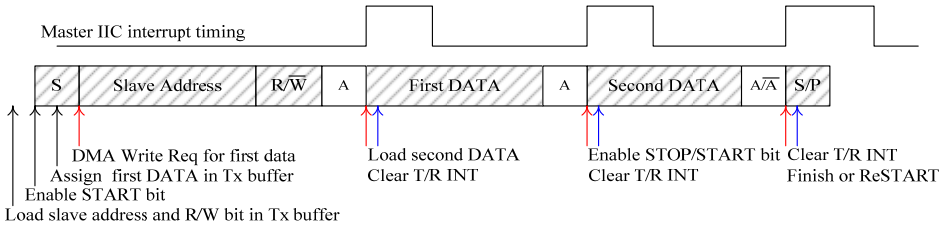


- When use DMA for I²C transmission, DMA proceeds transmitting or receiving data from RAM in master mode. In the meantime, the data in the RAM will only be treated as data transmission, does not contain the address.

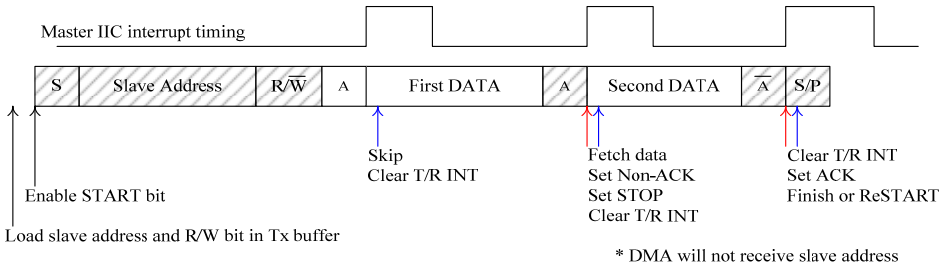
➢ I²C Command Timing Flow

I²C Command Timing Flow

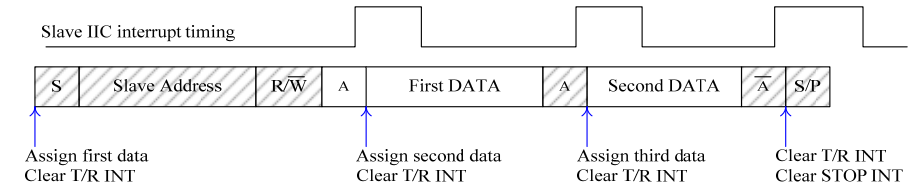
● Master-Transmitter mode



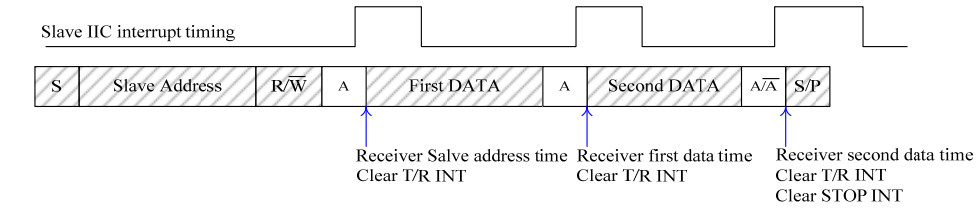
● Master-Receiver mode



● Slave-Transmitter mode



● Slave-Receiver mode



: From Slave to Master

: From Master to Slave

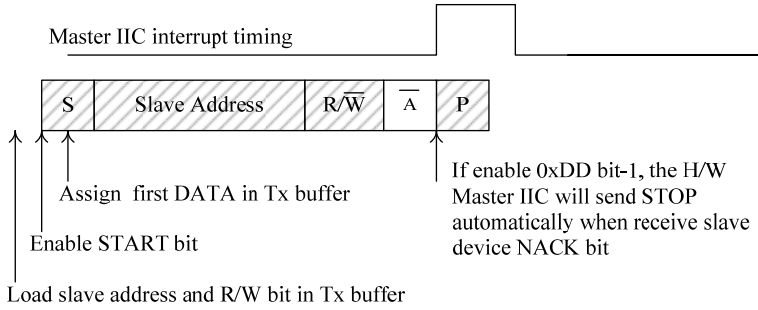
: Command Action during interrupt period

: DMA Request Time

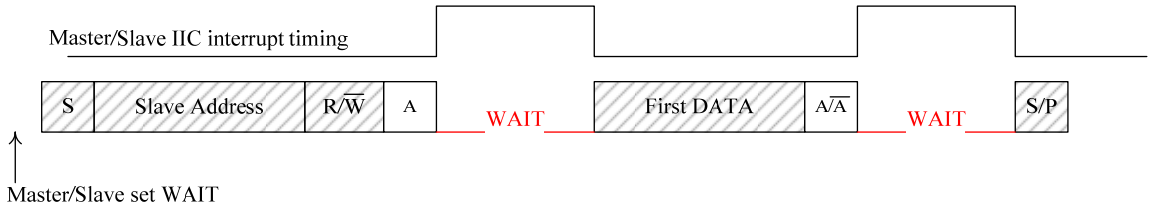
Command Limitation
Master Mode
1. Each command must-action in previous interrupt. **2. After set return Non-ACK bit, remember to recover it or it will return Non-ACK forever until set return ACK bit.** **3. START and STOP bit will not be latched, so we dose not recover it.**
Slave Mode
1. Each command must-action in previous interrupt (include WAIT command). **2. In Slave-Tx mode, the first byte will send initial Tx buffer data or you can load needed data as initial data before Slave I2C be selected.**

Master I²C Command Timing Flow 2

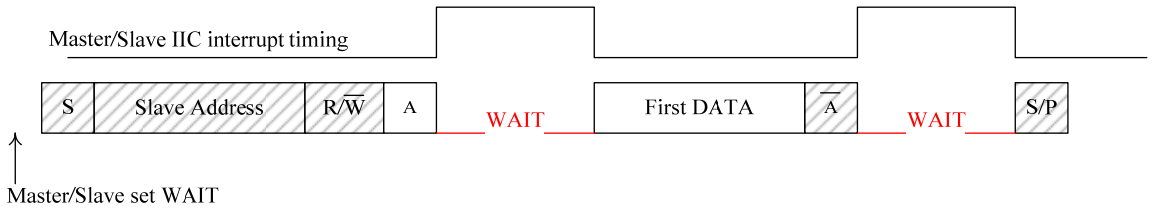
● Master I²C Auto-STOP



● Master Tx/Slave Rx Wait



● Master Rx/Slave Tx Wait



: From Slave to Master

: From Master to Slave

: Command Action during interrupt period

Command Limitation
Master Mode
1. Each command must-action in previous interrupt. **2. After set return Non-ACK bit, remember to recover it or it will return Non-ACK forever until set return ACK bit.** **3. START and STOP bit will not be latched, so we dose not recover it.**
Slave Mode
1. Each command must-action in previous interrupt (include WAIT command). **2. In Slave-Tx mode, the first byte will send initial Tx buffer data or you can load needed data as initial data before Slave I2C be selected.**

6.12.2 I²C Special Register

Register Name	Address	Reset Default (Hex)	Description
I²C Serial Interface Register 0 (I²C0)	**0x0020_5400~0x0020_57FF**		
IIC0_CTL	0x0020_5400	0x0000_0020	I²C0 setting
IIC0_STATUS	0x0020_5404		I²C0 status flag
IIC0_MI2CDSLV	0x0020_5408	0x0000_0000	I²C0 master transmit address
IIC0_TX_BUFFER	0x0020_540C	0x0000_00FF	I²C0 transmit data buffer
IIC0_RX_BUFFER	0x0020_5410		I²C0 receive data buffer
IIC0_SLAVE_ADDR	0x0020_5414	0x0000_0000	I²C0 slave address
IIC0_EXTEN_CTL	0x0020_5418	0x0000_0000	I²C0 extend setting
I²C Serial Interface Register 1 (I²C1)	**0x0020_5800~0x0020_5BFF**		
IIC1_CTL	0x0020_5800	0x0000_0020	I²C1 setting
IIC1_STATUS	0x0020_5804		I²C1 status flag
IIC1_MI2CDSLV	0x0020_5808	0x0000_0000	I²C1 master transmit address
IIC1_TX_BUFFER	0x0020_580C	0x0000_00FF	I²C1 transmit data buffer
IIC1_RX_BUFFER	0x0020_5810		I²C1 receive data buffer
IIC1_SLAVE_ADDR	0x0020_5814	0x0000_0000	I²C1 slave address
IIC1_EXTEN_CTL	0x0020_5818	0x0000_0000	I²C1 extend setting

I²C Control Register
IIC0_CTL (Address: 0x0020_5400)
IIC1_CTL (Address: 0x0020_5800) **Reset Value: 0x0000_0020**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	W	W	R/W	W	W
Name	MI2C_EN	MI2C_CLK[1:0]		MI2C_START	MI2C_STOP	MI2C_TXNAK	MI2C_CLR_RT	MI2C_CLR_STP

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	MI2C_EN	I²C enable setting 1: Enable I²C function enable 0: Disable I²C function disable (default)

Bit Number	Bit Mnemonic	Description
6-5	MI2C_CLK[1:0]	I^2C clock select setting 00: SCL Clock = 400 kHz 01: SCL Clock = 250 kHz (default) 10: SCL Clock = 125 kHz 11: SCL Clock = 62.5 kHz
4	MI2C_START	I^2C START bit setting 1: I^2C transmit START bit
3	MI2C_STOP	I^2C STOP bit setting 1: I^2C transmit STOP bit
2	MI2C_TXNAK	Master I^2C transmit ACK bit after next receive state 1: Transmit NACK 0: Transmit ACK (default)
1	MI2C_CLR_RT	Transmit & Receive interrupt clear setting 1: set 1 to clear transmit & receive interrupt (Master or Slave mode)
0	MI2C_CLR_STP	Slave mode STOP interrupt clear 1: set 1 to clear Slave mode STOP Interrupt

-: unimplemented.

I^2C Status Register
IIC0_STATUS (Address: 0x0020_5404)
IIC1_STATUS (Address: 0x0020_5804) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	MI2C_RDY	MI2C_INT_RT	MI2C_INT_STOP	MI2C_BB	MI2C_FIRST	MI2C_RW	MI2C_RXNAK	MI2C_DMAFAIL

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	MI2C_RDY	I^2C complete interrupt flag 1: IINT when I^2C receive/transmit 9 bits or Slave STOP phase.
6	MI2C_INT_RT	I^2C Receive/Transmit interrupt flag 1: INT when I^2C receive/transmit 9 bits
5	MI2C_INT_STOP	In I^2C Slave mode, STOP Interrupt Flag 1: INT when I2C slave mode STOP phase
4	MI2C_BB	I^2C Slave mode busy status 1: Slave mode bus is busy
3	MI2C_FIRST	Master/Slave mode FIRST phase 1: This is first byte from master I^2C with specific slave address

Bit Number	Bit Mnemonic	Description
2	MI2C_RW	I^2C Slave mode READ/WRITE phase（8^{th} bit of first byte） 1: Slave I²C as transmitter 0: Slave I²C as receiver
1	MI2C_RXNAK	ACK bit indicator when I^2C in slave transmit mode 1: Master mode return NACK 0: Master mode return ACK
0	MI2C_DMAFAIL	I^2C DMA fail state 1: I^2C DMA failed (DMA speed not enough), write 1 to I2C_CLR_Rt can clear this state

-: unimplemented.

I^2C Master Address Register
IIC0_MI2CDSLV (Address: 0x0020_5408)
IIC1_MI2CDSLV (Address: 0x0020_5808) **Reset Value:0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MI2C_DSLV[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	MI2C_DSLV	Master I^2C transmit slave address buffer

-: unimplemented.

I^2C Transmit Buffer Register
IIC0_TX_BUFFER (Address: 0x0020_540C)
IIC1_TX_BUFFER (Address: 0x0020_580C) **Reset Value:0x0000_00FF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	I2C_DTX[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	I2C_DTX[7:0]	I^2C Transmit Buffer Write data to this register will transmit data from I^2C transmit buffer

-: unimplemented.

I^2C Receive Buffer Register
IIC0_RX_BUFFER (Address: 0x0020_5410)
IIC1_RX_BUFFER (Address: 0x0020_5810) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	I2C0_DRX[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	I2C_DRX[7:0]	I^2C Receive Buffer Read data from this register will receive data from I^2C receive buffer

-: unimplemented.

I^2C Slave Address Register
IIC0_SLAVE_ADDR (Address: 0x0020_5414)
IIC1_SLAVE_ADDR (Address: 0x0020_5814) **Reset Value: :0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MI2C0_SADR[6:0]							I2C_SLVE

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-1	MI2C0_SADR[6:0]	I^2C slave address
0	MI2C_SLVE	I^2C Slave mode enable setting 1: enable I^2C slave mode 0: I^2C master mode (default)

-: unimplemented.

I^2C Extend Control Register
IIC0_EXTEN_CTL (Address: 0x0020_5418)
IIC1_EXTEN_CTL (Address: 0x0020_5818) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	R/W	R/W	R/W
Name	Reserved					MI2C_DMAEN	MI2C_AUTOSTP	MI2C_WAIT

Bit Number	Bit Mnemonic	Description
31-3	Reserved	-
2	MI2C_DMAEN	I^2C DMA enable setting 1: Enable I^2C DMA 0: Disable I^2C DMA (default)
1	MI2C_AUTOSTP	Master I^2C auto STOP setting 1: Enable master I^2C auto STOP when Transmit NACK bit
0	MI2C_WAIT	I^2C Wait enable setting 1: Enable SCL extend (In Slave mode, I^2C pull SCL low after 9^{th} bit to advise Master waiting for it; In Master mode, it will not send the CLOCK till the interrupt flag being cleared after data is transferred.)

-: unimplemented.

6.13 Serial Peripheral Interface (SPI)

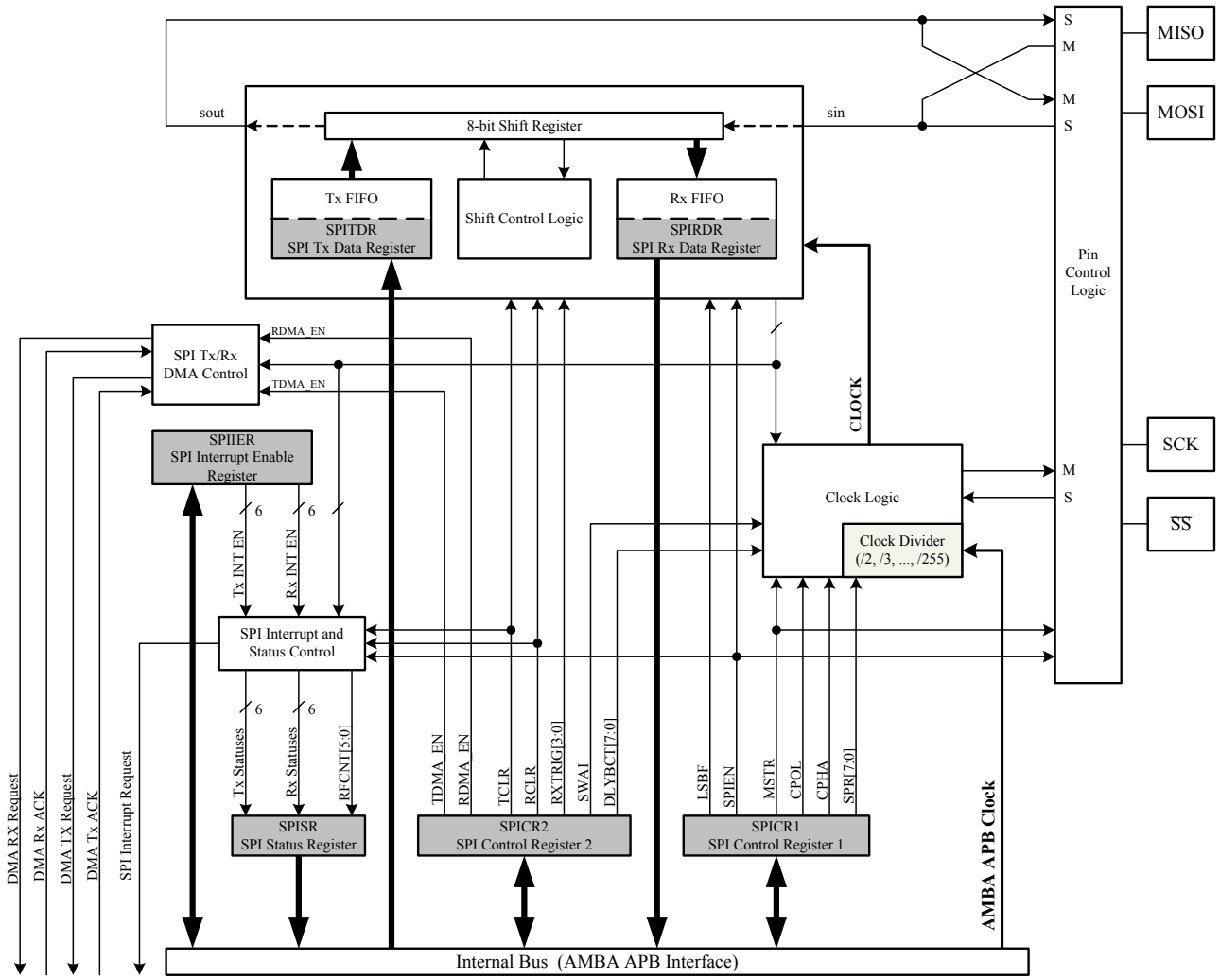
6.13.1 Features

WT59F164 supports two SPI. SPI is a synchronous serial interface, allows master to communicate with slave, supports full duplex data transmission, and also supports 4-wire communications.

- SPI supports both Master and Slave mode
- SCK can work at the speed of 1/2 APB clock
- Transmitted serial data can select LSB or MSB being transmitted first
- Support DMA transfer
- Support four SPI transmission modes
- Configurable Receiving Data Length Trigger: 1, 8, 16, 24, 28, 30, 31, and 32 Bytes Data Trigger are available
- Contain 32-byte Tx and 32-byte Rx FIFOs
- Each SPI communication uses four pins, as described below:
  - NSS: in Master mode as output; in Slave mode as input.

    In Master mode as enable slave I/O Port :
    - NSS = 1: Master disable Slave
    - NSS = 0: Master enable Slave
  - SCK: In Master mode clock output; in Slave mode clock input for data synchronization
  - MOSI: In Master mode data output; in Slave mode data input
  - MISO: In Master mode data output; in Slave mode data input

➢ SPI Block Diagram:



6.13.2 SPI Interrupt

Interrupt Event	Interrupt Flag	Interrupt Enable
Transmit FIFO Almost Empty flag	TFAE	IE_TFAE
Transmit FIFO Almost Full flag	TFAF	IE_TFAF
Transmit FIFO Buffer Overrun error	TFOV	IE_TFOV
Transmit FIFO Full flag	TFF	IE_TFF
Transmit FIFO Empty flag	TFE	IE_TFE
Transmit Empty flag	TXE	IE_TXE
Receive FIFO Almost Empty flag	RFAE	IE_RFAE
Receive FIFO Almost Full flag	RFAF	IE_RFAF
Receive FIFO Overrun error	RFOV	IE_RFOV
Receive FIFO Full flag	RFF	IE_RFF
Receive FIFO Empty flag	RFE	IE_RFE
Receive Data Ready flag	RXDR	IE_RXDR

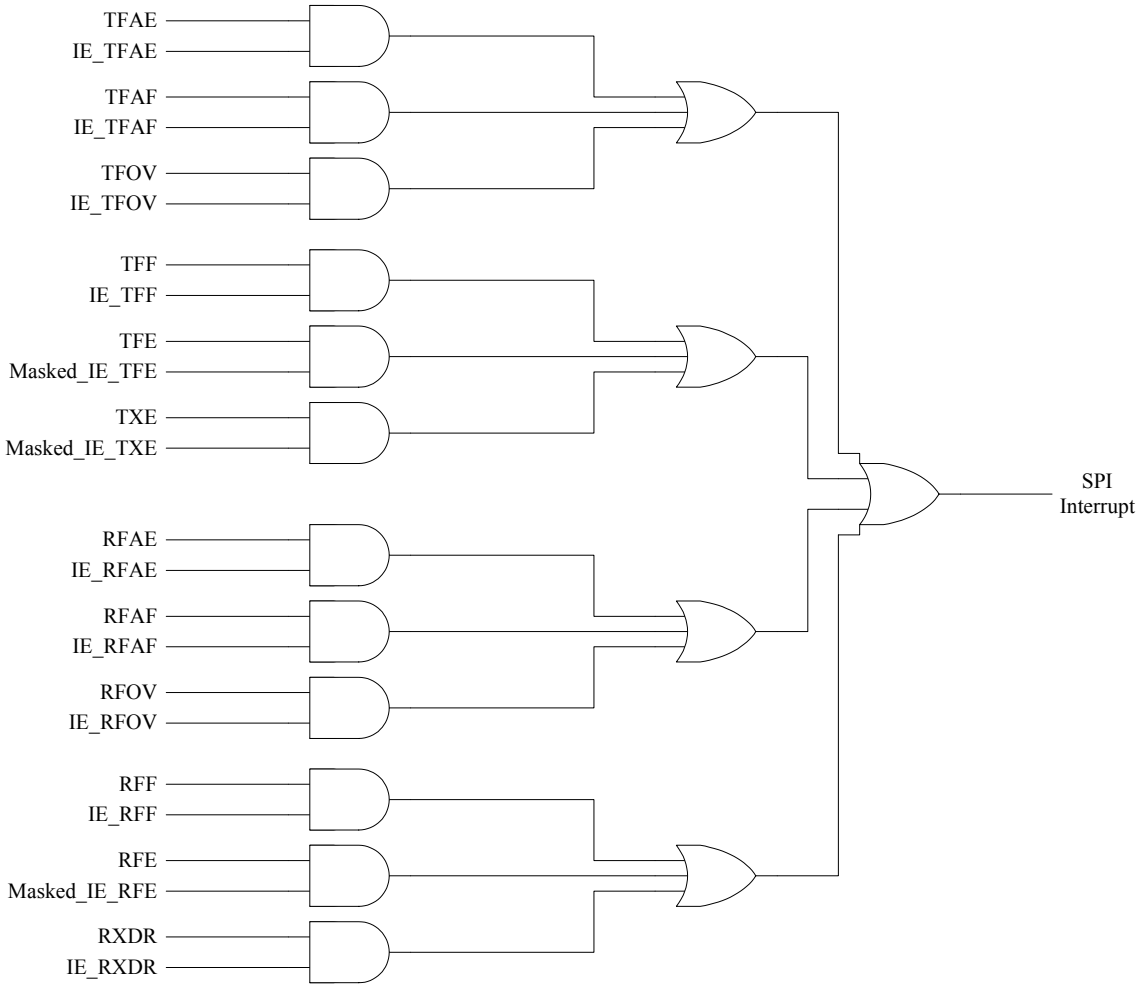


Fig. 2 SPI Interrupt Mapping Diagram

The SPI interrupt events are connected to the same interrupt vector (Fig.2). These events generate an interrupt if the corresponding Enable Control bits are set.

(1) During transmission: Tx Empty, Tx FIFO Empty, Tx FIFO Full, Tx FIFO Overrun, Tx FIFO Almost Full, or Tx FIFO Almost Empty Interrupt.

(2) While receiving: Rx Data Ready, Rx FIFO Empty, Rx FIFO Full, Rx FIFO Overrun, Rx FIFO Almost Full, or Rx FIFO Almost Empty interrupt.

(3) All the Tx/Rx empty event flags (TFE, TXE, and RFE) are 1 after reset. If the corresponding interrupt enable bits (IE_TFE, IE_TXE, and IE_RFE) are used directly, the SPI interrupt will be issued immediately before data transfer.

(4) Tx FIFO Empty Interrupt (TFE): if IE_TFE = 1 and all data in the Tx FIFO are completely transmitted, the TFE flag = 1 and the TFE interrupt is issued.

(5) Tx Empty Interrupt (TXE): If IE_TXE = 1, with all data in the Tx FIFO and the Tx shift register are completely transmitted, the TXE flag = 1 and the TXE interrupt is issued.

(6) Rx FIFO Empty Interrupt (RFE): If IE_TXE = 1, with all data in the Rx FIFO are read/moved by the MCU/DMA, the RFE flag = 1 and the RFE interrupt is issued.

6.13.3 SPI DMA Request Control

Tx DMA Request Control

spi_dma_tx_req	Condition
Request Issue	1. Tx FIFO is empty 2. Tx FIFO is not full
Request No issue	1. Tx FIFO is full 2. Tx DMA is disabled 3. DMA requests dma_tx_ack = 1

Rx DMA Request Control

Spi_dma_rx_req	Condition
Request Issue	Rx data count reaches trigger level (data ready)
Request No issue	1. Rx FIFO is empty 2. Rx DMA is disabled 3. DMA requests dma_tx_ack = 1

6.13.4 SPI Work mode

SPI supports four modes, as shown in Fig.3 and Fig.4.

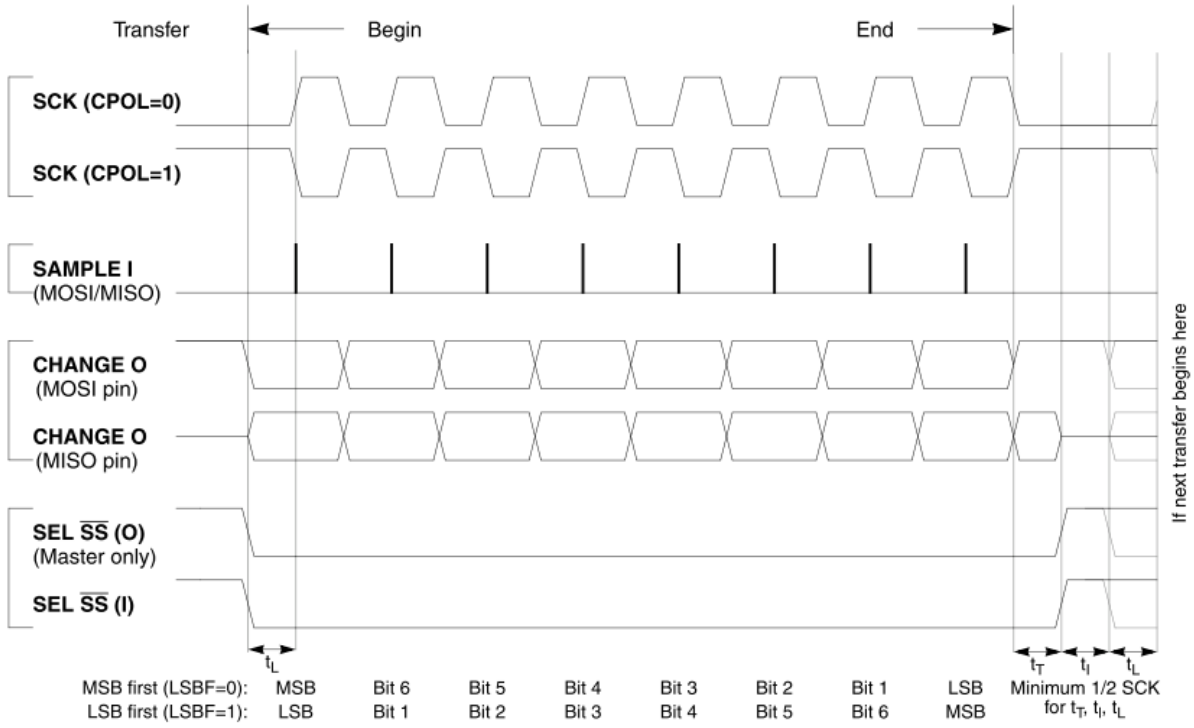


Fig. 3 SPI Clock type 0 (CPHA = 0, Mode 0/2)

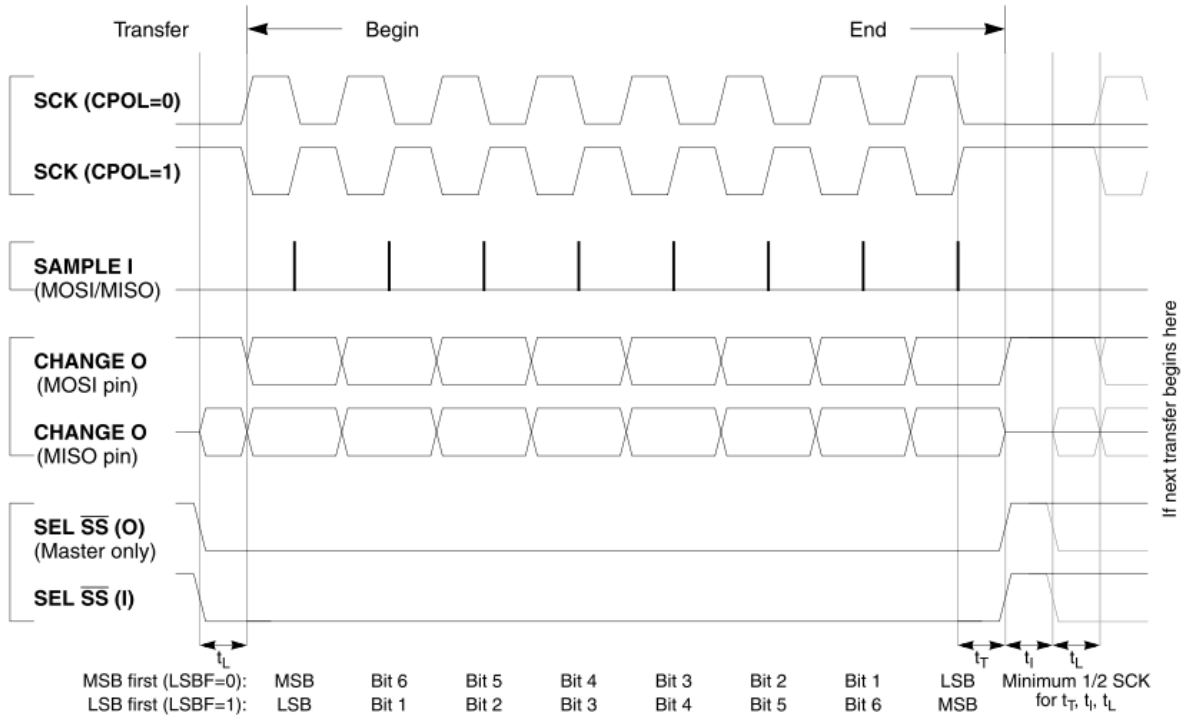


Fig. 4 SPI SPI Clock Type 1 (CPHA = 1, Mode 1/3)

In Master mode, the SS (NSS pin) is held to Low until all the data were completely transferred, as depicted in Fig. 5.

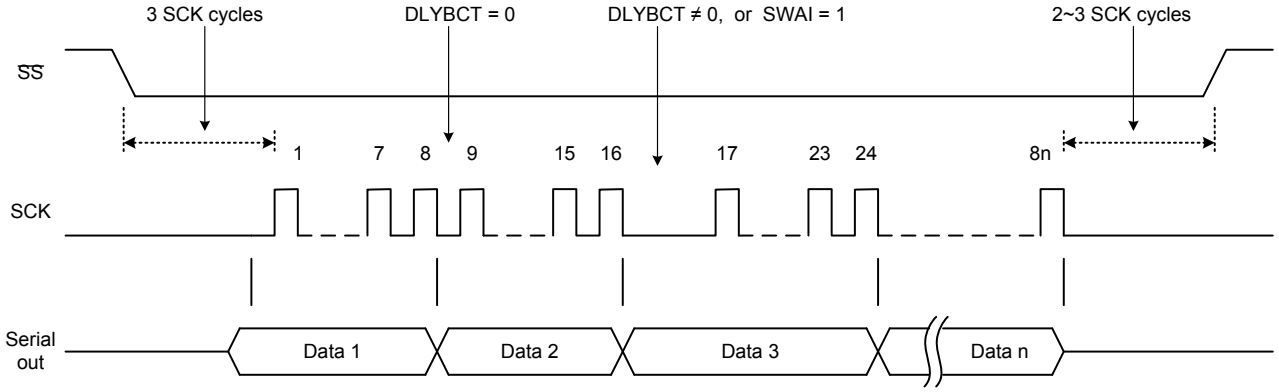
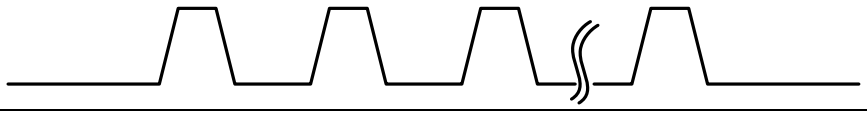


Fig. 5 The SS is held Low until all the data were completely transferred

In Master mode, the SPI Clock Duty Cycle of different modes as shown in Fig. 6.

CPOL & Duty Cycle	SCK Waveform Format
CPOL = 0 (Mode 0/1) **duty cycle: 33% ~ 50%**	SCK = 0 when idle 

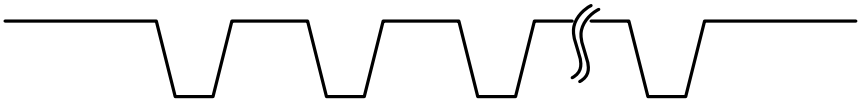
CPOL & Duty Cycle	SCK Waveform Format
CPOL = 1 (Mode 2/3) duty cycle: 50% ~ 67%	

Fig. 6 SPI Clock Duty Cycle of different modes

6.13.5 SPI Clock Structure and SCK Generator FSM

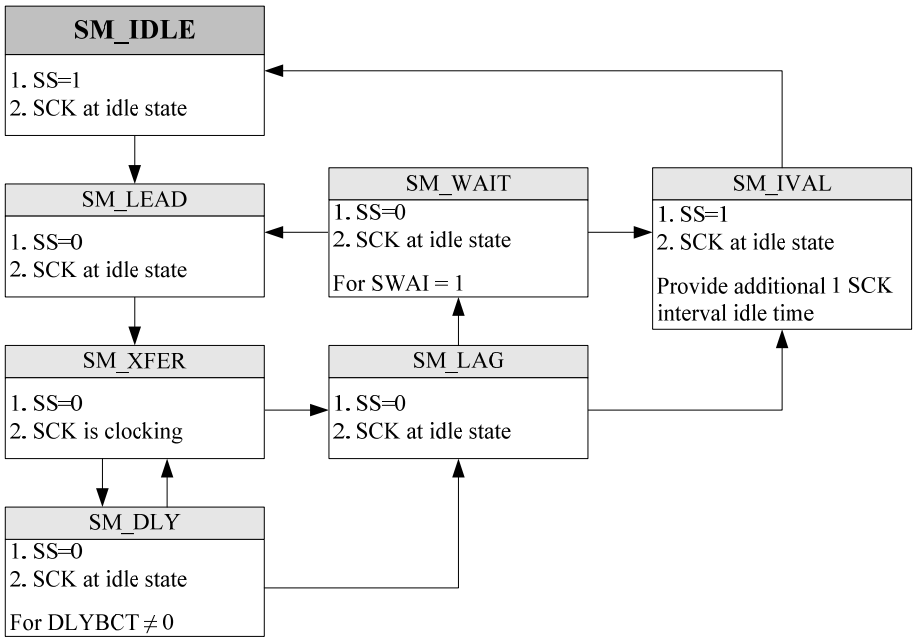


Fig. 7 SCK Generator Finite State Machine

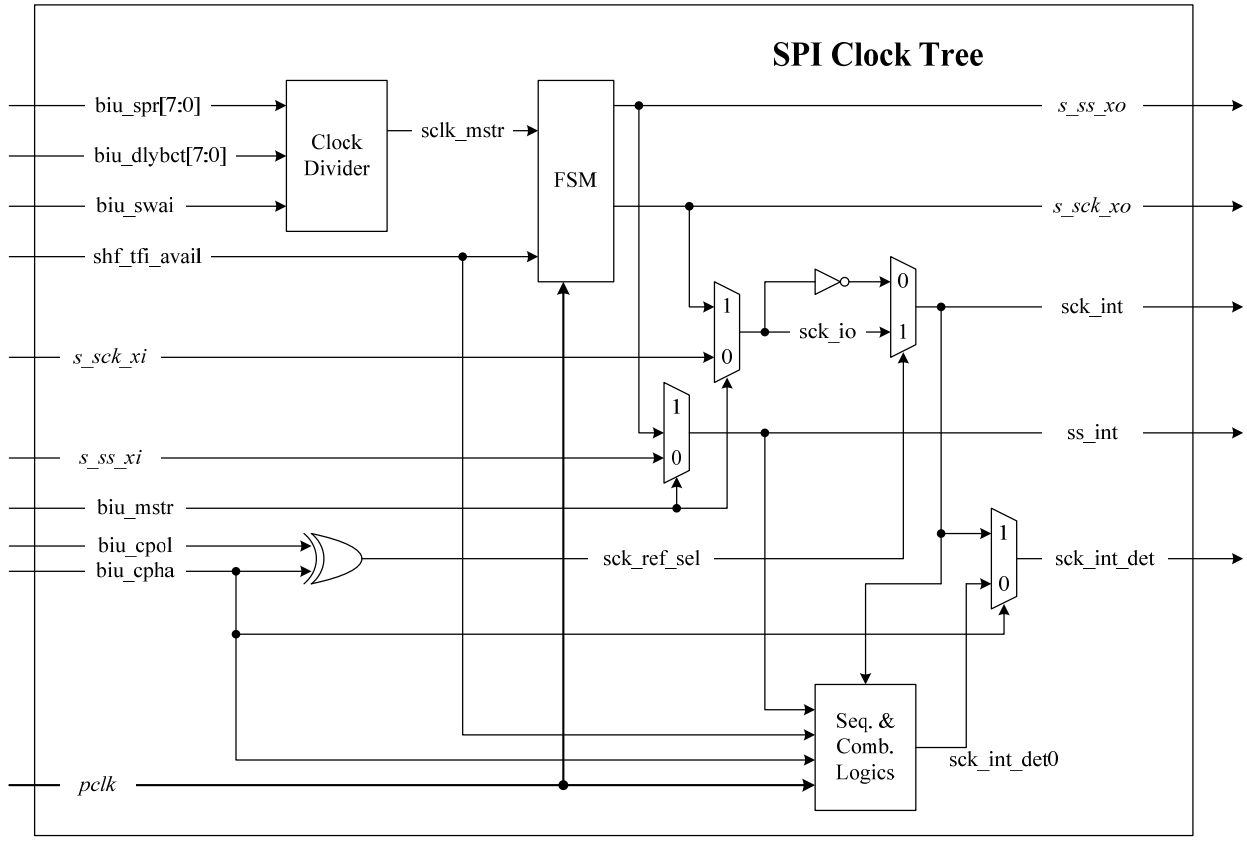


Fig. 8 SPI Clock Structure

6.13.6 SPI Firmware Configuration Flow Chart

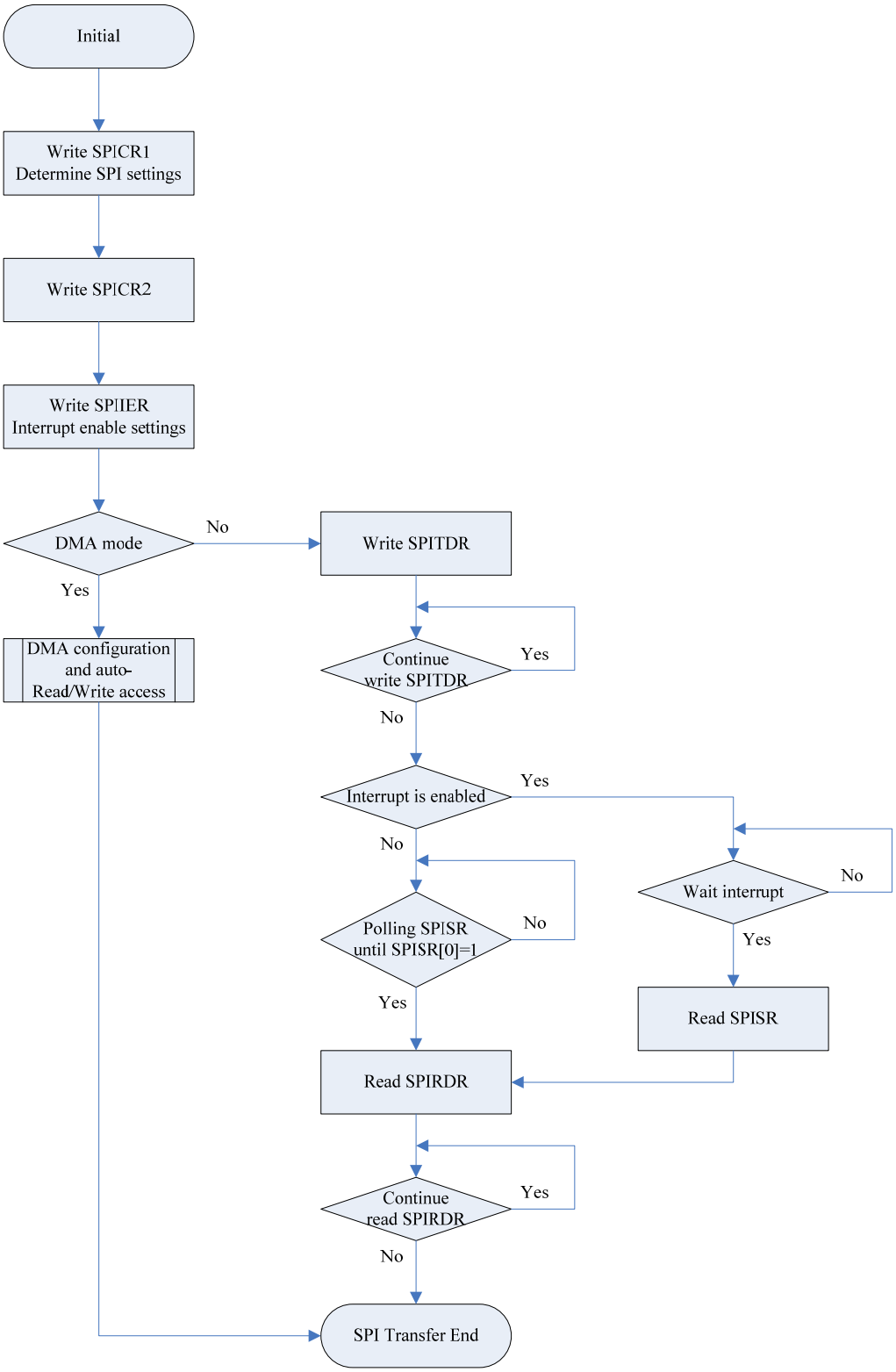


Fig. 9 Firmware Configuration Flow Chart

6.13.7 SPI Special Register

Register Name	Address	Reset Default (Hex)	Description
SPI Serial Interface Register 0 (SPI0)		**0x0020_4400~0x0020_47FF**	
SPI0_CR1	0x0020_4400	0x0000_0001	SPI0 setting
SPI0_CR2	0x0020_4404	0x0000_0000	SPI0 setting
SPI0_IER	0x0020_4408	0x0000_0000	SPI0 interrupt enable setting
SPI0_ISR	0x0020_440C	0x0001_0001	SPI0 status
SPI0_TDR	0x0020_4410	**0x0000_0000**	SPI0 transmit data buffer
SPI0_RDR	0x0020_4414	0x0000_0000	SPI0 receive data buffer
SPI Serial Interface Register 1 (SPI1)		**0x0020_4800~0x0020_4BFF**	
SPI1_CR1	0x0020_4800	0x0000_0001	SPI1 setting
SPI1_CR2	0x0020_4804	0x0000_0000	SPI1 setting
SPI1_IER	0x0020_4808	0x0000_0000	SPI1 interrupt enable setting
SPI1_ISR	0x0020_480C	0x0001_0001	SPI1 status
SPI1_TDR	0x0020_4810	0x0000_0000	SPI1 transmit data buffer
SPI1_RDR	0x0020_4814	0x0000_0000	SPI1 receive data buffer

SPI Control Register 1
SPI0_CR1 (Address: 0x0020_4400)
SPI1_CR1 (Address: 0x0020_4800) **Reset Value: 0x0000_0001**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	SPR[7:0]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	-	R/W	R/W	-	-	R/W	R/W
Name	SPIEN	Reserved	MSTR	LSBF	Reserved		CPOL	CPHA

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-8	SPR[7:0]	SPI Clock (SCK) rate select bits (SPI maximum speed = mcu_clk / 2) 0: mcu_clk / 2 (default) 1: mcu_clk / 2 2: mcu_clk / 2 3: mcu_clk / 3 … 255: mcu_clk / 255
7	SPIEN	SPI system enable

Bit Number	Bit Mnemonic	Description
		1 = SPI is enabled 0 = SPI is disabled (default)
6	Reserved	
5	MSTR	SPI Master/Slave mode select 1= Master mode 0 = Slave mode (default)
4	LSBF	SPI LSB first enable 1 = Data is transferred least significant bit (LSB) first 0 = Data is transferred most significant bit (MSB) first (default)
3-2	Reserved	-
1	CPOL	SPI clock polarity bit select 1: Active-low clocks selected. In idle state SCK is high 0: Active-high clocks selected. In idle state SCK is low (default)
0	CPHA	SPI clock phase bit select 1: Sampling of data occurs at even edges of SCK (default) 0: Sampling of data occurs at odd edges of SCK

-: unimplemented.

SPI Control Register 2
SPI0_CR2 (Address: 0x0020_4404)
SPI1_CR2 (Address: 0x0020_4804) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	R/W	R/W	-	-	-	-	-	-
Name	TDMA_EN	RDMA_EN	Reserved					
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	W	W	-	-	-	-	-	-
Name	TCLR	RCLR	Reserved					
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DLYBCT[7:0]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	-	-	-	R/W
Name	Reserved	RXTRIG[2:0]			Reserved			SWAI

Bit Number	Bit Mnemonic	Description
31	TDMA_EN	SPI Tx DMA enable setting 1: DMA ON. DMA request will be issued 0: DMA OFF. DMA request will not be issued (default)
30	RDMA_EN	SPI Rx DMA enable setting 1: DMA ON. DMA request will be issued 0: DMA OFF. DMA request will not be issued (default)
29-24	Reserved	-
23	TCLR	SPI Transmitter FIFO clear setting 1: the pointer of Rx FIFO will be cleared when TCLR is set to 1, and then the TCLR is self clearing to 0

Bit Number	Bit Mnemonic	Description
22	RCLR	SPI Receiver FIFO clear setting 1: the pointer of Rx FIFO will be cleared when RCFR is set to 1, and then the RCFR is self clearing to 0
21-16	Reserved	-
15-8	DLYBCT[7:0]	Delay between consecutive transfers 0: no delay (default) 1: delay 1 clock … 255: delay DLYBCT cycles (Max. 255 PCLK)
7	Reserved	-
6-4	RXTRIG[2:0]	SPI Rx data trigger level 000: 1 byte (default) 001: 8 bytes (1/4 full) 010: 16 bytes (1/2 full) 011: 24 bytes (3/4 full) 100: 28 bytes (7/8 full) 101: 30 bytes (15/16 full) 110: 31 bytes (31/32 full) 111: 32 bytes (full)
3-1	Reserved	-
0	SWAI	SPI Stop in WAIT mode 1: This bit is mainly for master mode use. It can halt SPI clock generation and keep SSN at low level after data transfer temporarily completes. If new data are written to data register, SCK generation and transfer will start again. (after data transfer completes, this bit is cleared and then SSN signal can be released to high level) 0: After all data transfer completes (data buffer is empty), and then SS signal can be released to high level. (default)

-: unimplemented.

SPI Interrupt Enable Register
SPI0_IER (Address: 0x0020_4408)
SPI1_IER (Address: 0x0020_4808) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved		IE_TFAE	IE_TFAF	IE_TFOV	IE_TFF	IE_TFE	IE_TXE
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved		IE_RFAE	IE_RFAF	IE_RFOV	IE_RFF	IE_RFE	IE_RXDR

Bit Number	Bit Mnemonic	Description
31-22	Reserved	-
21	IE_TFAE	SPI Tx FIFO Almost Empty Interrupt Mask 1: Interrupt is enabled 0: Interrupt is disabled (default)
20	IE_TFAF	SPI Tx FIFO Almost Full Interrupt Mask 1: Interrupt is enabled 0: Interrupt is disabled (default)
19	IE_TFOV	SPI Tx FIFO Overrun Error Interrupt Mask 1: Interrupt is enabled 0: Interrupt is disabled (default)
18	IE_TFF	SPI Tx FIFO Full Interrupt Mask 1: Interrupt is enabled 0: Interrupt is disabled (default)
17	IE_TFE	SPI Tx FIFO Empty Interrupt Mask 1: Interrupt is enabled 0: Interrupt is disabled (default))
16	IE_TXE	SPI Tx Empty Interrupt Mask 1: Interrupt is enabled 0: Interrupt is disabled (default)
15-6	Reserved	-
5	IE_RFAE	SPI Rx FIFO Almost Empty Interrupt Mask 1: Interrupt is enabled 0: Interrupt is disabled (default)
4	IE_RFAF	SPI Rx FIFO Almost Full Interrupt Mask 1: Interrupt is enabled 0: Interrupt is disabled (default)
3	IE_RFOV	SPI Rx FIFO Overrun Error Interrupt Mask 1: Interrupt is enabled 0: Interrupt is disabled (default)
2	IE_RFF	SPI Rx FIFO Full Interrupt Mask 1: Interrupt is enabled 0: Interrupt is disabled (default)
1	IE_RFE	SPI Rx FIFO Empty Interrupt Mask 1: Interrupt is enabled 0: Interrupt is disabled (default)
0	IE_RXDR	SPI Rx Data Ready Interrupt Mask 1: Interrupt is enabled 0: Interrupt is disabled (default)

-: unimplemented.

SPI Status Register
SPI0_ISR (Address: 0x0020_440C)
SPI1_ISR (Address: 0x0020_480C) **Reset Value: 0x0001_0001**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	R	R	R	R	R	R
Name	Reserved		TFAE	TFAF	TFOV	TFF	TFE	TXE
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	R	R	R	R	R	R
Name			RF_CNT[5:0]					
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	R	R	R	R	R	R
Name	Reserved		RFAE	RFAF	RFOV	RFF	RFE	RXDR

Bit Number	Bit Mnemonic	Description
31-22	Reserved	-
21	TFAE	SPI Tx FIFO Almost Empty Indicator 1: There is only 1 byte data in Tx FIFO. This bit is cleared by a read of the SPISR, a write of TCLR = 1, or Tx FIFO has 0 or more than 1 byte data.
20	TFAF	SPI Tx FIFO Almost Full Indicator 1: Tx FIFIO has been ritten until only 1 byte space left. This bit is cleared by a read of the SPISR, a write of TCLR = 1, or Tx FIFO is full or has more than 1 byte space.
19	TFOV	SPI Tx FIFO Overrun Error 1: SPI Tx FIFO Overrun Error. This bit is automatically cleared by a read of the SPI_TXD or a write of TCLR = 1
18	TFF	SPI Tx FIFO Full Inidcator 1: SPI Tx FIFO/Buffer is full. This bit is automatically cleared by a read of the SPI_TXD, a write of TCLR = 1, or after shift register loads data from Tx FIFO.
17	TFE	SPI Transmitter FIFO Register Empty Indicator 1: the TFE bit is set when the transmitter FIFO is empty. This bit is cleared by a reaad of the SPI_TXD, or after a least one byte data is written to the Tx FIFO.
16	TXE	SPI Tx Empty Indicator 1: SPI Tx FIFO and Shift register are empty. This bit is cleared by aread of the SPI_TXD, or a least one byte data is in the Tx FIFO/Shift register.
15-14	Reserved	-
13-8	RF_CNT[5:0]	SPI Rx FIFO Data Count from 0~32
7-6	Reserved	-
5	RFAE	SPI Rx FIFO Almost Empty Indicator 1: SPI Rx FIFO Almost Empty, there is only 1 byte data in Rx FIFO. This bit is cleared by a read of the SPI_RXD, a write of RCLR = 1, or Rx FIFO has 0 or more than 1 byte data.

Bit Number	Bit Mnemonic	Description
4	RFAF	SPI Rx FIFO Almost Full Indicator 1: SPI Rx FIFO has been written until only 1 byte space left. This bit is cleared by a read of the SPI_RXD, a write of RCLR = 1, or Rx FIFO is full or has more than 1 byte space.
3	RFOV	SPI Rx FIFO Overrun Error 1: SPI Rx FIFO Overrun Error. This bit is automatically cleared by a read of the SPI_RXD, or a write of RCLR = 1
2	RFF	SPI Rx FIFO Full Indicator 1: SPI Rx FIFO is full. This bit is automatically cleared by a read of the SPI_RXD, a write of RCLR = 1, or after shift register loads data from Rx FIFO
1	RFE	SPI Rx FIFO Empty Indicator 1: SPI Receiver FIFO is empty. This bit is cleared by a read of the SPI_RXD, or after at least one byte is received into the receiver FIFO
0	RXDR	SPI Rx Data Ready Indicator 1: SPI Rx data count reaches trigger level (data ready). When MCU/DMA reads SPI_RXD until the data count is under the trigger level, this bit is cleared. A write of RCLR = 1 also clears this bit.

-: unimplemented.

SPI0 Transmit Buffer Register
SPI0_TDR (Address: 0x0020_4410)
SPI1_TDR (Address: 0x0020_4810) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	SPITDR[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	SPI_TDR[7:0]	SPI Transmit Data Buffer

-: unimplemented.

SPI Receive Buffer Register
SPI0_RDR (Address: 0x0020_4414)
SPI1_RDR (Address: 0x0020_4814) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	SPIRDR[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	SPI_RDR[7:0]	SPI Receive Data Buffer

-: unimplemented.

6.14 Analog/Digital Converter (ADC)

6.14.1 Features

WT59F164 has a built-in 12-channel 12-bit Analog/Digital Converter, which last channel (Channel 11) is internally connected to temperature sensor output, and the remaining 11 Channels (Channel 0~10) can be used freely. ADC conversion time is 16 ADC clocks (ADC clock is configured by ADC_SLT_CLK[2:0]).

- **Single Mode:**

  Turning on the A/D Converter power (ADC Control Register ADC_ON = 1), and setting the STR_CVT = 1, the system will enter the Continuous Conversion Mode. When conversion is completed, the conversion data will be updated and an interrupt will be generated (ADFINISH_FLG = 1). If ADC convert finish Interrupt is enabled (EN_ADFINSH_INT = 1), the ADC interrupt will generate.

- **Continuous Mode:**

  If activate continuous convert control bit (ADC_MODE = 1), the system will enter the Continuous Conversion Mode.

- **Comparator Mode:**

  When turning on the A/D converter power (ADC Control Register ADC_ON = 1), and activating the Compare function (ADC Control Register ADCSEMP = 1 and EN_ADC_WK = 1), the conversion data of Analog input (ADC_IN) compares the data of Wakeup data register (ADC_WK_V). When the corresponding digital value of the voltage analog input is greater than (ADC_BIG = 1) or smaller than (ADC_BIG = 0) the setting value of ADC Wakeup Data register (ADC_WK_V), the ADC interrupt will occur. The Voltage Compare function of ADC module works as a wakeup source.

  When turning on comparator mode, AD convert mode is disabled.

- **Two Channels Toggle Mode:**

  When turning on ADC power (ADC Control Register ADC_ON = 1), and activating the Two Channels Toggle mode (ADC Control Register TOGGLE_MODE = 1), two analog inputs (set by EN_AD_CH and EN_AC_CH2) proceed with the AD conversion successively. In the meantime, by setting ADC_START = 1, the channel (set by EN_AD_CH) conversion will go first. When conversion is completed, an interrupt will be generated, and automatically toggled to the EN_AC_CH2 specified channel. By setting ADC_START = 1, the channel (set by EN_AC_CH2) will proceed with conversion. It can also work together with Continuous single mode to proceed with the continuous toggle conversion of two channels. It is easy to know that which channel will be converted next by ADC_CH_SEL.

6.14.2 Special Register

Register Name	Address	Reset Default (Hex)	Description
12-bit Analog/Digital Converter Register (ADC)		**0x0020_6400~0x0020_67FF**	
ADC_CTL	0x0020_6400	0x0000_0000	ADC control
ADC_DATA	0x0020_6404		ADC transfer data
ADC_EOC	0x0020_6408	0x0000_0000	ADC transfer complete
ADC_OPTION	0x0020_640C	0x0000_0000	ADC mode setting

Register Name	Address	Reset Default (Hex)	Description
ADC_WAKEUP_VOLTAGE	0x0020_6410	0x0000_0800	ADC wakeup compare voltage setting
ADC_CH_EN	0x0020_6418	0x0000_0000	ADC channel enable

Analog/Digital Converter Control Register ADC_CTL
(Address: 0x0020_6400) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				CLR_ADC_WK_INT	EN_ADC_INT	DMA	ALIGN
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	ADC_ON	STR_CVT	EN_ADC_WK	ADC_BIG	EN_AD_CH [3:0]			

Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11	CLR_ADC_WK_INT	ADC wakeup interrupt clear setting 1: Clear ADC wakeup interrupt
10	EN_ADC_INT	ADC EOC interrupt enable setting 1: Enable ADC EOC interrupt 0: Disable ADC EOC interrupt (default)
9	DMA	ADC DMA enable setting 1: Enable DMA 0: Disable DMA (default)
8	ALIGN	ADC data alignment 1: Left alignment 0: Right alignment (default)
7	ADC_ON	ADC module power setting 1: Enable ADC 0: Power down ADC (default)
6	STR_CVT	Start ADC converter setting 1: Start ADC converter, and will be automatically cleared after conversion is complete
5	EN_ADC_WK	ADC Wakeup mode enable setting 1: Enable ADC Wakeup mode 0: Disable ADC Wakeup mode (default)
4	ADC_BIG	Analog/Digital Converter data compare setting 1: data set if Vin > ADC_CMP_V[11:0] 0: data set if Vin < ADC_CMP_V[11:0] (default) Vin: channel selected by EN_AD_CH [11:0]

Bit Number	Bit Mnemonic	Description
3-0	EN_AD_CH[3:0]	ADC Channel select 0000: ADC Channel 0 (default) ... 1010: ADC Channel 10 1011: ADC Channel 11 (connect to Internal Temperature Sensor)

-: unimplemented.

Analog/Digital Converter Data Register ADC_DATA
(Address: 0x0020_6404) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R	R	R	R
Name	Reserved				AD_DATA[11:8]			
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	AD_DATA[7:0]							

Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11-0	AD_DATA[11:0]	AD convert data value

-: unimplemented.

Analog/Digital Converter Convert Complete Register ADC_EOC
(Address: 0x0020_6408) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	-	R/W
Name	Reserved							EOC

Bit Number	Bit Mnemonic	Description
31-1	Reserved	-

Bit Number	Bit Mnemonic	Description
0	EOC	ADC finish 1 conversion 1: ADC finish 1 conversion, cleared by software or by reading AD_DATA

-: unimplemented.

Analog/Digital Converter Control Register ADC_OPTION
(Address: 0x0020_640C) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved						ADC_DO[1:0]	
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	-	-	-
Name	ADC_SLT_CLK [2:0]			ADC_MODE	ADCSEMP	Reserved		

Bit Number	Bit Mnemonic	Description
31-10	Reserved	-
9-8	ADC_DO[1:0]	ADC data output bit setting 00: 12-bit (default) 01: 10-bit 1X: 8-bit
7-5	ADC_SLT_CLK[2:0]	ADC clock setting 000: 2 MHz (default) 001: 2 MHz / 2 010: 2 MHz / 4 011: 2 MHz / 8 100: 2 MHz / 16 101: 2 MHz / 32 110: 2 MHz / 64 111: 2 MHz / 128
4	ADC_MODE	ADC continuous converter mode setting 1: ADC continuous convert 0: ADC single convert (default)
3	ADCSEMP	ADC comparator enable setting 1: Enable ADC comparator 0: Disable ADC comparator (default)
2-0	Reserved	-

-: unimplemented.

Analog/Digital Converter Wakeup Voltage Setting Register ADC_WAKEUP_VOLTAGE
(Address: 0x0020_6410) **Reset Value: 0x0000_0800**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				ADC_WK_V [11:8]			
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	ADC_WK_V [7:0]							

Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11-0	ADC_WK_V [11:0]	ADC wakeup voltage data setting

-: unimplemented.

Analog/Digital Converter channel Enable Register ADC_EN_CH
(Address: 0x0020_6418) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	R/W
Name	Reserved							ADC_CH_SEL
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	-	-	R/W
Name	ADC_CH2_SLT[3:0]				Reserved			ADC_TOG_EN

Bit Number	Bit Mnemonic	Description
31-9	Reserved	-
8	AD_CH_SEL	Next AD channel flag to be converted 1: proceed EN_AD_CH2[3:0] specified channel 0: proceed EN_AD_CH [3:0] specified channel (default)
7-4	EN_AD_CH2[3:0]	ADC dual channel TOGGLE mode second channel setting 0000: ADC channel 0 (default) ... 1010: ADC channel 10

Bit Number	Bit Mnemonic	Description
		1011: ADC channel 11 (connect to internal temperature sensor)
3-1	Reserved	-
0	TOGGLE_MODE	ADC dual Channel TOGGLE mode enable setting 1: Enable ADC dual channel TOGGLE mode 0: Disable ADC dual channel TOGGLE mode (default)

-: unimplemented.

6.15 HDMI CEC

6.15.1 Features

- Transmit serial HDMI CEC input: digital filter (if the pulse < 1 * mcu_clk, the pulse can be filtered.)
- CEC sample clock base: 125 kHz

6.15.2 HDMI CEC Control Register

Register Name	Address	Reset Default (Hex)	Description
HDMI CEC Control Register (CEC) 0x0020_1400~0x0020_17FF			
CEC_TX_ADDR	0x0020_1400	0x0000_00FF	CEC initiator logical address field of transmit header block
CEC_TX_DATA1	0x0020_1404	0x0000_00FF	CEC transmit data buffer
CEC_TX_DATA2	0x0020_1408	0x0000_00FF	CEC transmit data buffer
CEC_TX_DATA3	0x0020_140C	0x0000_00FF	CEC transmit data buffer
CEC_TX_DATA4	0x0020_1410	0x0000_00FF	CEC transmit data buffer
CEC_TX_DATA5	0x0020_1414	0x0000_00FF	CEC transmit data buffer
CEC_TX_DATA6	0x0020_1418	0x0000_00FF	CEC transmit data buffer
CEC_TX_DATA7	0x0020_141C	0x0000_00FF	CEC transmit data buffer
CEC_TX_DATA8	0x0020_1420	0x0000_00FF	CEC transmit data buffer
CEC_TX_DATA9	0x0020_1424	0x0000_00FF	CEC transmit data buffer
CEC_TX_DATA10	0x0020_1428	0x0000_00FF	CEC transmit data buffer
CEC_TX_DATA11	0x0020_142C	0x0000_00FF	CEC transmit data buffer
CEC_TX_DATA12	0x0020_1430	0x0000_00FF	CEC transmit data buffer
CEC_TX_DATA13	0x0020_1434	0x0000_00FF	CEC transmit data buffer
CEC_TX_DATA14	0x0020_1438	0x0000_00FF	CEC transmit data buffer
CEC_TX_DATA15	0x0020_143C	0x0000_00FF	CEC transmit data buffer
CEC_RX_ADDR	0x0020_1400		CEC follower logical address field of receive header block
CEC_RX_DATA1	0x0020_1404		CEC receive data buffer
CEC_RX_DATA2	0x0020_1408		CEC receive data buffer
CEC_RX_DATA3	0x0020_140C		CEC receive data buffer
CEC_RX_DATA4	0x0020_1410		CEC receive data buffer
CEC_RX_DATA5	0x0020_1414		CEC receive data buffer
CEC_RX_DATA6	0x0020_1418		CEC receive data buffer
CEC_RX_DATA7	0x0020_141C		CEC receive data buffer
CEC_RX_DATA8	0x0020_1420		CEC receive data buffer
CEC_RX_DATA9	0x0020_1424		CEC receive data buffer
CEC_RX_DATA10	0x0020_1428		CEC receive data buffer
CEC_RX_DATA11	0x0020_142C		CEC receive data buffer
CEC_RX_DATA12	0x0020_1430		CEC receive data buffer
CEC_RX_DATA13	0x0020_1434		CEC receive data buffer
CEC_RX_DATA14	0x0020_1438		CEC receive data buffer
CEC_RX_DATA15	0x0020_143C		CEC receive data buffer

Register Name	Address	Reset Default (Hex)	Description
CEC_CTL	0x0020_1440	0x0000_0000	CEC enable control
CEC_INIT	0x0020_1444	0x0000_0010	CEC initiator setting
CEC_RETRY_CNT	0x0020_1448	0x0000_0000	CEC retry setting
CEC_FREE_CNT	0x0020_144C	0x0000_0046	CEC free time setting
CEC_FREE_TM	0x0020_1450	0x0000_0008	CEC free time setting
CEC_FREE_RESULT	0x0020_1454		CEC free time status
CEC_RX_LEN	0x0020_1460		CEC receive data length
CEC_ACK_STA	0x0020_1464	0x0000_0002	CEC ACK status
CEC_ADR2	0x0020_1468	0x0000_00F0	CEC address
CEC_BIT_STA	0x0020_1470		CEC bit status
CEC_INT	0x0020_1478		CEC interrupt flag
CEC_INT_CLR	0x0020_147C	0x0000_0000	CEC interrupt clear

HDMI CEC Control Register CEC_CTL (Address: 0x0020_1440) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	-	-	R	-	W	-	-
Name	EN_CEC	Reserved		CEC_BUSY	Reserved	CEC_L_3600US	Reserved	

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	EN_CEC	HDMI CEC enable setting 1: Enable HDMI CEC 0: Disable HDMI CEC (default)
6-5	Reserved	-
4	CEC_BUSY	HDMI CEC busy status 1: CEC line is busy (set by CEC line is low level or Initiator state) 0: CEC line is free (cleared by CEC Transmit/Receive finished or CEC line keeps high level till 6.144ms) (default)
3	Reserved	-
2	CEC_L_3600US	HDMI CEC line is pulled low 1: Force CEC line to low level till 3.6ms 0: Don't force CEC line to low level till 3.6ms (default)
1-0	Reserved	-

-: unimplemented.

6.15.3 HDMI CEC Initiator Register

HDMI CEC Initiator Register CEC_INIT (Address: 0x0020_1444) Reset Value: 0x0000_0008

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	-	-	R/W	R/W	R/W	R/W	R/W
Name	CEC_TR	Reserved		CEC_NACK_STOP	CEC_TX_LEN[3:0]			

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	CEC_TR	HDMI CEC initiator enable setting 1: Enable initiator state and transmit data 0: Follower state (default)
6-5	Reserved	-
4	CEC_NACK_STOP	HDMI CEC busy status 1: CEC line is busy (set by CEC line is in low level or Initiator state) (default) 0: CEC line is free (cleared by Transmit/Receive finished or CEC line keeps high level till 6.144ms
3-0	CEC_TX_LEN[3:0]	Tx length of a CEC message 0000: 1 block (header block) (default) 0001: 2 blocks (header block + 1 data block) … 1111: 16 blocks (header block + 15 data block)

-: unimplemented.

HDMI CEC Retry Setting Register CEC_INIT (Address: 0x0020_1448) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	-	-	R/W	R/W
Name	Reserved	CEC_RETRY_CNT[2:0]			Reserved		CEC_TX_RISING_SHIFT[1:0]	

Bit Number	Bit Mnemonic	Description
31-7	Reserved	-
6-4	CEC_RETRY_CNT[2:0]	Auto frame re-transmission counter (0~7 times)
3-2	Reserved	-
1-0	CEC_TX_RISING_SHIFT[1:0]	The advanced rising edge time of all bits (total bit timing unchanged) 00: normal mode (default) 01: advance mode 100us 10: advance mode 200us 11: advance mode 250us

-: unimplemented.

HDMI CEC FREE Counter Setting Register CEC_FREE_CNT
(Address: 0x0020_144C) **Reset Value: 0x0000_0046**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	CEC_PREVIOUS_FREE_BIT[3:0]				CEC_NEW_FREE_BIT[3:0]			

Bit Number	Bit Mnemonic	Description
31-7	Reserved	-
6-4	CEC_PREVIOUS_FREE_BIT[3:0]	Signal free time bit counter for previous attempt to send frame unsuccessful
3-0	CEC_NEW_FREE_BIT[3:0]	Signal free time bit counter for new initiator wants to send a frame

-: unimplemented.

HDMI CEC FREE Counter Setting Register CEC_FREE_TM
(Address: 0x0020_1450) **Reset Value: 0x0000_0008**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				CEC_PRESENT_FREE_BIT[3:0]			

Bit Number	Bit Mnemonic	Description
31-4	Reserved	-
3-0	CEC_PRESENT_FREE_BIT[3:0]	Signal free time bit counter for present initiator wants to send another frame immediately after its previous frame

-: unimplemented.

HDMI CEC FREE Result Register CEC_FREE_RESULT
(Address: 0x0020_1454) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	R	R	R
Name	Reserved					CEC_PREVIOUS_FREE	CEC_NEW_FREE	CEC_PRESENT_FREE

Bit Number	Bit Mnemonic	Description
31-3	Reserved	-
2	CEC_PREVIOUS_FREE	1: allow previous attempt to send frame unsuccessful set by CEC line keeps high level till CEC_PREVIOUS_FREE_BIT[3:0]X2.4ms, auto frame re-transmission wait CEC_PREVIOUS_FREE = 1 to retry to send the message 0: disallow (cleared by CEC line is low level)
1	CEC_NEW_FREE	1: allow new initiator wants to send a frame, set by CEC line keeps high level till CEC_NEW_FREE_BIT[3:0]X2.4ms 0: disallow (cleared by CEC line is low level)
0	CEC_PRESENT_FREE	1: allow present initiator wants to send another frame immediately after its previous frame, set by CEC line keeps high level till CEC_PRESENT_FREE_BIT[3:0]X2.4ms 0: disallow (cleared by CEC line is low level)

-: unimplemented.

6.15.4 HDMI CEC Follower Register

HDMI CEC Receive Length Register CEC_RX_LEN (Address: 0x0020_1460) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R	R	-	R	R	R	R
Name	Reserved	CEC_RX_EOM	CEC_MATCH_ADR	Reserved	CEC_RX_LEN[3:0]			

Bit Number	Bit Mnemonic	Description
31-7	Reserved	-
6	CEC_RX_EOM	EOM bit receive status 1: Receive EOM bit
5	CEC_MATCH_ADR	Address Match status 1: The follower logical address match (CEC_RX_DATA0L = CEC_TX_DATA0H) 0: The follower logical address (CEC_RX_DATA0L≠ CEC_TX_DATA0H)
4	Reserved	-
3-0	CEC_RX_LEN[3:0]	Received length of a CEC message 0000: 1 Block (header block) 0001: 2 Block (header block + 1 data block) 0010: 3 Block (header block + 2 data block) . . . 1111: 16 Block (header block + 15 data block)

-: unimplemented.

HDMI CEC Receive ACK Status Register CEC_ACK_STA
(Address: 0x0020_1464) Reset Value: 0x0000_0002

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				CEC_MIS_ADR_INT	CEC_RX_RANGE_SEL	CEC_BROADCAST_ACK	CEC_TXACK

Bit Number	Bit Mnemonic	Description
31-4	Reserved	-
3	CEC_MIS_ADR_INT	The follower logical address mismatch (CEC_RX_DATA0L ≠ CEC_TX_DATA0H) interrupt flag 1: interrupt occurred
2	CEC_RX_RANGE_SEL	Range of bit timing detection 0: 16 us (default) 1: 64 us
1	CEC_BROADCAST_ACK	ACK bit when broadcast address is detected 1: NACK (default) 0: ACK
0	CEC_TXACK	ACK bit when directed address is detected 1: NACK 0: ACK (default)

-: unimplemented.

HDMI CEC Second Address Register CEC_ADR2
(Address: 0x0020_1468) **Reset Value: 0x0000_00F0**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	-	-	R/W
Name	CEC_ADR2[3:0]				Reserved	Reserved	Reserved	CEC_ADR2_EN

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-4	CEC_ADR2[3:0]	Second CEC address setting
3-1	Reserved	-
0	CEC_ADR2_EN	Second CEC address enable setting 1: Enable second CEC address 0: Disable second CEC address (default)

-: unimplemented.

HDMI CEC Bit Status Register CEC_BIT_STA (Address: 0x0020_1470) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	R	R	R
Name	Reserved					CEC_BIT_H_OVER	CEC_BIT_L_OVER	CEC_BIT_L_LESS

Bit Number	Bit Mnemonic	Description
31-3	Reserved	-
2	CEC_BIT_H_OVER	1: High period of bit over than normal 0: Normal Cleared by CLR_TM_ERR_INT = 1 or the end of START bit
1	CEC_BIT_L_OVER	1: Low period of bit over than normal 0: Normal Cleared by CLR_TM_ERR_INT = 1 or the end of START bit
0	CEC_BIT_L_LESS	1: Low period of bit less than normal 0: Normal Cleared by CLR_TM_ERR_INT = 1 or the end of START bit

-: unimplemented.

6.15.5 HDMI CEC Interrupt Status & Clear Register

HDMI CEC Interrupt Status Register CEC_INT (Address: 0x0020_1478) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	-	R	R	R
Name	CEC_INT	CEC_TX_INT	CEC_RX_INT	CEC_DLOSS_INT	Reserved	CEC_LINE_ERR_INT	CEC_NACK_INT	CEC_TM_ERR_INT

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	CEC_INT	CEC interrupt flag 1: Event CEC interrupt (or bit 0~6 of register 7EH)

Bit Number	Bit Mnemonic	Description
6	CEC_TX_INT	Initiator finish transmit interrupt flag 1: Initiator finish to transmit a message from transmit buffer
5	CEC_RX_INT	Follower Finish receive interrupt flag 1: Follower finish to receive a message (EOM = 1 or receive buffer is full)
4	CEC_DLOSS_INT	Initiator arbitrate loss interrupt flag 1: Initiator arbitrate loss interrupt
3	Reserved	-
2	CEC_LINE_ERR_INT	Follower detect CEC Line error interrupt flag (high period of bit less than normal) 1: Follower detect CEC line error
1	CEC_NACK_INT	Initiator receive NACK interrupt flag 1: Initiator Receive NACK
0	CEC_TM_ERR_INT	Follower receive timing error of data /EOM/ACK bit interrupt flag 1: Follower receive timing error of data /EOM/ACK bit

-: unimplemented.

HDMI CEC Interrupt Clear Register CEC_INT_CLR
(Address: 0x0020_147C) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	W	W	W	-	W	W	W
Name	Reserved	CEC_TX_INT	CEC_RX_INT	CEC_DLOSS_INT	Reserved	CEC_LINE_ERR_INT	CEC_NACK_INT	CEC_TM_ERR_INT

Bit Number	Bit Mnemonic	Description
31-7	Reserved	-
6	CLR_TX_INT	Transmit finish interrupt clear setting 1: Clear Finish to transmit a message interrupt
5	CLR_RX_INT	Receive finish interrupt clear setting 1: Clear finish to receive a message interrupt
4	CLR_DLOSS_INT	Arbitrate loss interrupt clear setting 1: Clear arbitrate loss interrupt
3	Reserved	-
2	CLR_LINE_ERR_INT	CEC line error interrupt clear setting 1: Clear CEC line error interrupt
1	CLR_NACK_INT	NACK interrupt clear setting 1: Clear NACK interrupt
0	CLR_TM_ERR_INT	Data /EOM/ACK bit timing error interrupt clear flag 1: Clear data/EOM/ACK bit timing error interrupt

-: unimplemented.

6.15.6 HDMI CEC Initiator Transmit Buffer Register

HDMI CEC Transmit Address Register CEC_TX_ADDR
(Address: 0x0020_1400) **Reset Value: 0x0000_00FF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	CEC_TX_DATA0H[3:0]				CEC_TX_DATA0L[3:0]			

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-4	CEC_TX_DATA0H[3:0]	The CEC initiator logical address field of the CEC transmit header block
3-0	CEC_TX_DATA0L[3:0]	The CEC follower logical address field of the CEC transmit header block

-: unimplemented.

HDMI CEC Transmit Buffer Register 1 CEC_TX_DATA1
(Address: 0x0020_1404) **Reset Value: 0x0000_00FF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	CEC_TX_DATA1[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_TX_DATA1[7:0]	CEC transmit data 1

-: unimplemented.

HDMI CEC Transmit Buffer Register 2 CEC_TX_DATA2
(Address: 0x0020_1408) **Reset Value: 0x0000_00FF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	CEC_TX_DATA2[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_TX_DATA2[7:0]	CEC transmit data 2

-: unimplemented.

HDMI CEC Transmit Buffer Register 3 CEC_TX_DATA3
(Address: 0x0020_140C) **Reset Value: 0x0000_00FF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	CEC_TX_DATA3[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_TX_DATA3[7:0]	CEC transmit data 3

-: unimplemented.

HDMI CEC Transmit Buffer Register 4 CEC_TX_DATA4
(Address: 0x0020_1410) **Reset Value: 0x0000_00FF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	CEC_TX_DATA4[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_TX_DATA4[7:0]	CEC transmit data 4

-: unimplemented.

HDMI CEC Transmit Buffer Register 5 CEC_TX_DATA5
(Address: 0x0020_1414) **Reset Value: 0x0000_00FF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	CEC_TX_DATA5[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_TX_DATA5[7:0]	CEC transmit data 5

-: unimplemented.

HDMI CEC Transmit Buffer Register 6 CEC_TX_DATA6
(Address: 0x0020_1418) **Reset Value: 0x0000_00FF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	CEC_TX_DATA6[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_TX_DATA6[7:0]	CEC transmit data 6

-: unimplemented.

HDMI CEC Transmit Buffer Register 7 CEC_TX_DATA7
(Address: 0x0020_141C) **Reset Value: 0x0000_00FF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	CEC_TX_DATA7[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_TX_DATA7[7:0]	CEC transmit data 7

-: unimplemented.

HDMI CEC Transmit Buffer Register 8 CEC_TX_DATA8
(Address: 0x0020_1420) **Reset Value: 0x0000_00FF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	CEC_TX_DATA8[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_TX_DATA8[7:0]	CEC transmit data 8

-: unimplemented.

HDMI CEC Transmit Buffer Register 9 CEC_TX_DATA9
(Address: 0x0020_1424) **Reset Value: 0x0000_00FF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	CEC_TX_DATA9[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_TX_DATA9[7:0]	CEC transmit data 9

-: unimplemented.

HDMI CEC Transmit Buffer Register 10 CEC_TX_DATA10
(Address: 0x0020_1428) **Reset Value: 0x0000_00FF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	CEC_TX_DATA10[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_TX_DATA10[7:0]	CEC transmit data 10

-: unimplemented.

HDMI CEC Transmit Buffer Register 11 CEC_TX_DATA11
(Address: 0x0020_142C) **Reset Value: 0x0000_00FF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	CEC_TX_DATA11[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_TX_DATA11[7:0]	CEC transmit data 11

-: unimplemented.

HDMI CEC Transmit Buffer Register 12 CEC_TX_DATA12
(Address: 0x0020_1430) **Reset Value: 0x0000_00FF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	CEC_TX_DATA12[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_TX_DATA12[7:0]	CEC transmit data 12

-: unimplemented.

HDMI CEC Transmit Buffer Register 13 CEC_TX_DATA13
(Address: 0x0020_1434) **Reset Value: 0x0000_00FF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	CEC_TX_DATA13[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_TX_DATA13[7:0]	CEC transmit data 13

-: unimplemented.

HDMI CEC Transmit Buffer Register 14 CEC_TX_DATA14
(Address: 0x0020_1438) **Reset Value: 0x0000_00FF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	CEC_TX_DATA14[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_TX_DATA14[7:0]	CEC transmit data 14

-: unimplemented.

HDMI CEC Transmit Buffer Register 15 CEC_TX_DATA15
(Address: 0x0020_143C) **Reset Value: 0x0000_00FF**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	CEC_TX_DATA15[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_TX_DATA15[7:0]	CEC transmit data 15

-: unimplemented.

6.15.7 HDMI CEC Follower Receive Buffer Register

HDMI CEC Receive Address Register CEC_RX_ADDR
(Address: 0x0020_1400) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CEC_RX_DATA0H[3:0]				CEC_RX_DATA0L[3:0]			

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-4	CEC_RX_DATA0H[3:0]	The CEC initiator logical address field of the CEC receive header block
3-0	CEC_RX_DATA0L[3:0]	The CEC follower logical address field of the CEC receive header block

-: unimplemented.

HDMI CEC Receive Buffer Register 1 CEC_RX_DATA1
(Address: 0x0020_1404) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CEC_RX_DATA1[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_RX_DATA1[7:0]	CEC receive data 1

-: unimplemented.

HDMI CEC Receive Buffer Register 2 CEC_RX_DATA2
(Address: 0x0020_1408) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CEC_RX_DATA2[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_RX_DATA2[7:0]	CEC receive data 2

-: unimplemented.

HDMI CEC Receive Buffer Register 3 CEC_RX_DATA3
(Address: 0x0020_140C) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CEC_RX_DATA3[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_RX_DATA3[7:0]	CEC receive data 3

-: unimplemented.

HDMI CEC Receive Buffer Register 4 CEC_RX_DATA4
(Address: 0x0020_1410) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CEC_RX_DATA4[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_RX_DATA4[7:0]	CEC receive data 4

-: unimplemented.

HDMI CEC Receive Buffer Register 5 CEC_RX_DATA5
(Address: 0x0020_1414) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CEC_RX_DATA5[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_RX_DATA5[7:0]	CEC receive data 5

-: unimplemented.

HDMI CEC Receive Buffer Register 6 CEC_RX_DATA6
(Address: 0x0020_1418) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CEC_RX_DATA6[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_RX_DATA6[7:0]	CEC receive data 6

-: unimplemented.

HDMI CEC Receive Buffer Register 7 CEC_RX_DATA7
(Address: 0x0020_141C) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CEC_RX_DATA7[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_RX_DATA7[7:0]	CEC receive data 7

-: unimplemented.

HDMI CEC Receive Buffer Register 8 CEC_RX_DATA8
(Address: 0x0020_1420) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CEC_RX_DATA8[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_RX_DATA8[7:0]	CEC receive data 8

-: unimplemented.

HDMI CEC Receive Buffer Register 9 CEC_RX_DATA9
(Address: 0x0020_1424) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CEC_RX_DATA9[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_RX_DATA9[7:0]	CEC receive data 9

-: unimplemented.

HDMI CEC Receive Buffer Register 10 CEC_RX_DATA10
(Address: 0x0020_1428) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CEC_RX_DATA10[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_RX_DATA10[7:0]	CEC receive data 10

-: unimplemented.

HDMI CEC Receive Buffer Register 11 CEC_RX_DATA11
(Address: 0x0020_142C) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CEC_RX_DATA11[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_RX_DATA11[7:0]	CEC receive data 11

-: unimplemented.

HDMI CEC Receive Buffer Register 12 CEC_RX_DATA12
(Address: 0x0020_1430) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CEC_RX_DATA12[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_RX_DATA12[7:0]	CEC receive data 12

-: unimplemented.

HDMI CEC Receive Buffer Register 13 CEC_RX_DATA13
(Address: 0x0020_1434) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CEC_RX_DATA13[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_RX_DATA13[7:0]	CEC receive data 13

-: unimplemented.

HDMI CEC Receive Buffer Register 14 CEC_RX_DATA14
(Address: 0x0020_1438) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CEC_RX_DATA14[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_RX_DATA14[7:0]	CEC receive data 14

-: unimplemented.

HDMI CEC Receive Buffer Register 15 CEC_RX_DATA15
(Address: 0x0020_143C) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CEC_RX_DATA15[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	CEC_RX_DATA15[7:0]	CEC receive data 15

-: unimplemented.

6.16 Remote Control (IR)

6.16.1 Features

- IR input with digital filter, can be configured by Register IR_FILTER

6.16.2 Special Register

Register Name	Address	Reset Default (Hex)	Description
IR Register (IR Receiver) 0x0020_1800~0x0020_1BFF			
IR_CTL	0x0020_1800	0x0000_0000	IR control setting
IR_STATUS	0x0020_1804		IR status
IR_COUNT	0x0020_1808		IR count
IR_FILTER	0x0020_180C	0x0000_0000	IR filter

IR Control Register IR_CTL (Address: 0x0020_1800) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	W	-
Name	EN_IR	IR_SEDG	IR_RF	EN_OV_INT	PRE_SCAL[1:0]		CLR_IR_INT	Reserved

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	EN_IR	IR enable setting 1: Enable IR 0: Disable IR (default)
6	IR_SEDG	IR trigger mode setting 1: Single edge trigger 0: Both edges trigger (default)
5	IR_RF	IR rising/falling edge trigger setting 1: Rising edge trigger 0: Falling edge trigger (default)
4	EN_OV_INT	IR count overflow interrupt enable setting 1: Enable count overflow interrupt 0: Disable count overflow interrupt (default)
3-2	PRE_SCAL[1:0]	IR counter pre scaler time setting 00: 64us (default) 01: 32us 10: 128us 11: 1024us

Bit Number	Bit Mnemonic	Description
1	CLR_IR_INT	IR Interrupt Clear setting 1: Clear interrupt “IR_INT”
0	Reserved	

-: unimplemented.

IR Status Register IR_STATUS (Address: 0x0020_1804) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	R	R	R
Name	Reserved					IR_HL	IR_OVFLW	IR_INT

Bit Number	Bit Mnemonic	Description
31-3	Reserved	-
2	IR_HL	Read IR input H/L 1: IR input is high level 0: IR input is low level
1	IR_OVFLW	IR count overflow interrupt status 1: IR count overflow interrupt
0	IR_INT	IR interrupt status 1: IR Interrupt = edge trigger + overflow

-: unimplemented.

IR Counter Register IR_COUNT (Address: 0x0020_1808) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	IR_CNT[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	IR_CNT[7:0]	IR counter. If IR_CNT[7:0] = 0xFF: H/W generate overflow interrupt & keep count = 0xFF

-: unimplemented.

IR Digital Filter Register IR_FILTER (Address: 0x0020_180C) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				IR_FILTER[3:0]			

Bit Number	Bit Mnemonic	Description
31-4	Reserved	-
3-0	IR_FILTER[3:0]	IR digital filter time setting 0000: 2*84ns = 168ns (default) 0001: 1*32us = 32us 0010: 2*32us = 64us . . . 1111: 15*32us = 480us

-: unimplemented.

6.17 I²S

6.17.1 Features

- APB interface compatible
- I²S can operate as either master or slave
- Capable of handling 16, 24, and 32 bit word sizes
- I²S and MSB justified data format supported
- Support three output channels and three input channels
- Six 8 word FIFO data buffers are provided, three for transmit and three for receive
- Six DMA requests, three for transmit and three for receive
- Generates interrupt requests when buffer levels cross a programmable boundary (can set 1, 2, 3, or 4 words)
- The ratio of bit clock and left/right clock is selectable from 32/48/64

6.17.2 Functional Description

The main audio interface of the WT59F164 is I²S, which has two clock signals, BCLK (bit clock) and LRCK (left/right clock), and six data lines (DI0, DI1, DI2, DO0, DO1, and DO2) are used for data receiving and transmitting. One data line contains two channels. Because only one BCLK and LRCK, only I²S encoder or decoder can be enabled at the same time unless the connected DAC and ADC CODEC has the same BCLK and LRCK. The BCLK in master mode is divided from system clock and the clock period and high/low duration meets the I²S spec (±10%). The high/low duty of BCLK is configured by control register and the value infers the sampling rate.

6.17.3 The Basics of I²S Bus

Both master and slave modes of I²S are supported by the I²S interfaces of the WT59F164. Master mode means BCLK and LRCK are provided by the RM5001 as shown in Fig. 1(a). On the contrary, slave mode means BCLK and LRCK are provided by the I²S codecs as depicted in Fig. 1(b).

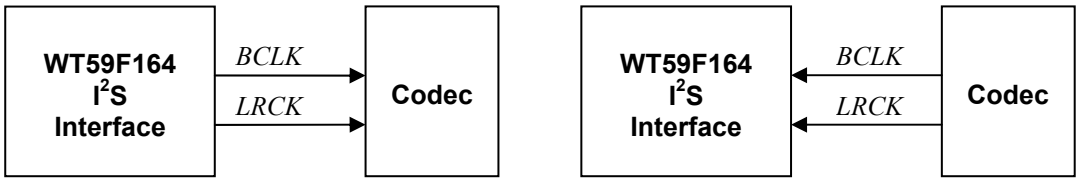


Fig. 1 (a) Master mode (b) Slave mode

Figure 2 indicates the basic waveform of I²S. Note that LRCK is generated at the negative edges of BCLK with the ratios 1/64. Data lines are transited at the negative edges of BCLK, and are sampled at the positive edges of BCLK by codecs in case of playback or by WT59F164 in case of recording.

For the I²S DAC controller, the audio data is transformed from the parallel format to the serial format before transmitted. Then, the bit data is shifted out one by one with the MSB first via DOUT signal. In the same manner that the audio data is transformed from the coming serial format to the parallel format for an I²S ADC controller.

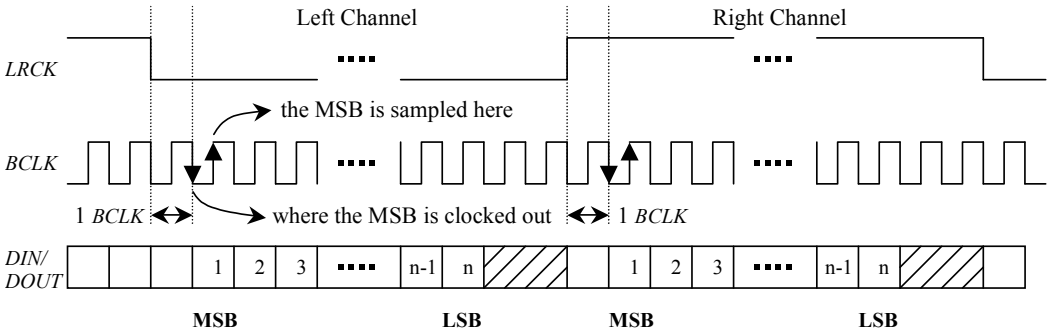


Fig. 2 The basic timing diagram of the I²S interface

6.17.4 Left Justified Mode

In the left justified mode of the I²S DAC controller, the MSB data bit is clocked out by the WT59F164 at the negative edge of BCLK which is aligned to the transition of LRCK. In the left justified mode of I²S ADC controllers, the MSB data bit is clocked out by codecs and sampled by the WT59F164 at the first positive edge of BCLK which follows a LRCK transition. LRCK is high during left channel transmission and low during right channel transmission in the left justified mode. Figure 3 shows all of these.

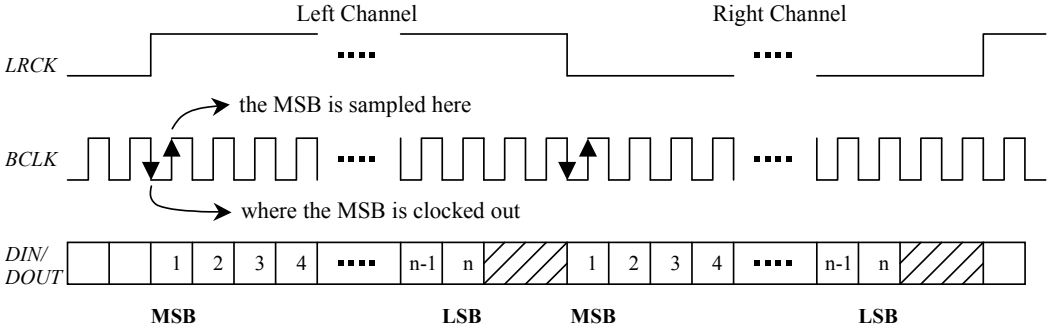


Fig. 3 Left justified mode timing diagram of the I²S interface

6.17.5 I²S mode

In the I²S mode of the I2S DAC controller, the MSB data bit is clocked out by WT59F164 at the first negative edge of BCLK which follows a LRCK transition. In the I²S mode of I²S ADC controllers, the MSB data bit is clocked out by codecs and sampled by the WT59F164 at the second positive edge of BCLK which follows a LRCK transition. LRCK is low during left channel transmission and high during right channel transmission in the I²S mode. Figure 4 indicates all of these.

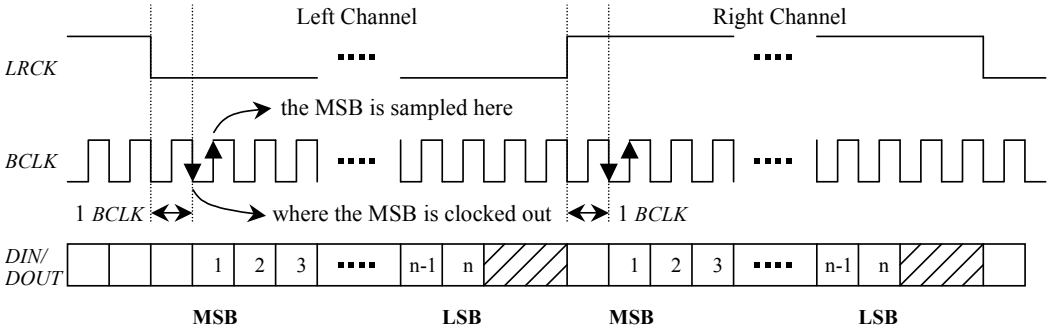


Fig. 4 I^2S mode timing diagram of I^2S interface

6.17.6 I^2S Clock Generation

The I^2S bit clock is divided from system clock in master mode and the relationship of clock high/low duty and sampling rate is described as below:

Ideal bit clock rate = (sampling rate) * (f_{BCLK} / f_{LRCK})

Bit clock rate = (Main clock)/((Clock high duty+1)+(Clock low duty+1))

Table 1

Main clock	Sampling rate	Clock high duty setting	Clock low duty setting	f_{BCLK} / f_{LRCK}	Bit clock rate	Ideal bit clock
18.432 MHz	48k	5	5	32	1536k	1536k
18.432 MHz	48k	3	3	48	2304k	2304k
18.432 MHz	48k	2	2	64	3072k	3072k
24.576 MHz	48k	7	7	32	1536k	1536k
24.576 MHz	48k	5	4	48	2234k	2304k
24.576 MHz	48k	3	3	64	3072k	3072k

Table 2 system clock = 24 MHz (assume $f_{BCLK} = 64*f_{LRCK}$)

Sampling rate	Clock high duty	Clock low duty	Bit clock rate	Ideal bit clock
8k	22	22	521.74k	512k
11.025k	16	16	705.88k	705.6k
12k	15	15	750k	768k
16k	11	11	1000k	1024k
22.025k	8	7	1411.76k	1411.2k
24k	7	7	1500k	1536k
32k	5	5	2000k	2048k
44.1k	3	3	3000k	2822.4k
48k	3	3	3000k	3072k
88.2k	1	1	6000k	5644.8k
96k	1	1	6000k	6144k
192k	0	0	12000k	12288k

Table 3 system clock = 12 MHz (assume f_{BCLK} = 64* f_{LRCK})

Sampling rate	Clock high duty	Clock low duty	Bit clock rate	Ideal bit clock
8k	11	10	521.74k	512k
11.025k	8	7	705.88k	705.6k
12k	7	7	750k	768k
16k	5	5	1000k	1024k
22.025k	4	3	1411.76k	1411.2k
24k	3	3	1500k	1536k
32k	2	2	2000k	2048k
44.1k	1	1	3000k	2822.4k
48k	1	1	3000k	3072k
88.2k	0	0	6000k	5644.8k
96k	0	0	6000k	6144k

6.17.7 Special Register

Register Name	Address	Reset Default (Hex)	Description
I^2S Serial Interface Register (I^2S) 0x0020_6C00~0x0020_6FFF			
I2S_CLK_CFG	0x0020_6C00	0x0000_2851	I^2S BCLK setting
I2S_CFG	0x0020_6C04	0x0000_0000	I^2S data length setting
I2S_CTRL	0x0020_6C08	0x0000_0000	I^2S control
I2S_TX_STAT	0x0020_6C0C	0x0050_5050	I^2S transmit status
I2S_RX_STAT	0x0020_6C10	0x0010_1010	I^2S receive status
I2S_TX0_BUF	0x0020_6C20		I^2S TX0 data buffer
I2S_TX1_BUF	0x0020_6C24		I^2S TX1 data buffer
I2S_TX2_BUF	0x0020_6C28		I^2S TX2 data buffer
I2S_RX0_BUF	0x0020_6C30		I^2S RX0 data buffer
I2S_RX1_BUF	0x0020_6C34		I^2S RX1 data buffer
I2S_RX2_BUF	0x0020_6C38		I^2S RX2 data buffer

I^2S Clock Control Register I^2S_CLK_CFG (Address: 0x0020_6C00) Reset Value: 0x0000_2851

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved						BCLK_LOW_DUTY[6:5]	
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	BCLK_LOW_DUTY[4:0]					BCLK_HIGH_DUTY[6:4]		

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	BCLK_HIGH_DUTY[3:0]				BCLK_RATE[1:0]		LJ_MODE	MASTER_SLAVE

Bit Number	Bit Mnemonic	Description
31-18	Reserved	-
17-11	BCLK_LOW_DUTY[6:0]	BCLK low level duty setting BCLK clock = system clock ((BCLK_LOW_DUTY[6:0]+1)+(BCLK_HIGH_DUTY[6:0]+1))
10-4	BCLK_HIGH_DUTY[6:0]	BCLK high level duty setting BCLK clock = system clock ((BCLK_LOW_DUTY[6:0]+1)+(BCLK_HIGH_DUTY[6:0]+1))
3-2	BCLK_RATE[1:0]	BCLK/ LRCK rate setting (f_{BCLK} /f_{LRCK}) 00: 32 (default) 01: 32 10: 48 11: 64
1	LJ_MODE	Left justified mode setting 1: Left Justified mode 0: I^2S mode (default)
0	MASTER_SLAVE	I^2S Master/Slave mode setting 1: I^2S Master mode (Master) (default) 0: I^2S Slave mode (Slave)

-: unimplemented.

I^2S Setting Register I2S_CFG (Address: 0x0020_6C04) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				RX2_THRESHOLD[1:0]		RX2_BLEN[1:0]	
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	RX1_THRESHOLD[1:0]		RX1_BLEN[1:0]		RX0_THRESHOLD[1:0]		RX0_BLEN[1:0]	
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				TX2_THRESHOLD[1:0]		TX2_BLEN[1:0]	
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	TX1_THRESHOLD[1:0]		TX1_BLEN[1:0]		TX0_THRESHOLD[1:0]		TX0_BLEN[1:0]	

Bit Number	Bit Mnemonic	Description
31-28	Reserved	-
27-26	RX2_THRESHOLD[1:0]	Generate INT/DMA when there are n words received in the FIFO (RX2 channel) 00: 1 word (default) 01: 2 words 10: 3 words 11: 4 words

Bit Number	Bit Mnemonic	Description
25-24	RX2_BLEN[1:0]	Number of bits of audio data (RX2 channel) 00: 16-bit (default) 01: 16-bit 10: 24-bit 11: 32-bit
23-22	RX1_THRESHOLD[1:0]	Generate INT/DMA when there are n words received in the FIFO (RX1 channel) 00: 1 word (default) 01: 2 words 10: 3 words 11: 4 words
21-20	RX1_BLEN[1:0]	Number of bits of audio data (RX1 channel) 00: 16-bit (default) 01: 16-bit 10: 24-bit 11: 32-bit
19-18	RX0_THRESHOLD[1:0]	Generate interrupt/DMA when there are n words received in the FIFO (RX0 channel) 00: 1 word (default) 01: 2 words 10: 3 words 11: 4 words
17-16	RX0_BLEN[1:0]	Number of bits of audio data (RX0 channel) 00: 16-bit (default) 01: 16-bit 10: 24-bit 11: 32-bit
15-12	Reserved	-
11-10	TX2_THRESHOLD[1:0]	Generate INT/DMA when there are n words free space in the FIFO (TX2 channel) 00: 1 word (default) 01: 2 words 10: 3 words 11: 4 words
9-8	TX2_BLEN[1:0]	Number of bits of audio data (TX2 channel) 00: 16-bit (default) 01: 16-bit 10: 24-bit 11: 32-bit
7-6	TX1_THRESHOLD[1:0]	Generate INT/DMA when there are n words free space in the FIFO (TX1 channel) 00: 1 word (default) 01: 2 words 10: 3 words 11: 4 words
5-4	TX1_BLEN[1:0]	Number of bits of audio data (TX1 channel) 00: 16-bit (default) 01: 16-bit 10: 24-bit 11: 32-bit

Bit Number	Bit Mnemonic	Description
3-2	TX0_THRESHOLD[1:0]	Generate INT/DMA when there are n words free space in the FIFO (TX0 channel) 00: 1 word (default) 01: 2 words 10: 3 words 11: 4 words
1-0	TX0_BLEN[1:0]	Number of bits of audio data (TX0 channel) 00: 16-bit (default) 01: 16-bit 10: 24-bit 11: 32-bit

-: unimplemented.

I^2S Control Register I2S_CTRL (Address: 0x0020_6C08) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	W	R/W	R/W	R/W
Name	Reserved				RX2_FLUSH	RX2_INT_EN	RX2_DMA_EN	RX2_EN
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	W	R/W	R/W	R/W	W	R/W	R/W	R/W
Name	RX1_FLUSH	RX1_INT_EN	RX1_DMA_EN	RX1_EN	RX0_FLUSH	RX0_INT_EN	RX0_DMA_EN	RX0_EN
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	W	R/W	R/W	R/W
Name	Reserved				TX2_FLUSH	TX2_INT_EN	TX2_DMA_EN	TX2_EN
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	R/W	R/W	R/W	W	R/W	R/W	R/W
Name	TX1_FLUSH	TX1_INT_EN	TX1_DMA_EN	TX1_EN	TX0_FLUSH	TX0_INT_EN	TX0_DMA_EN	TX0_EN

Bit Number	Bit Mnemonic	Description
31-28	Reserved	-
27	RX2_FLUSH	I^2S RX2 channel FIFO buffer clear setting 1: Write 1 to flush FIFO (RX2 channel)
26	RX2_INT_EN	I^2S RX2 channel interrupt enable setting 1: Enable interrupt (RX1 channel)
25	RX2_DMA_EN	I^2S RX2 channel DMA enable setting 1: Enable DMA (RX2 channel)
24	RX2_EN	I^2S RX2 channel enable setting 1: Enable I^2S (RX2 channel)
23	RX1_FLUSH	I^2S RX1 channel FIFO buffer clear setting 1: Write 1 to flush FIFO (RX1 channel)
22	RX1_INT_EN	I^2S RX1 channel interrupt enable setting 1: Enable Interrupt (RX1 channel)
21	RX1_DMA_EN	I^2S RX1 channel DMA enable setting 1: Enable DMA (RX1 channel)
20	RX1_EN	I^2S RX1 channel enable setting 1: Enable I^2S (RX1 channel)
19	RX0_FLUSH	I^2S RX0 channel FIFO buffer clear setting 1: Write 1 to flush FIFO (RX0 channel)

Bit Number	Bit Mnemonic	Description
18	RX0_INT_EN	I²S RX0 channel interrupt enable setting 1: Enable interrupt (RX0 channel)
17	RX0_DMA_EN	I²S RX0 channel DMA enable setting 1: Enable DMA (RX0 channel)
16	RX0_EN	I²S RX0 channel enable setting 1: Enable I²S (RX0 channel)
15-12	Reserved	-
11	TX2_FLUSH	I²S TX2 channel FIFO buffer clear setting 1: Write 1 to flush FIFO (TX2 channel)
10	TX2_INT_EN	I²S TX2 channel interrupt enable setting 1: Enable interrupt (TX2 channel)
9	TX2_DMA_EN	I²S TX2 channel DMA enable setting 1: Enable DMA (TX2 channel)
8	TX2_EN	I²S TX2 channel enable setting 1: Enable I²S (TX2 channel)
7	TX1_FLUSH	I²S TX1 channel FIFO buffer clear setting 1: Write 1 to flush FIFO (TX1 channel)
6	TX1_INT_EN	I²S TX1 channel interrupt enable setting 1: Enable Interrupt (TX1 channel)
5	TX1_DMA_EN	I²S TX1 channel DMA enable setting 1: Enable DMA (TX1 channel)
4	TX1_EN	I²S TX1 channel enable setting 1: Enable I²S (TX1 channel)
3	TX0_FLUSH	I²S TX0 channel FIFO buffer clear setting 1: Write 1 to flush FIFO (TX0 channel)
2	TX0_INT_EN	I²S TX0 channel interrupt enable setting 1: Enable Interrupt (TX0 channel)
1	TX0_DMA_EN	I²S TX0 channel DMA enable setting 1: Enable DMA (TX0 channel)
0	TX0_EN	I²S TX0 channel enable setting 1: Enable I²S (TX0 channel)

-: unimplemented.

I²S Transmit Status Register I2S_TX_STAT (Address: 0x0020_6C0C) Reset Value: 0x0050_5050

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	R/W	R	R	R	R	R	R	R
Name	TX2_ERROR	TX2_EMPTY	TX2_FULL	TX2_INT	TX2_CNT[3:0]			
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R	R	R	R	R	R	R
Name	TX1_ERROR	TX1_EMPTY	TX1_FULL	TX1_INT	TX1_CNT[3:0]			
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R	R	R	R	R	R	R
Name	TX0_ERROR	TX0_EMPTY	TX0_FULL	TX0_INT	TX0_CNT[3:0]			

Bit Number	Bit Mnemonic	Description
31-24	Reserved	-
23	TX2_ERROR	I^2S TX2 channel error status 1: An error (OV/UV) occurred (TX2 channel). Write 1 to clear.
22	TX2_EMPTY	I^2S TX2 channel transmit FIFO buffer empty status 1: TX2 channel transmit FIFO buffer is empty
21	TX2_FULL	I^2S TX2 channel transmit FIFO buffer full status 1: TX2 channel transmit FIFO buffer is full
20	TX2_INT	I^2S TX2 channel interrupt flag 1: I^2S TX2 channel interrupt occurred
19-16	TX2_CNT[3:0]	# of words currently in the FIFO (TX2 channel)
15	TX1_ERROR	I^2S TX1 channel error status 1: An error (OV/UV) occurred (TX1 channel). Write 1 to clear
14	TX1_EMPTY	I^2S TX1 channel transmit FIFO buffer empty status 1: TX1 channel transmit FIFO buffer is empty
13	TX1_FULL	I^2S TX1 channel transmit FIFO buffer full status 1: TX1 channel transmit FIFO buffer is full
12	TX1_INT	I^2S TX1 channel interrupt flag 1: I^2S TX1 channel interrupt occurred
11-8	TX1_CNT[3:0]	# of words currently in the FIFO (TX1 channel)
7	TX0_ERROR	I^2S TX0 channel error status 1: An error (OV/UV) occurred (TX1 channel). Write 1 to clear
6	TX0_EMPTY	I^2S TX0 channel transmit FIFO buffer empty status 1: TX0 channel transmit FIFO buffer is empty
5	TX0_FULL	I^2S TX0 channel transmit FIFO buffer full status 1: TX0 channel transmit FIFO Buffer is full
4	TX0_INT	I^2S TX0 channel interrupt flag 1: I^2S TX0 channel interrupt occurred
3-0	TX0_CNT[3:0]	# of words currently in the FIFO (TX0 channel)

-: unimplemented.

I^2S Receive Status Register I2S_RX_STAT (Address: 0x0020_6C10) Reset Value: 0x0010_1010

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	R/W	R	R	R	R	R	R	R
Name	RX2_ERROR	RX2_EMPTY	RX2_FULL	RX2_INT	RX2_CNT[3:0]			
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R	R	R	R	R	R	R
Name	RX1_ERROR	RX1_EMPTY	RX1_FULL	RX1_INT	RX1_CNT[3:0]			
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R	R	R	R	R	R	R
Name	RX0_ERROR	RX0_EMPTY	RX0_FULL	RX0_INT	RX0_CNT[3:0]			

Bit Number	Bit Mnemonic	Description
31-24	Reserved	-
23	RX2_ERROR	I^2S RX2 channel error status 1: An error (OV/UV) occurred (RX2 channel)
22	RX2_EMPTY	I^2S RX2 channel receive FIFO buffer empty status 1: RX2 channel receive FIFO buffer is empty
21	RX2_FULL	I^2S RX2 channel receive FIFO buffer full status 1: RX2 channel receive FIFO buffer is full
20	RX2_INT	I^2S RX2 channel interrupt flag 1: I^2S RX2 channel interrupt
19-16	RX2_CNT[3:0]	# of words currently in the FIFO (TX0 channel)
15	RX1_ERROR	I^2S RX1 channel error status 1: An error (OV/UV) occurred (RX1 channel). Write 1 to clear
14	RX1_EMPTY	I^2S RX1 channel receive FIFO buffer empty status 1: RX1 channel receive FIFO buffer is empty
13	RX1_FULL	I^2S RX1 channel receive FIFO buffer full status 1: RX1 channel receive FIFO buffer is full
12	RX1_INT	I^2S RX1 channel interrupt flag 1: I^2S RX1 channel interrupt
11-8	RX1_CNT[3:0]	# of words currently in the FIFO
7	RX0_ERROR	I^2S RX0 channel error status 1: an error (OV/UV) occurred (RX0 channel). Write 1 to clear.
6	RX0_EMPTY	I^2S RX0 channel receive FIFO buffer empty status 1: RX0 channel receive FIFO buffer is empty
5	RX0_FULL	I^2S RX0 channel receive FIFO buffer full status 1: RX0 channel receive FIFO buffer is full
4	RX0_INT	I^2S RX0 channel interrupt flag 1: I^2S RX0 channel interrupt
3-0	RX0_CNT[3:0]	# of words currently in the FIFO

-: unimplemented.

I^2S Transmit Data Register 0 I2S_TX0_BUF
(Address: 0x0020_6C20) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	W	W	W	W	W	W	W	W
Name	TX0_FIFO[31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	W	W	W	W	W	W	W	W
Name	TX0_FIFO[23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	TX0_FIFO[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	TX0_FIFO[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	TX0_FIFO[31-0]	I²S TX FIFO (TX0 channel) 16-bit data: [31:16] is right channel, [15:0] is left channel 24-bit data: [23:0] is right channel or left channel (left channel goes first) 32-bit data: [31:0] is right channel or left channel (left channel goes first)

-: unimplemented.

I²S Transmit Data Register 1 I2S_TX1_BUF
(Address: 0x0020_6C24) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	W	W	W	W	W	W	W	W
Name	TX1_FIFO[31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	W	W	W	W	W	W	W	W
Name	TX1_FIFO[23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	TX1_FIFO[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	TX1_FIFO[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	TX1_FIFO[31-0]	I²S TX FIFO (TX1 channel) 16-bit data: [31:16] is right channel, [15:0] is left channel 24-bit data: [23:0] is right channel or left channel (left channel goes first) 32-bit data: [31:0] is right channel or left channel (left channel goes first)

-: unimplemented.

I²S Transmit Data Register 2 I2S_TX2_BUF
(Address: 0x0020_6C28) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	W	W	W	W	W	W	W	W
Name	TX2_FIFO[31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	W	W	W	W	W	W	W	W
Name	TX2_FIFO[23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	TX2_FIFO[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	TX2_FIFO[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	TX2_FIFO[31-0]	I^2S TX FIFO (TX2 channel) 16-bit data: [31:16] is right channel, and [15:0] is left channel 24-bit data: [23:0] is right channel or left channel (left channel goes first) 32-bit data: [31:0] is right channel or left channel (left channel goes first)

-: unimplemented.

I^2S Receive Data Register 0 I2S_RX0_BUF
(Address: 0x0020_6C30) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	W	W	W	W	W	W	W	W
Name	RX0_FIFO[31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	W	W	W	W	W	W	W	W
Name	RX0_FIFO[23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	RX0_FIFO[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	RX0_FIFO[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	RX0_FIFO[31-0]	I^2S RX FIFO (RX0 channel) 16-bit Data: [31:16] is right channel, [15:0] is left channel 24-bit Data: [23:0] is right channel or left channel (left channel goes first) 32-bit data: [31:0 is right channel or left channel (left channel goes first)

-: unimplemented.

I^2S Receive Data Register 1 I2S_RX1_BUF
(Address: 0x0020_6C34) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	W	W	W	W	W	W	W	W
Name	RX1_FIFO[31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	W	W	W	W	W	W	W	W
Name	RX1_FIFO[23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	RX1_FIFO[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	RX1_FIFO[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	RX1_FIFO[31-0]	I^2S RX1 channel receive data register 16-bit data: [31:16] is right channel, [15:0] is left channel 24-bit data: [23:0] is right channel or left channel (left channel goes first) 32-bit data: [31:0] is right channel or left channel (left channel goes first)

-: unimplemented.

I^2S Receive Data Register 2 I2S_RX2_BUF
(Address: 0x0020_6C38) **Reset Value:**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	W	W	W	W	W	W	W	W
Name	RX2_FIFO[31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	W	W	W	W	W	W	W	W
Name	RX2_FIFO[23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	RX2_FIFO[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	RX2_FIFO[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	RX2_FIFO[31-0]	I^2S RX2 channel receive data register 16-bit data: [31:16] is right channel, [15:0] is left channel 24-bit data: [23:0] is right channel or left channel (left channel goes first) 32-bit data: [31:0] is right channel or left channel (left channel goes first)

-: unimplemented.

Note: When sampling rate is changed (high low duty is changed) in master mode, or master slave mode configuration is changed, please disable I^2S enable register and enable it after new setting is configured.

6.18 DMA Controller

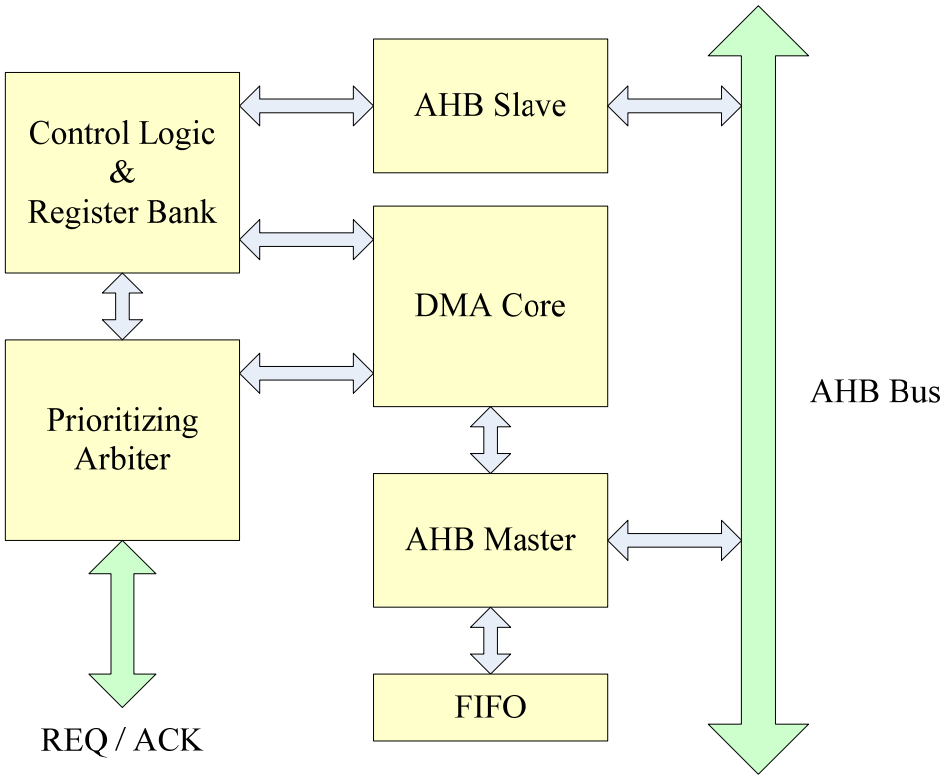
6.18.1 Features

- Compliant with AMBA V2.0
  - AHB slave interface for DMA controller configuration
  - AHB master interface for data transfers
  - Transfer Type: Single mode
  - Configurable 32-bits (word), 16-bits (half-word), 8-bits (byte) wide data transaction
- 7 configurable DMA channels
  - Support memory-to-peripheral transfer
  - Support peripheral-to-memory transfer
  - Support peripheral-to-peripheral transfer
- Peripheral supported:
  - UARTs (Tx/Rx)
  - Timers
  - I^2Cs (Tx/Rx)
  - ADC
  - I^2S (Tx /Rx)
  - USB (EP7_Tx /EP8_Rx)
  - SPI (Tx/Rx)
- Arbitration scheme
  - Round-robin arbitration
  - Configurable 4 level priorities
- Circular mode

6.18.2 Functional Description

The Direct Memory Access Controller can enhance the system performance and reduce the processor-interrupt generation. There are 7 configurable channels for memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers. Each channel is connected to dedicated hardware handshake signal.

6.18.3 Block Diagram



6.18.4 AHB Master Interface

The system can transfer data on AHB bus through this AHB master interface.

6.18.5 AHB Slave Interface

The system can configure the DMA controller or access the devices on AHB bus through this AHB slave interface.

6.18.6 FIFO Buffer

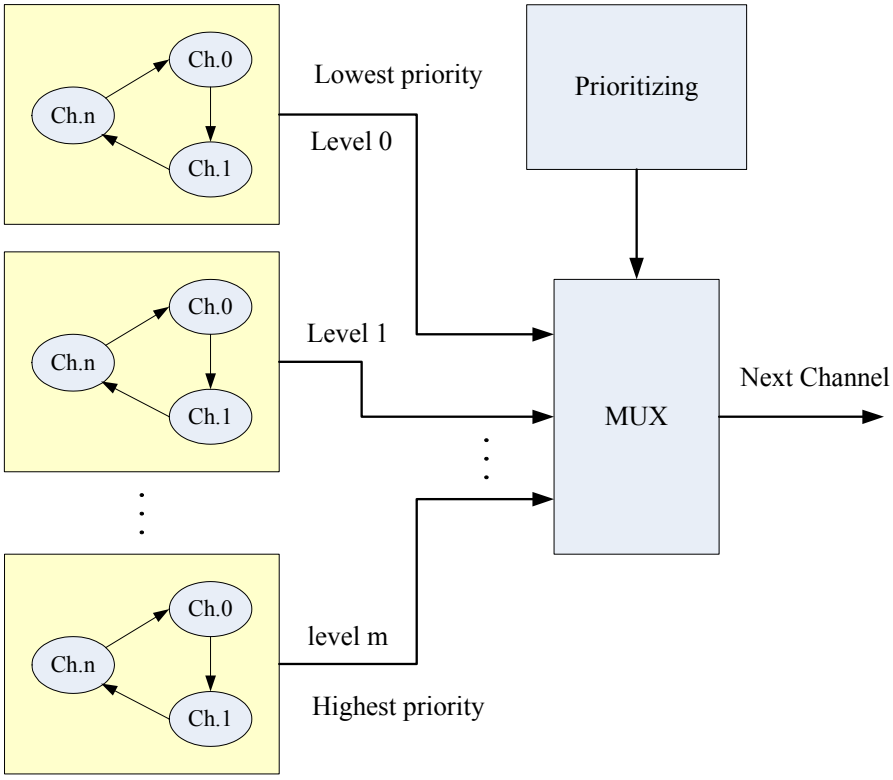
The FIFO buffer provides the data transfer buffer between the source and the destination.

6.18.7 DMA Core

The DMA data transfer engine.

6.18.8 Prioritizing Arbiter

To handle hardware handshake signals to start DMA transfer and configure up to 7-channels. They can group the round-robin arbitration scheme into 4 priority levels.



6.18.9 Control Logic & Register Bank

Register set from AHB slave interface and generate some control logic for DMA transfer.

6.18.10 DMA Interrupt Enable, Interrupt & Busy Status Special Register

Register Name	Address	Reset Default (Hex)	Description
Direct Memory Access Register (DMA)	**0x0030_0000~0x0030_03FF**		
DMA_BUSY_STATUS	0x0030_0004		DMA is busy
DMA_INT_STATUS	0x0030_0008		DMA interrupt status
DMA_INT_CLR	0x0030_000C	0x0000_0000	DMA interrupt clear

DMA Busy Status Register DMA_BUSY_STATUS (Address: 0x0030_0004) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R	R	R	R	R	R	R
Name	Reserved	DMA_BUSY6	DMA_BUSY5	DMA_BUSY4	DMA_BUSY3	DMA_BUSY2	DMA_BUSY1	DMA_BUSY0

Bit Number	Bit Mnemonic	Description
31-7	Reserved	-
6	DMA_BUSY6	DMA channel 6 busy status 1: DMA channel 6 is busy 0: DMA channel 6 is available
5	DMA_BUSY5	DMA channel 5 busy status 1: DMA channel 5 is busy 0: DMA channel 5 is available
4	DMA_BUSY4	DMA channel 4 busy status 1: DMA channel 4 is busy 0: DMA channel 4 is available
3	DMA_BUSY3	DMA channel 3 busy status 1: DMA channel 3 is busy 0: DMA channel 3 is available
2	DMA_BUSY2	DMA channel 2 busy status 1: DMA channel 2 is busy 0: DMA channel 2 is available
1	DMA_BUSY1	DMA channel 1 busy status 1: DMA channel 1 is busy 0: DMA channel 1 is available
0	DMA_BUSY0	DMA channel 0 busy status 1: DMA channel 0 is busy 0: DMA channel 0 is available

-: unimplemented.

DMA Interrupt Flag Register DMA_INT_STATUS (Address: 0x0030_0008) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	R	R	R
Name	Reserved					HALF_INT6	TOTAL_INT6	DMA_INT6
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	R	R	R	-	R	R	R
Name	Reserved	HALF_INT5	TOTAL_INT5	DMA_INT5	Reserved	HALF_INT4	TOTAL_INT4	DMA_INT4
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	R	R	R	-	R	R	R
Name	Reserved	HALF_INT3	TOTAL_INT3	DMA_INT3	Reserved	HALF_INT2	TOTAL_INT2	DMA_INT2
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R	R	R	-	R	R	R
Name	Reserved	HALF_INT1	TOTAL_INT1	DMA_INT1	Reserved	HALF_INT0	TOTAL_INT0	DMA_INT0

Bit Number	Bit Mnemonic	Description
31-27	Reserved	-
26	HALF_INT6	DMA channel 6 half interrupt flag 1: A half interrupt event on DMA channel 6 0: No half interrupt event on DMA channel 6
25	TOTAL_INT6	DMA channel 6 total interrupt flag 1: A total interrupt event on DMA channel 6 0: No total interrupt event on DMA channel 6
24	DMA_INT6	DMA channel 6 interrupt flag 1: A half or total interrupt event on DMA channel 6 0: No half or total interrupt event on DMA channel 6
23	Reserved	-
22	HALF_INT5	DMA channel 5 half interrupt flag 1: A half interrupt event on DMA channel 5 0: No half interrupt event on DMA channel 5
21	TOTAL_INT5	DMA channel 5 total interrupt flag 1: A total interrupt event on DMA channel 5 0: No total interrupt event on DMA channel 5
20	DMA_INT5	DMA channel 5 interrupt flag 1: A half or total interrupt event on DMA channel 5 0: No half or total interrupt event on DMA channel 5
19	Reserved	-
18	HALF_INT4	DMA channel 4 half interrupt flag 1: A half interrupt event on DMA channel 4 0: No half interrupt event on DMA channel 4
17	TOTAL_INT4	DMA channel 4 total interrupt flag 1: A total interrupt event on DMA channel 4 0: No total interrupt event on DMA channel 4
16	DMA_INT4	DMA channel 4 interrupt flag 1: A half or total interrupt event on DMA channel 4 0: No half or total interrupt event on DMA channel 4
15	Reserved	-
14	HALF_INT3	DMA channel 3 half interrupt flag 1: A half interrupt event on DMA channel 3 0: No half interrupt event on DMA channel 3
13	TOTAL_INT3	DMA channel 3 total interrupt flag 1: A total interrupt event on DMA channel 3 0: No total interrupt event on DMA channel 3
12	DMA_INT3	DMA channel 3 interrupt flag 1: A half or total interrupt event on DMA channel 3 0: No half or total interrupt event on DMA channel 3
11	Reserved	-
10	HALF_INT2	DMA channel 2 half interrupt flag 1: A half interrupt event on DMA channel 2 0: No half interrupt event on DMA channel 2
9	TOTAL_INT2	DMA channel 2 total interrupt flag 1: A total interrupt event on DMA channel 2 0: No total interrupt event on DMA channel 2
8	DMA_INT2	DMA channel 2 interrupt flag 1: A half or total interrupt event on DMA channel 2 0: No half or total interrupt event on DMA channel 2
7	Reserved	-

Bit Number	Bit Mnemonic	Description
6	HALF_INT1	DMA channel 1 half interrupt flag 1: A half interrupt event on DMA channel 1 0: No half interrupt event on DMA channel 1
5	TOTAL_INT1	DMA channel 1 total interrupt flag 1: A total interrupt event on DMA channel 1 0: No total interrupt event on DMA channel 1
4	DMA_INT1	DMA channel 1 interrupt flag 1: A half or total interrupt event on DMA channel 1 0: No half or total interrupt event on DMA channel 1
3	Reserved	-
2	HALF_INT0	DMA channel 0 half interrupt flag 1: A half interrupt event on DMA channel 0 0: No half interrupt event on DMA channel 0
1	TOTAL_INT0	DMA channel 0 total interrupt flag 1: A total interrupt event on DMA channel 0 0: No total interrupt event on DMA channel 0
0	DMA_INT0	DMA channel 0 Interrupt Flag 1: A half or total interrupt event on DMA channel 0 0: No half or total interrupt event on DMA channel 0

-: unimplemented.

DMA Interrupt Clear Register DMA_INT_CLR (Address: 0x0030_000C) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	W	W	W
Name	Reserved					CLR_HALF_INT6	CLR_TOTAL_INT6	CLR_INT6
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	W	W	W	-	W	W	W
Name	Reserved	CLR_HALF_INT5	CLR_TOTAL_INT5	CLR_INT5	Reserved	CLR_HALF_INT4	CLR_TOTAL_INT4	CLR_INT4
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	W	W	W	-	W	W	W
Name	Reserved	CLR_HALF_INT3	CLR_TOTAL_INT3	CLR_INT3	Reserved	CLR_HALF_INT2	CLR_TOTAL_INT2	CLR_INT2
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	W	W	W	-	W	W	W
Name	Reserved	CLR_HALF_INT1	CLR_TOTAL_INT1	CLR_INT1	Reserved	CLR_HALF_INT0	CLR_TOTAL_INT0	CLR_INT0

Bit Number	Bit Mnemonic	Description
31-27	Reserved	-
26	CLR_HALF_INT6	DMA channel 6 half interrupt clear setting 1: Clear HALF_INT6 interrupt flag
25	CLR_TOTAL_INT6	DMA channel 6 Total interrupt clear setting 1: Clear TOTAL_INT6 interrupt flag
24	CLR_INT6	DMA channel 6 interrupt clear setting 1: Clear DMA channel 6 DMA_INT6, TOTAL_INT6 and HALF_INT6 interrupt flag
23	Reserved	Reserved
22	CLR_HALF_INT5	DMA channel 5 half interrupt clear setting 1: Clear HALF_INT5 interrupt flag
21	CLR_TOTAL_INT5	DMA channel 5 total interrupt clear setting 1: Clear TOTAL_INT5 interrupt flag

Bit Number	Bit Mnemonic	Description
20	CLR_INT5	DMA channel 5 interrupt clear setting 1: Clear DMA channel 5 DMA_INT5, TOTAL_INT5 and HALF_INT5 interrupt flag
19	Reserved	Reserved
18	CLR_HALF_INT4	DMA channel 4 half interrupt clear setting 1: Clear HALF_INT4 interrupt flag
17	CLR_TOTAL_INT4	DMA channel 4 total interrupt clear setting 1: Clear TOTAL_INT4 interrupt flag
16	CLR_INT4	DMA channel 4 interrupt clear setting 1: Clear DMA channel 4 DMA_INT4, TOTAL_INT4 and HALF_INT4 interrupt flag
15	Reserved	Reserved
14	CLR_HALF_INT3	DMA channel 3 half interrupt clear setting 1: Clear HALF_INT3 interrupt flag
13	CLR_TOTAL_INT3	DMA channel 3 total interrupt clear setting 1: Clear TOTAL_INT3 interrupt flag
12	CLR_INT3	DMA channel 3 interrupt clear setting 1: Clear DMA channel 3 DMA_INT3, TOTAL_INT3 and HALF_INT3 interrupt flag
11	Reserved	Reserved
10	CLR_HALF_INT2	DMA channel 2 half interrupt clear setting 1: Clear HALF_INT2 interrupt flag
9	CLR_TOTAL_INT2	DMA channel 2 Total Interrupt Clear setting 1: Clear TOTAL_INT2 interrupt flag
8	CLR_INT2	DMA channel 2 interrupt clear setting 1: Clear DMA channel 2 DMA_INT2, TOTAL_INT2 and HALF_INT2 interrupt flag
7	Reserved	Reserved
6	CLR_HALF_INT1	DMA channel 1 half interrupt clear setting 1: Clear HALF_INT1 interrupt flag
5	CLR_TOTAL_INT1	DMA channel 1 total interrupt clear setting 1: Clear TOTAL_INT1 interrupt flag
4	CLR_INT1	DMA channel 1 interrupt clear setting 1: Clear DMA channel 1 DMA_INT1, TOTAL_INT1 and HALF_INT1 interrupt flag
3	Reserved	Reserved
2	CLR_HALF_INT0	DMA channel 0 half interrupt clear setting 1: Clear HALF_INT0 interrupt flag
1	CLR_TOTAL_INT0	DMA channel 0 total interrupt clear setting 1: Clear TOTAL_INT0 interrupt flag
0	CLR_INT0	DMA channel 0 interrupt clear setting 1: Clear DMA channel 0 DMA_INT0, TOTAL_INT0 and HALF_INT0 interrupt flag

-: unimplemented.

6.18.11 DMA Channel X Source Address Register

Base Address: 0x0030_0000
X = 0 ~ 6, where X is channel number
Channel X Address index = 0x10 + 0x10 * (channel number X)

Register Name	Address	Reset Default (Hex)	Description
Direct Memory Access Register (DMA) 0x0030_0000~0x0030_03FF			
DMA_SADDR0	0x0030_0010	0x0000_0000	DMA source address 0
DMA_SADDR1	0x0030_0020	0x0000_0000	DMA source address 1
DMA_SADDR2	0x0030_0030	0x0000_0000	DMA source address 2
DMA_SADDR3	0x0030_0040	0x0000_0000	DMA source address 3
DMA_SADDR4	0x0030_0050	0x0000_0000	DMA source address 4
DMA_SADDR5	0x0030_0060	0x0000_0000	DMA source address 5
DMA_SADDR6	0x0030_0070	0x0000_0000	DMA source address 6

DMA Source Address Control Register 0 DMA_SADDR0
(Address: 0x0030_0010) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR0[31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR0[23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR0[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR0[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	DMA_SADDR0[31:0]	DMA channel 0 source address

-: unimplemented.

DMA Source Address Control Register 1 DMA_SADDR1
(Address: 0x0030_0020) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR1 [31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR1[23:16]							

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR1[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR1[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	DMA_SADDR1[31:0]	DMA channel 1 source address

-: unimplemented.

DMA Source Address Control Register 2 DMA_SADDR2
(Address: 0x0030_0030) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR2[31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR2[23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR2[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR2[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	DMA_SADDR2[31:0]	DMA channel 2 source address

-: unimplemented.

DMA Source Address Control Register 3 DMA_SADDR3
(Address: 0x0030_0040) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR3[31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR3[23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR3[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR3[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	DMA_SADDR3[31:0]	DMA channel 3 source address

-: unimplemented.

DMA Source Address Control Register 4 DMA_SADDR4
(Address: 0x0030_0050) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR4[31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR4[23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR4[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR4[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	DMA_SADDR4[31:0]	DMA channel 4 source address

-: unimplemented.

DMA Source Address Control Register 5 DMA_SADDR5
(Address: 0x0030_0060) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR5[31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR5[23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR5[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR5[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	DMA_SADDR5[31:0]	DMA channel 5 source address

-: unimplemented.

DMA Source Address Control Register 6 DMA_SADDR6
(Address: 0x0030_0070) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR6[31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR6[23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR6[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_SADDR6[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	DMA_SADDR6[31:0]	DMA channel 6 source address

-: unimplemented.

6.18.12 DMA Channel X Destination Address Register

Base Address: 0x0030_0000
X = 0 ~ 6, where x is channel number
Channel X Address index: 0x14 + 0x10 * (channel number X)

Register Name	Address	Reset Default (Hex)	Description
Direct Memory Access Register (DMA) 0x0030_0000~0x0030_03FF			
DMA_DADDR0	0x0030_0014	0x0000_0000	DMA destination address 0
DMA_DADDR1	0x0030_0024	0x0000_0000	DMA destination address 1
DMA_DADDR2	0x0030_0034	0x0000_0000	DMA destination address 2
DMA_DADDR3	0x0030_0044	0x0000_0000	DMA destination address 3
DMA_DADDR4	0x0030_0054	0x0000_0000	DMA destination address 4
DMA_DADDR5	0x0030_0064	0x0000_0000	DMA destination address 5
DMA_DADDR6	0x0030_0074	0x0000_0000	DMA destination address 6

DMA Destination Address Control Register 0 DMA_DADDR0
(Address: 0x0030_0014) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR0[31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR0[23:16]							

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR0[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR0[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	DMA_DADDR0[31:0]	DMA channel 0 destination address

-: unimplemented.

DMA Destination Address Control Register 1 DMA_DADDR1
(Address: 0x0030_0024) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR1[31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR1[23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR1[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR1[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	DMA_DADDR1[31:0]	DMA channel 1 destination address

-: unimplemented.

DMA Destination Address Control Register 2 DMA_DADDR2
(Address: 0x0030_0034) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR2[31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR2[23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR2[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR2[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	DMA_DADDR2[31:0]	DMA channel 2 destination address

-: unimplemented.

DMA Destination Address Control Register 3 DMA_DADDR3
(Address: 0x0030_0044) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR3[31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR3[23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR3[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR3[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	DMA_DADDR3[31:0]	DMA channel 3 destination address

-: unimplemented.

DMA Destination Address Control Register 4 DMA_DADDR4
(Address: 0x0030_0054) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR4[31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR4[23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR4[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR4[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	DMA_DADDR4[31:0]	DMA channel 4 destination address

-: unimplemented.

DMA Destination Address Control Register 5 DMA_DADDR5
(Address: 0x0030_0064) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR5[31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR5[23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR5[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR5[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	DMA_DADDR5[31:0]	DMA channel 5 destination address

-: unimplemented.

DMA Destination Address Control Register 6 DMA_DADDR6
(Address: 0x0030_0074) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR6[31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR6[23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR6[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_DADDR6[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	DMA_DADDR6[31:0]	DMA channel 6 destination address

-: unimplemented.

6.18.13 DMA Channel X Number of Data Register

Base Address: 0x0030_0000
X = 0 ~ 6, where X is channel number
DMA Channel X Address index: 0x18 + 0x10 * (channel number X)

Register Name	Address	Reset Default (Hex)	Description
Direct Memory Access Register (DMA)	**0x0030_0000~0x0030_03FF**		
DMA_LENGTH0	0x0030_0018	0x0000_0000	DMA length 0
DMA_LENGTH1	0x0030_0028	0x0000_0000	DMA length 1
DMA_LENGTH2	0x0030_0038	0x0000_0000	DMA length 2
DMA_LENGTH3	0x0030_0048	0x0000_0000	DMA length 3
DMA_LENGTH4	0x0030_0058	0x0000_0000	DMA length 4
DMA_LENGTH5	0x0030_0068	0x0000_0000	DMA length 5
DMA_LENGTH6	0x0030_0078	0x0000_0000	DMA length 6

DMA Data Length Register 0 DMA_LENGTH0 (Address: 0x0030_0018) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	R/W
Name	Reserved							DMA_LENGTH0[8]
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_LENGTH0[7:0]							

Bit Number	Bit Mnemonic	Description
31-9	Reserved	-
8-0	DMA_LENGTH0[8:0]	DMA channel 0 total size transfer length: 1~511 0: DMA transfer stop

-: unimplemented.

DMA Data Length Register 1 DMA_LENGTH1 (Address: 0x0030_0028) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	R/W
Name	Reserved							DMA_LENGTH1[8]
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_LENGTH1[7:0]							

Bit Number	Bit Mnemonic	Description
31-9	Reserved	-
8-0	DMA_LENGTH1[8:0]	DMA channel 1 total size transfer length: 1~511 0: DMA transfer stop

-: unimplemented.

DMA Data Length Register 2 DMA_LENGTH2 (Address: 0x0030_0038) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	R/W
Name	Reserved							DMA_LENGTH2[8]
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_LENGTH2[7:0]							

Bit Number	Bit Mnemonic	Description
31-9	Reserved	-
8-0	DMA_LENGTH2[8:0]	DMA channel 2 total size transfer length 0: DMA transfer stop

-: unimplemented.

DMA Data Length Register 3 DMA_LENGTH3 (Address: 0x0030_0048) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	R/W
Name	Reserved							DMA_LENGTH3[8]
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_LENGTH3[7:0]							

Bit Number	Bit Mnemonic	Description
31-9	Reserved	-
8-0	DMA_LENGTH3[8:0]	DMA channel 3 total size transfer length 0: DMA transfer stop

-: unimplemented.

DMA Data Length Register 4 DMA_LENGTH4 (Address: 0x0030_0058) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	R/W
Name	Reserved							DMA_LENGTH4[8]
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_LENGTH4[7:0]							

Bit Number	Bit Mnemonic	Description
31-9	Reserved	-
8-0	DMA_LENGTH4[8:0]	DMA channel 4 total size transfer length 0: DMA transfer stop

-: unimplemented.

DMA Data Length Register 5 DMA_LENGTH5 (Address: 0x0030_0068) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	R/W
Name	Reserved							DMA_LENGTH5[8]
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_LENGTH5[7:0]							

Bit Number	Bit Mnemonic	Description
31-9	Reserved	-
8-0	DMA_LENGTH5[8:0]	DMA channel 5 total size transfer length 0: DMA transfer stop

-: unimplemented.

DMA Data Length Register 6 DMA_LENGTH6 (Address: 0x0030_0078) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	R/W
Name	Reserved							DMA_LENGTH6[8]
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	DMA_LENGTH6[7:0]							

Bit Number	Bit Mnemonic	Description
31-9	Reserved	-
8-0	DMA_LENGTH6[8:0]	DMA channel 6 total size transfer length 0: DMA transfer stop

-: unimplemented.

6.18.14 DMA Channel X Configuration Register

Base Address: 0x0030_0000
X = 0 ~ 6, where X is DMA channel
DMA channel X Control Register Shift = 0x1C + 0x10 * (X)

Register Name	Address	Reset Default (Hex)	Description
Direct Memory Access Register (DMA) 0x0030_0000~0x0030_03FF			
DMA_CONFIG0	0x0030_001C	0x0000_0000	DMA configuration 0
DMA_CONFIG1	0x0030_002C	0x0000_0000	DMA configuration 1
DMA_CONFIG2	0x0030_003C	0x0000_0000	DMA configuration 2
DMA_CONFIG3	0x0030_004C	0x0000_0000	DMA configuration 3
DMA_CONFIG4	0x0030_005C	0x0000_0000	DMA configuration 4
DMA_CONFIG5	0x0030_006C	0x0000_0000	DMA configuration 5
DMA_CONFIG6	0x0030_007C	0x0000_0000	DMA configuration 6

DMA Configuration Register 0 DMA_CONFIG0 (Address: 0x0030_001C) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
Name	SRC_WIDTH[1:0]		DST_WIDTH[1:0]		Reserved	CIRC_MODE0	PRI_CH0[1:0]	
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
Name	SRC_ADR0_CTL[1:0]		DST_ADR0_CTL[1:0]		Reserved	DMA_HALF_INT0_EN	DMA_TOTAL_INT0_EN	DMA_CHEN0

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-14	SRC_WIDTH[1:0]	DMA channel 0 source data width configuration 00: 8-bits (default) 01: 16-bits 10: 32-bits 11: Reserved
13-12	DST_WIDTH[1:0]	DMA channel 0 destination data width configuration 00: 8-bits (default) 01: 16-bits 10: 32-bits 11: Reserved
11	Reserved	-
10	CIRC_MODE0	DMA channel 0 circular buffer mode enable configuration 1: Enable circular buffer mode 0: Disable circular buffer mode (default)
9-8	PRI_CH0[1:0]	DMA channel 0 priority level 00: Low priority (default) 01: Medium priority 10: High priority 11: Highest priority
7-6	SRC_ADR0_CTL[1:0]	DMA channel 0 source address control 00: Increment source address (default) 01: Decrement source address 10: Fixed source address 11: Reserved
5-4	DST_ADR0_CTL[1:0]	DMA channel 0 destination address control 00: Increment destination address (default) 01: Decrement destination address 10: Fixed destination address 11: Reserved
3	Reserved	-
2	DMA_HALF_INT0_EN	DMA channel 0 HALF interrupt enable configuration 1: Enable HALF interrupt 0: Disable HALF interrupt (default)
1	DMA_TOTAL_INT0_EN	DMA channel 0 TOTAL interrupt enable configuration 1: Enable TOTAL interrupt 0: Disable TOTAL interrupt (default)
0	DMA_CHEN0	DMA channel 0 enable Configuration 1: Enable DMA channel 0 0: Disable DMA channel 0 (default)

-: unimplemented.

DMA Configuration Register 1 DMA_CONFIG1 (Address: 0x0030_002C) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
Name	SRC_WIDTH[1:0]		DST_WIDTH[1:0]		Reserved	CIRC_MODE1	PRI_CH1[1:0]	
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
Name	SRC_ADR1_CTL[1:0]		DST_ADR1_CTL[1:0]		Reserved	DMA_HALF_INT1_EN	DMA_TOTAL_INT1_EN	DMA_CHEN1

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-14	SRC_WIDTH[1:0]	DMA channel 1 source data width configuration 00: 8-bits (default) 01: 16-bits 10: 32-bits 11: Reserved
13-12	DST_WIDTH[1:0]	DMA channel 1 destination data width configuration 00: 8-bits (default) 01: 16-bits 10: 32-bits 11: Reserved
11	Reserved	-
10	CIRC_MODE1	DMA channel 1 circular buffer mode enable configuration 1: Enable circular buffer mode 0: Disable circular buffer mode (default)
9-8	PRI_CH1[1:0]	DMA channel 1 priority level configuration 00: Low priority (default) 01: Medium priority 10: High priority 11: Highest priority
7-6	SRC_ADR1_CTL[1:0]	DMA channel 1 source address control 00: Increment source address (default) 01: Decrement source address 10: Fixed source address 11: Reserved
5-4	DST_ADR1_CTL[1:0]	DMA channel 1 destination address control 00: Increment destination address (default) 01: Decrement destination address 10: Fixed destination address 11: Reserved
3	Reserved	-
2	DMA_HALF_INT1_EN	DMA channel 1 HALF interrupt enable configuration 1: Enable HALF interrupt 0: Disable HALF interrupt (default)

Bit Number	Bit Mnemonic	Description
1	DMA_TOTAL_INT1_EN	DMA channel 1 TOTAL interrupt enable configuration 1: Enable TOTAL interrupt 0: Disable TOTAL interrupt (default)
0	DMA_CHEN1	DMA channel 1 enable configuration 1: Enable DMA channel 1 0: Disable DMA channel 1 (default)

-: unimplemented.

DMA Configuration Register 2 DMA_CONFIG2 (Address: 0x0030_003C) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
Name	SRC_WIDTH[1:0]		DST_WIDTH[1:0]		Reserved	CIRC_MODE2	PRI_CH2[1:0]	
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
Name	SRC_ADR2_CTL[1:0]		DST_ADR2_CTL[1:0]		Reserved	DMA_HALF_INT2_EN	DMA_TOTAL_INT2_EN	DMA_CHEN2

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-14	SRC_WIDTH[1:0]	DMA channel 2 source data width configuration 00: 8-bits (default) 01: 16-bits 10: 32-bits 11: Reserved
13-12	DST_WIDTH[1:0]	DMA channel 2 destination data width configuration 00: 8-bits (default) 01: 16-bits 10: 32-bits 11: Reserved
11	Reserved	-
10	CIRC_MODE2	DMA channel 2 circular buffer mode enable configuration 1: Enable circular buffer mode 0: Disable circular buffer mode (default)
9-8	PRI_CH2[1:0]	DMA channel 2 priority level configuration 00: Low priority (default) 01: Medium priority 10: High priority 11: Highest priority
7-6	SRC_ADR2_CTL[1:0]	DMA channel 2 source address control 00: Increment source address (default) 01: Decrement source address 10: Fixed source address 11: Reserved

Bit Number	Bit Mnemonic	Description
5-4	DST_ADR2_CTL[1:0]	DMA channel 2 destination address control 00: Increment destination address (default) 01: Decrement destination address 10: Fixed destination address 11: Reserved
3	Reserved	-
2	DMA_HALF_INT2_EN	DMA channel 2 HALF interrupt enable configuration 1: Enable HALF interrupt 0: Disable HALF interrupt (default)
1	DMA_TOTAL_INT2_EN	DMA channel 2 TOTAL interrupt enable configuration 1: Enable TOTAL interrupt 0: Disable TOTAL interrupt (default)
0	DMA_CHEN2	DMA channel 2 enable Configuration 1: Enable DMA channel 2 0: Disable DMA channel 2 (default)

-: unimplemented.

DMA Configuration Register 3 DMA_CONFIG3 (Address: 0x0030_004C) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
Name	SRC_WIDTH[1:0]		DST_WIDTH[1:0]		Reserved	CIRC_MODE3	PRI_CH3[1:0]	
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
Name	SRC_ADR3_CTL[1:0]		DST_ADR3_CTL[1:0]		Reserved	DMA_HALF_INT3_EN	DMA_TOTAL_INT3_EN	DMA_CHEN3

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-14	SRC_WIDTH[1:0]	DMA channel 3 source data width configuration 00: 8-bits (default) 01: 16-bits 10: 32-bits 11: Reserved
13-12	DST_WIDTH[1:0]	DMA channel 3 destination data width configuration 00: 8-bits (default) 01: 16-bits 10: 32-bits 11: Reserved
11	Reserved	-
10	CIRC_MODE3	DMA channel 3 circular buffer mode enable configuration 1: Enable circular buffer mode 0: Disable circular buffer mode (default)

Bit Number	Bit Mnemonic	Description
9-8	PRI_CH3[1:0]	DMA channel 3 priority level configuration 00: Low priority (default) 01: Medium priority 10: High priority 11: Highest priority
7-6	SRC_ADR3_CTL[1:0]	DMA channel 3 source address control 00: Increment source address (default) 01: Decrement source address 10: Fixed source address 11: Reserved
5-4	DST_ADR3_CTL[1:0]	DMA channel 3 destination address control 00: Increment destination address (default) 01: Decrement destination address 10: Fixed destination address 11: Reserved
3	Reserved	-
2	DMA_HALF_INT3_EN	DMA channel 3 HALF interrupt enable configuration 1: Enable HALF interrupt 0: Disable HALF interrupt (default)
1	DMA_TOTAL_INT3_EN	DMA channel 3 TOTAL interrupt enable configuration 1: Enable TOTAL interrupt 0: Disable TOTAL interrupt (default)
0	DMA_CHEN3	DMA channel 3 enable configuration 1: Enable DMA channel 3 0: Disable DMA channel 3 (default)

-: unimplemented.

DMA Configuration Register 4 DMA_CONFIG4 (Address: 0x0030_005C) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
Name	SRC_WIDTH[1:0]		DST_WIDTH[1:0]		Reserved	CIRC_MODE4	PRI_CH4[1:0]	

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
Name	SRC_ADR4_CTL[1:0]		DST_ADR4_CTL[1:0]		Reserved	DMA_HALF_INT4_EN	DMA_TOTAL_INT4_EN	DMA_CHEN4

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-14	SRC_WIDTH[1:0]	DMA channel 4 source data width configuration 00: 8-bits (default) 01: 16-bits

Bit Number	Bit Mnemonic	Description
		10: 32-bits 11: Reserved
13-12	DST_WIDTH[1:0]	DMA channel 4 destination data width configuration 00: 8-bits (default) 01: 16-bits 10: 32-bits 11: Reserved
11	Reserved	-
10	CIRC_MODE3	DMA channel 4 circular buffer mode enable setting 1: Enable circular buffer mode 0: Disable circular buffer mode (default)
9-8	PRI_CH4[1:0]	DMA channel 4 priority level configuration 00: Low priority (default) 01: Medium priority 10: High priority 11: Highest priority
7-6	SRC_ADR4_CTL[1:0]	DMA channel 4 source address control 00: Increment source address (default) 01: Decrement source address 10: Fixed source address 11: Reserved
5-4	DST_ADR4_CTL[1:0]	DMA channel 4 destination address control 00: Increment destination address (default) 01: Decrement destination address 10: Fixed destination address 11: Reserved
3	Reserved	-
2	DMA_HALF_INT4_EN	DMA channel 4 HALF interrupt enable setting 1: Enable HALF interrupt 0: Disable HALF interrupt (default)
1	DMA_TOTAL_INT4_EN	DMA channel 4 TOTAL interrupt enable setting 1: Enable TOTAL interrupt 0: Disable TOTAL interrupt (default)
0	DMA_CHEN4	DMA channel 4 enable setting 1: Enable DMA channel 4 0: Disable DMA channel 4 (default)

-: unimplemented.

DMA Configuration Register 5 DMA_CONFIG5 (Address: 0x0030_006C) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
Name	SRC_WIDTH[1:0]		DST_WIDTH[1:0]		Reserved	CIRC_MODE5	PRI_CH5[1:0]	

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
Name	SRC_ADR5_CTL[1:0]		DST_ADR5_CTL[1:0]		Reserved	DMA_HALF_INT5_EN	DMA_TOTAL_INT5_EN	DMA_CHEN5

Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-14	SRC_WIDTH[1:0]	DMA channel 5 source data width setting 00: 8-bits (default) 01: 16-bits 10: 32-bits 11: Reserved
13-12	DST_WIDTH[1:0]	DMA channel 5 destination data width setting 00: 8-bits (default) 01: 16-bits 10: 32-bits 11: Reserved
11	Reserved	-
10	CIRC_MODE5	DMA channel 5 circular buffer mode enable setting 1: Enable circular buffer mode 0: Disable circular buffer mode (default)
9-8	PRI_CH5[1:0]	DMA channel 5 priority setting 00: Low priority (default) 01: Medium priority 10: High priority 11: Highest priority
7-6	SRC_ADR5_CTL[1:0]	DMA channel 5 source address control 00: Increment source address (default) 01: Decrement source address 10: Fixed source address 11: Reserved
5-4	DST_ADR5_CTL[1:0]	DMA channel 5 destination address control 00: Increment destination address (default) 01: Decrement destination address 10: Fixed destination address 11: Reserved
3	Reserved	-
2	DMA_HALF_INT5_EN	DMA channel 5 HALF interrupt enable setting 1: Enable HALF interrupt 0: Disable HALF interrupt (default)
1	DMA_TOTAL_INT5_EN	DMA channel 5 TOTAL interrupt enable setting 1: Enable TOTAL interrupt 0: Disable TOTAL interrupt (default)
0	DMA_CHEN5	DMA channel 5 enable setting 1: Enable DMA channel 5 0: Disable DMA channel 5 (default)

-: unimplemented.

DMA Configuration Register 6 DMA_CONFIG6 (Address: 0x0030_007C) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
Name	SRC_WIDTH[1:0]		DST_WIDTH[1:0]		Reserved	CIRC_MODE6	PRI_CH6[1:0]	
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
Name	SRC_ADR6_CTL[1:0]		DST_ADR6_CTL[1:0]		Reserved	DMA_HALF_INT6_EN	DMA_TOTAL_INT6_EN	DMA_CHEN6

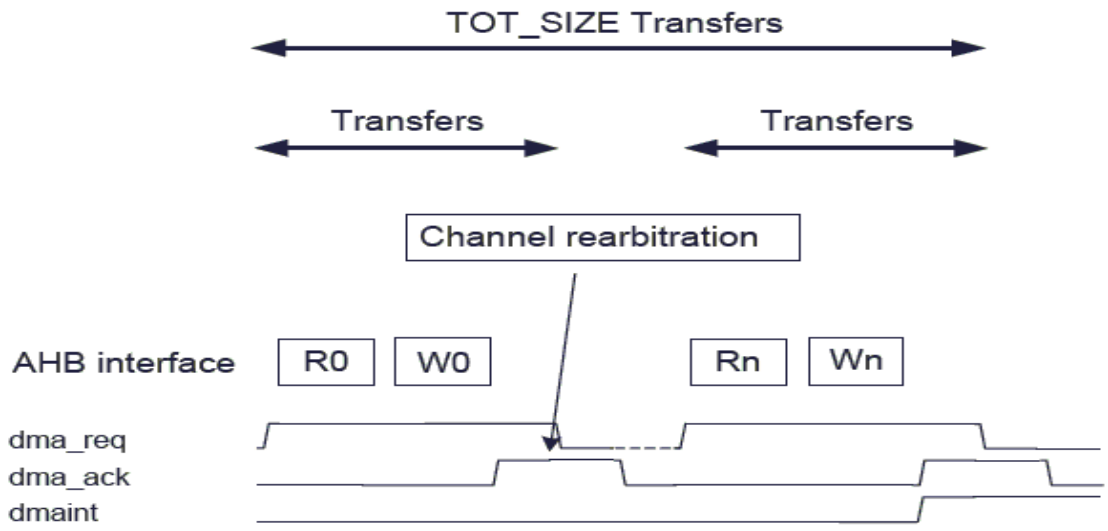
Bit Number	Bit Mnemonic	Description
31-16	Reserved	-
15-14	SRC_WIDTH[1:0]	DMA channel 6 source data width configuration 00: 8-bits (default) 01: 16-bits 10: 32-bits 11: Reserved
13-12	DST_WIDTH[1:0]	DMA channel 6 destination data width configuration 00: 8-bits (default) 01: 16-bits 10: 32-bits 11: Reserved
11	Reserved	-
10	CIRC_MODE6	DMA channel 6 circular buffer mode enable setting 1: Enable circular buffer mode 0: Disable circular buffer mode (default)
9-8	PRI_CH6[1:0]	DMA channel 6 priority level configuration 00: Low priority (default) 01: Medium priority 10: High priority 11: Highest priority
7-6	SRC_ADR6_CTL[1:0]	DMA channel 6 source address control 00: Increment source address (default) 01: Decrement source address 10: Fixed source address 11: Reserved
5-4	DST_ADR6_CTL[1:0]	DMA channel 6 destination address control 00: Increment destination address (default) 01: Decrement destination address 10: Fixed destination address 11: Reserved
3	Reserved	-
2	DMA_HALF_INT6_EN	DMA channel 6 HALF interrupt enable setting 1: Enable HALF interrupt 0: Disable HALF interrupt (default)
1	DMA_TOTAL_INT6_EN	DMA channel 6 TOTAL interrupt enable setting 1: Enable TOTAL interrupt 0: Disable TOTAL interrupt (default)

Bit Number	Bit Mnemonic	Description
0	DMA_CHEN6	DMA channel 6 enable setting 1: Enable DMA channel 6 0: Disable DMA channel 6 (default)

-: unimplemented.

6.18.15 DMA Transfer Flow

Each time you enable DMA channel for transfer data. You must configure four registers first, the source address register, destination address register, total transfer length register and configuration register. The configuration register must be configured at last.



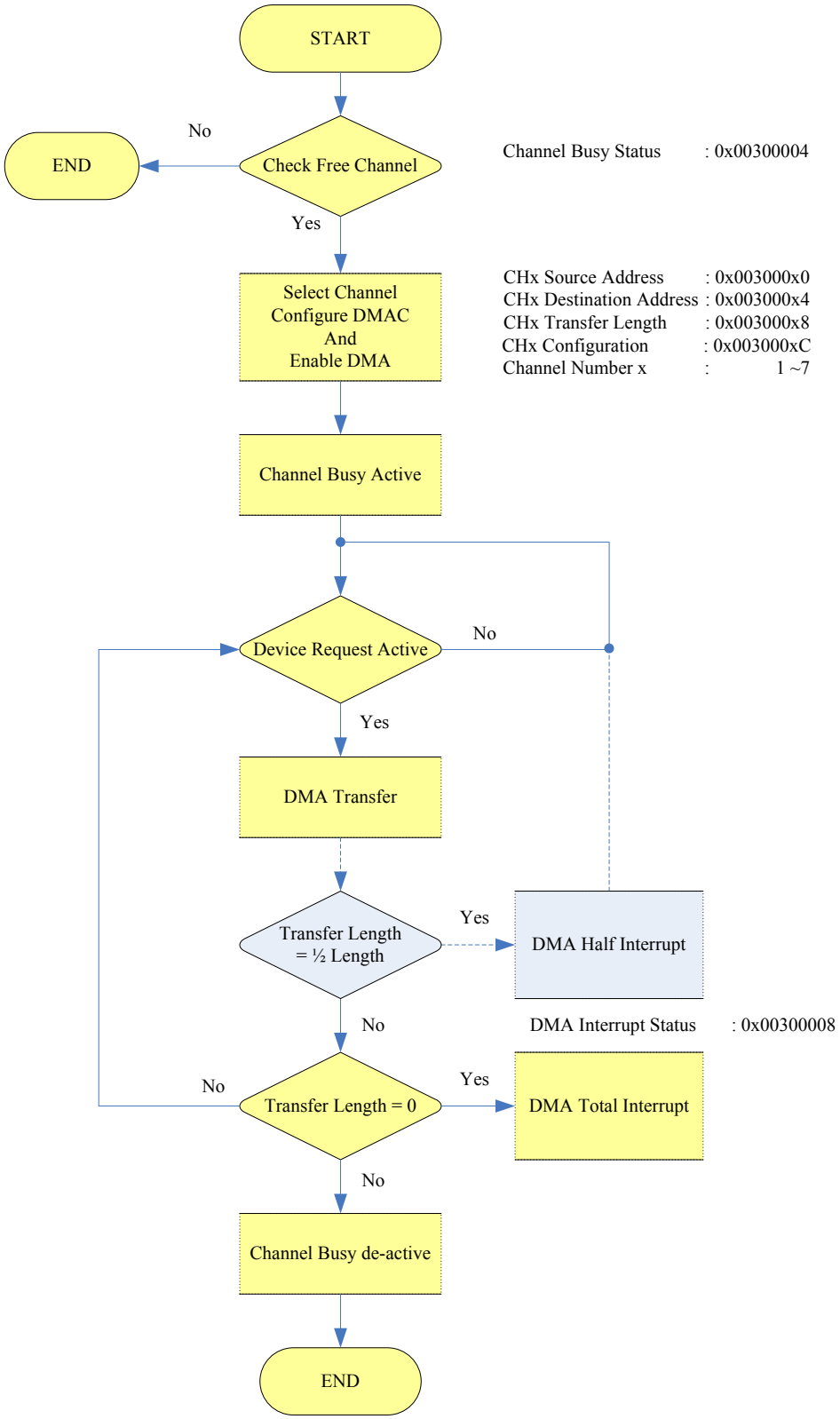


Fig.1 Normal Mode Flow Chart

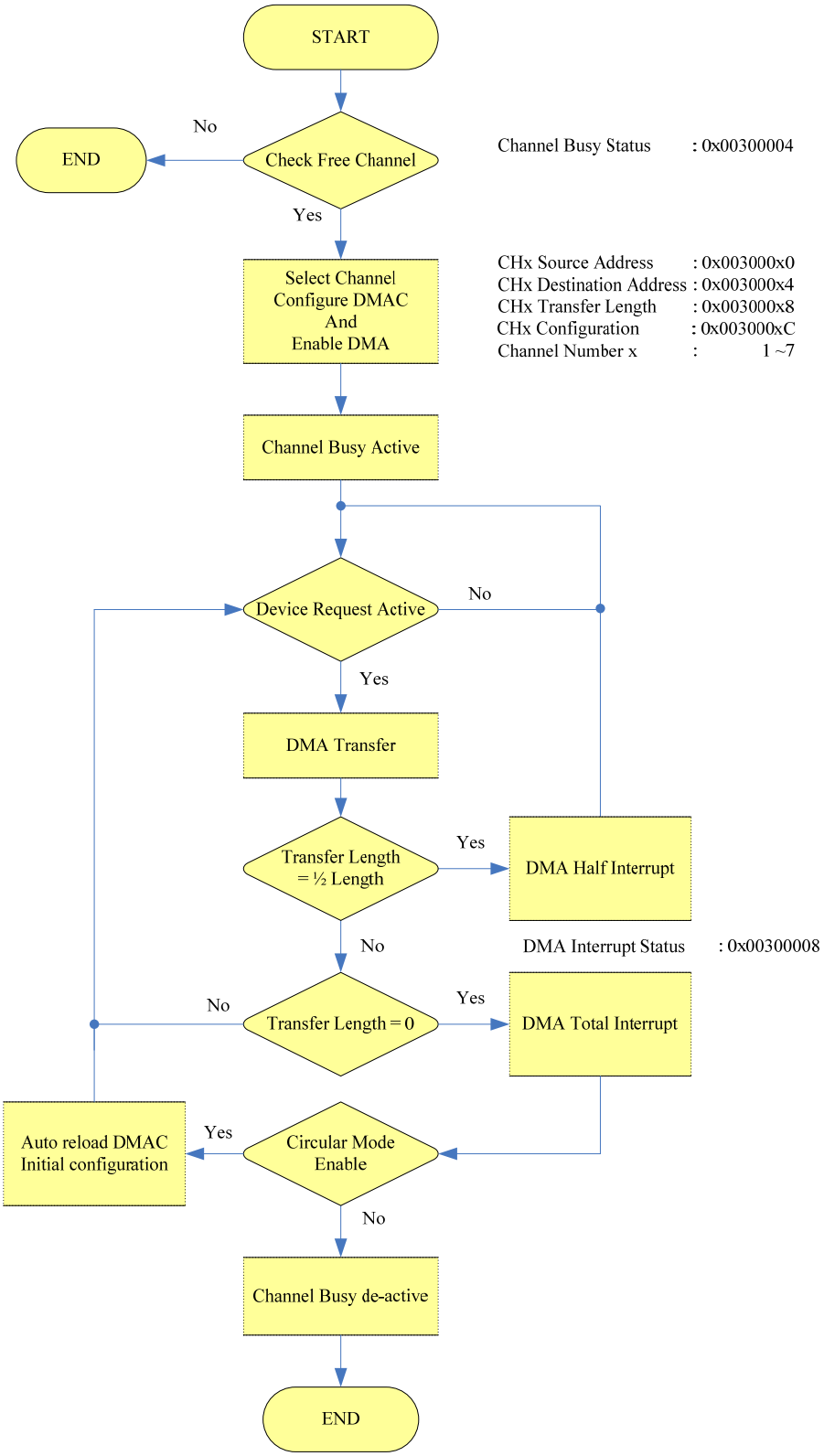


Fig.2 Circular Mode Flow Chart

6.18.16 Circular mode

The circular mode is available to handle circular buffer by SRAM.

1. When DMA half length data transfer done, the DMA interrupt sent to MCU and MCU move the first half data from SRAM. At the same time, DMA transfer the last half data from the device to SRAM.
2. When DMA total length data transfer done, the DMA interrupt send to MCU and MCU move the last half data from SRAM. At the same time, DMA reload the initial DMA configuration automatically and transfer the first half data from the device to SRAM.
3. If circular buffer mode is disabled, the DMA will stop after all of the total length data transfer done.

6.18.17 Peripheral to Memory

1. Check which channel available
2. MCU sets the DMA channel register
   a. SrcAddr is device address
   b. DstAddr is memory write start address
   c. Length is total number in DMA transaction
   d. Config is set priority, address control, interrupt enable and DMA channel enable

1- DMA hardware handshake

a. After channel wins the arbitration, DMAC will wait the device req_i signal to be asserted before starting DMA transfer
b. When the device receives the ack_o, the device de-asserts the req_i.
c. DMAC de-assert ack_o, update Length, DstAddr and re-arbitrates among all DMA requests.

2- DMA transfer complete

a. The channel Length is 0
b. The DMAC generates an interrupt to MCU
c. MCU read Interrupt Flag Register to know which channel the interrupt bit was asserted.
d. The MCU write 1 to the Interrupt Clear Register to clear DMA channel interrupt
e. Release channel

6.18.18 Memory to Peripheral

1. Check which channel available
2. MCU set the DMA channel register
   a. SrcAddr is device address
   b. DstAddr is memory write start address
   c. Length is total number in DMA transaction
   d. Config is set priority, address control, interrupt enable and channel enable

3- DMA hardware handshake

a. After channel wins the arbitration, DMAC will wait the device req_i signal to be asserted before starting DMA requests
b. When the device receives the ack_o, the device de-asserts the req_i.
c. DMAC de-assert ack_o, update Length, DstAddr and re-arbitrates among all DMA requests

4- DMA transfer complete

a. The channel Length is 0
b. The DMAC generates an interrupt signal to MCU
c. MCU read DMAC Interrupt Flag Register to know which channel the interrupt bit was asserted
d. The MCU write one to the Interrupt Clear Register to clear DMA channel interrupt
e. Release channel

6.18.19 Peripheral to Peripheral

1. Check which channel available
2. MCU set the DMA channel register
   a. SrcAddr is device address
   b. DstAddr is memory write start address
   c. Length is total number in DMA transaction
   d. Config is set priority, address control, interrupt enable and channel enable

5- DMA Hardware handshake

a. After channel wins the arbitration, DMAC will wait both of the source and destination the device req_i to be asserted before starting DMA transfer
b. When the device receive the ack_o, the both of the device de-assert the req_i
c. DMA de-assert ack_o, update Data Length, Destination address and re-arbitrates among all DMA requests

6- DMA Transfer complete

b. The channel Length is 0
c. The DMA generates an interrupt to MCU
d. MCU read DMAC Interrupt Status Register to know which channel the interrupt bit was asserted
e. The MCU write one to the Interrupt Clear Register to clear DMA channel interrupt
f. Release channel

6.18.20 DMA Support Peripherals

Device Name	Device Address
TIMER0	0x0020_1C00
TIMER1	0x0020_2000
TIMER2	0x0020_2400
TIMER3	0x0020_2800
TIMER4	0x0020_2C00
TIMER5	0x0020_3000
UART0 TX	0x0020_340C
UART0 RX	0x0020_3410
UART1 TX	0x0020_380C
UART1 RX	0x0020_3810
UART2 TX	0x0020_3C0C
UART2 RX	0x0020_3C10
SPI0 TX	0x0020_4410
SPI0 RX	0x0020_4414
SPI1 TX	0x0020_4810
SPI1 RX	0x0020_4814
I^2C0 TX	0x0020_540C
I^2C0 RX	0x0020_5410
I^2C1 TX	0x0020_580C
I^2C1 RX	0x0020_5810
ADC	0x0020_6400
I^2S TX0	0x0020_6C20
I^2S TX1	0x0020_6C24
I^2S TX2	0x0020_6C28

Device Name	Device Address
I^2S RX0	0x0020_6C30
I^2S RX1	0x0020_6C34
I^2S RX2	0x0020_6C38
USB EP7_TX	0x0020_7890
USB EP8_RX	0x0020_78B0

6.19 USB

6.19.1 Features

- Compatible with USB 2.0 full speed operation
- Compatible with USB audio device class spec V1.0
- One Control Endpoint (Endpoint0), IN/OUT each with 64 bytes (8/16/32/64B programmable) FIFO
- Six Generic Endpoints (IN/OUT, INT/Bulk programmable); Endpoint 4, 5, 6 can also be configured as OUT token for Endpoints 1, 2, 3
- Two Isochronous endpoints (Endpoint 7, 8) with DMA channel between SRAM and USB FIFO
- Total FIFO for Endpoints 0~8: 1K Bytes + 512 Bytes
  - Endpoint 7 & 8: share 1K Bytes (512*2, supports DMA)
  - Endpoint 0: IN 64 Bytes, out 64 Bytes
  - Endpoint 1~ 6: 64 Bytes/each
- Support USB Suspend, Wakeup (Resume) and Remote-Wakeup
- USB function could be disabled for non-USB application

6.19.2 Main Blocks

The USB function interface manages communications between the Host and the USB function. The WT59F164 interface consists of the USB full speed transceiver, the serial bus engine (SIE), the system interface logic (SIL), and the transmit/receive FIFOs. The USB transceiver in WT59f164 provides a physical interface to USB lines. The SIE handles communication protocol of USB. The SIL handles data transfer and provides the interface among the SIE, the N903-S CPU and the function FIFOs.

The main blocks in the USB module are:

1. USB full speed Receiver: This is an on-chip transceiver having one differential driver to transmit the USB data onto the USB bus and single ended receivers on the D+ and D- lines as well as a differential receiver to receive the USB data signal on the USB bus.

2. Serial Bus Interface Engine (SIE): The SIE does all front-end functions of USB protocol such as clock/data separation, sync-field identification, NRZI-NRZ conversion, token packet decoding, bit stripping, bit stuffing, NRZ-NRZI conversion, CRC5 checking and CRC16 generation and checking. Besides, it manages detecting of rest, suspend and resume signals on the upstream port of the WT59F164 to wakeup the system from the suspend state. It also provides serial-to-parallel conversion for the serial packet from the full speed USB transceiver to 8 bit parallel data to the system interface logic and for the 8 bit parallel data from the system interface logic to serial packet to the full speed USB transceiver.

3. System Interface Logic (SIL): The SIL operates in conjunction with the CPU to provide the capabilities of controlling the operation of the FIFOs. The SIL also monitors the status of the data transactions, transfers event control to the CPU through interrupt requests at the appropriate moment, initiate resume signaling to USB bus while the WT59F164 is in power-down mode. Operation of the SIL is controlled through the use of external function registers.

1- **Device Function:** The WT59F164 device function interface has eight endpoints that can support four types of USB data transfer: control, interrupt, bulk and isochronous transfer. Transmit FIFOs are written by CPU, then read by SIL for transmission. Receive FIFO is written by the SIL following reception, then read by the CPU. Endpoint 0 supports control transfer for configuration/command/status type communication flows between client software and function. Endpoints 1~6 supports interrupt/bulk transfer. Endpoint 7 supports isochronous IN transfer. Endpoint 8 supports isochronous OUT transfer.

6.19.3 Function Endpoint

The WT59F164 supports 8 device function endpoints. Endpoint 0 contains two FIFOs for transmit and receive, respectively. Endpoint 1 to 6 can be programmed to transmit or receive. Endpoint 0 handles control data transfer. Endpoint 1 to 6 can be interrupt transfer or bulk transfer. The EPINDEX register selects the endpoint for any given data transaction. Endpoint 7 and 8 are dedicated isochronous endpoints which have their control and data registers which are not indexed by EPINDEX.

6.19.4 Transmit FIFO Buffer

6.19.4.1 Features

The USB transmit FIFOs are data buffers with the following features (see Figure 1):

- USB support for one data set of not greater than 8/16/32/64 bytes (programmable by counter setting)
- One byte count register to store the number of bytes in the data set
- Protection against overwriting data in a full FIFO
- Capable of retransmitting the current data set

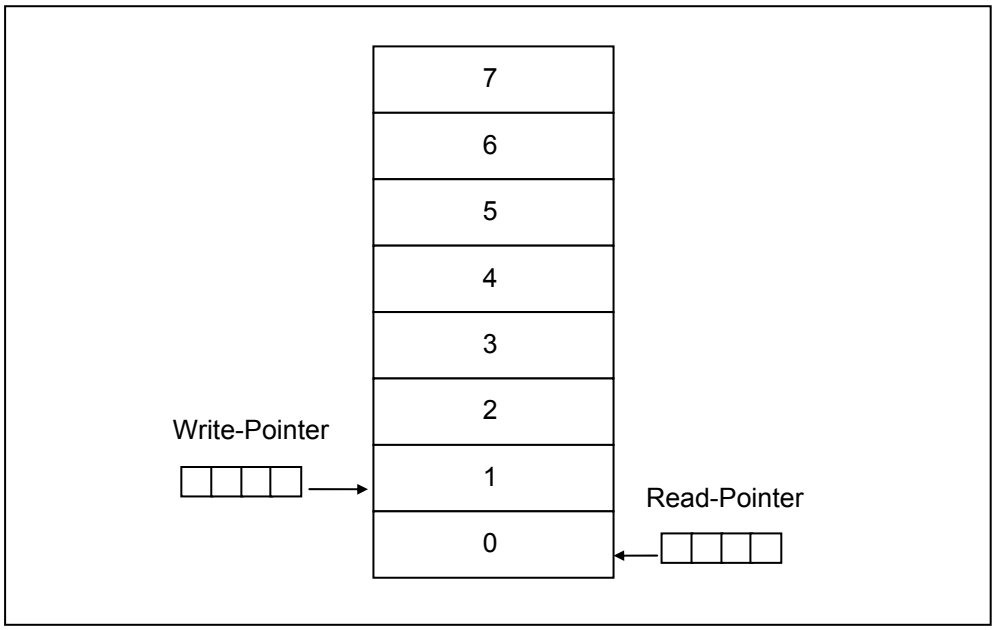


Figure 1. Transmit FIFO Buffer Outline (example for 8 bytes FIFO)

The CPU writes to the FIFO location specified by the write-pointer also used as the byte-counter to indicate how many bytes have been written and not yet read by the SIL. The write-pointer automatically increments by one after a write, and it decrements by one after a read. The read-pointer points the next FIFO location to be read by the SUB SIL. The read-pointer automatically increments by one after a read. The transmit FIFO is inhibited to be read by the SIL when it is empty or before a data set has been successfully written into it.

Transmit Data Set Management

TXFULL = 1 in the TXFLG register, indicates data set has been written into the FIFO and is ready for transmission. Following reset, TXFULL = 0 and TXEMP = 1, signifying an empty FIFO. Only the first eight bytes of the data set which size is greater than eight are written into the FIFO. In this case, TXFULL is not set until a write to TXCNT. In the case of TXFULL = 1 farther writing to TXDAT or TXCNT are ignored.

Please note that the content of TXCNT determines the number of bytes transmitted over the USB lines. Discrepancy between the byte number written to TXCNT and number of bytes actually written to the FIFO will cause an unexpected result. Read the FIFO is prohibited when the FIFO is empty or TXFULL = 0.

Two events cause the TXFLG.TXFULL to be updated:

1. A new data set is written to the FIFO: The CPU writes bytes to the FIFO via TXDAT and writes the number of bytes to TXCNT. TXFLG.TXFULL is only set after the write to TXCNT. Set TXCNT = 0 indicates a zero length transmission. In this case, TXFLG.TXFULL is set and TXFLG.TXEMP remains unchanged to indicate the FIFO is still empty. This process is illustrated in Table 1.
2. A data set in the FIFO is successfully transmitted: The SIL reads the data set from the FIFO for transmission. When a good transmission is acknowledged, the TXFLG.TXFULL is cleared and TXFLG.TXEMP is set.

TX FULL	TX EMP	Zero Length Transmission	Write bytes to TXDAT / Write byte count to TXCNT	Data Set Written	TX FULL	TX EMP
0	0	No		Yes	1	0
0	1	No		Yes	1	0
0	1	Yes		No	1	1
1	-	-		Write Ignored	1	-

Table 1. Writing to the Byte Count Register (TXCNT)

When a good transmission is completed, both read pointer and write pointer is advanced to the start point of the FIFO to set up for transmitting the next data set. When a bad transmission is encountered, he read pointer is received to the start point of the FIFO to enable the SIL to re-read the last data set for retransmission. The pointer reversal and advance are accomplished automatically by hardware. Table 2 summarizes how actions following a transmission depend on TXSTAT.TXERR and TXSTAT.TXACK.

TXERR	TXACK	Action at End of Transfer Cycle
0	0	No operation
0	1	Read Pointer and Write Pointer both are set to the start point of FIFO
1	0	Read Pointer is set to the start point of FIFO

Table 2. Truth Table for Transmit FIFO Management

Transmit FIFO Buffer Registers

TXDAT: Transmit FIFO Buffer Data Register
TXCNT: Transmit FIFO Buffer Data Counter Register
TXCON: Transmit FIFO Buffer Control Register
TXFLG: Transmit FIFO Buffer Flag Register

These registers are endpoint indexed. They are used as a set to control the operation of the transmit FIFO, associated with the current endpoint specified by the EPINDEX register.

6.19.5 Receive FIFO Buffer

Features

The receive USB FIFO is a data buffer with the following features (see Figure 2):

- Support for one data set not greater than 8/16/32/64 bytes
- A byte count register accessed the number of bytes in the data set
- Flag to signal a full FIFO and an empty FIFO
- Capability to re-receive the last data set

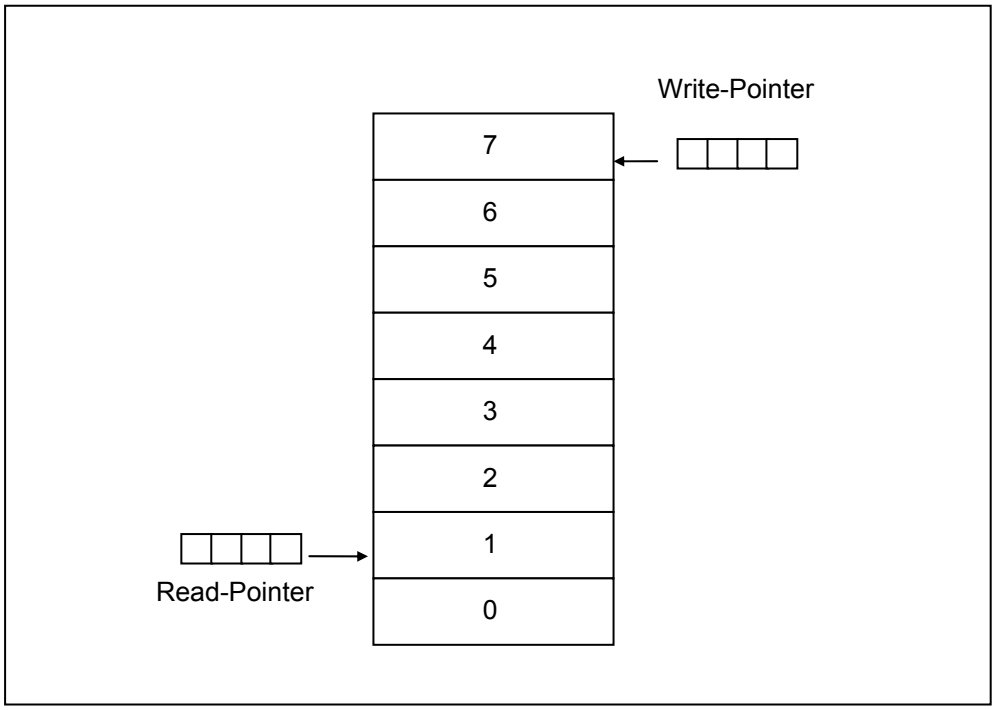


Figure 2. Receive FIFO Buffer Outline (example for 8 bytes FIFO)

The SIL writes to the FIFO location specified by the write pointer also used as the byte-counter to indicate how many bytes have been written and not yet ready by the CPU. The write-pointer automatically increments by one after a write and decrements by one after a read. The read-pointer points the next FIFO locations to be read by the CPU. The read-pointer automatically increments by one after a read. The receive FIFO is inhibited to be read by the CPU when it is empty or before a data set has been successfully written into it. **When a SETUP token is detected by the SIL, the SIL flushes the FIFO even if the FIFO is being read by the CPU.**

Receive Data Set Management

RXFULL = 1 in the RXFLG register, indicates the data set has been written into the FIFO and is ready for reception. Following reset, RXFULL = 0 and RXFLG.RXEMP = 1, signifying an empty FIFO. Only the first eight bytes of the data set which size is greater than eight are written into FIFO. RXFULL is however not set until reception is done and successfully acknowledged. RXFULL is cleared by setting the FFRC bit of RXCON in firmware to indicate the data set has successfully read by CPU. In the case of RXFULL =1 farther writes to FIFO are ignored. Please note that the content of RXCNT should be read by CPU to determine the numbers of bytes need to be read from FIFO by CPU. Further reading from an empty FIFO is ignored.

Table 3. Status of the Receive FIFO Data Set

RXFULL	RXEMP	Status
0	0	Data set is being written to FIFO
0	1	Empty
1	0	Data set already written to FIFO
1	1	Zero length packet received

When a good reception is completed and the data set has been successfully read by CPU, firmware must set the FFRC bit of RXCON to advance the write pointer and read pointer to the start point of the FIFO to set up for receiving the next data set. When a bad reception is completed, the write pointer can be reversed to the position of the start point of the FIFO to enable the SIL to re-write the last data set for reception. The pointer advance and reversal are accomplished automatically by hardware. Table 4 summarizes how actions following a reception depend on RXERR and RXACK.

Table 4. Truth Table for Receive FIFO Management

RXERR	RXACK	Action at End of Transfer Cycle
0	0	No operation
0	1	Read Pointer and Write Pointer are set to the start point of FIFO when firmware sets the FFRC bit of RXCON
1	0	Write Pointer is set to the start point of FIFO

Receive FIFO Buffer Registers

RXDAT: Receive FIFO Buffer Data Register
RXCNT: Receive FIFO Buffer Data Counter Register
RXCON: Receive FIFO Buffer Control Register
RXFLG: Receive FIFO Buffer Flag Register

These registers are endpoint indexed. They are used as a set to control the specification of the receive FIFO associated with the current endpoint specified by the EPINDEX register.

6.19.6 Setup Token Receive FIFO Buffer Handling

Setup tokens received by the endpoint zero must be acknowledged, even if the receive FIFO is not empty. When a SETUP token is detected by the SIL, the SIL flushes the FIFO and sets the STOVW bit of RXSTAT for reset and locking the read pointer. These prevent RXURF bit of RXFLG and the read pointer from being set if the receive FIFO flush occurs in the middle of a CPU data read cycle. The STOW bit is cleared and the EDOVW bit is set when a SETUP packet has been successfully acknowledged. The read pointer will remain locked until both the STOVW and EDOVW bits are cleared. For SETUP packets only, firmware must clear EDOVW before reading data from the FIFO. If this is not done, data from the FIFO will be invalid. After processing a SETUP packet, firmware should always check the STOVW and EDOVW flags before setting the RXFFRC bit. When a SETUP packet either has been or is being received, setting of RXFFRC has no effect if either STOVW or EDOVW is set.

6.19.7 Suspend and Resume

In order to reduce the power consumption, WT59F164 automatically enters the suspend state when it has observed no bus traffic for 3 ms. When in suspend, the CPU and its peripherals are in power down mode, an interrupt is enabled to support remote wakeup. The entire chip consumes less than 500uA in suspended state.

WT59F164 exists suspend mode when there is bus activity. A USB device may also request the host exists from suspend or selective suspend by using electrical signaling to indicate remote wakeup. The ability of a device to signal remove wakeup is optional. WT59F164 allows the host to enable or disable this capability. Device states are described. In Figure 3.

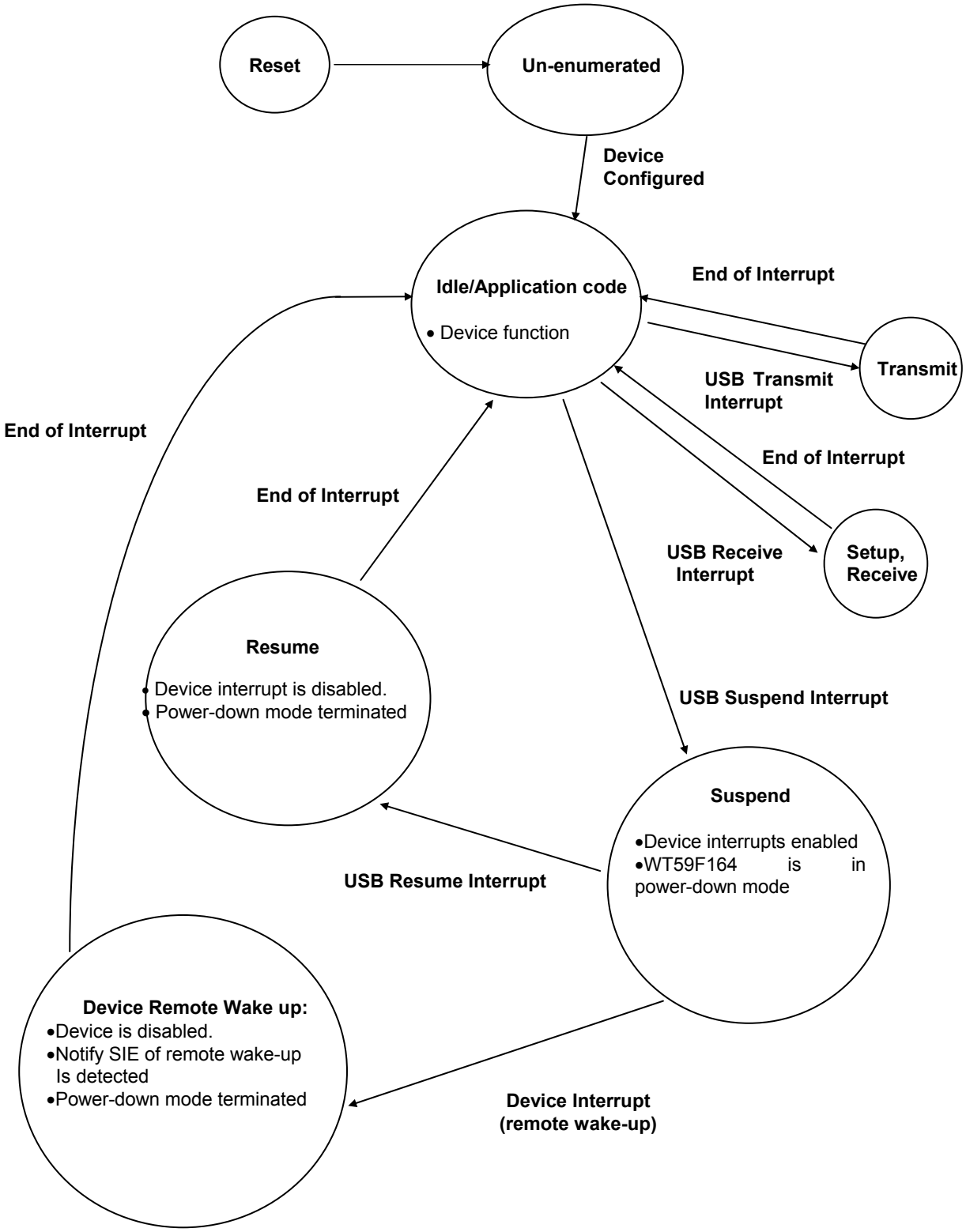


Figure 3. Suspend and Resume State Diagram

6.19.8 USB Register Summary Table

Register Name	Address	Reset Default (Hex)	Description
USB Serial Interface Register (USB)	**0x0020_7800~0x0020_7BFF**		
FADDR	0x0020_7800	0x0000_0000	USB device address
USBFI	0x0020_7804	0x0000_0000	USB interrupt flag
USBFIE	0x0020_7808	0x0000_0000	USB interrupt enable
SIEI	0x0020_780C	0x0000_0000	USB interface setting
EPINDEX	0x0020_7814	0x0000_0000	USB endpoint index
EPCON	0x0020_7818	0x0000_0025	USB endpoint control
TXDAT	0x0020_7820		USB transmit data buffer
TXCON	0x0020_7824	0x0000_0000	USB transmit control setting
TXFLG	0x0020_7828	0x0000_0008	USB transmit flag
TXCNT	0x0020_782C	0x0000_0000	USB transmit data length setting
TXSTAT	0x0020_7830	0x0000_0000	USB transmit status
USBFI_CLR	0x0020_7840	0x0000_0000	USB interrupt clear
USBFI2	0x0020_7844	0x0000_0000	USB interrupt flag
USBFIE2	0x0020_7848	0x0000_0000	USB interrupt enable setting
REP	0x0020_784C	0x0000_0000	USB endpoint pairing setting
TXEN	0x0020_7850	0x0000_0000	USB transmit status
RXDAT	0x0020_7860		USB receive data buffer
RXCON	0x0020_7864	0x0000_0000	USB receive control
RXFLG	0x0020_7868	0x0000_0008	USB receive flag
RXCNT	0x0020_786C	0x0000_0000	USB receive data length
RXSTAT	0x0020_7870	0x0000_0000	USB receive status
EP7_CON	0x0020_7880	0x0000_0000	USB endpoint 7 control
EP7_STAT	0x0020_7884	0x0000_0000	USB endpoint 7 status
EP7_BASE	0x0020_7888	0x0000_0000	USB endpoint 7 FIFOs allocation base register
EP7_LIMIT	0x0020_788C	0x0000_0100	USB endpoint 7 FIFOs allocation length
EP7_W_BYTE	0x0020_7890		USB endpoint 7 data write buffer
EP8_CON	0x0020_78A0	0x0000_0000	USB endpoint 8 control
EP8_STAT	0x0020_78A4	0x0000_0800	USB endpoint 8 status
EP8_BASE	0x0020_78A8	0x0000_0100	USB endpoint 8 FIFOs allocation base register
EP8_LIMIT	0x0020_78AC	0x0000_0100	USB endpoint 8 FIFO length setting
EP8_R_BYTE	0x0020_78B0		USB endpoint 8 data write buffer
FRAME	0x0020_78C0	0x0000_0000	USB frame number

USB Function Address Register FADDR (Address: 0x0020_7800) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	FA[6:0]						

This register holds the address for the USB function. During bus enumeration, it is written with a unique value assigned by the host. Reset state is by USB reset or hardware reset.

Bit Number	Bit Mnemonic	Description
31-7	Reserved	-
6-0	FA[6:0]	7-bit Programmable Function Address: This register is programmed through the commands received via endpoint 0 on configuration, which should be the only time the firmware should change the value of this register. This register is hardware read-only.

-: unimplemented.

USB Endpoint Interrupt Flag Register USBFI (Address: 0x0020_7804) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	USBX6INT	USBX5INT	USBX4INT	USBX3INT	USBX2INT	USBX1INT	USBRX0INT	USBTX0INT

USB Function Interrupt Register. A '1' indicates that an interrupt (INT3 of N903-S CPU) is actively pending. User should write '1' to register USBFI_CLR to clear corresponding USBFI interrupt register bit. Reset state is by the USB reset or hardware reset.

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	USBX6INT	USB endpoint 6 interrupt flag 1: Function transmit/receive done flag for endpoint 6
6	USBX5INT	USB endpoint 5 interrupt flag 1: Function transmit/receive done flag for endpoint 5
5	USBX4INT	USB endpoint 4 interrupt flag 1: Function transmit/receive done flag for endpoint 4

Bit Number	Bit Mnemonic	Description
4	USBX3INT	USB endpoint 3 interrupt flag 1: Function transmit/receive done flag for endpoint 3
3	USBX2INT	USB endpoint 2 interrupt flag 1: Function transmit/receive done flag for endpoint 2
2	USBX1INT	USB endpoint 1 interrupt flag 1: Function transmit/receive done flag for endpoint 1
1	USBRX0INT	USB Endpoint 0 receive interrupt flag 1: Function receive done flag for endpoint 6
0	USBTX0INT	USB Endpoint 0 transmit interrupt flag 1: Function transmit done flag for endpoint 6

-: unimplemented.

USB Endpoint Interrupt Enable Register USBFIE (Address: 0x0020_7808) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	USBX6INT_IE	USBX5INT_IE	USBX4INT_IE	USBX3INT_IE	USBX2INT_IE	USBX1INT_IE	USBRX0INT_IE	USBTX0INT_IE

For all bits, a ‘1’ means the interrupt is enabled and will cause an interrupt to be signaled to the micro-controller. A ‘0’ means the associated interrupt source is disabled and cannot cause an interrupt.

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	USBX6INT_IE	Endpoint 6 receive/transmit interrupt enable setting 1: Enable endpoint 6 receive/transmit interrupt 0: Disable endpoint 6 receive/transmit interrupt (default)
6	USBX5INT_IE	Endpoint 5 receive/transmit interrupt enable setting 1: Enable endpoint 5 receive/transmit interrupt 0: Disable endpoint 5 receive/transmit interrupt (default)
5	USBX4INT_IE	Endpoint 4 receive/transmit interrupt enable setting 1: Enable endpoint 4 receive/transmit interrupt 0: Disable endpoint 4 receive/transmit interrupt (default)
4	USBX3INT_IE	Endpoint 3 receive/transmit interrupt enable setting 1: Enable endpoint 3 receive/transmit interrupt 0: Disable endpoint 3 receive/transmit interrupt (default)
3	USBX2INT_IE	Endpoint 2 receive/transmit interrupt enable setting 1: Enable endpoint 2 receive/transmit interrupt 0: Disable endpoint 2 receive/transmit interrupt (default)

Bit Number	Bit Mnemonic	Description
2	USBX1INT_IE	Endpoint 1 receive/transmit interrupt enable setting 1: Enable endpoint 1 receive/transmit interrupt 0: Disable endpoint 1 receive/transmit interrupt (default)
1	USBRX0INT_IE	Endpoint 0 receive interrupt enable setting 1: Enable endpoint 0 receive interrupt 0: Disable endpoint 0 receive interrupt (default)
0	USBTX0INT_IE	Endpoint 0 transmit interrupt enable setting 1: Enable endpoint 0 transmit interrupt 0: Disable endpoint 0 transmit interrupt (default)

-: unimplemented.

USB SIE Control Register SIEI (Address: 0x0020_780C) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved		USBEN	DM	PSOFEN	USBRSTEN	DP	WAKEUP

Bit 5.4.2.1 are reset by hardware reset only. Bit 0 is reset by USB reset or hardware reset.

Bit Number	Bit Mnemonic	Description
31-6	Reserved	-
5	USBEN	USB transceiver enable setting 1: Enable USB transceiver 0: Disable USB transceiver (default)
4	DM	DM Pull-up enable setting 1: Enable DM Pull-up 0: Disable DM Pull-up (default) When this bit is cleared, CEXT does not provide 3.3V output and is in high impedance state. In this case, the 1.5KΩ resistor does not connect to the DM line and the upstream port of the device is disconnected. Set this bit for normal operation. This bit is not reset by USB reset.
3	PSOFEN	Enable Pseudo-SOF (PSOF) generator 1: Enable Pseudo-SOF generator (if not received SOF within the expected time, MCU will generate PSOF automatically) 0: Disable Pseudo-SOF generator (default)
2	USBRSTEN	USB reset enable setting 1: Enable USB reset 0: Disable USB reset (default) This bit should be set at least 500us after DPEN is set. This bit is not reset by USB reset.

Bit Number	Bit Mnemonic	Description
1	DP	DP Pull-up enable setting 1: Enable DP Pull-up 0: Disable DP Pull-up (default) When this bit is cleared, CEXT does not provide 3.3V output and is in high impedance state. In this case, the 1.5KΩ resistor does not connect to the DM line and the upstream port of the device is disconnected. Set this bit for normal operation. This bit is not reset by USB reset.
0	WAKEUP	This bit is used by USB function to initiate a remote wakeup. 1: Set by firmware to drive resume signaling on the USB lines to the HOST or upstream hub. Cleared by hardware when resume signaling is done.

-: unimplemented.

USB Endpoint Index Register EPINDEX (Address: 0x0020_7814) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	R/W	R/W	R/W
Name	Reserved					EPINDEX[2:0]		

Endpoint Index Register. This register identifies the endpoint pair. Its contents select the transmit and receive FIFO pair and serve as an index to endpoint registers. Reset state is by USB reset or hardware reset. The value in this register selects the associated bank of endpoint-indexed registers including (TXDAT, TXCON, TXFLG, TXCNT, TXSTAT, RXDAT, RXCON, RXFLG, RXCNT, RXSTAT, EPCON, and EPREP). Reset state is by the USB reset or hardware reset.

Bit Number	Bit Mnemonic	Description
31-3	Reserved	-
2-0	EPINX[2:0]	Endpoint Index setting : 000 = endpoint 0 (default) 001 = endpoint 1 010 = endpoint 2 011 = endpoint 3 100.= endpoint 4 101 = endpoint 5 110 = endpoint 6 111 = reserved

-: unimplemented.

USB Endpoint Control Register EPCON (Address: 0x0020_7818) **Reset Value: 0x0000_0025 (EP0) 0x0000_0000(OTHER)**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Name	RXSTL	TXSTL	CTLEP	Reserved	RXIE	RXEPEN	TXOE	TXEPEN

This register configures the operation of the endpoint specified by EPINDEX. Reset state is by USB reset or hardware reset.

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	RXSTL	Stall Receive Endpoint setting: Set this bit to stall the receive endpoint. Clear this bit only when the host has intervened through commands sent down endpoint 0. When this bit is set and RXSETUP is clear, the receive endpoint will respond with a STALL handshake to a valid OUT token. When this bit is set and RXSETUP is set, the receive endpoint will NAK. This bit does not affect the reception of SETUP token by a control endpoint.
6	TXSTL	Stall Transmit Endpoint setting: Set this bit to stall the transmit endpoint. This bit should be cleared only when the host has intervened through commands sent down endpoint 0. When this bit is set and RXSETUP is clear, the receive endpoint will respond with a STALL handshake to a valid IN token. When this bit is set and RXSETUP is set, the receive endpoint will NAK.
5	CTLEP	Control Endpoint setting: Set this bit to configure the endpoint as a control endpoint. Only control endpoint is capable of receiving SETUP tokens.
4	Reserved	-
3	RXIE	Receive Input Enable setting: Set this bit to enable data from the USB to be written into the receive FIFO. If cleared, the endpoint will not write the received data into the receive FIFO and at the end of reception, but will return a NAK handshake on a valid OUT token if he RXSTL bit is not set. This bit does not affect a valid SETUP token. A valid SETUP token and packet overrides this bit if it is cleared, and place the receive data in the FIFO.
2	RXEPEN	Receive Endpoint Enable setting: Set this bit to enable the receive endpoint. When disabled, the endpoint does not respond to valid OUT or SETUP token. This bit is hardware read-only and has the highest priority among RXIE and RXSTL. Note that endpoint 0 is enabled for reception upon reset.

Bit Number	Bit Mnemonic	Description
1	TXOE	Transmit Output Enable setting: This bit is used to enable the data in TXDAT to be transmitted. If cleared, the endpoint returns a NAK handshake to a valid IN token if the TXSTL bit is not set.
0	TXEPEN	Transmit Endpoint Enable setting This bit is used to enable the transmit endpoint. When disabled, the endpoint does not response to a valid IN token. This bit is hardware read-only. Note that endpoint 0 is enabled for transmission upon reset.

-: unimplemented.

USB Transmit Data Register TXDAT (Address: 0x0020_7820) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	TXDAT[7:0]							

Transmit FIFO data specified by EPINDEX is stored and read from this register.

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	TXDAT[7:0]	Transmit Data Byte (read-only): To write data to the transmit FIFO, the SIL writes to this register. To read data from the transmit FIFO, the CPU reads from this register. The writer-point are incremented automatically after a write.

-: unimplemented.

USB Transmit Control Register TXCON (Address: 0x0020_7824) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	-	-	-	-	-	-	-
Name	TXLCR	Reserved						

Transmit FIFO Control Register. Controls the transmit FIFO specified by EPINDEX. Reset state is by hardware reset.

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	TXLCR	Clear the transmit FIFO setting: Clear Transmit FIFO Buffer data, reset read pointer and write pointer. Set TXFLG.EMPTY = 1, and clear the bits in TXFLG except TXFLG.EMPTY. When clear is completed, hardware will clear this bit automatically.
6-0	Reserved	-

-: unimplemented.

USB Transmit Status Register TXFLG (Address: 0x0020_7828) Reset Value: 0x0000_0008

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R	R	R/W	R/W
Name	Reserved				TXEMP	TXFULL	TXURF	TXOVF

These flags indicate the status of data packets in the transmit FIFO specified by EPINDEX. Reset state is by hardware reset.

Bit Number	Bit Mnemonic	Description
31-8	-	Reserved: Values read from these bits are indeterminate. Write zeros to these bits.
3	TXEMP	Transmit FIFO Empty Flag (read only): Hardware sets this bit when the data set has been read out of the transmit FIFO by SIL. Hardware clears this bit when the empty condition no longer exists. This bit always tracks the current transmit FIFO status. This flag is also set when a zero-length data packet is transmitted.
2	TXFULL	Transmit FIFO Full Flag (read only): This flag indicates the data set is present in the transmit FIFO. This bit is set after write to TXCNT to reflect the condition of the data set. Hardware clears this bit when the data set has been successfully transmitted.

Bit Number	Bit Mnemonic	Description
1	TXURF	Transmit FIFO Under-run Flag (read-, clear-only): Hardware sets this flag when an addition byte is read from an empty transmit FIFO. This is a sticky bit that must be cleared through firmware by writing a "0" to this bit. When the transmit FIFO under-runs, the read pointer will not advance – it remains locked in the empty position.
0	TXOVF	Transmit FIFO Buffer Overrun Flag (read-, clear-only): This bit is set when an additional byte is written to a FIFO with TXFULL = 1. This bit is sticky bit that must be cleared through firmware by writing a "0" to this bit. When the transmit FIFO overruns, the write pointer will not advance – it remains locked in the full position.

-: unimplemented.

USB Transmit Data Length Register TXCNT (Address: 0x0020_782C) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	W	W	W	W	W	W	W
Name	Reserved	TXCNT[6:0]						

This register indicate the data set has been written into the FIFO and is ready for transmission specified by EPINDEX. Reset state is by hardware reset.
The transmission of responding to a control write status, control command without data, or an empty packet is completed after TXCNT is set to 0.

Bit Number	Bit Mnemonic	Description
31-7	Reserved	-
6-0	TXCNT[6:0]	Transmit Byte Count (write-only): The number of bytes in the data set written to the transmit FIFO. When this register is written, TXFULL is set. Write the byte count to this register after writing data set to TXDAT.

-: unimplemented.

USB Transmit Status Register TXSTAT (Address: 0x0020_7830) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	-	-	-	-	R	R	R
Name	TXSEQ	Reserved				TXVOID	TXERR	TXACK

Contains the current endpoint status of the transmit FIFO specified by EPINDEX. Reset state is by hardware reset.

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	TXSEQ	Transmit Current Sequence Bit (read, clear-only): This bit will be transmitted in the next PID and toggled on a valid ACK handshake. This bit is toggled by hardware on a valid SETUP token. The SIE will handle all sequence bit tracking. This bit should only be used when initializing a new configuration or interface.
6-3	Reserved	- Write zeros to these bits.
2	TXVOID	Transmit Void (read only): A void condition has occurred in response to a valid IN token. Transmit void is closely associated with the NAK/STALL handshake returned by the function after a valid IN token, due to the condition that cause the transmit FIFO to be unable or not ready to transmit. Use this bit to check any NAK/STALL handshake returned by the function. This bit does not affect the USBTxxINT, TXERR or TXACK bit. This bit is updated by hardware at the end of a non-isochronous transaction in response to a valid IN token.
1	TXERR	Transmit Error (read only): An error condition has occurred with the transmission. Complete or partial data has been transmitted. The error can be one of the following: 1. Data transmitted successfully but no handshake received. 2. Transmit FIFO goes into under-run condition while transmitting. The corresponding transmit done bit is set when active. This bit is updated by hardware along with the TXACK bit at the end of data transmission (this bit is mutually exclusive with TXACK).
0	TXACK	Transmit Acknowledge (read only): Data transmission completed and acknowledge successfully. The corresponding transmission done bit is set when active. This bit is updated by hardware along with the TXERR bit at the end of data transmission (this bit is mutually exclusive with TXERR)

-: unimplemented.

USB Endpoint Interrupt Clear Register USBFI_CLR
(Address: 0x0020_7840) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	USBX6INT_CLR	USBX5INT_CLR	USBX4INT_CLR	USBX3INT_CLR	USBX2INT_CLR	USBX1INT_CLR	USBRX0INT_CLR	USBTX0INT_CLR

User should write “1” to register USBF1_CLR to clear corresponding USBFI interrupt register bit. This register is “write only” and “auto-clear”.

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	USBX6INT_CLR	USB endpoint 6 interrupt clear setting 1: Write “1” to clear USB endpoint 6 interrupt
6	USBX5INT_CLR	USB endpoint 5 interrupt clear setting 1: Write “1” to clear USB endpoint 5 interrupt
5	USBX4INT_CLR	USB endpoint 4 interrupt clear setting 1: Write “1” to clear USB endpoint 4 interrupt
4	USBX3INT_CLR	USB endpoint 3 interrupt clear setting 1: Write “1” to clear USB endpoint 3 interrupt
3	USBX2INT_CLR	USB endpoint 2 interrupt clear setting 1: Write “1” to clear USB endpoint 2 interrupt
2	USBX1INT_CLR	USB endpoint 1 interrupt clear setting 1: Write “1” to clear USB endpoint 1 interrupt
1	USBRX0INT_CLR	USB endpoint 0 receive interrupt clear setting 1: Write “1” to clear USB endpoint 0 receive interrupt
0	USBTX0INT_CLR	USB endpoint 0 transmit interrupt clear setting 1: Write “1” to clear USB endpoint 0 receive interrupt

-: unimplemented.

USB Interrupt Flag Register 2 USBFI2 (Address: 0x0020_7844) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	-	R/W	-	-	-
Name	USBRST_INT	RESUME_INT	SUSPEND_INT	Reserved	SOF_INT	Reserved	Reserved	Reserved

USB Function Interrupt Flag. Contains RESET, REUME, and SUSPEND interrupts. When the corresponding bit is set, it indicates the corresponding interrupt is generated, and the firmware will clear the corresponding bit of Interrupt. These interrupts share the Interrupt source INT2 of CPU (N903-S). Bit 6~3 is reset by USB reset and hardware reset. Bit 7 is reset by hardware reset only.

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	USBRST_INT	1: USB RESET interrupt occurred
6	RESUME_INT	1: USB RESMUE interrupt occurred USB SIE has detected a RESUME signaling on the USB lines. This interrupt is used to terminate the power-down mode.
5	SUSPEND_INT	1: USB SUSPEND interrupt occurred USB SIE has detected a RESUME signaling on the USB lines. The corresponding ISR should put the whole chip into power-down mode.
4	Reserved	-
3	SOF_INT	1: USB SOF interrupt occurred
2-0	Reserved	-

-: unimplemented.

USB Interrupt Enable Register 2 USBFIE2 (Address: 0x0020_7848) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
Name	NAKINT_IE	RESUME_IE	SUSPEND_IE	STALLINT_IE	TGERR_IE	SOF_IE	USBRST_IE	Reserved

For all bits, a “1” means the interrupt is enabled and will cause an interrupt to be signaled to the micro-controller. A “0” means the associated interrupt source is disabled and cannot cause an interrupt. Reset state is by USB reset or hardware reset.

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	NAKINT_IE	NAK interrupt enable setting: 1: Enable USB NAK interrupt, set this bit to enable USB interrupt for hub and function even if ACK, NAK, or STALL handshake is returned. 0: Disable USB NAK interrupt, interrupt only occurred in response to ACK (default).
6	RESUME_IE	RESUME interrupt enable setting: 1: Enable USB RESUME interrupt 0: Disable USB RESUME interrupt (default)

Bit Number	Bit Mnemonic	Description
5	SUSPEND_IE	SUSPEND interrupt enable setting: 1: Enable USB SUSPEND interrupt. An interrupt occurs when the USB signal is suspended for over 3ms. 0: Disable USB SUSPEND interrupt (default)
4	STALLINT_IE	STALL interrupt enable setting: 1: Enable USB STALL interrupt. An interrupt occurs in response to STALL 0: Disable USB STALL interrupt (default)
3	TGERR_IE	RX-TOGGLE-ERROR interrupt enable setting: 1: Enable RX-TOGGLE-ERROR interrupt. An interrupt occurs if data toggle mismatch is found (RX_ERR/RXACK is cleared). 0: Disable RX-TOGGLE-ERROR interrupt (default)
2	SOF_IE	SOF interrupt enable setting: 1: Enable SOF interrupt. An interrupt occurs if SOF is received 0: Disable SOF interrupt (default)
1	USBRST_IE	USB reset interrupt enable setting: 1: Enable USB reset interrupt. An interrupt occurs if USB Reset is received 0: Disable USB reset interrupt (default)
0	Reserved	-

-: unimplemented.

USB Endpoint Replacement Register REP (Address: 0x0020_784C) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	R/W	R/W	R/W
Name	Reserved					REP2	REP1	REP0

This register is used for Endpoint pairing setting, such as Endpoint 6 and Endpoint 1 can be matched as pairing Endpoint 1 input and Endpoint 1 output.

Bit Number	Bit Mnemonic	Description
31-3	Reserved	-
2	REP2	Endpoint 4 & endpoint 3 pairing setting: 1: Endpoint 4 is TX/RX of Endpoint 3 0: Endpoint 4 remains original setting (default)
1	REP1	Endpoint 5 & Endpoint 2 pairing setting: 1: Endpoint 5 is TX/RX of Endpoint 2 0: Endpoint 5 remains original setting (default)
0	REP0	Endpoint 6 & Endpoint 1 pairing setting: 1: Endpoint 6 is TX/RX of Endpoint 1 0: Endpoint 6 remains original setting (default)

-: unimplemented.

USB Transmit / Receive Flag Register TXEN (Address: 0x0020_7850) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	-	R
Name	Reserved							TXEN

Bit Number	Bit Mnemonic	Description
31-1	Reserved	-
0	TXEN	Read only TXEN = 0, SETUP or OUT token. TXEN = 1, IN token

-: unimplemented.

USB Receive Data Register RXDAT (Address: 0x0020_7860) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	RXDAT[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	RXDAT[7:0]	Receive data register (read only): To write data to the receive FIFO, the SIL writes to this register. To read data from the receive FIFO, the CPU reads from this register. The write pointer and read pointer are incremented automatically after a write and read, respectively.

-: unimplemented.

USB Receive Control Register RXCON (Address: 0x0020_7864) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	-	-	R/W	-	-	-	-
Name	RXCLR	Reserved		RXFFRC	Reserved			

This register is used to control the receive FIFO specified by EPINDEX. Reset state is by USB reset or hardware reset.

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	RXCLR	Clear Receive FIFO Buffer setting: 1: Set this bit to flush the entire receive FIFO. All flags in RXFLG revert their reset states (RXEMP is set; all other flags clear). Hardware clears this bit when the flush operation is complete.
6-5	Reserved	-
4	RXFFRC	Receive FIFO Buffer Read Complete setting: 1: Set this bit to release the receive FIFO when a data set read is complete. Setting this bit clears the RXFLG.RXFULL bit corresponding to the data set that was just read. Hardware clears this bit after the RXFULL bit is cleared. All data from this bit set must have been read. Note that FIFO Read Complete only work if STOVW and EDOVW are cleared.
3-0	Reserved	-

-: unimplemented.

USB Receive Flag Register RXFLG (Address: 0x0020_7868) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	-	R	R	R/W	R/W
Name	SENDNAK	SENDSTALL	TGERR	Reserved	RXEMP	RXFULL	RXURF	RXOVF

These flags indicate the status of data packets in the Receive FIFO specified by EPINDEX. Reset state is by USB reset or hardware reset.

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	SENDNAK	NAK flag (read-, clear-only): 1: this flag indicates a NAK is returned to host while NAKINT_IE is set.
6	SENDSTALL	STALL flag (read-, clear-only): 1: this flag indicates a STALL returned to host while STALLINT_IE is set.
5	TGERR	Receive Data Toggle Error Flag (read-, clear-only): 1: this flag indicates data toggle error is found while TGERR_IE is set.
4	Reserved	-
3	RXEMP	Receive FIFO Buffer Empty Flag (read-only): 1: hardware sets this bit when the data set has been read out of the receive FIFO. Hardware clears this bit when the empty condition no longer exists. This is not a sticky bit and always tracks the current status. This flag is also set when a zero-length packet is received.
2	RXFULL	Receive FIFO Buffer is Full Flag (read-only): 1: this flag indicates the data set is present in the receive FIFO. Hardware sets this bit when the data set has been successfully received. This bit is cleared after write to RXCNT to reflect the condition of the data set. Likewise, this bit is cleared after setting of the RXFFRC bit.
1	RXURF	Receive FIFO Buffer Data Under-run Flag (read-, clear-only) 1: Hardware sets this bit when an additional byte is read from an empty receive FIFO. This bit is cleared through firmware by writing a “0” to this bit. When the receive FIFO under-runs, the read-pointer will not advance – it remains locked in the empty position. When set, all transmission are NAKed.
0	RXOVF	Receive FIFO Buffer Data Overrun Flag (read-, clear-only) 1: This bit is set when the SIL writes an additional byte to a receive FIFO with RXFULL = 1, and the write pointer will not advance – it remains locked in the full position. This is a sticky bit that must be

Bit Number	Bit Mnemonic	Description
		cleared through firmware by writing a “0” to this bit, although it can be cleared by hardware if a SETUP packet is received after a RXOVF error had already occurred. When set, all transmission are NAKed.

-: unimplemented.

USB Receive Byte Count Register RXCNT (Address: 0x0020_786C) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R	R	R	R	R	R	R
Name	Reserved	RXCNT[6:0]						

This register is used to store the number of byte for the data packet received in the FIFO specified by EPINDEX. Reset state is by USB reset or hardware reset.

Bit Number	Bit Mnemonic	Description
31-7	Reserved	-
6-0	RXCNT[6:0]	Receive FIFO Buffer Byte Count (read-only): The number of bytes in data set written to the receive FIFO. When this register is written, RXFULL is not set until reception is successfully acknowledged. After the SIL writes a data set to the RXFIFO, it writes the byte count to this register. The CPU reads the byte count from this register to determine how many bytes to read from the RXFIFO.

-: unimplemented.

USB Receive Status Register RXSTAT (Address: 0x0020_7870) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R	R/W	-	R	R	R
Name	RXSEQ	RXSETUP	STOVW	EDOVW	Reserved	RXVOID	RXERR	RXACK

Contains the current endpoint status of the receive FIFO specified by EPINDEX.

Reset state is by USB reset or hardware reset.

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7	RXSEQ	Receive Endpoint Sequence Bit (read, clear-only): This bit will be toggled on completion of an ACK handshake in response to an OUT token. This bit will be set (or created) by hardware after reception of SETUP token. This SIE will handle all sequence bit tracking. This bit should only be used when initialing a new configuration or interface. If you don't want to change sequence bit, set this bit to "1" when you write this register.
6	RXSETUP	Receive SETUP Token (read-, clear-only): This bit is set by hardware when a valid SETUP token has been received. When SIL set this bit, it causes received IN or OUT token to be NAKed until this bit is cleared to allow a control transaction to clear a stalled endpoint. Clear this bit upon detection of a SETUP token after the firmware is ready to complete the setup stage of control transaction.
5	STOVW	Start Overwrite Flag (read-only): Set by hardware upon receipt of SETUP token for any control endpoint to indicate that the receive FIFO is being overwritten with new SETUP data. When set, the FIFO state (RXFILL and read pointer) resets and is locked for this endpoint until EDOVW is set. This prevents a prior, ongoing firmware read from corrupting the read pointer as the receive FIFO is being cleared and new data is being written into it. This bit is cleared by hardware at the end of handshake phase transmission of the setup stage. This bit is used only for control endpoint.
4	EDOVW	End Overwrite Flag (read-, clear-only): This flag is set by hardware during the handshake phase of a SETUP stage. It is set after every SETUP packet is received and must be cleared prior to reading the contents of the FIFO. When set, the FIFO state (RXFULL and read pointer) remains locked for this endpoint until this bit is cleared. This prevents a prior, ongoing firmware read from corrupting the read pointer after the new data has been written into the receive FIFO. This bit is only used for control endpoint. Note: Make sure the EDOVW bit is cleared prior to reading the contents of the receive FIFO.
3	Reserved	Write zero to this bit.
2	RXVOID	Receive Void Condition (read-only): This bit is set when no valid data is received in response to a SETUP or OUT token due to one of the following conditions: 1. The receive FIFO is still locked. 2. The EPCON register's RXSTL bit is set. This bit is set and cleared by hardware. This bit is updated by hardware at the end of the transaction in response to a valid OUT token.

Bit Number	Bit Mnemonic	Description
1	RXERR	Receive Error status (read-only) Set when an error condition has occurred with reception. Complete or partial data has been written into the receive FIFO. No handshake is returned. The error can be one of the following conditions: 1. Data failed CRC check 2. Bit stuffing error 3. A receive FIFO goes into overrun or underrun condition while receiving. This bit is updated by hardware at the end of a valid SETUP or OUT token transaction. The corresponding receive done bit is set when active. This bit updated with the RXACK bit at the end of data reception and is mutually exclusive with RXACK.
0	RXACK	Receive ACK status (read-only): This bit is set when data is received completely into a receive FIFO and an ACK handshake is sent. This read-only bit is updated by hardware at the end of valid SETUP or OUT token transaction. The corresponding receive done bit when active. This bit is updated with the RXERR bit at the end of data reception and is mutually exclusive with RXERR.

-: unimplemented.

USB Asynchronous Endpoints Control Register description:

USB Endpoint 7 Control Register EP7_CON (Address: 0x0020_7880) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved						EP7_DMA_EN	EP7_EN

Bit Number	Bit Mnemonic	Description
31-2	Reserved	-
1	EP7_DMA_EN	USB endpoint 7 DMA transfer enable setting 1: Enable endpoint 7 DMA transfer 0: Disable endpoint 7 DMA transfer (default)
0	EP7_EN	USB endpoint 7 enable setting 1: Enable endpoint 7 function 0: Disable endpoint 7 function (default)

-: unimplemented.

USB Endpoint 7 Status Register EP7_STA (Address: 0x0020_7884) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	R	-	-	R	R
Name	Reserved			EP7_TX_FULL	Reserved		EP7_TX_LEN[9:8]	
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	EP7_TX_LEN[7:0]							

Bit Number	Bit Mnemonic	Description
31-13	Reserved	-
12	EP7_TX_FULL	USB endpoint 7 transmit FIFO buffer is full status 1: Endpoint 7 (EP7) transmit FIFO buffer is full
11-10	Reserved	-
9-0	EP7_TX_LEN[9:0]	Transmit FIFO data length

-: unimplemented.

USB Endpoint 7 BASE Register EP7_BASE (Address: 0x0020_7888) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	R/W
Name	Reserved							EP7_BASE[8]
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	EP7_BASE[7:0]							

Bit Number	Bit Mnemonic	Description
31-9	Reserved	-
8-0	EP7_BASE[8:0]	Endpoint 7(EP7) Transmit FIFO Buffer Base pointer setting: Endpoint 7 & endpoint 8 share 512 bytes of FIFO buffer. Use this register to set endpoint 7 transmit FIFO buffer base pointer location

-: unimplemented.

USB Endpoint 7 LIMIT Register EP7_LIMIT (Address: 0x0020_788C) Reset Value: 0x0000_0100

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	R/W
Name	Reserved							EP7_LIMIT[8]
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	EP7_LIMIT[7:0]							

Bit Number	Bit Mnemonic	Description
31-9	Reserved	-
8-0	EP7_LIMIT[8:0]	Endpoint 7 (EP7) transmit FIFO buffer size setting: Endpoint 7 & endpoint 8 share 512 bytes of FIFO buffer. Use this register to set endpoint 7 transmit FIFO buffer size

-: unimplemented.

USB Endpoint 7 Data Register EP7_W_BYTE (Address: 0x0020_7890) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	EP7_W_BYTE[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	EP7_W_BYTE[7:0]	Endpoint 7 (EP7) transmit FIFO buffer Data Write Register

-: unimplemented.

USB Endpoint 8 Control Register EP8_CON (Address: 0x0020_78A0) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved						EP8_DMA_EN	EP8_EN

Bit Number	Bit Mnemonic	Description
31-2	Reserved	-
1	EP8_DMA_EN	USB endpoint 8 DMA transfer enable setting 1: Enable endpoint 8 DMA transfer 0: Disable endpoint 8 DMA transfer (default)
0	EP8_EN	USB endpoint 8 enable setting 1: Enable endpoint 8 function 0: Disable endpoint 8 function (default)

-: unimplemented.

USB Endpoint 8 Status Register EP8_STA (Address: 0x0020_78A4) Reset Value: 0x0000_0800

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	R	R	R	R
Name	Reserved				EP8_RX_EMPTY	EP8_RX_ERR	EP8_RX_LEN[9:8]	
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	EP8_RX_LEN[7:0]							

Bit Number	Bit Mnemonic	Description
31-12	Reserved	-
11	EP8_RX_EMPTY	USB endpoint 8 receive FIFO buffer is empty 1: Endpoint 8 (EP8) receive FIFO buffer is empty
10	EP8_RX_ERR	USB endpoint 8 error status 1: Endpoint 8 (EP8) packet error (CRC ERROR)
9-0	EP8_RX_LEN[9:0]	Endpoint 8 (EP8) receive FIFO buffer data length

-: unimplemented.

USB Endpoint 8 BASE Register EP8_BASE (Address: 0x0020_78A8) Reset Value: 0x0000_0100

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	R/W
Name	Reserved							EP8_BASE[8]
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	EP8_BASE[7:0]							

Bit Number	Bit Mnemonic	Description
31-9	Reserved	-
8-0	EP8_BASE[8:0]	Endpoint 8 (EP8) Receive FIFO Buffer Base Pointer setting: Endpoint 7 & Endpoint 8 share 512 bytes of FIFO Buffer. Use this register to set Endpoint 8 Receive FIFO Buffer base pointer location

-: unimplemented.

USB Endpoint 8 LIMIT Register EP8_LIMIT (Address: 0x0020_78AC) Reset Value: 0x0000_0100

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	R/W
Name	Reserved							EP8_LIMIT[8]
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	EP8_LIMIT[7:0]							

Bit Number	Bit Mnemonic	Description
31-9	Reserved	-
8-0	EP8_LIMIT[8:0]	Endpoint 8 (EP8) receive FIFO buffer size setting: Endpoint 7 & endpoint 8 share 512 bytes of FIFO Buffer. Use this register to set endpoint 8 transmit FIFO buffer size

-: unimplemented.

USB Endpoint 8 data register EP8_R_BYTE (Address: 0x0020_78B0) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	EP8_R_BYTE[7:0]							

Bit Number	Bit Mnemonic	Description
31-8	Reserved	-
7-0	EP8_R_BYTE[7:0]	Endpoint 8 (EP8) receive FIFO buffer data read register

-: unimplemented.

USB SOF Status Register USB_SOF_FRAME (Address: 0x0020_78C0) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	R	R	R	R	R
Name	Reserved			FRAME_MISS	FRAME_ERROR	FRAM[10:8]		
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	FRAM[7:0]							

Bit Number	Bit Mnemonic	Description
31-13	Reserved	-
12	FRAME_MISS	USB frame is missed 1: indicates expected SOF packet is missed (valid only when PSOF function is enabled)
11	FRAME_ERROR	USB frame error status 1: indicates last SOF packet has error
10-0	FRAM[10:0]	USB frame number

6.20 Low Voltage Detection (LVD)

6.20.1 Features

WT59F164 has a built-in Low Voltage Detection circuitry which can monitor the supply voltage (3.3V) drops below the configured voltage threshold then generates an interrupt.

- The Enable and Disable function of Low Voltage Detection are controlled by the software (special Register SYS_OPTION3.LVDON)
- Low Voltage Detection level provides 8-level of voltage for selection which can be configured by software (special Register SYS_OPTION3.LVD_LEVEL[2:0]) with setting value as below:
  LVD VOLTAGE = 2.2V+0.1* LVD_LEVEL[2:0]
- Tell whether low power low level status occurred by Register SYS_RES2.LVDF

6.20.2 Special Register

Register Name	Address	Reset Default (Hex)	Description
System Register & Low Voltage Detection and Reset Register (System Control)			**0x0020_0000~0x0020_03FF**
SYS_OPTION3	0x0020_0024	0x0000_0010	LVD setting
SYS_RES2	0x0020_0028		LVD flag

System Control Register 3 SYS_OPTION3 (Address: 0x0020_0024) Reset Value: 0x0000_0010

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved						EN_MCUCLK_O[2:1]	
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	EN_MCUCLK_O[0]	EN_32KCLK_I	EN_32KCLK_O	LVD_LEVEL[2:0]			LVRON	LVDON

Bit Number	Bit Mnemonic	Description
31-10	Reserved	-
9-7	EN_MCUCLK_O[2:0]	MCU clock output selection (output from GPIOA[8]) xx0: Disable MCU clock output to GPIOA[8] (default) 001: MCU clock output to GPIOA[8] 011: MCU clock/2 output to GPIOA[8] 101: AUX_PLL clock output to GPIOA[8] 111: USB_PLL clock output to GPIOA[8]
6	EN_32KCLK_I	(Testing purpose) 1: 32K clock source is GPIOA[8]
5	EN_32KCLK_O	(Testing purpose) 1: 32K clock output to GPIOA[8]

Bit Number	Bit Mnemonic	Description
4-2	LVD_LEVEL[2:0]	Low Voltage Detection (LVD) voltage detection setting (Reset by POR) LVD detection voltage = 2.2 + 0.1* LVD_LEVEL[2:0]
1	LVRON	Low Voltage Reset (LVR) enable 1: Enable low voltage reset 0: Disable low voltage reset (default)
0	LVDON	Low voltage detection (LVD) enable setting 1: Enable low voltage detection 0: Disable low voltage detection (default)

-: unimplemented.

Low Voltage Detection Status Register SYS_RES2 (Address: 0x0020_0028) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	-	R
Name	Reserved							LVDF

Bit Number	Bit Mnemonic	Description
31-1	Reserved	-
0	LVDF	Low Voltage Detection (LVD) status flag 1: detected low voltage

-: unimplemented.

6.21 Emulated E²PROM

6.21.1 Features

The WT59F164 can use Flash PROM space to emulate E²PROM.

- All Flash space is 16384x32 + 512x32
- Supports Page Erase, each Page unit is 1024 bytes
- Single write 4 bytes; when enable multi-word operation, single write up to 32 bytes

6.21.2 Special Register

Register Name	Address	Reset Default (Hex)	Description
Emulated E²PROM Register (Flash Programmer) 0x0020_0400~0x0020_07FF			
EER_EN0	0x0020_0400	0x0000_0000	Emulated E²PROM function enable setting
EER_EN1	0x0020_0404	0x0000_0000	Emulated E²PROM function enable setting
EER_ADDR	0x0020_0408	0x0000_0000	Emulated E²PROM address setting
EER_CTL	0x0020_040C	0x0000_0008	Emulated E²PROM function setting
EER_W_DATA	0x0020_0410	0x0000_0000	Emulated E²PROM write data buffer
EER_WAKEUP_ENABLE	0x0020_0414	0x0000_0001	Emulated E²PROM wakeup enable & status
EER_R_DATA	0x0020_0418		Emulated E²PROM read data buffer
EER_WAKEUP_ENABLE_EXT	0x0020_041C	0x0000_0001	Emulated E²PROM wakeup enable & status
EER_W_DATA0	0x0020_0420	0x0000_0000	Emulated E²PROM write data buffer
EER_W_DATA1	0x0020_0424	0x0000_0000	Emulated E²PROM write data buffer
EER_W_DATA2	0x0020_0428	0x0000_0000	Emulated E²PROM write data buffer
EER_W_DATA3	0x0020_042C	0x0000_0000	Emulated E²PROM write data buffer
EER_W_DATA4	0x0020_0430	0x0000_0000	Emulated E²PROM write data buffer
EER_W_DATA5	0x0020_0434	0x0000_0000	Emulated E²PROM write data buffer
EER_W_DATA6	0x0020_0438	0x0000_0000	Emulated E²PROM write data buffer
EER_W_DATA7	0x0020_043C	0x0000_0000	Emulated E²PROM write data buffer
EER_ADDR_EXT	0x0020_0440	0x0000_0000	Emulated E²PROM address setting
EER_CTL_EXT	0x0020_0444	0x0000_0008	Emulated E²PROM function setting

E²PROM Enable Register 0 EER_EN0 (Address: 0x0020_0400) Reset Value:0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	W	W	W	W
Name	Reserved				FP_EN0[3:0]			

Bit Number	Bit Mnemonic	Description
31-4	Reserved	-
3-0	FP_EN0[3:0]	E^2PROM Enable Register 0, FP_EN0[3:0] = 0x0A & FP_EN1[3:0] = 0x05 to enable E^2PROM function

-: unimplemented.

E^2PROM Enable Register 1 EER_EN1 (Address: 0x0020_0404) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	W	W	W	W
Name	Reserved				FP_EN1[3:0]			

Bit Number	Bit Mnemonic	Description
31-4	Reserved	-
3-0	FP_EN1[3:0]	E^2PROM Enable Register 1, FP_EN1[3:0] = 0x05 & FP_EN0[3:0] = 0x0A to enable E^2PROM function

-: unimplemented.

E^2PROM Address Setting Register EER_ADDR (Address: 0x0020_0408) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved		FP_ADDR[13:8]					
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	FP_ADDR[7:0]							

Bit Number	Bit Mnemonic	Description
31-14	Reserved	-
13-0	FP_ADDR[13:0]	E^2PROM Address Setting. FP_ADDR[2:0] should be 0 for multi-word programming operation. The address directed by FP_ADDR[13:0] x 4 is the actual Flash ROM Address.

-: unimplemented.

E^2PROM Control Register EER_CTL (Address: 0x0020_040C) Reset Value:0x0000_0008

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	W	W
Name	Reserved						FP_VERIFY	FP_MAS1
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	FP_READ	FP_IFREN	FP_ERASE	FP_PROG	FP_TCTL[3:0]			

Bit Number	Bit Mnemonic	Description
31-10	Reserved	-
9	FP_VERIFY	E^2PROM verify enable setting 1: FP verify (auto clear) (only supports multi-word mode)
8	FP_MAS1	E^2PROM mass erase enable setting 1: FP mass erase (auto clear)
7	FP_READ	E^2PROM Read Enable setting 1: FP read (auto clear)
6	FP_IFREN	FLASH section selection operation 1: INFORMATION BLOCK enable 0: data block enable (64K bytes program section)
5	FP_ERASE	E^2PROM Page Erase enable setting 1: FP Erase (auto clear)
4	FP_PROG	E^2PROM Program enable setting 1: FP program (auto clear) (single word if use this reg)
3-0	FP_TCTL[3:0]	E^2PROM Page Erase & Program time setting Program time = (TCLT-1)*4 us Erase time = (TCLT+2)*4 ms

-: unimplemented.

E²PROM Data Write Register EER_W_DATA (Address: 0x0020_0410) Reset Value: 0x0000_0000

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA[31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA[23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	FP_WDATA[31:0]	E²PROM Data Write Register

-: unimplemented.

E²PROM Status Register EER_WAKEUP_ENABLE (Address: 0x0020_0414) Reset Value: 0x0000_0001

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	R/W	R/W	R/W
Name						VERIFY_FLG	DONE_FLG	FP_WAKEUP_EN

Bit Number	Bit Mnemonic	Description
31-3	Reserved	-
2	VERIFY_FLG	E²PROM verify status flag 1: 32 bytes data are verified ok (only supports multi-word mode), it can be cleared by setting this bit to be 1 or write data to register EER_CTL or EER_EXT_CTL
1	DONE_FLG	E²PROM done flag 1: when the Mass Erase, Page Erase, Program, Read or Verify process is finished, it can be cleared by setting this bit to be 1 or write data to register EER_CTL or EER_EXT_CTL

Bit Number	Bit Mnemonic	Description
0	FP_WAKEUP_EN	E^2PROM wakeup enable setting 1: MCU will enter standby mode when flash is programmed and be wakeup after programming is finished (default). 0: MCU will stop to fetch instruction when flash is programmed and start to fetch instruction after programming is finished.

-: unimplemented.

E^2PROM Data Read Register EER_R_DATA (Address: 0x0020_0418) Reset Value:

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	W	W	W	W	W	W	W	W
Name	FP_RDATA[31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	W	W	W	W	W	W	W	W
Name	FP_RDATA[23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	FP_RDATA[15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	FP_RDATA[7:0]							

Bit Number	Bit Mnemonic	Description
31-0	FP_RDATA[31:0]	E^2PROM Data Read Register

-: unimplemented.

E^2PROM Extend Status Register
EER_WAKEUP_ENABLE_EXT (Address: 0x0020_041C) Reset Value: 0x0000_0001

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	R/W	R/W	R/W
Name						VERIFY_FLG	DONE_FLG	FP_WAKEUP_EN

Bit Number	Bit Mnemonic	Description
31-3	Reserved	-
2	VERIFY_FLG	E^2PROM Verify Status Flag in programming multi-word operation 1: 32 bytes data are verified ok (only supports multi-word mode), it can be cleared by setting this bit to be 1 or write data to register EER_CTL or EER_EXT_CTL
1	DONE_FLG	E^2PROM Done Flag in programming multi-word operation 1: when the Mass Erase, Page Erase, Program, Read or Verify process is finished, it can be cleared by setting this bit to be 1 or write data to register EER_CTL or EER_EXT_CTL
0	FP_WAKEUP_EN	E^2PROM Wakeup Enable setting in programming multi-word operation 1: MCU will enter standby mode when flash is programmed and be wakeup after programming is finished (default). 0: MCU will stop to fetch instruction when flash is programmed and start to fetch instruction after programming is finished.

-: unimplemented.

E^2PROM Extend Data Write Register 0 EER_W_DATA0
(Address: 0x0020_0420) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA0 [31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA0 [23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA0 [15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA0 [7:0]							

Bit Number	Bit Mnemonic	Description
31-0	FP_WDATA0[31:0]	E2PROM Extend Data Write Register 0

-: unimplemented.

E^2PROM Extend Data Write Register 1 EER_W_DATA1
(Address: 0x0020_0424) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA1 [31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA1 [23:16]							

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA1 [15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA1 [7:0]							

Bit Number	Bit Mnemonic	Description
31-0	FP_WDATA1[31:0]	E^2PROM Extend Data Write Register 1

-: unimplemented.

E^2PROM Extend Data Write Register 2 EER_W_DATA2
(Address: 0x0020_0428) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA2 [31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA2 [23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA2 [15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA2 [7:0]							

Bit Number	Bit Mnemonic	Description
31-0	FP_WDATA2[31:0]	E^2PROM Extend Data Write Register 2

-: unimplemented.

E^2PROM Extend Data Write Register 3 EER_W_DATA3
(Address: 0x0020_042C) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA3 [31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA3 [23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA3 [15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA3 [7:0]							

Bit Number	Bit Mnemonic	Description
31-0	FP_WDATA3[31:0]	E^{2}PROM Extend Data Write Register 3

-: unimplemented.

E^{2}PROM Extend Data Write Register 4 EER_W_DATA4
(Address: 0x0020_0430) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA4 [31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA4 [23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA4 [15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA4 [7:0]							

Bit Number	Bit Mnemonic	Description
31-0	FP_WDATA4[31:0]	E^{2}PROM Extend Data Write Register 4

-: unimplemented.

E^{2}PROM Extend Data Write Register 5 EER_W_DATA5
(Address: 0x0020_0434) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA5 [31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA5 [23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA5 [15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA5 [7:0]							

Bit Number	Bit Mnemonic	Description
31-0	FP_WDATA5[31:0]	E^{2}PROM Extend Data Write Register 5

-: unimplemented.

E²PROM Extend Data Write Register 6 EER_W_DATA6
(Address: 0x0020_0438) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA6 [31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA6 [23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA6 [15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA6 [7:0]							

Bit Number	Bit Mnemonic	Description
31-0	FP_WDATA6[31:0]	E²PROM Extend Data Write Register 6

-: unimplemented.

E²PROM Extend Data Write Register 7 EER_W_DATA7
(Address: 0x0020_043C) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA7 [31:24]							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA7 [23:16]							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA7 [15:8]							
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	FP_WDATA7 [7:0]							

Bit Number	Bit Mnemonic	Description
31-0	FP_WDATA7[31:0]	E²PROM Extend Data Write Register 7

-: unimplemented.

E²PROM Extend Address Setting Register EER_ADDR_EXT
(Address: 0x0020_0440) **Reset Value: 0x0000_0000**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							

Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved		FP_ADDR_EXT[13:8]					
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	FP_ADDR_EXT[7:0]							

Bit Number	Bit Mnemonic	Description
31-14	Reserved	-
13-0	FP_ADDR_EXT[13:0]	E^2PROM address setting while using multi-word operation, EER_EXT_ADDR[2:0] must be cleared. The address directed by EER_EXT_ADDR[13:0] x 4 is the actual Flash ROM Address.

-: unimplemented.

E^2PROM Extend Control Register EER_CTL_EXT
(Address: 0x0020_0444) **Reset Value: 0x0000_0008**

Bit	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Status	-	-	-	-	-	-	-	-
Name	Reserved							
Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Status	-	-	-	-	-	-	W	W
Name	Reserved						FP_VERIFY	FP_MAS1
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	FP_READ	FP_IFREN	FP_ERASE	FP_PROG	FP_TCTL[3:0]			

Bit Number	Bit Mnemonic	Description
31-10	Reserved	-
9	FP_VERIFY	E^2PROM Verify enable setting 1: FP verify (auto clear) (only supports multi-word mode)
8	FP_MAS1	E^2PROM Mass Erase enable setting 1: FP mass erase (auto clear)
7	FP_READ	E^2PROM Read enable setting 1: FP read (auto clear)
6	FP_IFREN	FLASH block selection operation 1: INFORMATION BLOCK section 0: Data section (64K bytes program section) (default)
5	FP_ERASE	E^2PROM Page Erase enable setting 1: FP Erase (auto clear)

Bit Number	Bit Mnemonic	Description
4	FP_PROG	E^2PROM Program enable setting 1: FP program (auto clear) (single word if use this reg)
3-0	FP_TCTL[3:0]	E^2PROM Page Erase & Program time setting Program time = (TCLT-1)*4 us Erase time = (TCLT+2)*4 ms

-: unimplemented.

Note:

1. In programming, erasing, or ready, E^2PROM, all function are halt state of 8051.
2. The time required during WT59F164 programming or erasing E^2PROM data:
   Programming time = 20 μsec ~ 40 μsec
   Erasing time = 20 msec ~ 40 msec

6.22 Read Out Protection

WT59F164 with program code read out protection which prevents program code been read out. When Address 0x200 in Information Block of Flash ROM did not equal to 0xAA, the content of Flash ROM cannot be read out.

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Min.	Max.	Units
D.C. Supply Voltage		3.6	V
Ambient Temperature	-40	85	℃
Storage Temperature	-60	150	℃

7.2 Recommended Operating Parameters

Parameter	Symbol	Condition	Specification			Units
			Min.	Typ.	Max.	
Power Voltage 3.3V	V_{DD33}			3.3		V
Operating Temperature	T_{OPR}		-40		85	℃

7.3 Power Supply

Parameter	Symbol	Condition	Specification			Units
			Min.	Typ.	Max.	
Normal mode at 24 MHz Working Current	I_{VDD24M}	No load on output		22		mA
Normal mode at 12 MHz Working Current	I_{VDD12M}	No load on output		12		mA
SUSPEND mode	$I_{VDDSUSP}$	No load on output		10		μA

7.4 Digital I/O

Parameter	Symbol	Condition	Specification			Units
			Min.	Typ.	Max.	
Schmitt Trigger Low-to-High threshold Point	V_{T+}		2.0		5.5	V
Schmitt Trigger High-to-Low threshold Point	V_{T-}		-0.3		0.8	V
Output High Voltage	V_{OH}	I_{OH} = 8mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
Input Leakage Current	I_{OZ}	V_O = 0V or 3.3V		±0.01	±1	μA
Pull-Up Resistor	R_{PH}			47		KΩ
Pull-Down Resistor	R_{PD}			47		KΩ

7.5 Low VDD Reset

Parameter	Symbol	Condition	Specification			Units
			Min.	Typ.	Max.	
Low VDD18 Reset Voltage	V_{LVD18}		1.3	1.4	1.5	V
Low VDD18 Reset Current	I_{LVD18}	VDD18 = 1.8V		25		μA

7.6 A/D Converter (VDD = 3.3V) (-40℃ ~ +85℃)

Parameter	Symbol	Condition	Specification			Units
			Min.	Typ.	Max.	
Resolution				9		bit
Integral Nonlinearity Error (including INL, DNL..)		V_{REF} = 3.3V, VDD33 = 3.3V		2		LSB
Input Voltage	V_{ADCIN}		VSS		VREF	V
ADC Reference Voltage	V_{REF}		1		AVDD	V
ADC Frequency	F_{ADC}			2		MHz
ADC Current	I_{ADC}	VDD33 = 3.3V		2		mA

7.7 Internal 3.3V to 1.8V LDO (VDD = 3.3V) (-40℃ ~ +85℃)

Parameter	Symbol	Condition	Specification			Units
			Min.	Typ.	Max.	
LDO 1.8V Power Current @VDD = 3.3V	I_{VDDC33}			50		mA
LDO 1.8V Power Current @VDD = 2.0V	I_{VDDC20}			10		mA

7.8 Internal 12 MHz RC Oscillator Temperature Tolerance table (-40℃ ~ +85℃)

Parameter	Symbol	Condition	Specification			Units
			Min.	Typ.	Max.	
RC Frequency	F_{RC}	VDD33 = 3.3V		12		MHz
Frequency Tolerance	$\Delta F_{RC}/F_{RC}$	Without crystal oscillator calibration		± 5		%
		With crystal oscillator calibration			± 2	%

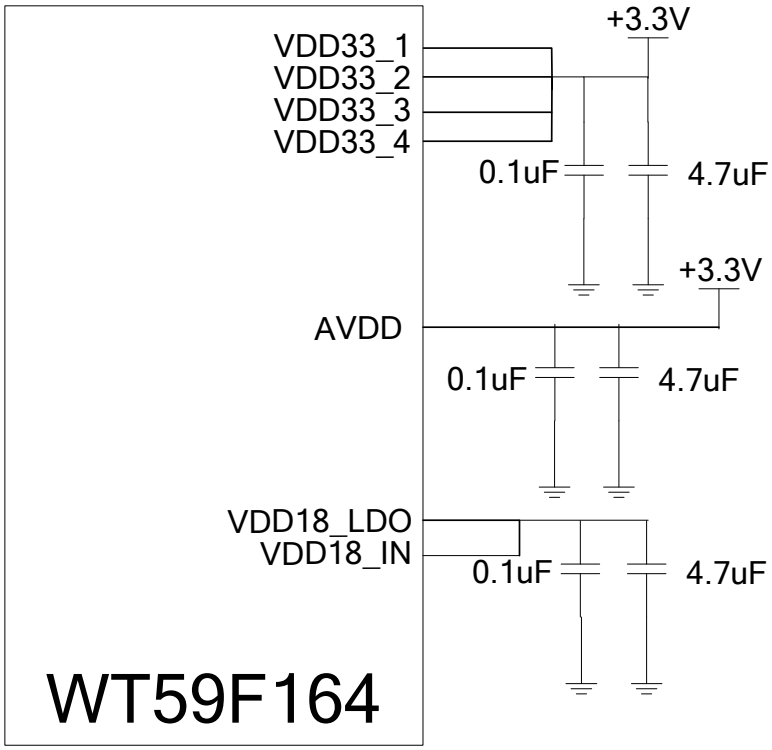
Parameter	Symbol	Condition	Specification			Units
			Min.	Typ.	Max.	
RCOSC Current	I_{RCOSC}	VDD33 = 3.3V			50	μA

7.9 External 32.768 kHz Oscillator Temperature Tolerance table (-40℃ ~ +85℃)

Parameter	Symbol	Condition	Specification			Units
			Min.	Typ.	Max.	
RC Frequency	F_{RC}			32.768		kHz
Load Capacitance	C_L			12.5		pF
External Capacitance	C1/C2					Pf
Frequency Tolerance	$\Delta F/F_O$	At 25℃		30		ppm
Frequency Shift	$\Delta F/F_O$	-10℃~70℃		+10 -100		ppm
RTC Working Current	I_{DDRTC}	VDD33 = 3.3V			2	μA

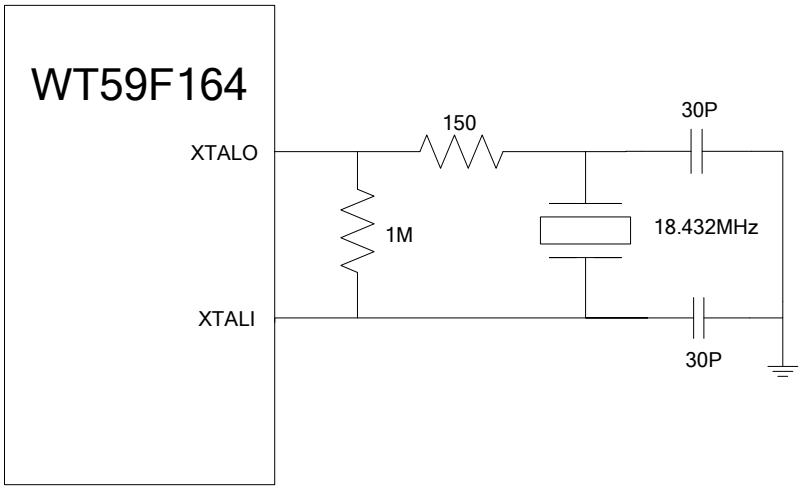
8. Application Circuits

8.1 Power Supply



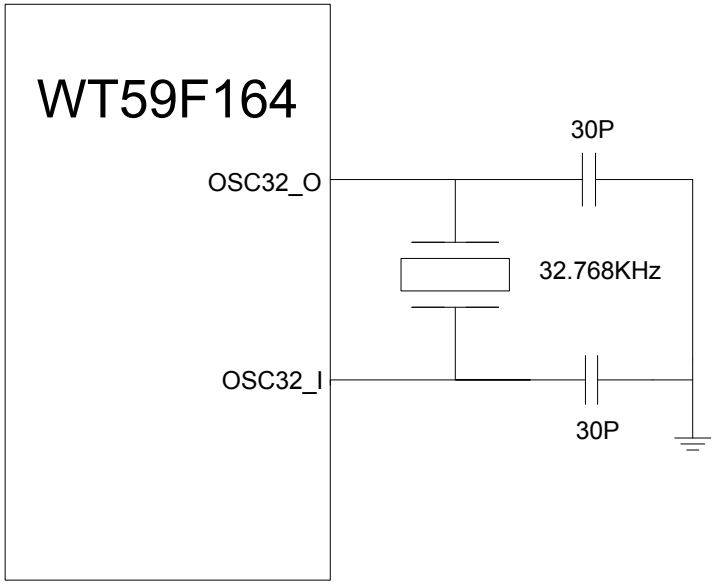
8.2 Oscillator Circuits

8.2.1 External 18.432 MHz Crystal Oscillator

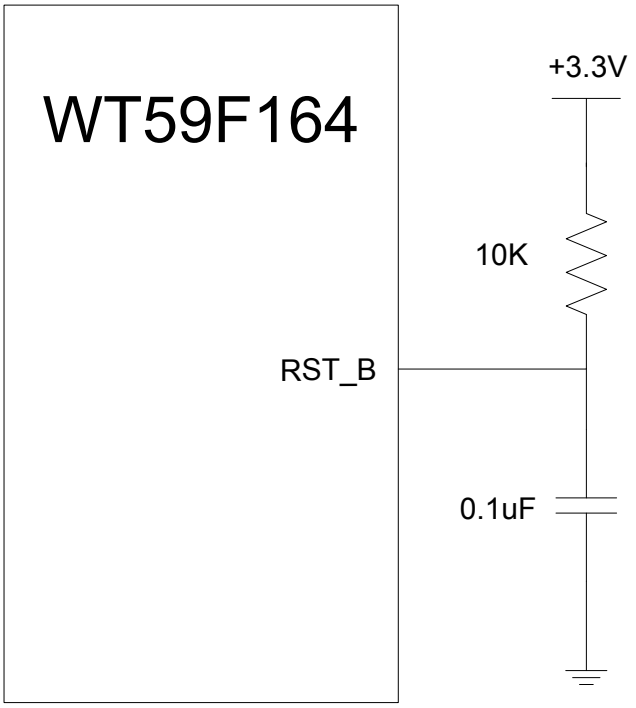


Note: WT59F164 has built-in internal 12/24 MHz RC oscillators, thus external crystal oscillators are not essential. If for more precise application, external crystal oscillator is available for use.

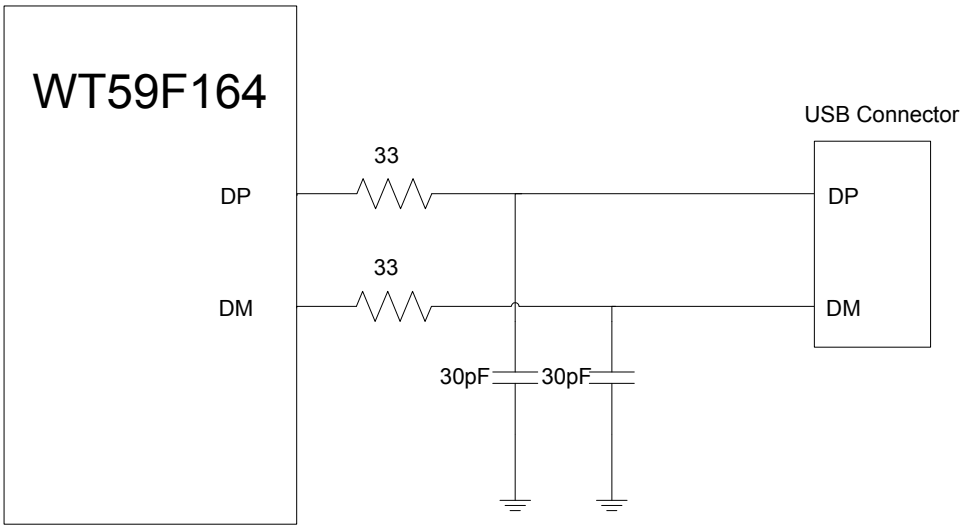
8.2.2 External 32.768 kHz Crystal Oscillator



8.3 RESET Circuit



8.4 USB DP/DM Circuit



9. Ordering Information

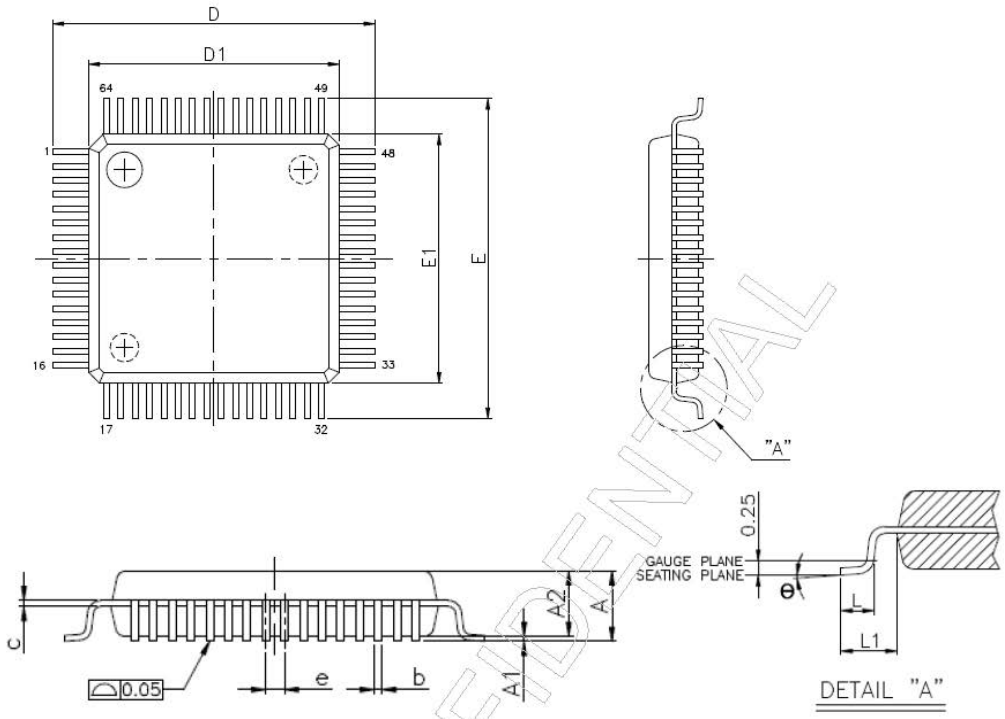
Package Type	Package Outline	Part Number
64-pin LQFP	7mm x 7mm	59F164-RG64AWT
48-pin LQFP	7mm x 7mm	59F164-RG48AWT
32-pin QFN	5mm x 5mm	59F164-UG32AWT

10. Package Dimension

10.1 64-Pin LQFP

Low-Profile Quad Flat Package

LQFP-64 PIN



SYMBOLS	MIN	NOR	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	-	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ°	0	3.5	7

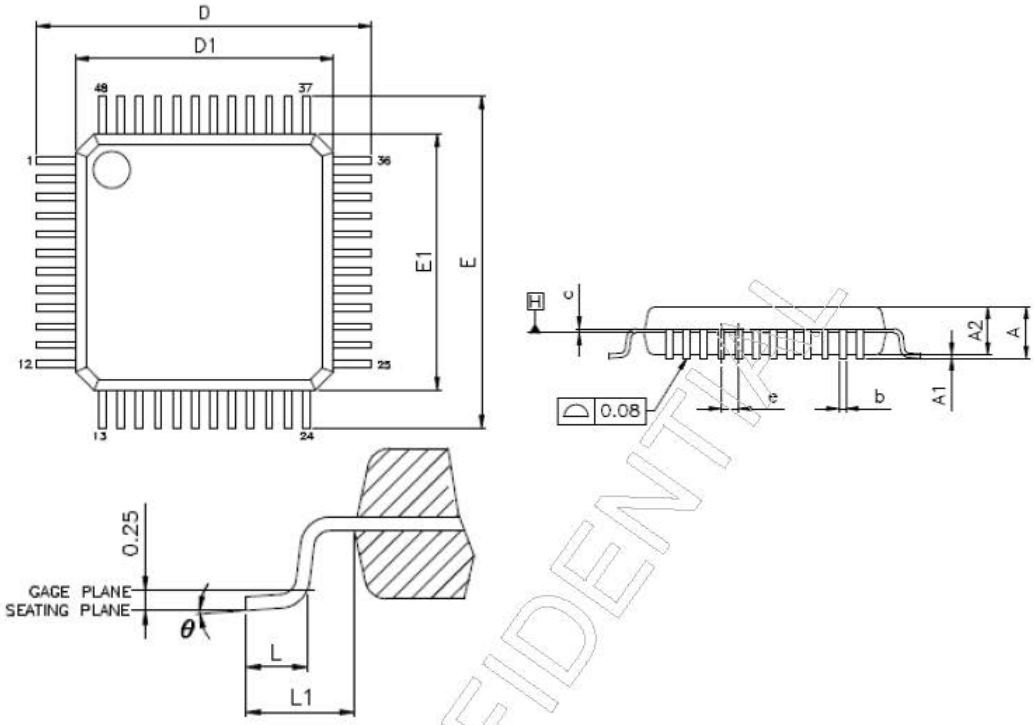
UNIT: mm

NOTES:
1. JEDEC outline : MS-026 BBD
2. Dimensions "D1" and "E1" do not include mold protrusion. Allowable protrusion is 0.25mm per side. "D1" and "E1" are maximum plastic body size dimensions including mold mismatch.
3. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" dimension by more than 0.08mm.

PREPARE	Cynthia	DATE: 2012/7/27
CHECK	Lawrence	DATE: 2012/7/27
APPROVE	Eric	DATE: 2012/7/27

10.2 48-Pin LQFP

Low-Profile Quad Flat Package **LQFP-48 PIN**



SYMBOLS	MIN	NOR	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ°	0	3.5	7

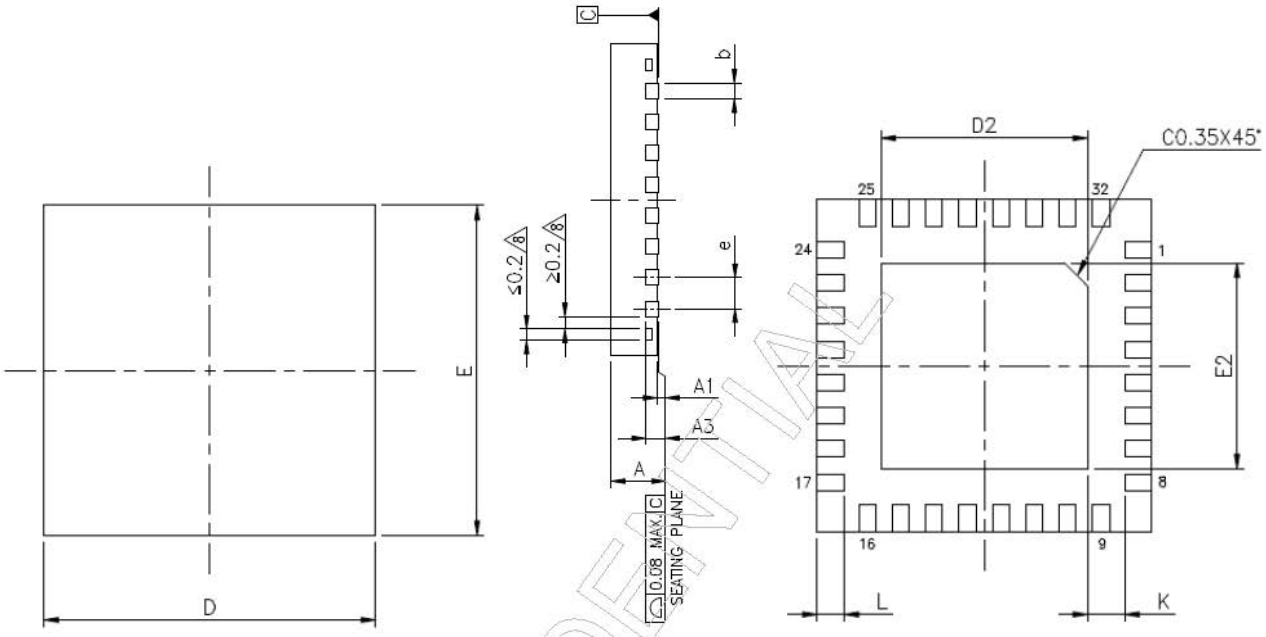
UNIT: mm

NOTES:
1. JEDEC outline : MS-026 BBC
2. Datum plane H is located at the bottom of the mold parting line coincident with where the lead exits the body.
3. Dimensions "D1" and "E1" do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions "D1" and "E1" do include mold mismatch and are determined at datum plane H.
4. Dimension "b" does not include dambar protrusion.
5.

PREPARE	Cynthia	DATE: 2012/7/26
CHECK	Lawrence	DATE: 2012/7/26
APPROVE	Eric	DATE: 2012/7/26

10.3 32-Pin QFN

Quad Flat No-Lead Plastic Package **QFN-32 PIN**



SYMBOLS	MIN	NOR	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	-	-
D2	3.10	3.20	3.25
E2	3.10	3.20	3.25

UNIT: mm

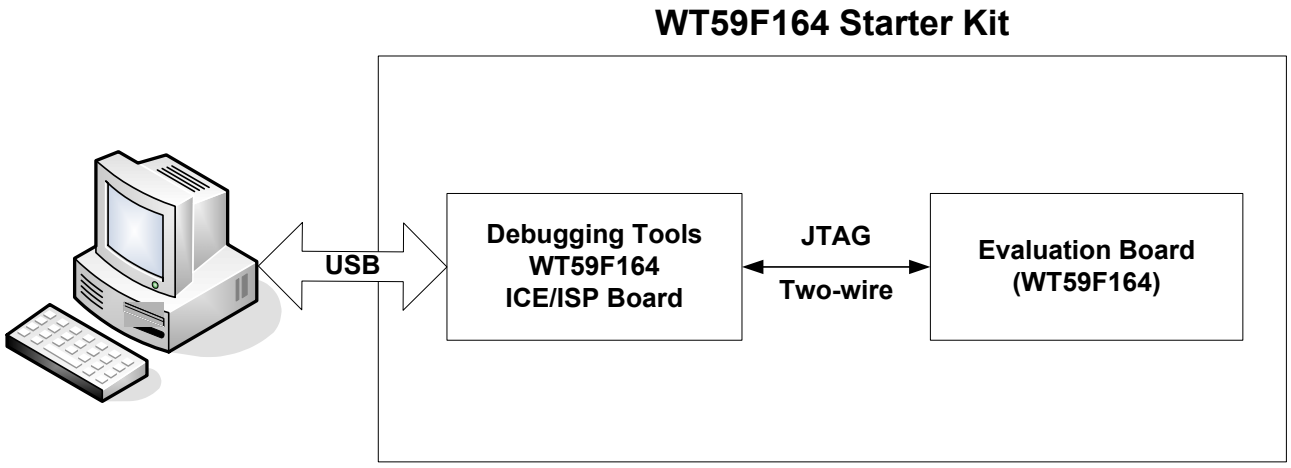
NOTES:
1. JEDEC outline : MO-220
2. Dimension "b" applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension "b" should not be measured in that radius area.
3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

PREPARE	Cynthia	DATE: 2012/8/1
CHECK	Lawrence	DATE: 2012/8/1
APPROVE	Eric	DATE: 2012/8/1

11. Development Tools

WT59F164 can work together with compiler software AndeSight. Debugging Tools, demo board application software can perform In_Circuit Emulator (ICE) and In-System Programming (ISP) in Windows 2000/XP/Vista/Win7.

The development kits are illustrated in the figure below:



12. Revision History

Version	History	Date
1.0	Initial issue	June 27, 2012
1.01	Revision	December 26, 2012
1.02	1. add 32-pin QFN package type 2. add 32-pin QFN Pin Configuration 3. add 32-pin QFN Pin Description 4. modify Power Supply Electrical Characteristics 5. add 8.4 USB DP/DM Circuit 6. add 32-pin QFN Ordering Information 7. add 32-pin QFN Package Dimension	January 17, 2013
1.021	Update typo on p. 17 Pin Number 39 -> 29 (RG480WT)	March 21, 2013
1.022	1. RG480WT -> RG48AWT 2. Update Ordering Information	September 12, 2013