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CYW20730

Single-Chip Bluetooth Transceiver for Wireless Input Devices

The Cypress® CYW20730 is a Bluetooth 5.1-compliant, stand-alone baseband processor with an integrated 2.4 GHz transceiver. It is ideal for wireless input device applications including game controllers, keyboards, 3D glasses, remote controls, gestural input devices, and sensor devices. Built-in firmware adheres to the Bluetooth Human Interface Device (HID) profile and Bluetooth Device ID profile specifications.

The CYW20730 radio has been designed to provide low power, low cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with Bluetooth Radio Specification 5.1.

The single-chip Bluetooth transceiver is a monolithic component implemented in a standard digital CMOS process and requires minimal external components to make a fully compliant Bluetooth device. The CYW20730 is available in three package options: a 32-pin, 5 mm × 5 mm QFN, a 40-pin, 6 mm × 6 mm QFN, and a 64-pin, 7 mm × 7 mm BGA.

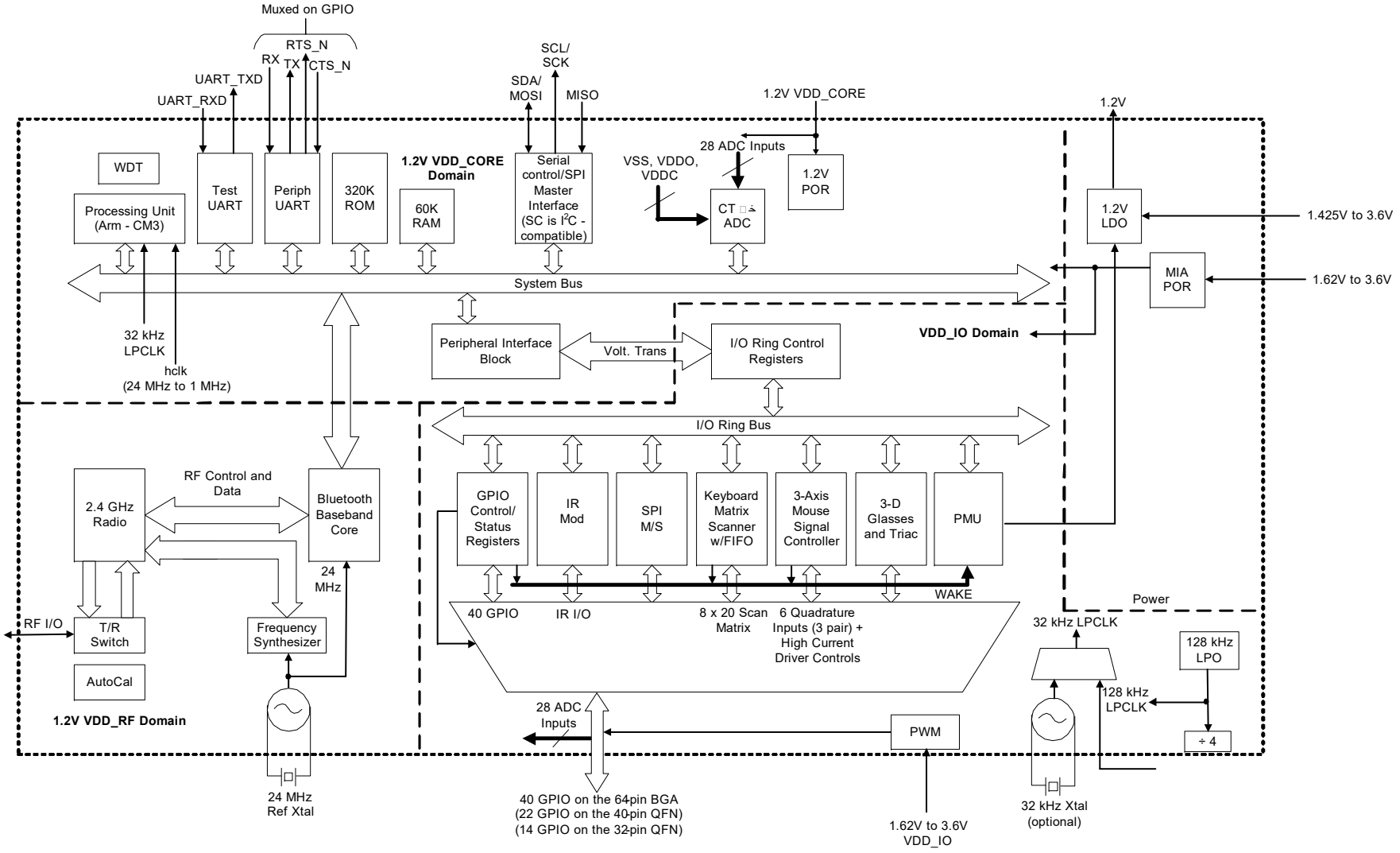
Features

- On-chip support for common keyboard and mouse interfaces eliminates external processor
- Programmable keyscan matrix interface, up to 8 × 20 key-scanning matrix
- 3-axis quadrature signal decoder
- Shutter control for 3D glasses
- Infrared modulator
- Triac control
- Triggered bluetooth Fast Connect (Only supported on CYW20730A1)
- Supports Adaptive Frequency Hopping
- Excellent receiver sensitivity
- Bluetooth specification 5.1 compatible
- Bluetooth HID profile version 1.1 compliant
- Bluetooth Device ID profile version 1.3 compliant
- Bluetooth AVRCP-CT profile version 1.3 compliant
- 10-bit auxiliary ADC with 28 analog channels
- On-chip support for serial peripheral interface (master and slave modes)
- Serial Communications interface (compatible with Philips® (now NXP) I^2C slaves)
- Programmable output power control meets Class 2 or Class 3 requirements
- Class 1 operation supported with external PA and T/R switch
- Integrated ARM Cortex™-M3 based microprocessor core
- On-chip power-on reset (POR)
- Support for EEPROM and serial flash interfaces
- Integrated low-dropout regulator (LDO)
- On-chip software controlled power management unit
- Three package types are available:
  - 32-pin QFN package (5 mm × 5 mm)
  - 40-pin QFN package (6 mm × 6 mm)
  - 64-pin BGA package (7 mm × 7 mm)
- RoHS compliant

Applications

- Wireless pointing devices: mice, trackballs, gestural controls
- Wireless keyboards
- 3D glasses
- Remote controls
- Game controllers
- Point-of-sale (POS) input devices
- Remote sensors
- Home automation
- Personal health and fitness monitoring

Figure 1. Functional Block Diagram



Contents

1. Functional Description

1.1 Keyboard Scanner

The keyboard scanner is designed to autonomously sample keys and store them into buffer registers without the need for the host microcontroller to intervene. The scanner has the following features:

- Ability to turn off its clock if no keys pressed.
- Sequential scanning of up to 160 keys in an 8 x 20 matrix.
- Programmable number of columns from 1 to 20.
- Programmable number of rows from 1 to 8.
- 16-byte key-code buffer (can be augmented by firmware).
- 128 kHz clock – allows scanning of full 160-key matrix in about 1.2 ms.
- N-key rollover with selective 2-key lockout if ghost is detected.
- Keys are buffered until host microcontroller has a chance to read it, or until overflow occurs.
- Hardware debouncing and noise/glitch filtering.
- Low-power consumption. Single-digit µA-level sleep current.

1.1.1 Theory of Operation

The key scan block is controlled by a state machine with the following states:

Idle

The state machine begins in the idle state. In this state, all column outputs are driven high. If any key is pressed, a transition occurs on one of the row inputs. This transition causes the 128 kHz clock to be enabled (if it is not already enabled by another peripheral) and the state machine to enter the scan state. Also in this state, an 8-bit row-hit register and an 8-bit key-index counter is reset to 0.

Scan

In the scan state, a row counter counts from 0 up to a programmable number of rows minus 1. Once the last row is reached, the row counter is reset and the column counter is incremented. This cycle repeats until the row and column counters are both at their respective terminal count values. At that point, the state machine moves into the Scan-End state.

As the keys are being scanned, the key-index counter is incremented. This counter is the value compared to the modifier key codes stored, or in the key-code buffer if the key is not a modifier key. It can be used by the microprocessor as an index into a lookup table of usage codes.

Also, as the n-th row is scanned, the row-hit register is ORed with the current 8-bit row input values if the current column contains two or more row hits. During the scan of any column, if a key is detected at the current row, and the row-hit register indicates that a hit was detected in that same row on a previous column, then a ghost condition may have occurred, and a bit in the status register is set to indicate this.

Scan End

This state determines whether any keys were detected while in the scan state. If yes, the state machine returns to the scan state. If no, the state machine returns to the idle state, and the 128 kHz clock request signal is made inactive.

The microcontroller can poll the key status register.

1.2 Mouse Quadrature Signal Decoder

The mouse signal decoder is designed to autonomously sample two quadrature signals commonly generated by optomechanical mouse apparatus. The decoder has the following features:

- Three pairs of inputs for X, Y, and Z (typical scroll wheel) axis signals. Each axis has two options:
  - For the X axis, choose P2 or P32 as X0 and P3 or P33 as X1.
  - For the Y axis, choose P4 or P34 as Y0 and P5 or P35 as Y1.
  - For the Z axis, choose P6 or P36 as Z0 and P7 or P37 as Z1.
- Control of up to four external high current GPIOs to power external optoelectronics:
  - Turn-on and turn-off time can be staggered for each HC-GPIO to avoid simultaneous switching of high currents and having multiple high-current devices on at the same time.
  - Sample time can be staggered for each axis.
  - Sense of the control signal can be active high or active low.
  - Control signal can be tristated for off condition or driven high or low, as appropriate.

1.2.1 Theory of Operation

The mouse decoder block has four 16-bit PWMs for controlling external quadrature devices and sampling the quadrature inputs at its core.

The GPIO signals may be used to control such items as LEDs, external ICs that may emulate quadrature signals, photodiodes, and photodetectors.

1.3 Shutter Control for 3D Glasses

The CYW20730, combined with the CYW20702, provides full system support for 3D glasses on televisions. The CYW20702 gets frame synchronization signals from the TV, converts them into proprietary timing control messages, then passes these messages to the CYW20730. The CYW20730 uses these messages to synchronize the shutter control for the 3D glasses with the television frames.

The CYW20730 can provide up to four synchronized control signals for left and right eye shutter control. These four lines can output pulses with microsecond resolution for on and off timing. The total cycle time can be set for any period up to 65535 msec. The pulses are synchronized to each other for left and right eye shutters.

The CYW20730 seamlessly adjusts the timing of the control signals based on control messages from the CYW20702, ensuring that the 3D glasses remain synchronized to the TV display frame.

3D hardware control on the CYW20730 works independently of the rest of the system. The CYW20730 negotiates sniff with the CYW20702 and, except for sniff resynchronization periods, most of the CYW20730 circuitry remains in a low power state while the 3D glasses subsystem continues to provide shutter timing and control pulses. This significantly reduces total system power consumption.

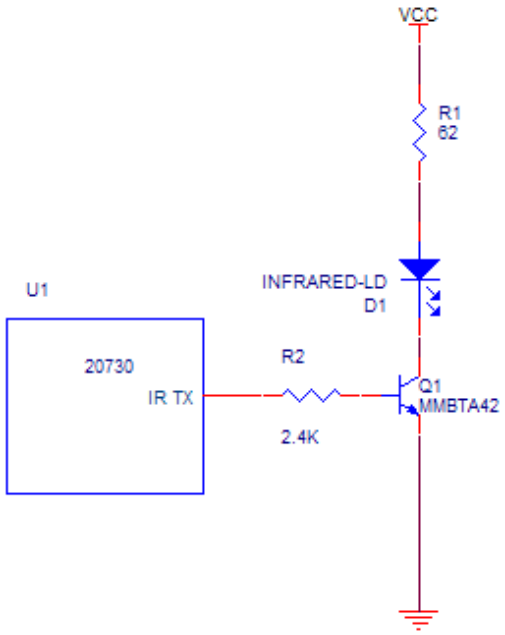
The CYW20730A2 has the new BT SIG 3DG profile, as well as legacy mode 3DG, included in ROM. This allows it to support a smaller and lower cost external memory of 4 KB.

1.4 Infrared Modulator

The CYW20730 includes hardware support for infrared TX. The hardware can transmit both modulated and unmodulated waveforms. For modulated waveforms, hardware inserts the desired carrier frequency into all IR transmissions. IR TX can be sourced from firmware-supplied descriptors, a programmable bit, or the peripheral UART transmitter.

If descriptors are used, they include IR on/off state and the duration between 1–32767 µsec. The CYW20730 IR TX firmware driver inserts this information in a hardware FIFO and makes sure that all descriptors are played out without a glitch due to underrun. See Figure 2.

Figure 2. Infrared TX



1.5 Triac Control

The CYW20730 includes hardware support for zero-crossing detection and trigger control for up to four triacs. The CYW20730 detects zero-crossing on the AC zero detection line and uses that to provide a pulse that is offset from the zero-crossing. This allows the CYW20730 to be used in dimmer applications, as well as any other applications that require a control signal that is offset from an input event.

1.6 Broadcom Proprietary Control Signaling and Triggered Bluetooth Fast Connect (Only supported on CYW20730A1)

Bluetooth Proprietary Control Signaling and Triggered Bluetooth Fast Connect (TBFC) are bluetooth proprietary baseband (ACL) suspension and low latency reconnection mechanisms that reestablish the baseband connection with the peer controller that also supports BPCS/TBFC.

The CYW20730 uses BPCS primitives to allow a Human Interface Device (HID) to suspend all RF traffic after a configurable idle period with no reportable activity. To conserve power, it can then enter one of its low power states while still logically remaining connected at the L2CAP and HID layers with the peer device. When an event requires the HID to deliver a report to the peer device, the CYW20730 uses the TBFC and BPCS mechanisms to reestablish the baseband connection and can immediately resume L2CAP traffic, greatly reducing latency between the event and delivery of the report to the peer device.

Certain applications may make use of the CYW20730 Baseband Fast Connect (BFC) mechanism for power savings and lower latencies not achievable by using even long sniff intervals by completely eliminating the need to maintain an RF link, while still being able to establish ACL and L2CAP connections much faster than regular methods.

1.7 Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time-critical functions required for high performance Bluetooth operation. The BBC manages the buffering, segmentation, and data routing for all connections. It also buffers data that passes through it, handles data flow control, schedules ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase TX/RX data reliability and security before sending over the air:

- Receive Functions: symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening.
- Transmit Functions: data framing, FEC generation, HEC generation, CRC generation, link key generation, data encryption, and data whitening.

1.7.1 Frequency Hopping Generator

The frequency hopping sequence generator selects the correct hopping channel number depending on the link controller state, Bluetooth clock, and device address.

1.7.2 E0 Encryption

The encryption key and the encryption engine are implemented using dedicated hardware to reduce software complexity and provide minimal processor intervention.

1.7.3 Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the Link Control Unit (LCU). This layer consists of the Command Controller, which takes software commands, and other controllers that are activated or configured by the Command Controller to perform the link control tasks. Each task performs a different Bluetooth link controller state. STANDBY and CONNECTION are the two major states. In addition, there are five substates: page, page scan, inquiry, inquiry scan, and sniff.

1.7.4 Adaptive Frequency Hopping

The CYW20730 gathers link quality statistics on a channel-by-channel basis to facilitate channel assessment and channel map selection. The link quality is determined by using both RF and baseband signal processing to provide a more accurate frequency hop map.

1.7.5 Bluetooth Version 5.1 Features

The CYW20730 supports Bluetooth 5.1, including the following options:

- Enhanced Power Control
- Unicast Connectionless Data
- HCI Read Encryption Key Size command

The CYW20730 also supports the following Bluetooth version 2.1 features:

- Extended Inquiry Response
- Sniff Subrating
- Encryption Pause and Resume
- Secure Simple Pairing
- Link Supervision Timeout Changed Event
- Erroneous Data Reporting
- Non-Automatically-Flushable Packet Boundary Flag
- Security Mode 4

1.7.6 Test Mode Support

The CYW20730 fully supports Bluetooth Test mode, as described in Part 1 of the Bluetooth 5.1 specification. This includes the transmitter tests, normal and delayed loopback tests, and the reduced hopping sequence.

In addition to the standard Bluetooth Test mode, the device supports enhanced testing features to simplify RF debugging and qualification as well as type-approval testing.

1.8 ADC Port

The CYW20730 contains a 16-bit ADC (effective number of bits is 10).

Additionally:

- There are 28 analog input channels in the 64-pin package, 12 analog input channels in the 40-pin package, and 9 analog input channels in the 32-pin package. All channels are multiplexed on various GPIOs.
- The conversion time is 10 µs.
- There is a built-in reference with supply- or band-gap based reference modes.
- The maximum conversion rate is 187 kHz.
- There is a rail-to-rail input swing.

The ADC consists of an analog ADC core that performs the actual analog-to-digital conversion and digital hardware that processes the output of the ADC core into valid ADC output samples. Directed by the firmware, the digital hardware also controls the input multiplexers that select the ADC input signal V_{inp} and the ADC reference signals V_{ref}.

Table 2. ADC Modes

Mode	ENOB (Typical)	Maximum Sampling Rate (kHz)	Latency[1] (µs)
0	13	5.859	171
1	12.6	11.7	85
2	12	46.875	21
3	11.5	93.75	11
4	10	187	5

Note
1. Settling time after switching channels.

1.9 Serial Peripheral Interface

The CYW20730 has two independent SPI interfaces. One is a master-only interface and the other can be either a master or a slave. Each interface has a 16-byte transmit buffer and a 16-byte receive buffer. To support more flexibility for user applications, the CYW20730 has optional I/O ports that can be configured individually and separately for each functional pin, as shown in Table 5. The CYW20730 acts as an SPI master device that supports 1.8V or 3.3V SPI slaves, as shown in Table 5. The CYW20730 can also act as an SPI slave device that supports a 1.8V or 3.3V SPI master, as shown in Table 5.

Table 3. CYW20730 First SPI Set (Master Mode)

Pin Name	SPI_CLK	SPI_MOSI	SPI_MISO	SPI_CS[2]
Configuration set 1	SCL	SDA	P24	–
Configuration set 2	SCL	SDA	P26	–
Configuration set 3 (Default for serial flash)	SCL	SDA	P32	P33
Configuration set 4	SCL	SDA	P39	–

Note
2. Any GPIO can be used as SPI_CS when SPI is in master mode

Table 4. CYW20730 Second SPI Set (Master Mode)

Pin Name	SPI_CLK	SPI_MOSI	SPI_MISO	SPI_CS[3]
Configuration set 1	P3	P0	P1	–
Configuration set 2	P3	P0	P5	–
Configuration set 3	P3	P2	P1	–
Configuration set 4	P3	P2	P5	–
Configuration set 5	P3	P4	P1	–
Configuration set 6	P3	P4	P5	–
Configuration set 7	P3	P27	P1	–
Configuration set 8	P3	P27	P5	–
Configuration set 9	P3	P38	P1	–
Configuration set 10	P3	P38	P5	–
Configuration set 11	P7	P0	P1	–
Configuration set 12	P7	P0	P5	–
Configuration set 13	P7	P2	P1	–
Configuration set 14	P7	P2	P5	–
Configuration set 15	P7	P4	P1	–
Configuration set 16	P7	P4	P5	–
Configuration set 17	P7	P27	P1	–
Configuration set 18	P7	P27	P5	–
Configuration set 19	P7	P38	P1	–
Configuration set 20	P7	P38	P5	–
Configuration set 21	P24	P0	P25	–
Configuration set 22	P24	P2	P25	–
Configuration set 23	P24	P4	P25	–

Note
3. Any GPIO can be used as SPI_CS when SPI is in master mode.

Table 4. CYW20730 Second SPI Set (Master Mode) (Cont.)

Pin Name	SPI_CLK	SPI_MOSI	SPI_MISO	SPI_CS[3]
Configuration set 24	P24	P27	P25	–
Configuration set 25	P24	P38	P25	–
Configuration set 26	P36	P0	P25	–
Configuration set 27	P36	P2	P25	–
Configuration set 28	P36	P4	P25	–
Configuration set 29	P36	P27	P25	–
Configuration set 30	P36	P38	P25	–

Note
3. Any GPIO can be used as SPI_CS when SPI is in master mode.

Table 5. CYW20730 Second SPI Set (Slave Mode)[4]

Pin Name	SPI_CLK	SPI_MOSI	SPI_MISO	SPI_CS
Configuration set 1	P3	P0	P1	P2
Configuration set 2	P3	P0	P5	P2
Configuration set 3	P3	P4	P1	P2
Configuration set 4	P3	P4	P5	P2
Configuration set 5	P7	P0	P1	P2
Configuration set 6	P7	P0	P5	P2
Configuration set 7	P7	P4	P1	P2
Configuration set 8	P7	P4	P5	P2
Configuration set 9	P3	P0	P1	P6
Configuration set 10	P3	P0	P5	P6
Configuration set 11	P3	P4	P1	P6
Configuration set 12	P3	P4	P5	P6
Configuration set 13	P7	P0	P1	P6
Configuration set 14	P7	P0	P5	P6
Configuration set 15	P7	P4	P1	P6
Configuration set 16	P7	P4	P5	P6
Configuration set 17	P24	P27	P25	P26
Configuration set 18	P24	P33	P25	P26
Configuration set 19	P24	P38	P25	P26
Configuration set 20	P36	P27	P25	P26
Configuration set 21	P36	P33	P25	P26
Configuration set 22	P36	P38	P25	P26
Configuration set 23	P24	P27	P25	P32
Configuration set 24	P24	P33	P25	P32
Configuration set 25	P24	P38	P25	P32

Note
4. Additional configuration sets are available upon request.

Table 5. CYW20730 Second SPI Set (Slave Mode)[4]

Pin Name	SPI_CLK	SPI_MOSI	SPI_MISO	SPI_CS
Configuration set 26	P36	P27	P25	P32
Configuration set 27	P36	P33	P25	P32
Configuration set 28	P36	P38	P25	P32
Configuration set 29	P24	P27	P25	P39
Configuration set 30	P24	P33	P25	P39
Configuration set 31	P24	P38	P25	P39
Configuration set 32	P36	P27	P25	P39
Configuration set 33	P36	P33	P25	P39
Configuration set 34	P36	P38	P25	P39

Note
4. Additional configuration sets are available upon request.

1.10 Microprocessor Unit

The CYW20730 microprocessor unit (µPU) executes software from the link control (LC) layer up to the application layer components that ensure adherence to the Bluetooth Human Interface Device (HID) profile and Audio/Video Remote Control Profile (AVRCP). The microprocessor is based on an ARM Cortex™-M3, 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. The µPU has 320 KB of ROM for program storage and boot-up, 60 KB of RAM for scratch-pad data, and patch RAM code.

The internal boot ROM provides power-on reset flexibility, which enables the same device to be used in different HID applications with an external serial EEPROM or with an external serial flash memory. At power-up, the lowest layer of the protocol stack is executed from the internal ROM memory.

External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes and feature additions. The device can also support the integration of user applications.

1.10.1 EEPROM Interface

The CYW20730 provides a Serial Control master interface. The BSC is programmed by the CPU to generate four types of BSC bus transfers: read-only, write-only, combined read/write, and combined write/read. BSC supports both low-speed and fast mode devices. The BSC is compatible with a Philips® (now NXP) I^2C slave device, except that master arbitration (multiple I^2C masters contending for the bus) is not supported.

The EEPROM can contain customer application configuration information including: application code, configuration data, patches, pairing information, BD_ADDR, baud rate, SDP service record, and file system information used for code.

Native support for the Microchip® 24LC128, Microchip 24AA128, and ST Micro® M24128-BR is included.

1.10.2 Serial Flash Interface

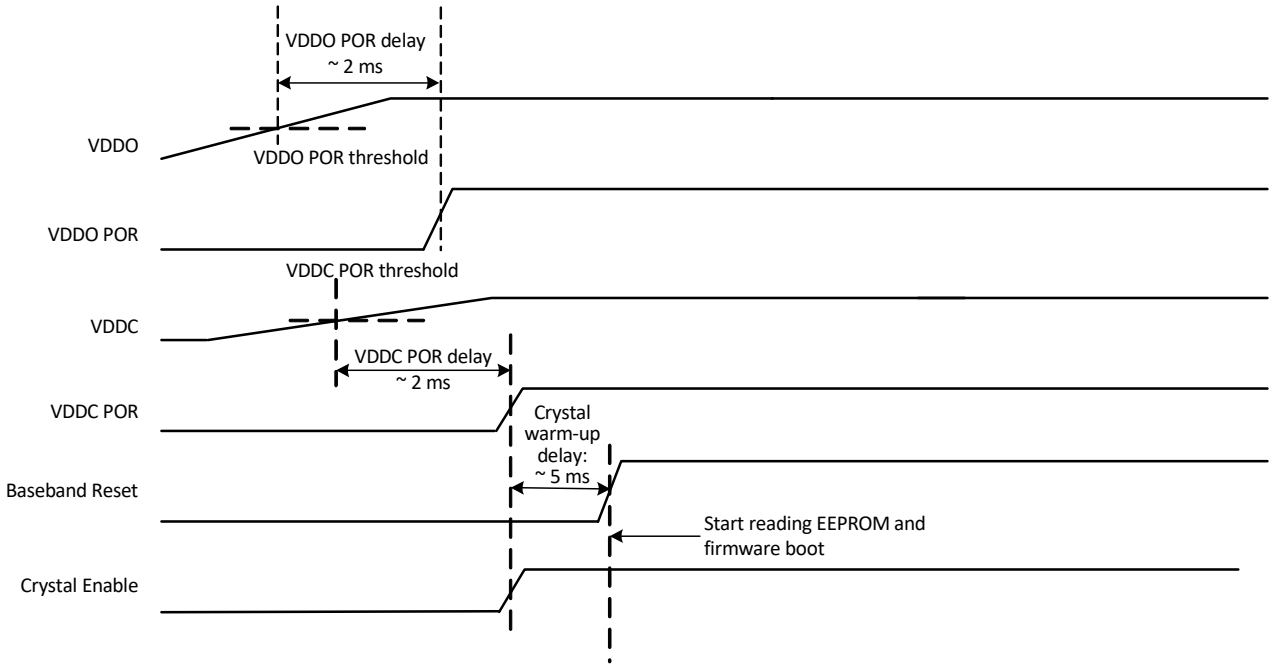
The CYW20730 includes an SPI master controller that can be used to access serial flash memory. The SPI master contains an AHB slave interface, transmit and receive FIFOs, and the SPI core PHY logic.

Devices natively supported include the following:

- Atmel® AT25BCM512B
- MXIC® MX25V512ZUI-20G

1.10.3 Internal Reset

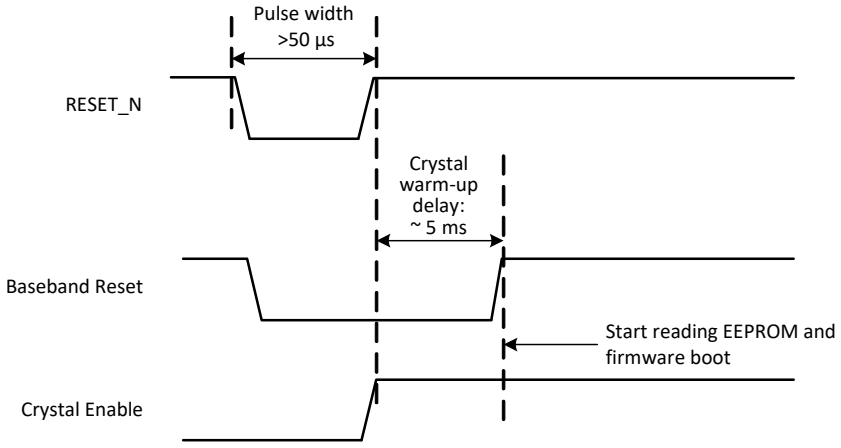
Figure 3. Internal Reset Timing



1.10.4 External Reset

The CYW20730 has an integrated power-on reset circuit that completely resets all circuits to a known power-on state. An external active low reset signal, RESET_N, can be used to put the CYW20730 in the reset state. The RESET_N pin has an internal pull-up resistor and, in most applications, it does not require that anything be connected to it. RESET_N should only be released after the VDDO supply voltage level has been stabilized.

Figure 4. External Reset Timing



1.11 Integrated Radio Transceiver

The CYW20730 has an integrated radio transceiver that is optimized for 2.4 GHz Bluetooth® wireless systems. It has been designed to provide low power, low cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with Bluetooth Radio Specification 5.1 and meets or exceeds the requirements to provide the highest communication link quality of service.

1.11.1 Transmitter Path

The CYW20730 features a fully integrated transmitter. The baseband transmit data is GFSK modulated in the 2.4 GHz ISM band.

Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal.

Power Amplifier

The CYW20730 has an integrated power amplifier (PA) that can transmit up to +4 dBm for class 2 operation.

1.11.2 Receiver Path

The receiver path uses a low IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order, on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, which has built-in out-of-band attenuation, enables the CYW20730 to be used in most applications without off-chip filtering.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Receiver Signal Strength Indicator

The radio portion of the CYW20730 provides a receiver signal strength indicator (RSSI) to the baseband. This enables the controller to take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

1.11.3 Local Oscillator

The local oscillator (LO) provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The CYW20730 uses an internal loop filter.

1.11.4 Calibration

The CYW20730 radio transceiver features a self-contained automated calibration scheme. No user interaction is required during normal operation or during manufacturing to provide optimal performance. Calibration compensates for filter, matching network, and amplifier gain and phase characteristics to yield radio performance within 2% of what is optimal. Calibration takes process and temperature variations into account, and it takes place transparently during normal operation and hop setting times.

1.11.5 Internal LDO Regulator

The CYW20730 has an integrated 1.2V LDO regulator that provides power to the digital and RF circuits. The 1.2V LDO regulator operates from a 1.425V to 3.63V input supply with a 30 mA maximum load current.

Note: Always place the decoupling capacitors near the pins as closely together as possible.

1.12 Peripheral Transport Unit

1.12.1 Serial Communications Interface

The CYW20730 provides a 2-pin master interface, which can be used to retrieve configuration information from an external EEPROM or to communicate with peripherals such as track-ball or touch-pad modules, and motion tracking ICs used in mouse devices. The BSC interface is compatible with I^2C slave devices. The BSC does not support multimaster capability or flexible wait-state insertion by either master or slave devices.

The following transfer clock rates are supported are:

- 100 kHz
- 400 kHz
- 800 kHz (Not a standard I^2C-compatible speed.)
- 1 MHz (Compatibility with high-speed I^2C-compatible devices is not guaranteed.)

The following transfer types are supported by the BSC:

- Read (Up to 16 bytes can be read.)
- Write (Up to 16 bytes can be written.)
- Read-then-Write (Up to 16 bytes can be read and up to 16 bytes can be written.)
- Write-then-Read (Up to 16 bytes can be written and up to 16 bytes can be read.)

Hardware controls the transfers, requiring minimal firmware setup and supervision.

The clock pin (SCL) and data pin (SDA) are both open-drain I/O pins. Pull-up resistors external to the CYW20730 are required on both the SCL and SDA pins for proper operation.

1.12.2 UART Interface

The UART is a standard 2-wire interface (RX and TX) and has adjustable baud rates from 9600 bps to 1.5 Mbps. The baud rate can be selected via a vendor-specific UART HCI command. The interface supports the Bluetooth 5.1 UART HCI (H5) specification. The default baud rate for H5 is 115.2 kbaud.

Both high and low baud rates can be supported by running the UART clock at 24 MHz.

The CYW20730 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±5%.

1.13 Clock Frequencies

The CYW20730 is set with crystal frequency of 24 MHz.

1.13.1 Crystal Oscillator

The crystal oscillator requires a crystal with an accuracy of ±20 ppm as defined by the Bluetooth specification. Two external load capacitors in the range of 5 pF to 30 pF are required to work with the crystal oscillator. The selection of the load capacitors is crystal dependent. Table 6 on page 15 shows the recommended crystal specification.

Figure 5. Recommended Oscillator Configuration—12 pF Load Crystal

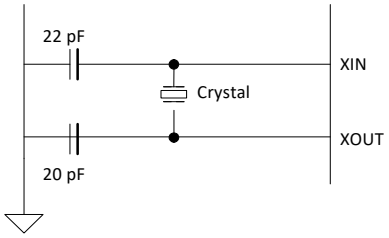


Table 6. Reference Crystal Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Nominal frequency	–	–	24.000	–	MHz
Oscillation mode	–		Fundamental		–
Frequency tolerance	@25°C	–	±10	–	ppm
Tolerance stability over temp	@0°C to +70°C	–	±10	–	ppm
Equivalent series resistance	–	–	–	50	W
Load capacitance	–	–	12	–	pF
Operating temperature range	–	0	–	+70	°C
Storage temperature range	–	–40	–	+125	°C
Drive level	–	–	–	200	µW
Aging	–	–	–	±10	ppm/year
Shunt capacitance	–	–	–	2	pF

HID Peripheral Block

The peripheral blocks of the CYW20730 all run from a single 128 kHz low-power RC oscillator. The oscillator can be turned on at the request of any of the peripherals. If the peripheral is not enabled, it shall not assert its clock request line.

The keyboard scanner is a special case in that it may drop its clock request line even when enabled and then reassert the clock request line if a keypress is detected.

32 kHz Crystal Oscillator

Figure 6 shows the 32 kHz crystal (XTAL) oscillator with external components and Table 7 on page 16 lists the oscillator's characteristics. It is a standard Pierce oscillator using a comparator with hysteresis on the output to create a single-ended digital output. The hysteresis was added to eliminate any chatter when the input is around the threshold of the comparator and is ~100 mV. This circuit can be operated with a 32 kHz or 32.768 kHz crystal oscillator or be driven with a clock input at similar frequency. The default component values are: R1 = 10 MΩ, C1 = C2 = ~10 pF. The values of C1 and C2 are used to fine-tune the oscillator.

Figure 6. 32 kHz Oscillator Block Diagram

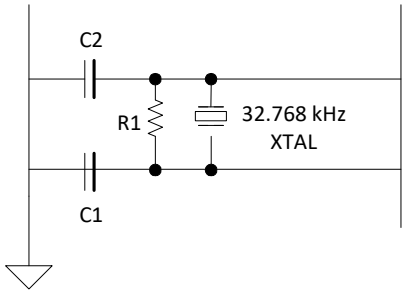


Table 7. XTAL Oscillator Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output frequency	F_{oscout}	–	–	32.768	–	kHz
Frequency tolerance	–	Crystal dependent	–	100	–	ppm
Start-up time	$T_{startup}$	–	–	–	500	ms
XTAL drive level	P_{drv}	For crystal selection	0.5	–	–	µW
XTAL series resistance	R_{series}	For crystal selection	–	–	70	kΩ
XTAL shunt capacitance	C_{shunt}	For crystal selection	–	–	1.3	pF

1.14 GPIO Port

The CYW20730 has 14 general-purpose I/Os (GPIOs) in the 32-pin package, 22 GPIOs in the 40-pin package, and 40 GPIOs in the 64-pin package. All GPIOs support programmable pull-up and pull-down resistors, and all support a 2 mA drive strength except P26, P27, P28, and P29, which provide a 16 mA drive strength at 3.3V supply.

1.14.1 Port 0–Port 1, Port 8–Port 23, and Port 28–Port 38

All of these pins can be programmed as ADC inputs.

1.14.2 Port 26–Port 29

P[26:29] consists of four pins. All pins are capable of sinking up to 16 mA for LED. These pins also have the PWM function, which can be used for LED dimming.

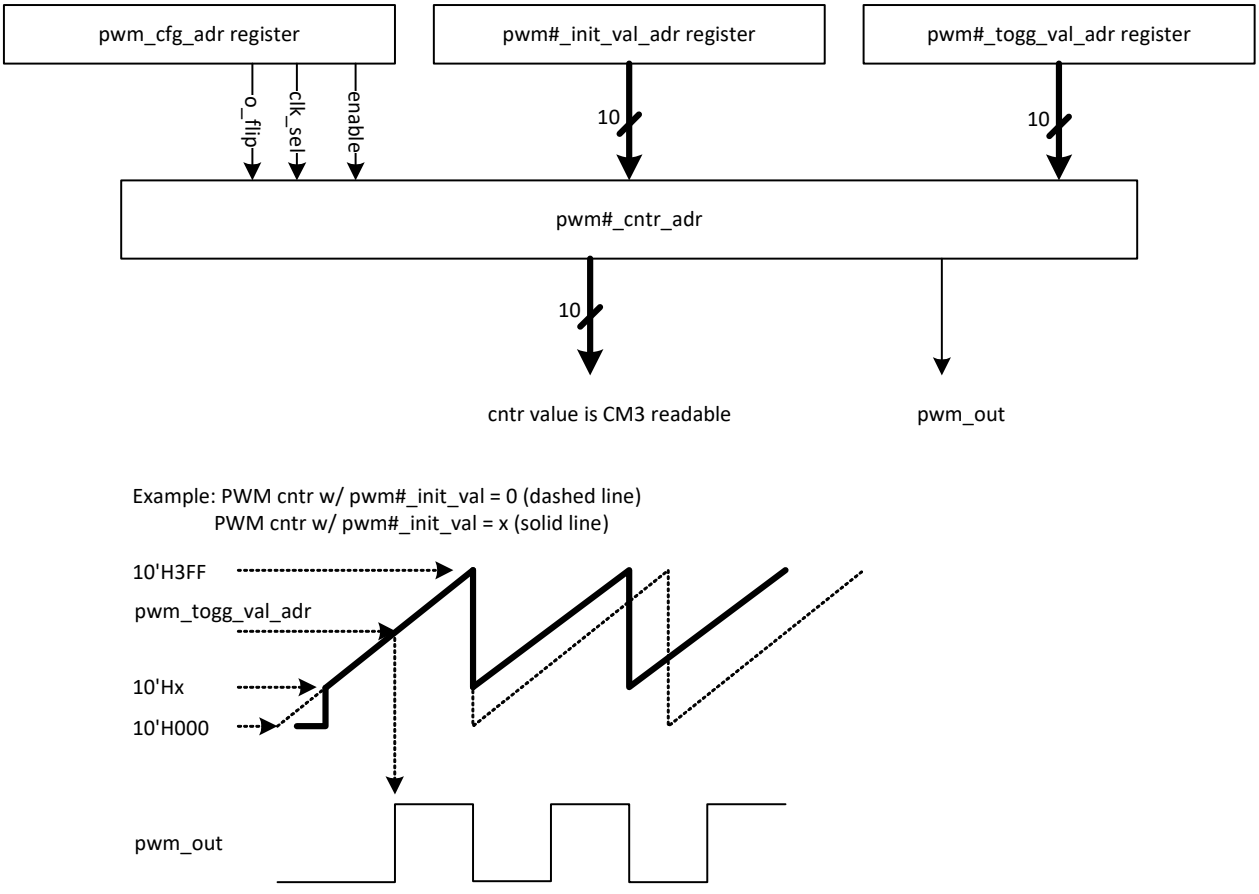
1.15 PWM

The CYW20730 has four internal PWM channels. The PWM module consists of the following:

- PWM1–4
- Each of the four PWM channels, PWM1–4, contains the following registers:
  - 10-bit initial value register (read/write)
  - 10-bit toggle register (read/write)
  - 10-bit PWM counter value register (read)
- The PWM configuration register is shared among PWM1–4 (read/write). This 12-bit register is used:
  - To configure each PWM channel.
  - To select the clock of each PWM channel
  - To change the phase of each PWM channel

Figure 7 shows the structure of one PWM channel.

Figure 7. PWM Channel Block Diagram



1.16 Power Management Unit

The Power Management Unit (PMU) provides power management features that can be invoked by software through power management registers or packet-handling in the baseband core.

1.16.1 RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver, which then processes the power-down functions accordingly.

1.16.2 Host Controller Power Management

Power is automatically managed by the firmware based on input device activity. As a power-saving task, the firmware controls the disabling of the on-chip regulator when in deep Sleep mode.

1.16.3 BBC Power Management

There are several low-power operations for the BBC:

- Physical layer packet handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth-specified low-power connection sniff mode. While in these low-power connection modes, the CYW20730 runs on the Low Power Oscillator and wakes up after a predefined time period.

The CYW20730 automatically adjusts its power dissipation based on user activity. The following power modes are supported:

- Active mode
- Idle mode
- Sleep mode
- HIDOFF mode

The CYW20730 transitions to the next lower state after a programmable period of user inactivity. Busy mode is immediately entered when user activity resumes.

In HIDOFF mode, the CYW20730 baseband and core are powered off by disabling power to LDOOUT. The VDDO domain remains powered up and will turn the remainder of the chip on when it detects user events. This mode minimizes chip power consumption and is intended for long periods of inactivity.

2. Pin Assignments

2.1 Pin Descriptions

Table 8. Pin Descriptions

Pin Number			Pin Name	I/O	Power Domain	Description
32-Pin QFN	40-pin QFN	64-pin BGA				
Radio I/O						
6	8	F1	RF	I/O	VDD_RF	RF antenna port
RF Power Supplies						
4	6	D1	VDDIF	I	VDD_RF	IFPLL power supply
5	7	E1	VDDFE	I	VDD_RF	RF front-end supply
7	9	H1	VDDVCO	I	VDD_RF	VCO, LOGEN supply
8	10	H2	VDDPLL	I	VDD_RF	RFPLL and crystal oscillator supply
Power Supplies						
11	13	H6	VDDC	I	N/A	Baseband core supply
–	–	D4, E2, E5, F2, G1, G2	VSS	I	N/A	Ground
28	34	A6, D7	VDDO	I	VDDO	I/O pad and core supply
14	16	–	VDDM	I	VDDM	I/O pad supply
Clock Generator and Crystal Interface						
9	11	H3	XTALI	I	VDD_RF	Crystal oscillator input. See “Crystal Oscillator” on page 14 for options.
10	12	G3	XTALO	O	VDD_RF	Crystal oscillator output.
1	40	A3	XTALI32K	I	VDDO	Low-power oscillator (LPO) input is used. Alternative Function: ■ P11 and P27 in 32-QFN only ■ P11 in 40-QFN only ■ P39 in 64-BGA only
32	39	B3	XTALO32K	O	VDDO	Low-power oscillator (LPO) output. Alternative Function: ■ P12 and P26 in 32-QFN only ■ P12 in 40-QFN only ■ P38 in 64-BGA only
Core						
18	20	G8	RESET_N	I/O PU	VDDO	Active-low system reset with open-drain output & internal pull-up resistor
17	19	G7	TMC	I	VDDO	Test mode control High: test mode Connect to GND if not used.

Table 8. Pin Descriptions (Cont.)

Pin Number			Pin Name	I/O	Power Domain	Description
32-Pin QFN	40-pin QFN	64-pin BGA				
UART						
12	14	H5	UART_RXD	I	VDDM[5]	UART serial input – Serial data input for the HCI UART interface. Leave unconnected if not used. Alternative function: ■ GPIO3
13	15	G5	UART_TXD	O, PU	VDDM[5]	UART serial output – Serial data output for the HCI UART interface. Leave unconnected if not used. Alternative Function: ■ GPIO2
Serial Control						
15	17	F7	SDA	I/O, PU	VDDM[5]	Data signal for an external I^2C device. Alternative function: ■ SPI_1: MOSI (master only) ■ GPIO0 ■ CTS
16	18	E8	SCL	I/O, PU	VDDM[5]	Clock signal for an external I^2C device. Alternative function: ■ SPI_1: SPI_CLK (master only) ■ GPIO1 ■ RTS
LDO Regulator Power Supplies						
2	4	B1	LDOIN	I	LDO	Battery input supply for the LDO
3	5	C1	LDOOUT	O	LDO	LDO output

Note
5. VDDO for 64-pin package.

Table 9. GPIO Pin Descriptions[6]

Pin Number			Pin Name	Default Direction	After POR	Power Domain	Alternate Function Description
32-Pin QFN	40-pin QFN	64-pin BGA					
19	21	F6	P0	Input	Floating	VDDO	■ GPIO: P0 ■ Keyboard scan input (row): KSI0 ■ A/D converter input ■ Peripheral UART: puart_tx ■ SPI_2: MOSI (master and slave) ■ IR_RX ■ 60 Hz_main ■ Not available during TMC=1
20	22	G6	P1	Input	Floating	VDDO	■ GPIO: P1 ■ Keyboard scan input (row): KSI1 ■ A/D converter input ■ Peripheral UART: puart_rts ■ SPI_2: MISO (master and slave) ■ IR_TX
22	24	H8	P2	Input	Floating	VDDO	■ GPIO: P2 ■ Keyboard scan input (row): KSI2 ■ Quadrature: QDX0 ■ Peripheral UART: puart_rx ■ Triac control 2 ■ SPI_2: SPI_CS (slave only) ■ SPI_2: SPI_MOSI (master only)
21	23	F8	P3	Input	Floating	VDDO	■ GPIO: P3 ■ Keyboard scan input (row): KSI3 ■ Quadrature: QDX1 ■ Peripheral UART: puart_cts ■ SPI_2: SPI_CLK (master and slave)
23	25	H7	P4	Input	Floating	VDDO	■ GPIO: P4 ■ Keyboard scan input (row): KSI4 ■ Quadrature: QDY0 ■ Peripheral UART: puart_rx ■ SPI_2: MOSI (master and slave) ■ IR_TX

Note
6. During Power-On Reset, all inputs are disabled.

Table 9. GPIO Pin Descriptions[6]

Pin Number			Pin Name	Default Direction	After POR	Power Domain	Alternate Function Description
32-Pin QFN	40-pin QFN	64-pin BGA					
–	26	E6	P5	Input	Floating	VDDO	■ GPIO: P5 ■ Keyboard scan input (row): KSI5 ■ Quadrature: QDY1 ■ Peripheral UART: puart_tx ■ SPI_2: MISO (master and slave)
–	27	F5	P6 PWM2	Input	Floating	VDDO	■ GPIO: P6 ■ Keyboard scan input (row): KSI6 ■ Quadrature: QDZ0 ■ Peripheral UART: puart_rts ■ SPI_2: SPI_CS (slave only) ■ 60Hz_main ■ Triac control 1
–	28	C5	P7	Input	Floating	VDDO	■ GPIO: P7 ■ Keyboard scan input (row): KSI7 ■ Quadrature: QDZ1 ■ Peripheral UART: puart_cts ■ SPI_2: SPI_CLK (master and slave)
24	29	F4	P8	Input	Floating	VDDO	■ GPIO: P8 ■ Keyboard scan output (column): KSO0 ■ A/D converter input ■ External T/R switch control: ~tx_pd Alternative Function: ■ P33 in 32-QFN only
–	3	A1	P9	Input	Floating	VDDO	■ GPIO: P9 ■ Keyboard scan output (column): KSO1 ■ A/D converter input ■ External T/R switch control: tx_pd
–	2	D2	P10 PWM3	Input	Floating	VDDO	■ GPIO: P10 ■ Keyboard scan output (column): KSO2 ■ A/D converter input
1	40	C2	P11	Input	Floating	VDDO	■ GPIO: P11 ■ Keyboard scan output (column): KSO3 ■ A/D converter input ■ XTALI32K (32-QFN and 40-QFN only) Alternative Function: ■ P27 in 32-QFN only
32	39	B2	P12	Input	Floating	VDDO	■ GPIO: P12 ■ Keyboard scan output (column): KSO4 ■ A/D converter input ■ XTALO32K (32-QFN and 40-QFN only) Alternative Function: ■ P26 in 32-QFN only

Note
6. During Power-On Reset, all inputs are disabled.

Table 9. GPIO Pin Descriptions[6]

Pin Number			Pin Name	Default Direction	After POR	Power Domain	Alternate Function Description
32-Pin QFN	40-pin QFN	64-pin BGA					
29	35	F3	P13 PWM3	Input	Floating	VDDO	■ GPIO: P13 ■ Keyboard scan output (column): KSO5 ■ A/D converter input ■ Triac control 3 Alternative Function:P28 in 32-QFN only
30	36	D3	P14 PWM2	Input	Floating	VDDO	■ GPIO: P14 ■ Keyboard scan output (column): KSO6 ■ A/D converter input ■ Triac control 4 Alternative Function ■ P38 in 32-QFN only
31	37	A2	P15	Input	Floating	VDDO	■ GPIO: P15 ■ Keyboard scan output (column): KSO7 ■ A/D converter input ■ IR_RX ■ 60Hz_main
–	–	C8	P16	Input	Floating	VDDO	■ GPIO: P16 ■ Keyboard scan output (column): KSO8
–	–	H4	P17	Input	Floating	VDDO	■ GPIO: P17 ■ Keyboard scan output (column): KSO9 ■ A/D converter input
–	–	C7	P18	Input	Floating	VDDO	■ GPIO: P18 ■ Keyboard scan output (column): KSO10 ■ A/D converter input
–	–	B8	P19	Input	Floating	VDDO	■ GPIO: P19 ■ Keyboard scan output (column): KSO11 ■ A/D converter input
–	–	A8	P20	Input	Floating	VDDO	■ GPIO: P20 ■ Keyboard scan output (column): KSO12 ■ A/D converter input
–	–	C6	P21	Input	Floating	VDDO	■ GPIO: P21 ■ Keyboard scan output (column): KSO13 ■ A/D converter input ■ Triac control 3
–	–	G4	P22	Input	Floating	VDDO	■ GPIO: P22 ■ Keyboard scan output (column): KSO14 ■ A/D converter input ■ Triac control 4
–	–	E3	P23	Input	Floating	VDDO	■ GPIO: P23 ■ Keyboard scan output (column): KSO15 ■ A/D converter input

Note
6. During Power-On Reset, all inputs are disabled.

Table 9. GPIO Pin Descriptions[6]

Pin Number			Pin Name	Default Direction	After POR	Power Domain	Alternate Function Description
32-Pin QFN	40-pin QFN	64-pin BGA					
27	33	A7	P24	Input	Floating	VDDO	■ GPIO: P24 ■ Keyboard scan output (column): KSO16 ■ SPI_2: SPI_CLK (master and slave) ■ SPI_1: MISO (master only) ■ Peripheral UART: puart_tx
26	32	B7	P25	Input	Floating	VDDO	■ GPIO: P25 ■ Keyboard scan output (column): KSO17 ■ SPI_2: MISO (master and slave) ■ Peripheral UART: puart_rx
32	38	A4	P26 PWM0	Input	Floating	VDDO	■ GPIO: P26 ■ Keyboard scan output (column): KSO18 ■ SPI_2: SPI_CS (slave only) ■ SPI_1: MISO (master only) ■ Optical control output: QOC0 ■ Triac control 1 Alternative Function: ■ P12 in 32-QFN only Current: 16 mA
1	1	B4	P27 PWM1	Input	Floating	VDDO	■ GPIO: P27 ■ Keyboard scan output (column): KSO19 ■ SPI_2: MOSI (master and slave) ■ Optical control output: QOC1 ■ Triac control 2 Alternative Function: ■ P11 in 32-QFN only Current: 16 mA
29	–	B5	P28 PWM2	Input	Floating	VDDO	■ GPIO: P28 ■ Optical control output: QOC2 ■ A/D converter input ■ LED1 ■ IR_TX Alternative Function: ■ P13 in 32-QFN only Current: 16 mA
–	–	A5	P29 PWM3	Input	Floating	VDDO	■ GPIO: P29 ■ Optical control output: QOC3 ■ A/D converter input ■ LED2 ■ IR_RX Current: 16 mA
–	–	E4	P30	Input	Floating	VDDO	■ GPIO: P30 ■ A/D converter input ■ Pairing button pin in default FW ■ Peripheral UART: puart_rts

Note
6. During Power-On Reset, all inputs are disabled.

Table 9. GPIO Pin Descriptions[6]

Pin Number			Pin Name	Default Direction	After POR	Power Domain	Alternate Function Description
32-Pin QFN	40-pin QFN	64-pin BGA					
–	–	E7	P31	Input	Floating	VDDO	■ GPIO: P31 ■ A/D converter input ■ EEPROM WP pin in default FW ■ Peripheral UART: puart_tx
25	31	D6	P32	Input	Floating	VDDO	■ GPIO: P32 ■ A/D converter input ■ Quadrature: QDX0 ■ SPI_2: SPI_CS (slave only) ■ SPI_1: MISO (master only) ■ Auxiliary clock output: ACLK0 ■ Peripheral UART: puart_tx
24	30	D8	P33	Input	Floating	VDDO	■ GPIO: P33 ■ A/D converter input ■ Quadrature: QDX1 ■ SPI_2: MOSI (slave only) ■ Auxiliary clock output: ACLK1 ■ Peripheral UART: puart_rx Alternative Function: ■ P8 in 32-QFN only
–	–	B6	P34	Input	Floating	VDDO	■ GPIO: P34 ■ A/D converter input ■ Quadrature: QDY0 ■ Peripheral UART: puart_rx ■ External T/R switch control: tx_pd
–	–	D5	P35	Input	Floating	VDDO	■ GPIO: P35 ■ A/D converter input ■ Quadrature: QDY1 ■ Peripheral UART: puart_cts
–	–	C4	P36	Input	Floating	VDDO	■ GPIO: P36 ■ A/D converter input ■ Quadrature: QDZ0 ■ SPI_2: SPI_CLK (master and slave) ■ Auxiliary Clock Output: ACLK0 ■ Battery detect pin in default FW ■ External T/R switch control: ~tx_pd
–	–	C3	P37	Input	Floating	VDDO	■ GPIO: P37 ■ A/D converter input ■ Quadrature: QDZ1 ■ SPI_2: MISO (slave only) ■ Auxiliary clock output: ACLK1

Note
6. During Power-On Reset, all inputs are disabled.

Table 9. GPIO Pin Descriptions[6]

Pin Number			Pin Name	Default Direction	After POR	Power Domain	Alternate Function Description
32-Pin QFN	40-pin QFN	64-pin BGA					
30	–	B3	P38	Input	Floating	VDDO	■ GPIO: P38 ■ A/D converter input ■ SPI_2: MOSI (master and slave) ■ IR_TX ■ XTALO32K (64-BGA only) Alternative Function: ■ P14 in 32-QFN only
–	–	A3	P39	Input	Floating	VDDO	■ GPIO: P39 ■ SPI_2: SPI_CS (slave only) ■ SPI_1: MISO (master only) ■ Infrared control: IR_RX ■ External PA ramp control: PA_Ramp ■ XTALI32K (64-BGA only) ■ 60Hz_main

Note
6. During Power-On Reset, all inputs are disabled.

2.2 Ball Maps

Figure 8. 32-Pin QFN Ball Map

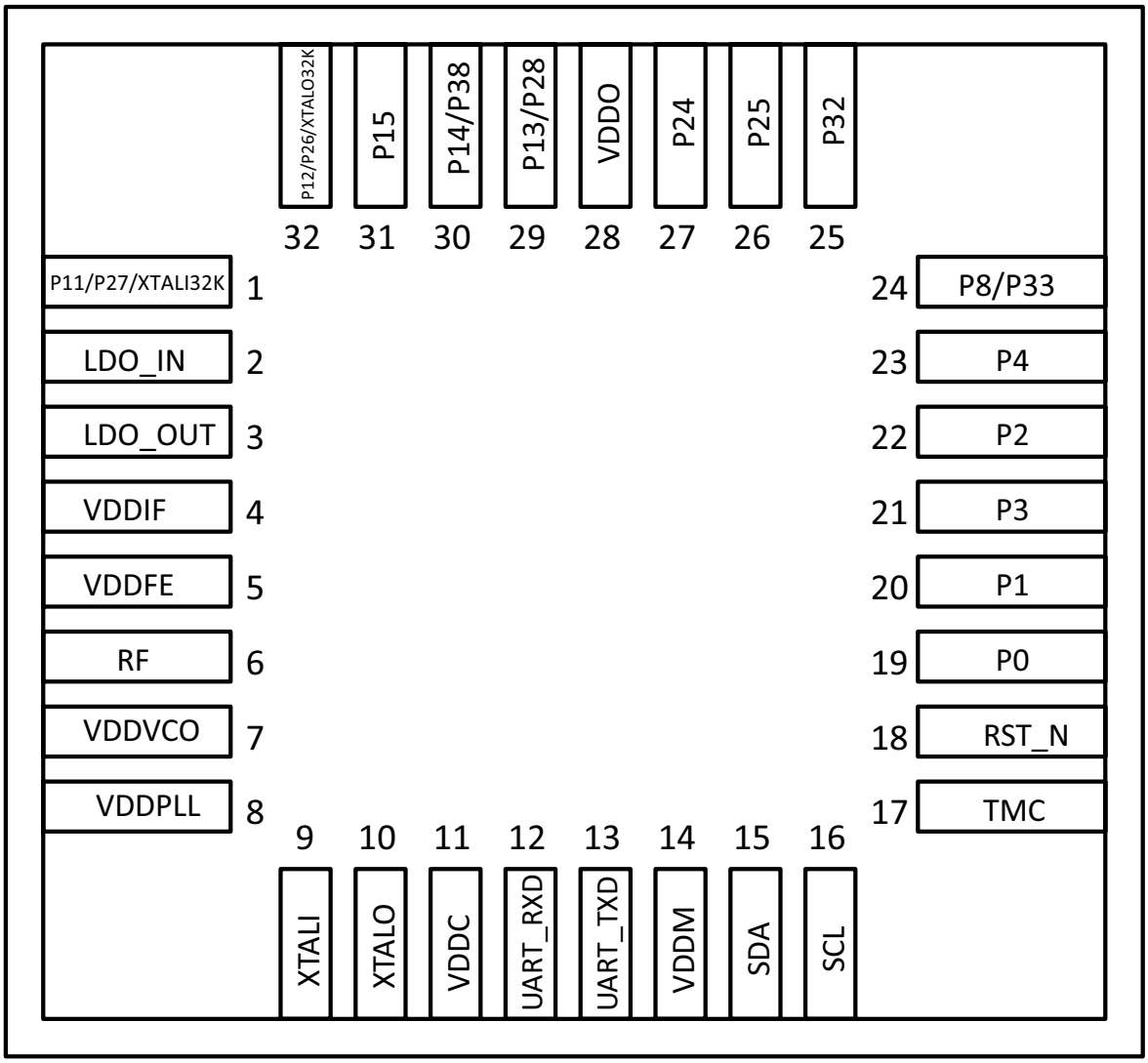


Figure 9. 40-pin QFN Ball Map

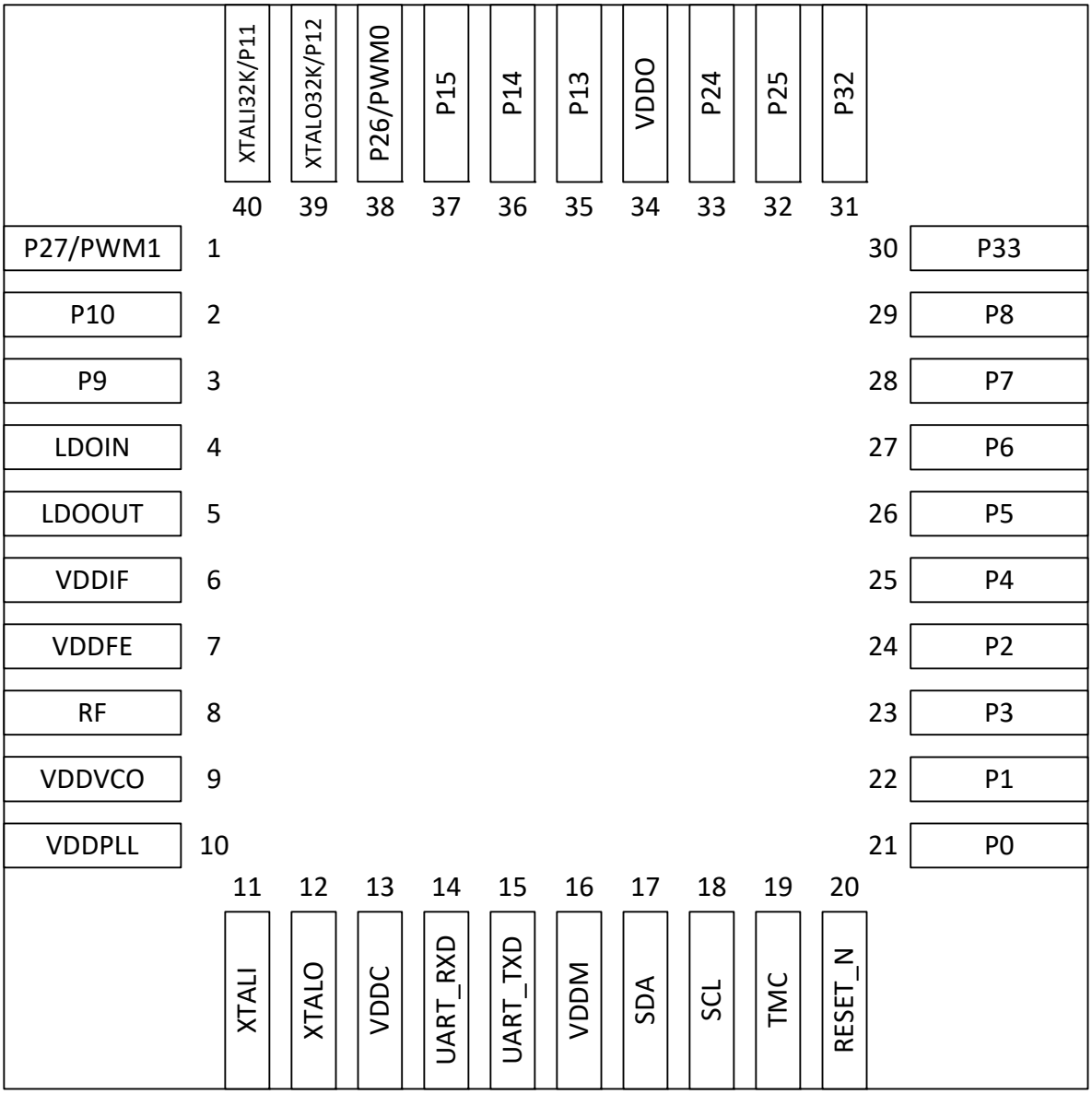
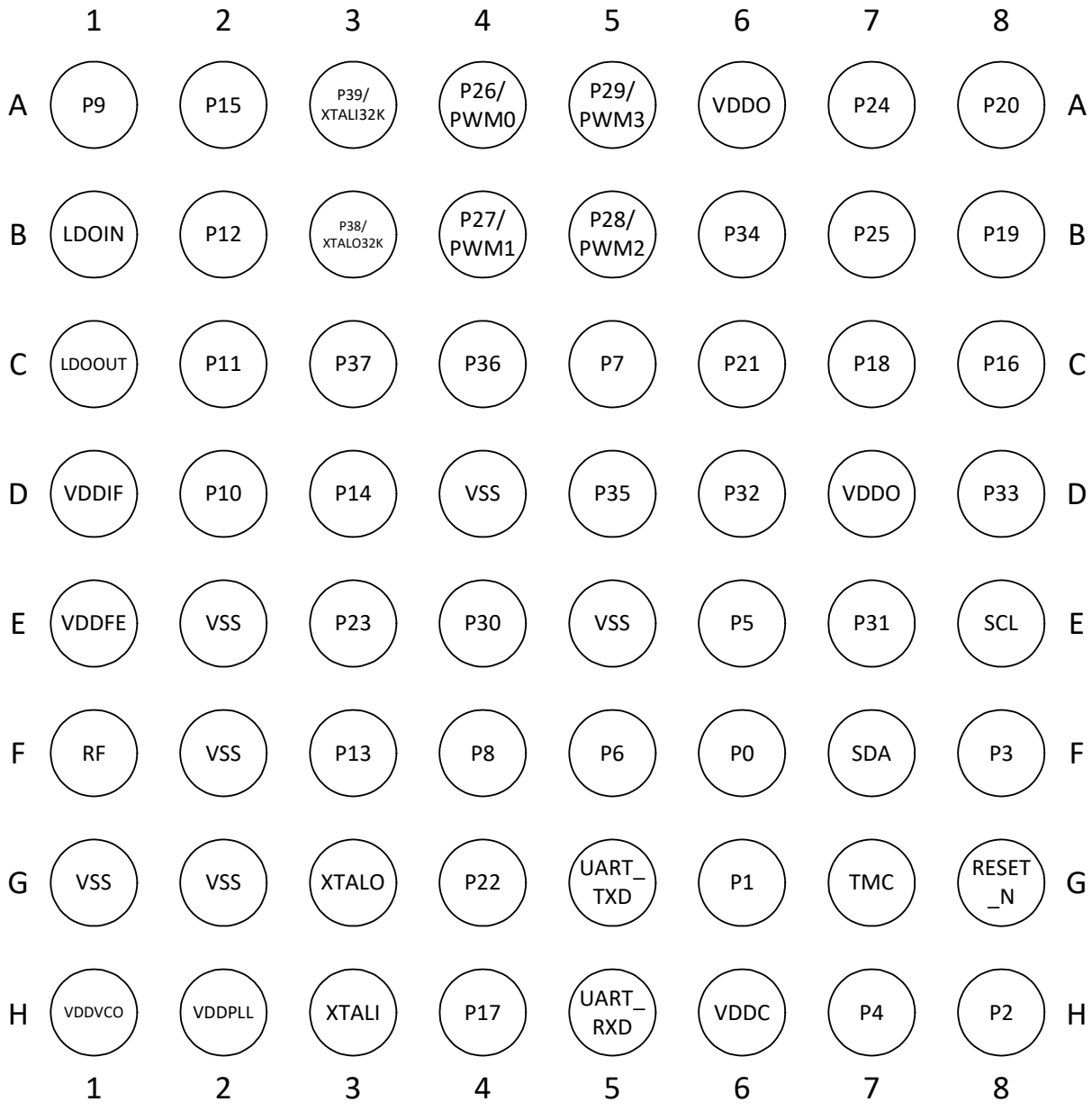


Figure 10. 64-pin BGA Ball Map



3. Specifications

3.1 Electrical Characteristics

Table 10 shows the maximum electrical rating for voltages referenced to VDD pin.

Table 10. Maximum Electrical Rating

Rating	Symbol	Value	Unit
DC supply voltage for RF domain	–	1.4	V
DC supply voltage for core domain	–	1.4	V
DC supply voltage for VDDM domain (UART/I^{2}C)	–	3.8	V
DC supply voltage for VDDO domain	–	3.8	V
DC supply voltage for VR3V	–	3.8	V
DC supply voltage for VDDFE	–	1.4	V
Voltage on input or output pin	–	V_{SS} – 0.3 to V_{DD} + 0.3	V
Operating ambient temperature range	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	–40 to +125	°C

Table 11 shows the power supply characteristics for the range T_J = 0 to 125°C.

Table 11. Power Supply

Parameter	Minimum[7]	Typical	Maximum[7]	Unit
DC supply voltage for RF	1.14	1.2	1.26	V
DC supply voltage for Core	1.14	1.2	1.26	V
DC supply voltage for VDDM (UART/I^{2}C)	1.62	–	3.63	V
DC supply voltage for VDDO	1.62	–	3.63	V
DC supply voltage for LDOIN	1.425	–	3.63	V
DC supply voltage for VDDFE	1.14	1.2[8]	1.26	V
Supply noise for VDDO (peak-to-peak)	–	–	100	mV
Supply noise for LDOIN (peak-to-peak)	–	–	100	mV

Notes
7. Overall performance degrades beyond minimum and maximum supply voltages.
8. 1.2V for Class 2 output with internal VREG.

Table 13 shows the digital level characteristics for (VSS = 0V).

Table 12. LDO Regulator Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Input voltage range	–	1.425	–	3.63	V
Default output voltage	–	–	1.2	–	V
Output voltage	Range	0.8	–	1.4	V
	Step size	–	40 or 80	–	mV
	Accuracy at any step	–5	–	+5	%
Load current	–	–	–	30	mA
Line regulation	Vin from 1.425 to 3.63V, I_{load} = 30 mA	–0.2	–	0.2	$\%V_O/V$
Load regulation	I_{load} from 1 µA to 30 mA, Vin = 3.3V, Bonding R = 0.3Ω	–	0.1	0.2	$\%V_O/mA$
Quiescent current	No load @Vin = 3.3V *Current limit enabled	–	6	–	µA
Power-down current	Vin = 3.3V, worst@70°C	–	5	200	nA

Table 13. ADC Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ADC Characteristics						
Number of Input channels	–	–	–	28	–	–
Channel switching rate	f_{ch}	–	–	–	133.33	kch/s
Input signal range	V_{inp}	–	0	–	3.63	V
Reference settling time	–	Changing refsel	7.5	–	–	µs
Input resistance	R_{inp}	Effective, single-ended	–	500	–	kΩ
Input capacitance	C_{inp}	–	–	–	5	pF
Conversion rate	f_C	–	5.859	–	187	kHz
Conversion time	T_C	–	5.35	–	170.7	µs
Resolution	R	–	–	16	–	bits
Effective number of bits	–	–	–	See Table 2	–	
Absolute voltage measurement error	–	Using on-chip ADC firmware driver	–	±2	–	%
Current	I	$I_{avdd1p2} + I_{avdd3p3}$	–	–	1	mA
Power	P	–	–	1.5	–	mW
Leakage current	$I_{leakage}$	T = 25°C	–	–	100	nA
Power-up time	$T_{powerup}$	–	–	–	200	µs
Integral nonlinearity[9]	INL	–	–1	–	1	LSB[9]
Differential nonlinearity[9]	DNL	–	–1	–	1	LSB[9]

Note
9. LSBs are expressed at the 10-bit level.

Table 14. Digital Level[10]

Characteristics	Symbol	Min	Typ	Max	Unit
Input low voltage	V_{IL}	–	–	0.4	V
Input high voltage	V_{IH}	0.75 × VDDO	–	–	V
Input low voltage (VDDO = 1.62V)	V_{IL}	–	–	0.4	V
Input high voltage (VDDO = 1.62V)	V_{IH}	1.2	–	–	V
Output low voltage[10]	V_{OL}	–	–	0.4	V
Output high voltage[11]	V_{OH}	VDDO – 0.4	–	–	V
Input capacitance (VDDMEM domain)	C_{IN}	–	0.12	–	pF

Notes
10. This table is also applicable to VDDMEM domain.
11. At the specified drive current for the pad.

Table 15. Current Consumption[12]

Operational Mode	Conditions	Typ	Max	Unit
Receive	Receiver and baseband are both operating, 100% ON.	–	26.6	mA
Transmit	Transmitter and baseband are both operating, 100% ON.	–	24 at 2 dBm, 19 at 0 dBm	mA
DM1	Average current when the device is in the transmit state, 100% utilization of available slots.	15.2	–	mA
DH1	Average current when the device is in the receive state, 100% utilization of available slots.	16.67	–	mA
Sleep	Internal LPO is in use.	28.4	–	µA
HIDOFF	–	1.5	–	µA
Sniff mode, 11.25 ms	Slave	2.8	–	mA
Sniff mode, 22.5 ms	Slave	1.27	–	mA
Sniff mode, 60 ms	Slave	750	–	µA
Sniff mode, 100 ms	Slave	500	–	µA
Sniff mode, 495 ms	Slave	125	–	µA

Note
12. Current consumption measurements are taken at VBAT with the assumption that VBAT is connected to VDDIO and LDOIN.

Caution: This device is susceptible to permanent damage from electrostatic discharge (ESD). Proper precautions are required during handling and mounting to avoid excessive ESD.

Table 16. ESD Tolerance

Model	Tolerance
Human Body Model (HBM)	± 2000V
Charged Device Model (CDM)	± 400V
Machine Model (MM)	± 150V

3.2 RF Specifications

Table 17. Receiver RF Specifications

Parameter	Mode and Conditions	Min	Typ	Max	Unit
Receiver Section					
Frequency range	–	2402	–	2480	MHz
RX sensitivity (standard)	GFSK, 0.1%BER, 1 Mbps	–	–88.0	–84.0	dBm
RX sensitivity (low current)		–	–84.0	–	dBm
Input IP3	–	–16	–	–	dBm
Maximum input	–	–10	–	–	dBm
Interference Performance					
C/I co channel	GFSK, 0.1%BER[13]	–	–	11.0	dB
C/I 1 MHz adjacent channel	GFSK, 0.1%BER[13]	–	–	0.0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1%BER[13]	–	–	–30.0	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1%BER[13]	–	–	–40.0	dB
C/I image channel	GFSK, 0.1%BER[13]	–	–	–9.0	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1%BER[13]	–	–	–20.0	dB
Out-of-Band Blocking Performance (CW)[14]					
30 MHz to 2000 MHz	0.1%BER	–	–10.0	–	dBm
2000 MHz to 2399 MHz	0.1%BER	–	–27	–	dBm
2498 MHz to 3000 MHz	0.1%BER	–	–27	–	dBm
3000 MHz to 12.75 GHz	0.1%BER	–	–10.0	–	dBm
Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–57.0	dBm
1 GHz to 12.75 GHz	–	–	–	–55.0	dBm

Notes
13. Desired signal is 10 dB above the reference sensitivity level (defined as –70 dBm).
14. Desired signal is 3 dB above the reference sensitivity level (defined as –70 dBm).

Table 18. Transmitter RF Specifications

Parameter	Min	Typ	Max	Unit
Transmitter Section				
Frequency range	2402	–	2480	MHz
Output power adjustment range	–6.0	–	4.0	dBm
Default output power	–	4.0	–	dBm
Output power variation	–	2.0	–	dB
20 dB bandwidth	–	900	1000	kHz
Adjacent Channel Power				
|M – N| = 2	–	–	–20	dBm
|M – N| ≥ 3	–	–	–40	dBm
Out-of-Band Spurious Emission				
30 MHz to 1 GHz	–	–	–36.0	dBm
1 GHz to 12.75 GHz	–	–	–30.0	dBm
1.8 GHz to 1.9 GHz	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–47.0	dBm
LO Performance				
Initial carrier frequency tolerance	–	–	±75	kHz
Frequency Drift				
DH1 packet	–	–	±25	kHz
DH3 packet	–	–	±40	kHz
DH5 packet	–	–	±40	kHz
Drift rate	–	–	20	kHz/50 µs
Frequency Deviation				
Average deviation in payload (sequence used is 00001111)	140	–	175	kHz
Maximum deviation in payload (sequence used is 10101010)	115	–	–	kHz
Channel spacing	–	1	–	MHz

3.3 Timing and AC Characteristics

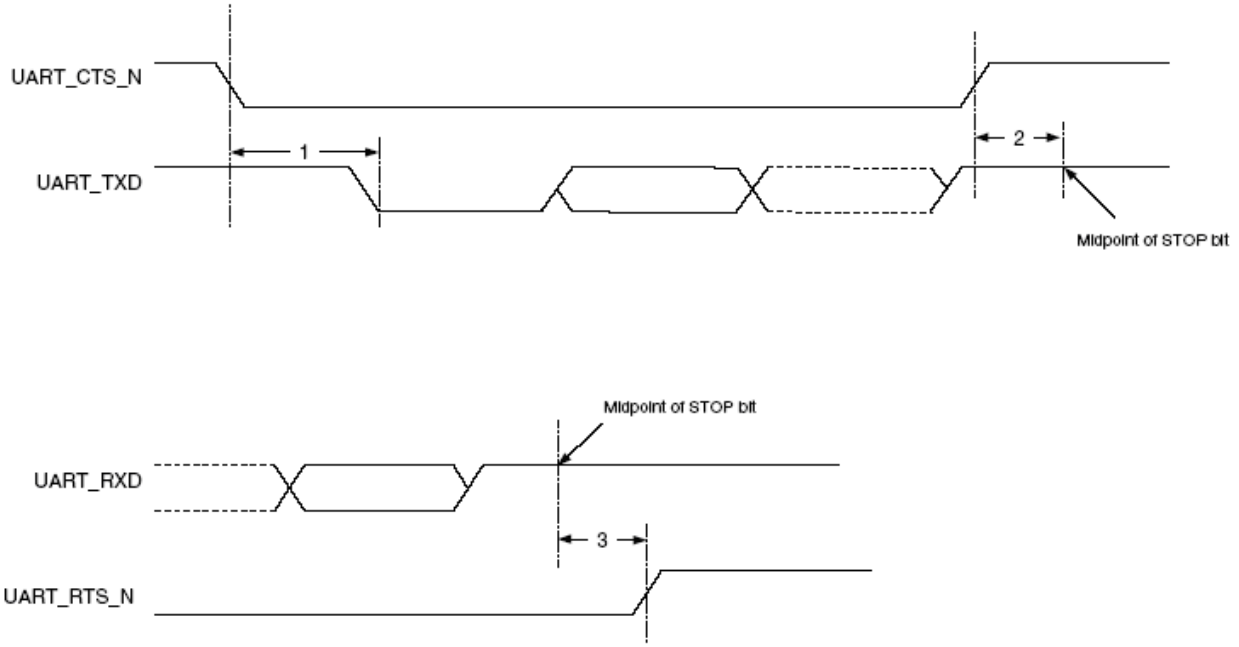
In this section, use the numbers listed in the **Reference** column of each table to interpret the following timing diagrams.

3.3.1 UART Timing

Table 19. UART Timing Specifications

Reference	Characteristics	Min	Max	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	24	Baud out cycles
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	10	ns
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	2	Baud out cycles

Figure 11. UART Timing



3.3.2 SPI Timing

The SPI interface supports clock speeds up to 12 MHz with VDDIO ≥ 2.2V. The supported clock speed is 6 MHz when 2.2V ≥ VDDIO ≥ 1.62V.

Figure 12 shows the timing diagram. SPI timing values for different values of SCLK and VDDM are shown in Table 20, Table 21 on page 37, Table 22 on page 37, Table 23 on page 38.

Figure 12. SPI Timing Diagram

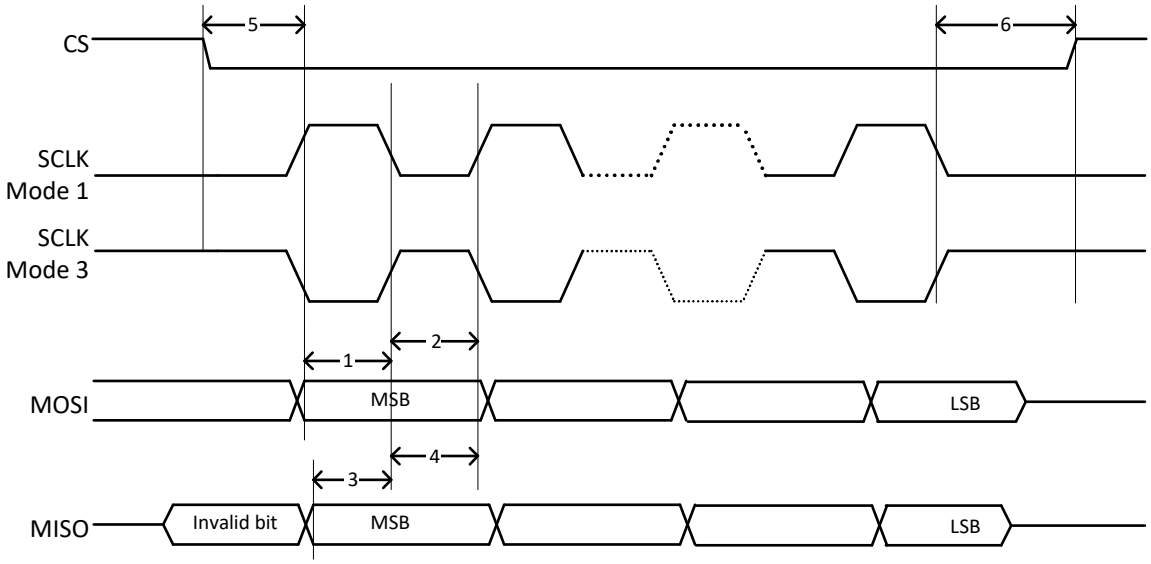


Table 20. SPI1 Timing Values—SCLK = 12 MHz and VDDM = 3.2V[15]

Reference	Characteristics	Symbol	Min	Typical[16]	Max	Unit
1	Output setup time, from MOSI data valid to sample edge of SCLK	Tds_mo	–	20	–	ns
2	Output hold time, from sample edge of SCLK to MOSI data update	Tdh_mo	–	63	–	ns
3	Input setup time, from MISO data valid to sample edge of SCLK	Tds_mi	–	TBD	–	ns
4	Input hold time, from sample edge of SCLK to MISO data update	Tdh_mi	–	TBD	–	ns
5[17]	Time from CS assert to first SCLK edge	Tsu_cs	½ SCLK period – 1	–	–	ns
6[17]	Time from first SCLK edge to CS deassert	Thd_cs	½ SCLK period	–	–	ns

Notes
15. The SCLK period is based on the limitation of Tds_mi. SCLK is designed for a maximum speed of 12 MHz. The speed can be adjusted to as low as 400 Hz by configuring the firmware.
16. Typical timing based on 20 pF/1 MΩ load and SCLK = 12 MHz.
17. CS timing is firmware controlled.

Table 21. SPI1 Timing Values—SCLK = 6 MHz and VDDM = 1.62V[18]

Reference	Characteristics	Symbol	Min	Typical[19]	Max	Unit
1	Output setup time, from MOSI data valid to sample edge of SCLK	Tds_mo	–	41	–	ns
2	Output hold time, from sample edge of SCLK to MOSI data update	Tdh_mo	–	120	–	ns
3	Input setup time, from MISO data valid to sample edge of SCLK	Tds_mi	–	TBD	–	ns
4	Input hold time, from sample edge of SCLK to MISO data update	Tdh_mi	–	TBD	–	ns
5[20]	Time from CS assert to first SCLK edge	Tsu_cs	½ SCLK period – 1	–	–	ns
6[20]	Time from first SCLK edge to CS deassert	Thd_cs	½ SCLK period	–	–	ns

Notes
18. The SCLK period is based on the limitation of Tds_mi. SCLK is designed for a maximum speed of 6 MHz. The speed can be adjusted to as low as 400 Hz by configuring the firmware.
19. Typical timing based on 20 pF/1 MΩ load and SCLK = 6 MHz.
20. CS timing is firmware controlled.

Table 22. SPI2 Timing Values—SCLK = 12 MHz and VDDM = 3.2V[21]

Reference	Characteristics	Symbol	Min	Typical[22]	Max	Unit
1	Output setup time, from MOSI data valid to sample edge of SCLK	Tds_mo	–	26	–	ns
2	Output hold time, from sample edge of SCLK to MOSI data update	Tdh_mo	–	56	–	ns
3	Input setup time, from MISO data valid to sample edge of SCLK	Tds_mi	–	TBD	–	ns
4	Input hold time, from sample edge of SCLK to MISO data update	Tdh_mi	–	TBD	–	ns
5[23]	Time from CS assert to first SCLK edge	Tsu_cs	½ SCLK period – 1	–	–	ns
6[23]	Time from first SCLK edge to CS deassert	Thd_cs	½ SCLK period	–	–	ns

Notes
21. The SCLK period is based on the limitation of Tds_mi. SCLK is designed for a maximum speed of 6 MHz. The speed can be adjusted to as low as 400 Hz by configuring the firmware.
22. Typical timing based on 20 pF/1 MΩ load and SCLK = 6 MHz.
23. CS timing is firmware controlled in master mode and can be adjusted as required in slave mode.

Table 23. SPI2 Timing Values—SCLK = 6 MHz and VDDM = 1.62V[24]

Reference	Characteristics	Symbol	Min	Typical[25]	Max	Unit
1	Output setup time, from MOSI data valid to sample edge of SCLK	Tds_mo	–	50	–	ns
2	Output hold time, from sample edge of SCLK to MOSI data update	Tdh_mo	–	120	–	ns
3	Input setup time, from MISO data valid to sample edge of SCLK	Tds_mi	–	TBD	–	ns
4	Input hold time, from sample edge of SCLK to MISO data update	Tdh_mi	–	TBD	–	ns
5[26]	Time from CS assert to first SCLK edge	Tsu_cs	½ SCLK period – 1	–	–	ns
6[26]	Time from first SCLK edge to CS deassert	Thd_cs	½ SCLK period	–	–	ns

Notes

24. The SCLK period is based on the limitation of Tds_mi. SCLK is designed for a maximum speed of 6 MHz. The speed can be adjusted to as low as 400 Hz by configuring the firmware.
25. Typical timing based on 20 pF/1 MΩ load and SCLK = 6 MHz.
26. CS timing is firmware controlled in master mode and can be adjusted as required in slave mode.

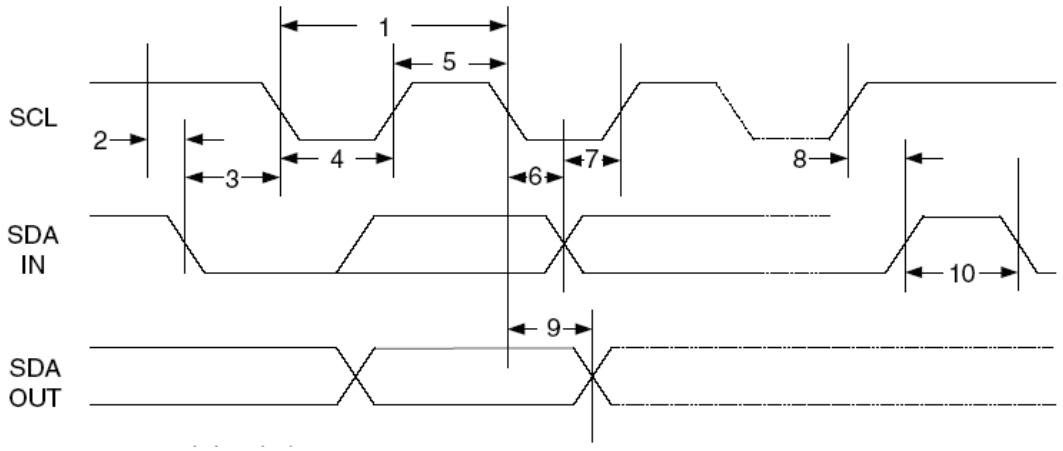
3.3.3 Interface Timing

Table 24. Interface Timing Specifications

Reference	Characteristics	Min	Max	Unit
1	Clock frequency	–	100	kHz
			400	
			800	
			1000	
2	START condition setup time	650	–	ns
3	START condition hold time	280	–	ns
4	Clock low time	650	–	ns
5	Clock high time	280	–	ns
6	Data input hold time[27]	0	–	ns
7	Data input setup time	100	–	ns
8	STOP condition setup time	280	–	ns
9	Output valid from clock	–	400	ns
10	Bus free time[28]	650	–	ns

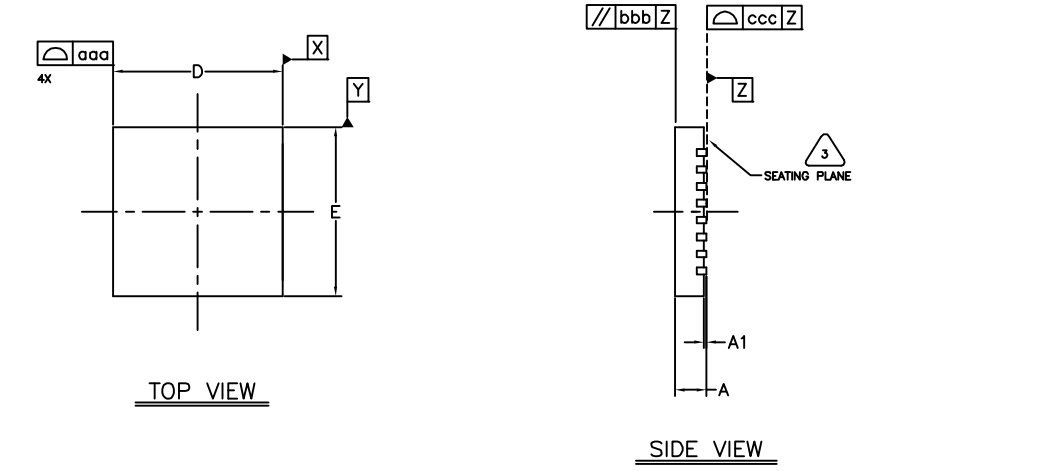
Notes
27. As a transmitter, 300 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
28. Time that the cbus must be free before a new transaction can start.

Figure 13. Interface Timing Diagram



4. Mechanical Information

Figure 14. 32-Pin QFN Package



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	1.00
A1	0.00	0.02	0.05
D	4.90	5.00	5.10
D1		3.70 BSC	
E	4.90	5.00	5.10
E1		3.70 BSC	
b	0.18	0.25	0.30
e		0.50 BSC	
L	0.30	0.40	0.50
aaa	–	–	0.15
bbb	–	–	0.10
ccc	–	–	0.05
ddd	–	–	0.15

Filename: MOD-016-1133-000

4. EXACT SHAPE AND SIZE OF PIN #1 MARKING MAY VARY

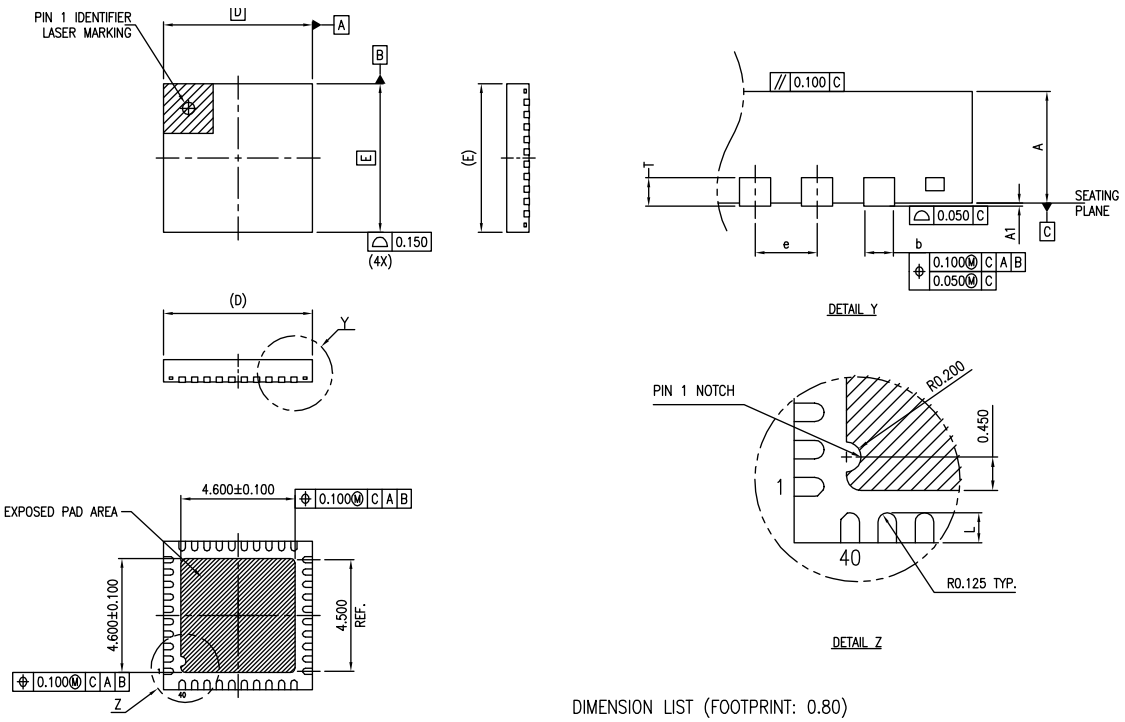
3. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING

2. MAX COPLANARITY IS 0.05MM AND APPLIES TO THE EXPOSED PAD AS WELL AS THE LEADS.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 15. 40-pin QFN Package



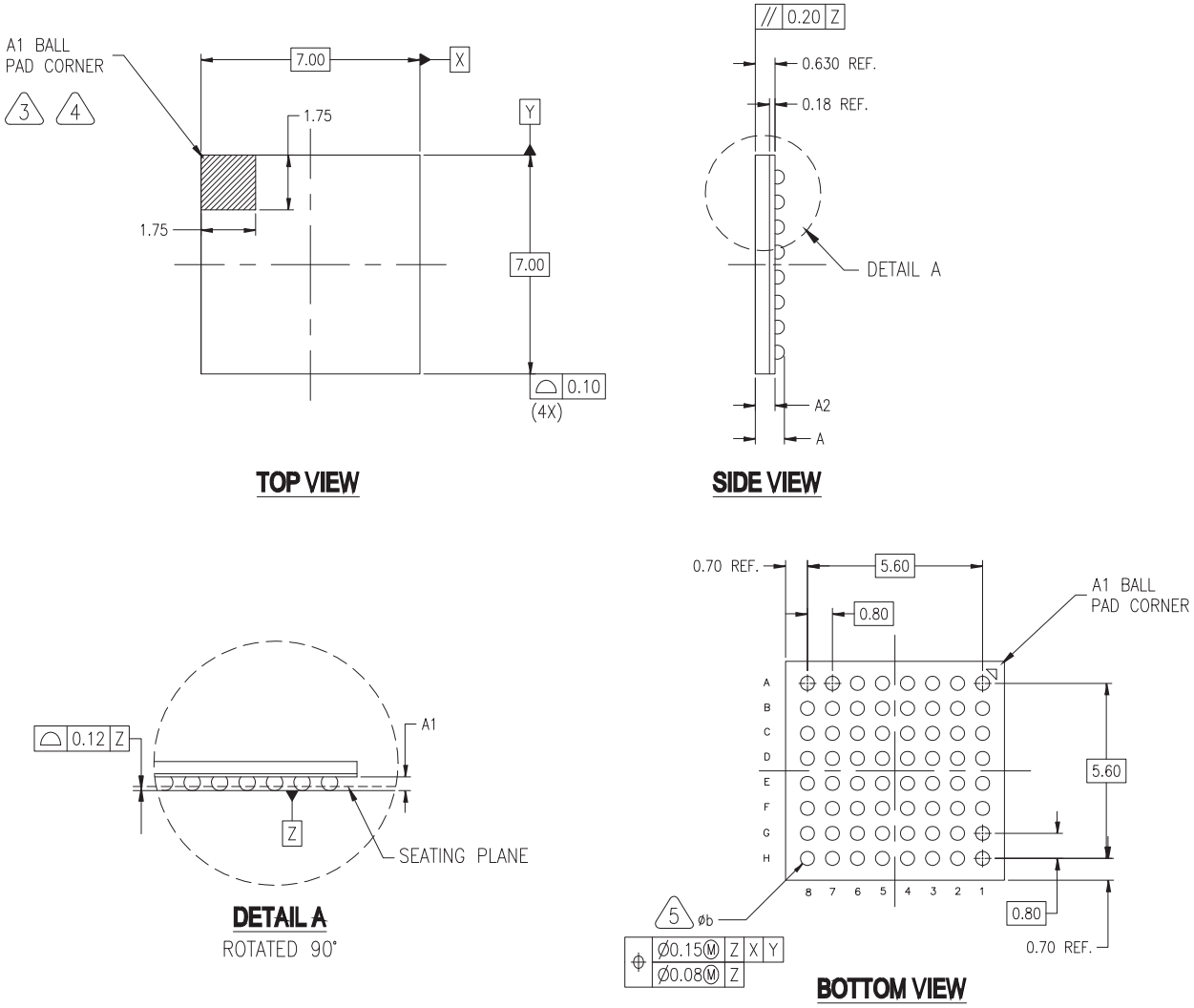
DIMENSION LIST (FOOTPRINT: 0.80)

S/N	SYM	DIMENSIONS	REMARKS
1	A	0.900±0.100	OVERALL HEIGHT
2	A1	0.020 $^{+0.030}_{-0.020}$	STANDOFF
3	D	6.000±0.100	PKG. LENGTH
4	E	6.000±0.100	PKG. WIDTH
5	L	0.400±0.075	FOOT LENGTH
6	T	0.203 REF	FRAME THICKNESS
7	b	0.250±0.050	LEAD WIDTH
8	e	0.500 BASE	LEAD PITCH

NOTES :

S/N	DESCRIPTION		SPEC.
1	GENERAL TOLERANCE.	DISTANCE	±0.100
		ANGLE	±2.5°
2	MATTE FINISH ON PACKAGE BODY SURFACE EXCEPT EJECTION AND PIN 1 MARKING.		Ra 0.3~1.2 um
3	FRAME BASE METAL THICKNESS		0.203 BASE
4	ALL MOLDED BODY SHARP CORNER RADII UNLESS OTHERWISE SPECIFIED.		MAX. R0.200
5	DRAWING DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OR CUTTING BURR.		
6	COMPLIANT TO JEDEC STANDARD: MO-220		

Figure 16. 64-pin FBGA Package



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	--	0.93	1.00
A1	0.25	0.30	0.35
A2	0.56	0.63	0.70
b	0.40	0.45	0.50
NUMBER OF BALLS 64			

1. All DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M–1994.
2. TERMINAL POSITIONS DESIGNATION PER JESD 95–1, SPP–010.
3. CORNER DETAILS PER STATS ChipPAC OPTION.
4. PIN 1 IDENTIFIER CAN BE CHAMFER, INK MARK, METALLIZED MARK OR SHINY DOT, MUST BE BUT LOCATED WITHIN ZONE INDICATED
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM Z
6. COMPLIANT TO JEDEC REGISTERED OUTLINE MO–192, VARIATION DAG–1 WITH EXCEPTION TO MOLD SURFACE FLATNESS AND OTHER GD&T CONTROL.
7. RAW SOLDER BALL SIZE DURING ASSEMBLY IS ø0.40mm.

4.1 Tape Reel and Packaging Specifications

Table 25. CYW20730 5 × 5 × 1 mm QFN, 32-Pin Tape Reel Specifications

Parameter	Value
Quantity per reel	2500 pieces
Reel diameter	13 inches
Hub diameter	7 inches
Tape width	12 mm
Tape pitch	8 mm

Table 26. CYW20730 6 × 6 × 1 mm QFN, 40-Pin Tape Reel Specifications

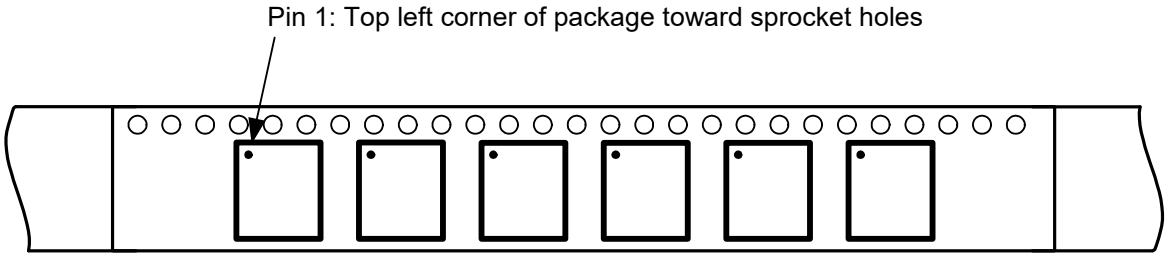
Parameter	Value
Quantity per reel	4000 pieces
Reel diameter	13 inches
Hub diameter	4 inches
Tape width	16 mm
Tape pitch	12 mm

Table 27. CYW20730 7 × 7 × 0.8 mm WFBGA, 64-Pin Tape Reel Specifications

Parameter	Value
Quantity per reel	2500 pieces
Reel diameter	13 inches
Hub diameter	4 inches
Tape width	16 mm
Tape pitch	12 mm

The top left corner of the CYW20730 package is situated near the sprocket holes, as shown in Figure 17.

Figure 17. Pin 1 Orientation



5. Ordering Information

Table 28. Ordering Information

Part Number	Package	Ambient Operating Temperature
CYW20730A2KML2G	32-pin QFN	0°C to 70°C
CYW20730A2KMLG	40-pin QFN	0°C to 70°C
CYW20730A2KFBG	64-pin BGA	0°C to 70°C
CYW20730A1KML2G	32-pin QFN	0°C to 70°C
CYW20730A1KMLG	40-pin QFN	0°C to 70°C
CYW20730A1KFBG	64-pin BGA	0°C to 70°C

6. Additional Information

6.1 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined upon first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary.

6.2 References

The references in this section may be used in conjunction with this document.

Note: Cypress provides customer access to technical documentation and software through its Customer Support Portal (CSP) and Downloads & Support site (see on page 2).

For documents, replace the “x” in the document number with the largest number available in the repository to ensure that you have the most current version of the document.

Document Name	Broadcom Number	Cypress Number
[1] Single-Chip Bluetooth® Transceiver and Baseband Processor	20702-DS10x-R	002-14772

6.3 IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (https://community.cypress.com/)

Document History

Document Title: CYW20730 Single-Chip Bluetooth Transceiver for Wireless Input Devices Document Number: 002-14824			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	–	04/27/2010	20730-DS100-RI: Initial release
*A	–	06/25/2010	20730-DS101-R: Added: “Shutter Control for 3D Glasses” on page 10. “Infrared Modulator” on page 10. “Infrared Learning” on page 11. “Triac Control” on page 12. “Broadcom Proprietary Control Signalling and Triggered Baseband Fast Connect” on page 12. Figure 5: “Internal Reset Timing,” on page 17. Figure 6: “External Reset Timing,” on page 17. Figure 10: “40-pin QFN Ball Map,” on page 33. Figure 11: “64-pin BGA Ball Map,” on page 34. “SPI Timing” on page 41. Figure 16: “40-pin QFN,” on page 44. Figure 17: “64-pin FBGA,” on page 45. Revised: “Microprocessor Unit” on page 16. Table 6: “Pin Descriptions,” on page 25. Table 11: “ADC Specifications,” on page 36. Table 14: “Receiver RF Specifications,” on page 38. Table 15: “Transmitter RF Specifications,” on page 39. Table 21: “Ordering Information,” on page 50.
*B	–	03/23/2011	20730-DS102-R: Added: Table 1: “ADC Modes,” on page 18 Revised: Figure 1: “Functional Block Diagram,” on page 2 “ADC Port” on page 17 “Internal LDO Regulator” on page 22 “UART Interface” on page 23 Table 6: “XTAL Oscillator Characteristics,” on page 25 Table 8: “GPIO Pin Descriptions,” on page 30 Table 10: “Power Supply,” on page 39 Table 11: “LDO Regulator Electrical Specifications,” on page 40 Table 12: “ADC Specifications,” on page 41 Table 14: “Current Consumption,” on page 42 Table 15: “Receiver RF Specifications,” on page 43 Table 16: “Transmitter RF Specifications,” on page 44 Table 18: “SPI Interface Timing Specifications,” on page 46 Table 21: “BCM20730 6 × 6 × 1 mm QFN, 40-Pin Tape Reel Specifications,” on page 52 Table 22: “BCM20730 7 × 7 × .8 mm WFBGA, 64-Pin Tape Reel Specifications,” on page 52 Deleted: Placeholder for Figure 4: Triac Control Placeholder for Figure 18: BCM20730, 6 x 6 QFN Package Tray Placeholder for Figure 19: BCM20730, 7 x 7 FBGA Package Tray
*C	–	04/06/2011	20730-DS103-R: Revised: Table 14: “Current Consumption,” on page 42 Table 23: “Ordering Information,” on page 54

Document Title: CYW20730 Single-Chip Bluetooth Transceiver for Wireless Input Devices Document Number: 002-14824			
Revision	**ECN**	**Submission Date**	**Description of Change**
*D	–	05/09/2011	20730-DS104-R: **Revised:** Figure 1: “Functional Block Diagram,” on page 2 “ADC Port” on page 17 Table 10: “Power Supply,” on page 39
*E	–	06/29/2011	20730-DS105-R: **Added:** Figure 9: “32-Pin QFN Ball Map,” on page 39 Figure 16: “32-Pin QFN Package,” on page 52 Table 20: “BCM20730 5 × 5 × 1 mm QFN, 32-Pin Tape Reel Specifications,” on page 55 **Revised:** General Description and Features on Cover Figure 1: “Functional Block Diagram,” on page 2 “ADC Port” on page 17 Table 2: “BCM20730 First SPI Set (Master Mode),” on page 18 Table 2: “BCM20730 First SPI Set (Master Mode),” on page 18 Table 2: “BCM20730 First SPI Set (Master Mode),” on page 18 Figure 5: “External Reset Timing,” on page 22 “GPIO Port” on page 27 “BBC Power Management” on page 29 Table 7: “Pin Descriptions,” on page 30 Table 8: “GPIO Pin Descriptions,” on page 32 Table 12: “ADC Specifications,” on page 44
*F	–	09/20/2011	**20730-DS106-R:** Changed from a Preliminary Data Sheet to a Data Sheet.
*G	–	10/10/2012	**20730-DS107-R:** **Revised:** “SPI Timing” on page 49
*H	–	09/09/2013	20730-DS108-R: Revised: <Cross-Ref>Section 1.3: “Shutter Control for 3D Glasses,” on page 5 Table 28, “Ordering Information,” on page 44 Added: Table 16, “ESD Tolerance,” on page 32
*I	5522944	11/16/2016	Updated to Cypress template
*J	5700376	04/25/2017	Updated Cypress Logo and Copyright.
*K	6893048	06/08/2020	Removed “Cypress Part Numbering Scheme” table from page 1. Replaced “Broadcom Serial Control” with “Serial control” and “3.0” with “5.0” Removed “IR learning” from Features. Removed Infrared Learning section.

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