ELECTRET MICROPHONE AMPLIFIER

This project aims to design an electret microphone amplifier. 3 NPN bipolar junction transistors will be used for the amplification. The main criterion of this project is to achieve enough gain to drive the speaker with an 8Ω impedance. For this criterion, the gain will be tested by an oscilloscope, and the speaker will be field-tested to see if the speaker outputs audible audio.

The small voltage input will be connected to the base terminal of the common emitter BJT amplifier, which is cascaded to an NPN Darlington pair amplifier where the signal gets amplified even more. The Darlington pair provides a gain approximately equal to the product of the individual transistor's gains. As audio amplifiers require a higher gain, using the Darlington pair is more efficient than cascading more than two transistors.

The average potential difference observed between the microphone terminals will be used to determine the required overall gain.

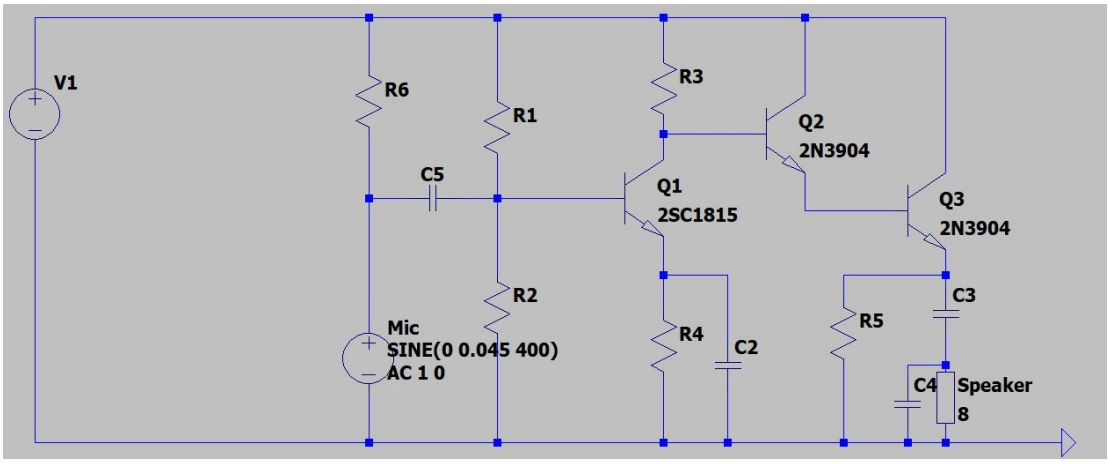
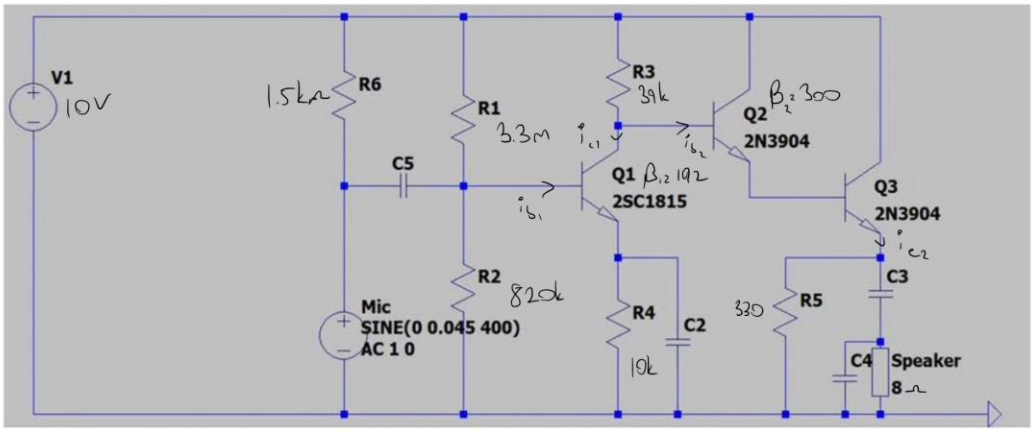


Figure 1: The circuit design

The transistors will be decided depending on their current gains, but the two transistors that form the Darlington pair will be the same kind of transistors. The cut-off frequencies will be considered since the audible spectrum must remain within the passband of the amplifier. The exact values will be found with circuit analysis and simulation in LTSpice, followed by a laboratory experiment for testing the values before printing the PCB designed in Dip Trace. When the circuit is finalized and soldered onto PCB, it will be tested for gain amount, Q point analysis, output distortions, cut-off points, and the existence of harmonics.

1. CIRCUIT ANALYSIS



KCL at B_1:

$$\frac{V_B - 10}{R_1} + \frac{V_B}{R_2} + i_{b_1} = 0, \quad V_B = i_{b_1}(192+1)\cdot R_4 + 0.7\,V$$

$$R_{TH} = R_1 \parallel R_2 = \frac{R_1 \cdot R_2}{R_1 + R_2}$$

$$\frac{V_B}{R_1 \parallel R_2} + i_{b_1} = \frac{10}{R_1}$$

$$i_{b_1}\left(\frac{193 \cdot R_4}{R_1 \parallel R_2} + 1\right) = \frac{10}{R_1} - \frac{.7}{R_1 \parallel R_2}$$

$$i_{b_1} = \frac{9.3R_2 - 0.7R_1}{193R_4(R_1+R_2) + R_1 \cdot R_2} \quad (I)$$

KCL at C_1:

$$\frac{V_{c_1} - 10}{R_3} + i_{c_1} + i_{b_2} = 0, \quad V_{c_1} = R_5 \cdot i_{b_2}(90000) + 0.7$$

$$i_{c_1} = 192 \cdot i_{b_1}$$

$$i_{b_2}\left(1 + \frac{R_5}{R_3} \cdot 90000\right) + 192\, i_{b_1} = \frac{9.3}{R_3}$$

$$i_{b_2} = \frac{9.3 - 192 \cdot R_3 \cdot i_{b_1}}{R_3 + R_5 \cdot 90000} \quad (II)$$

$V_o = R_5 \cdot 90001 \cdot i_{b_2}$ V_{CE2Q} is desired to be equal distance to saturation and cutoff points for the optimal Q point

$V_{CE2Q} = 10 - V_o \simeq \frac{10 - 0.7}{2} = 4.65\,V$

$\rightarrow V_o = 5.35\,V$

for $V_o = 5.35\,V$, $i_{b2} = \frac{5.35}{R_5 \cdot 90001}$, $i_{e2} = \frac{5.35}{R_5}$

desired i_{b2} should be low as high I_{EQ} will result in high temperatures.

→ choose $i_{e2} = 17\,mA$, $R_5 = 315\,\Omega$, round R_5 to

$i_{e2} = 16.2\,mA$ $R_5 = 330\,\Omega$, $V_{CEQ} = 4.65\,V$ normal resistor value 330

$i_{b2} = 0.182\,\mu A$ plug these values in (II)

$$\rightarrow 182 \cdot 10^{-9} = \frac{9.3 - 192 \cdot R_3 \cdot i_{b1}}{R_3 + 330 \cdot 90000} \quad (II)$$

The rest of the circuit is chosen by trial and error and approximation.

$R_1 = 3.3\,M\Omega$, $R_2 = 820k\,\Omega$, $R_3 = 39k\Omega$, $R_4 = 10k\,\Omega$

plugging these values into (I) and (II) we get

$i_{b1} = 0.499\,\mu A$, $i_{c1} = 192 \cdot i_{b1} = 96\,\mu A$

DC analysis: $\beta_1 = 192$ $\beta_2 = 300 \rightarrow \beta_D = 300^2$

$$\frac{V_B - 10}{3.3M} + \frac{V_B}{820k} + i_{b1} = 0 \quad , \quad V_B = i_{b1}(192+1)\cdot 10k + 0.7\,V$$

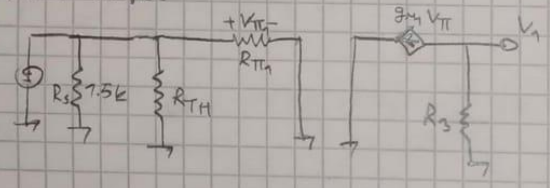
Solving these equations gives $i_{b1} = 0.499\,\mu A$

$$\frac{V_{c1} - 10}{39k} + i_{c1} + i_{b2} = 0 \quad , \quad V_{c1} = 330\, i_{b2}(90000) + 0.7$$

$i_{c1} = 192\, i_{b1} = 96\,\mu A$, $i_{b2} = 0.187\,\mu A$

To find the gain with small signal analysis, the gains of each stage can be found seperately and then be multiplied.

First stage:



$$g_{m1} = \frac{I_{c1Q}}{V_T}$$

$$V_1 = -V_s \cdot \frac{I_{c1Q}}{V_T} \cdot R_3$$

$$A_{V1} = \frac{I_{c1Q}}{V_T} \cdot R_3 = \frac{96.10^{-6}}{0.026}\, 39000 = 144$$

Second stage (Darlington pair):

Darlington pairs have voltage gain close to 1 but they have huge current gain.

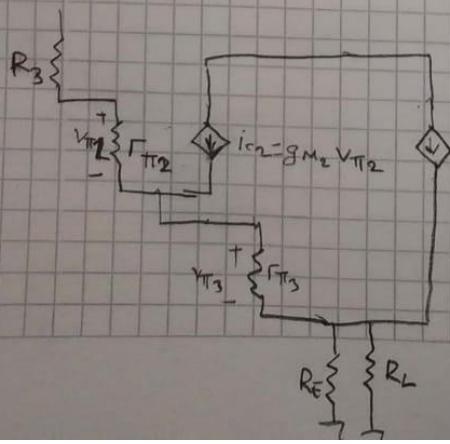
$R_E \| R_L = 7.8\,\Omega$ $\quad g_{m2} = \frac{I_{c2}}{V_T}$

$$A_{V2} = \frac{R_E \| R_L}{\frac{1}{g_{m2}} + R_E \| R_L} = 0.83$$

$I_{C_2} = 0.187.10^{-6} \cdot (300^2) \cdot \frac{300}{301}$

$g_{m2} = 0.645$

$$A_{V1} \cdot A_{V2} = A_V = 144.(0.83) = 119.5$$



$$Z_b = \beta_D \times \left[\frac{1}{g_{m2}} + R_E\right]$$

$$A_i = \frac{\beta_D \times R_3}{R_3 + Z_B} = 117.48$$

2. SOFTWARE SIMULATION & PCB DESIGN

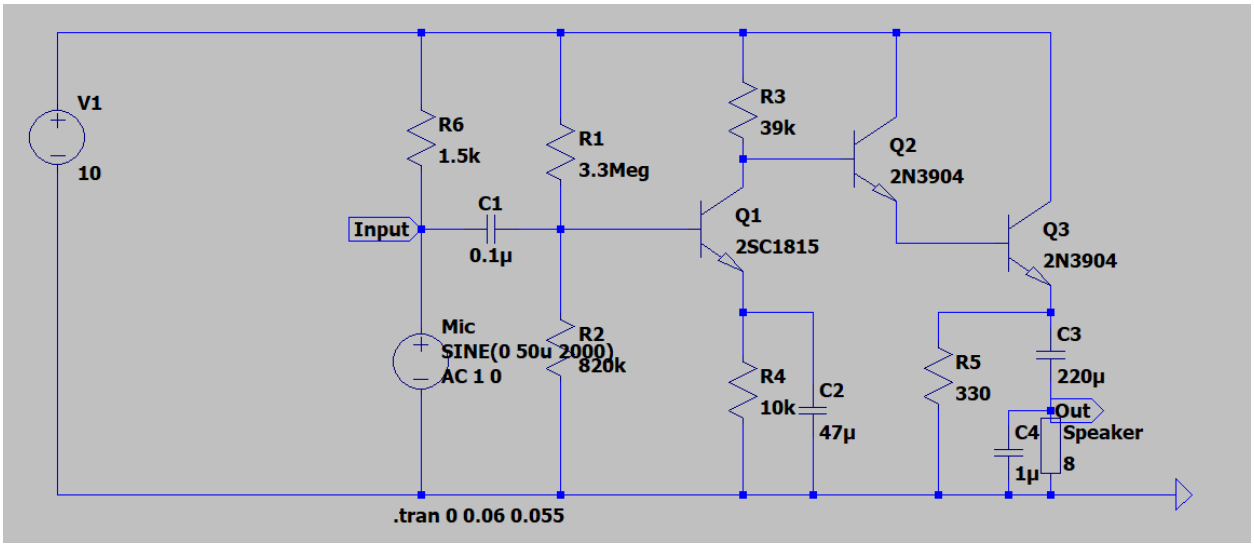


Figure 2: Finalized circuit design

The final circuit design is given in Figure 2. The values of the capacitors and resistors are found with inspiration from the equations and computer aid as numerous variables could be changed. One of the critical components was the current passing through the transistors, as they should not be too high to increase efficiency and reduce heat dissipation.

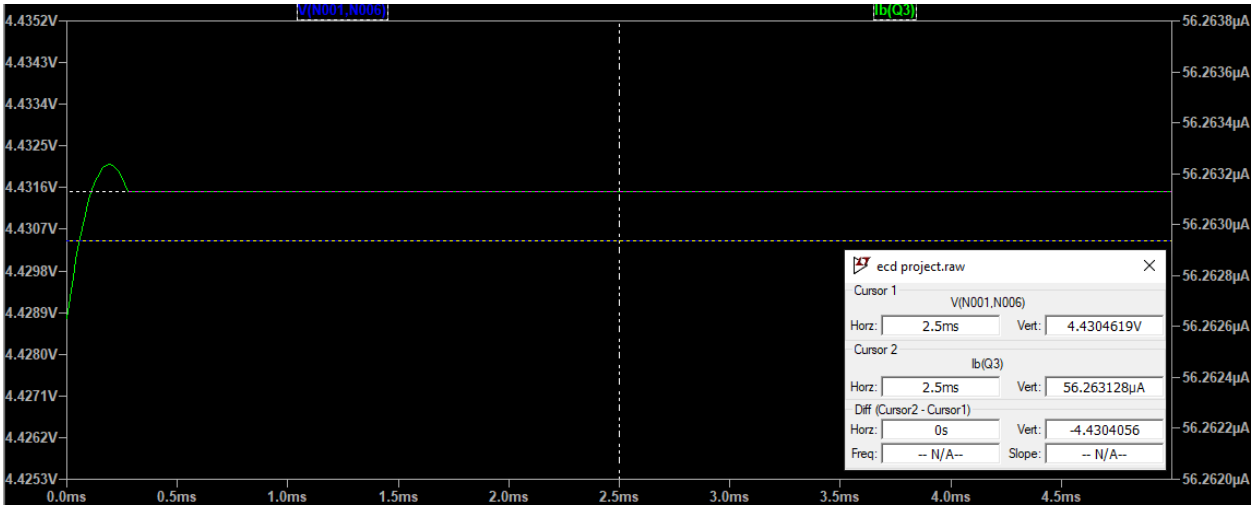


Figure 3: Ib2q current and Vce2q voltage

As can be seen in Figure 3, DC analysis calculations are parallel with the actual values of the base current that goes into the Darlington pair and the collector potential at the out of the Darlington pair. Comparing the calculated values of 187 nA for I_{B2Q} and 4.45 V for V_{CE2Q} to

simulated values of 181 nA for I_{B2Q} and 4.43 V for V_{CE2Q}, it can be seen that error percentages are -3.2% and +0.45%, respectively. These amounts of minor errors point that the calculations are indeed correct.

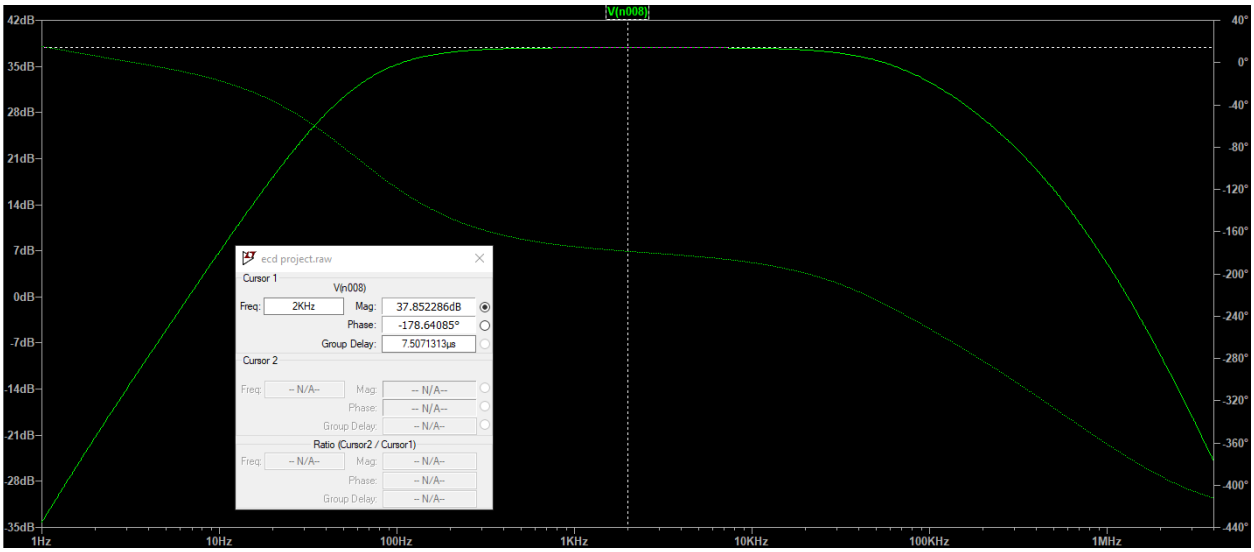


Figure 4: Frequency response of the circuit

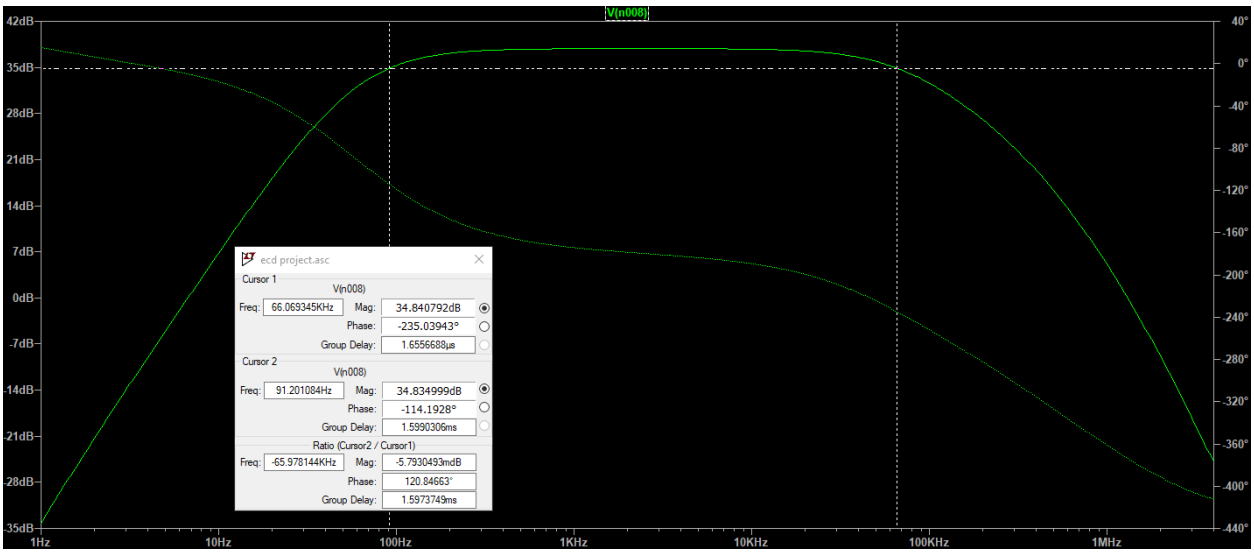


Figure 5: Cut-off points of the circuit

The lower cut-off point of the circuit is at 91.20 Hz, which could be better, but it is not a problem for the human voice frequency range, which is the range the microphone operates.

The higher cut-off point of the circuit is 66.07 kHz; even though 3μF results in 21.9 kHz 3dB cut-off, the only available single-piece capacitor close to that value was 1μF so we changed the design according to the situation after testing if it stops the noise.

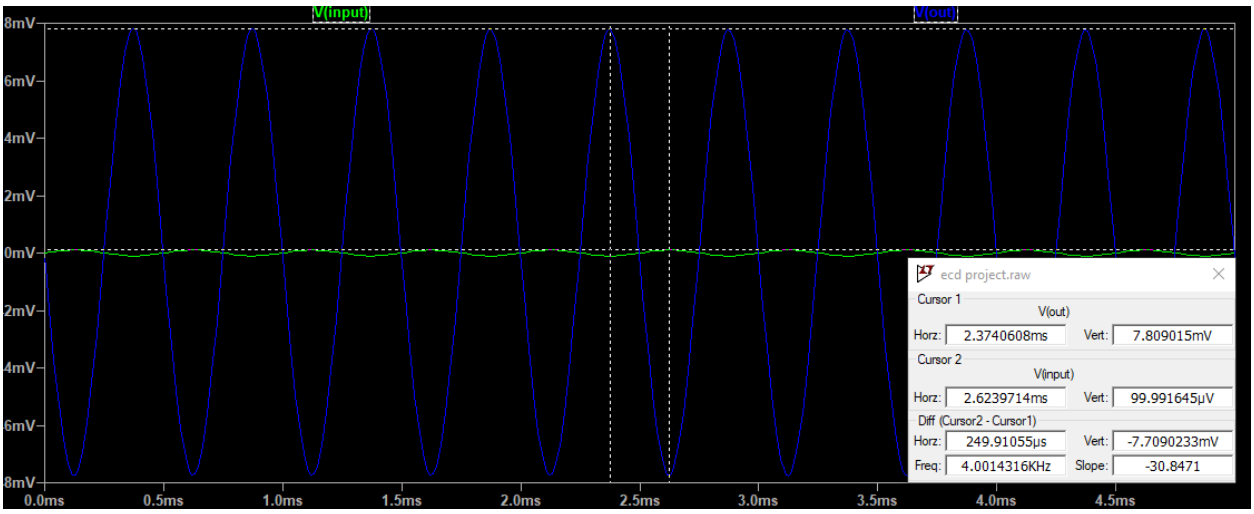


Figure 6: 0.2 mV peak to peak small-signal input

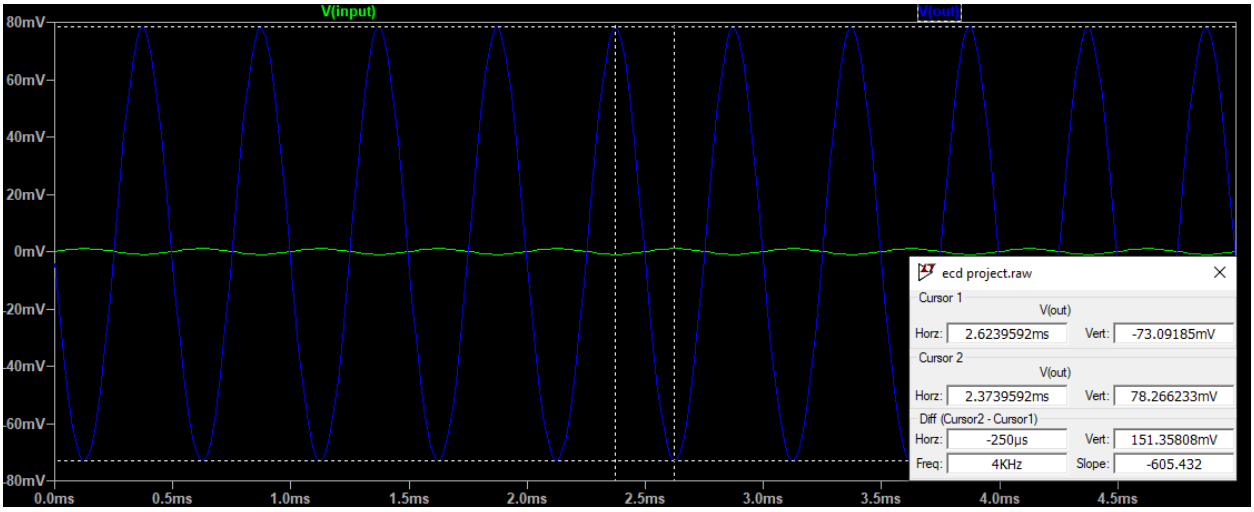


Figure 7: 2 mV peak to peak small-signal input

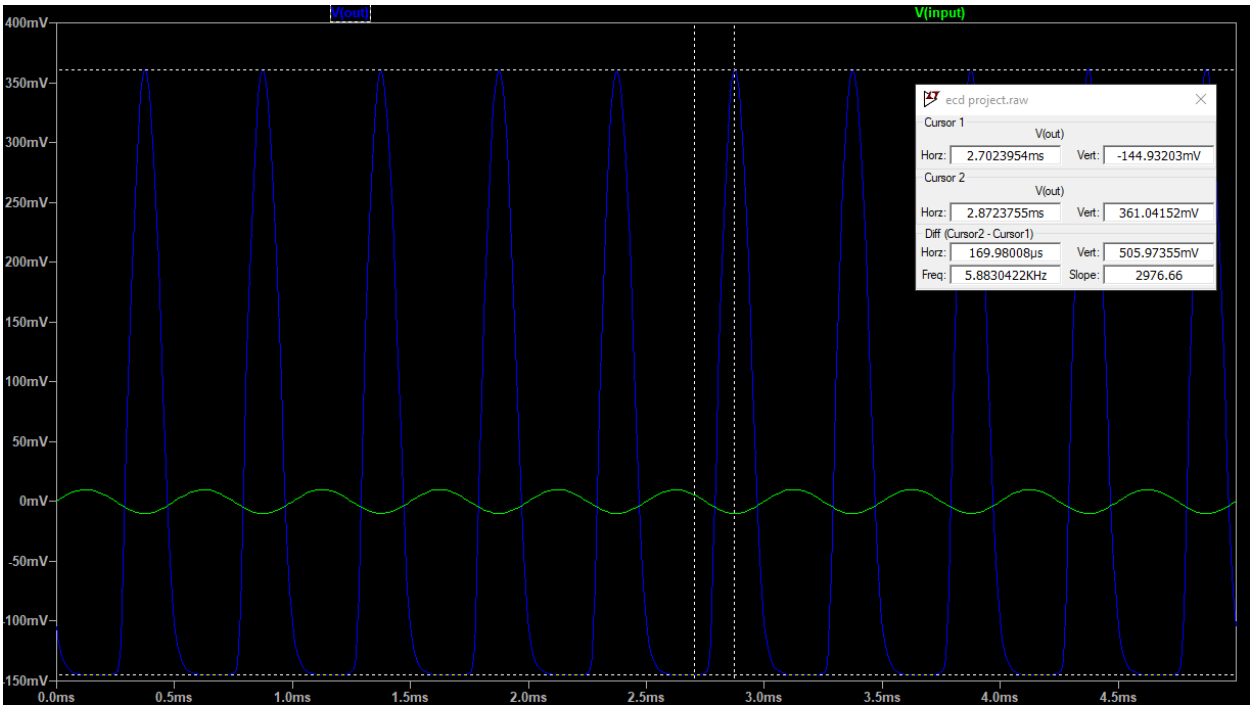


Figure 8: 20 mV peak to peak small-signal input

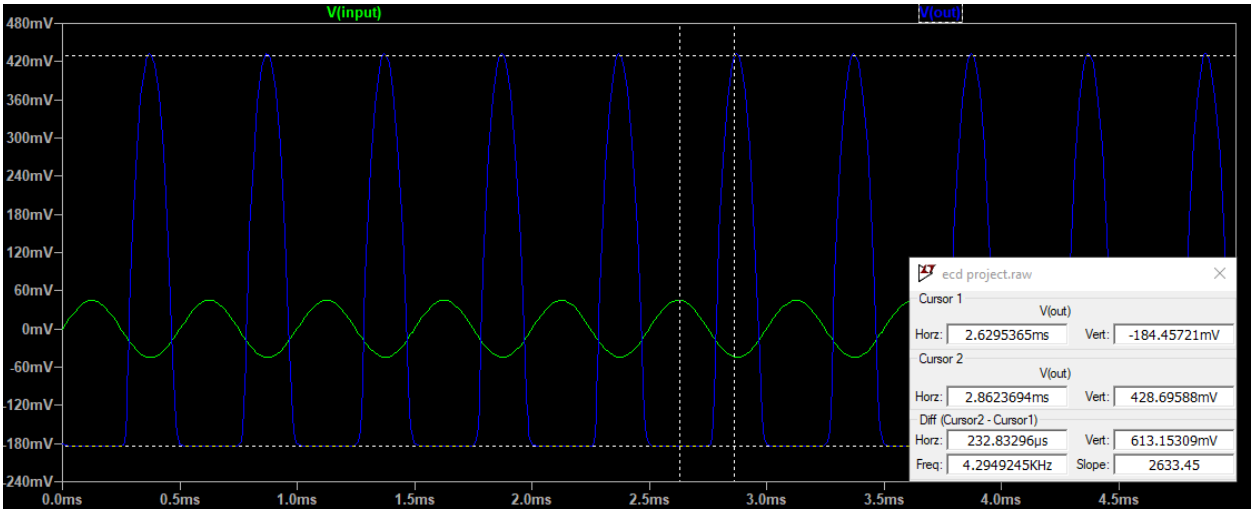


Figure 9: 90 mV peak to peak small-signal input

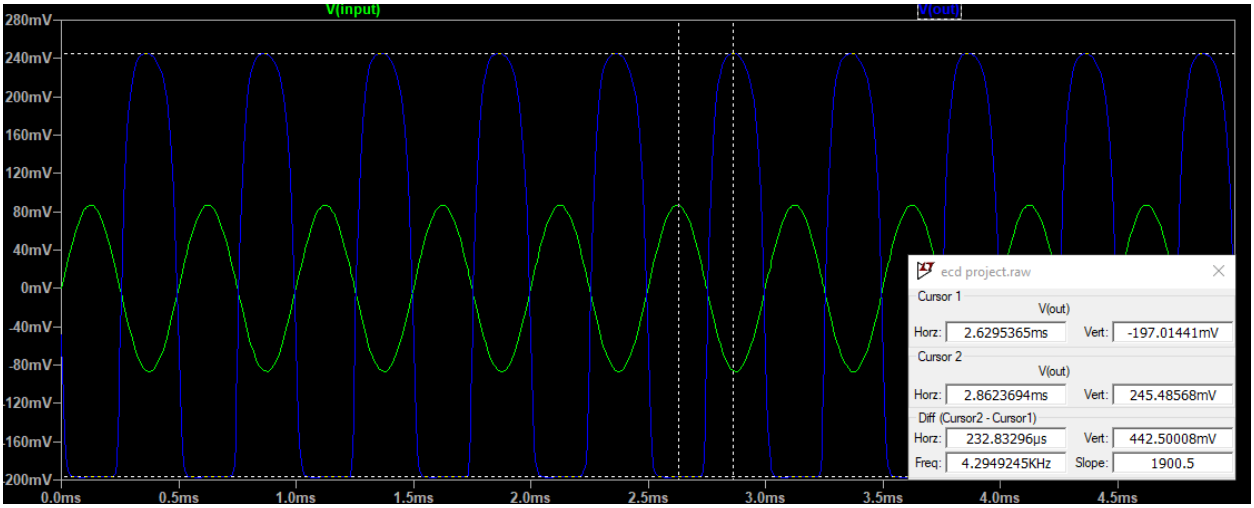


Figure 10: 170 mv peak to peak small-signal input

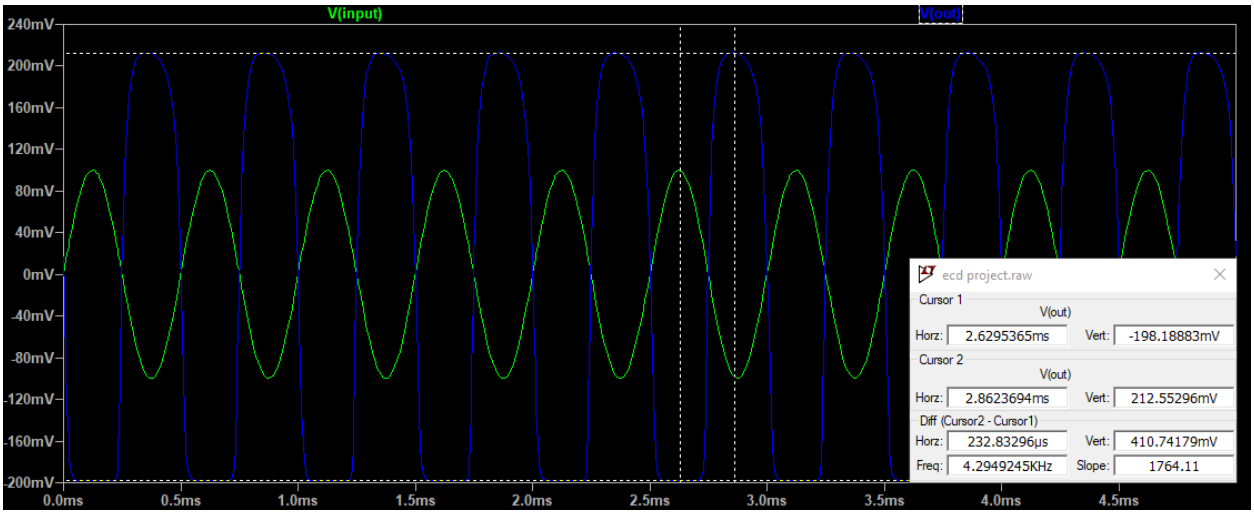


Figure 11: 0.2 V peak to peak small-signal input

Table 1: Input amplitude vs gain

Input (peak to peak mV)	Output (mV) (peak to peak mV)	Gain ($A_v = {}^{V_o}/_{V_i}$)
0.2	15.618	78.09
2	151.36	75.679
20	505.97	25.3
90	613.15	6.813
174	442.5	2.543
200	410	2.05

From Figure 6 to Figure 11, it can be seen that the gain drops as the input voltage grows. This happens due to the clipping resulting from the Darlington pair's last transistor going into the cut-off state. The current in between the Darlington pair transistors, i.e., the base current of the second transistor in the pair, drops to before the sinusoidal cycle is completed, so it gets cut.

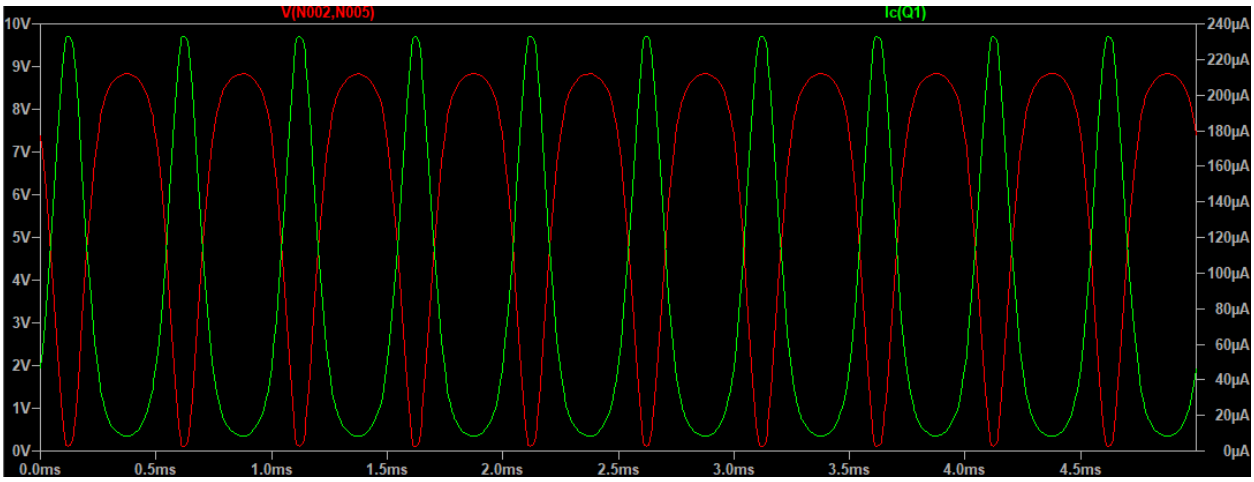


Figure 12: Vce and current of the first stage transistor

As can be seen in Figure 12, V_{CE} It decreases down to 0, and the transistor changes its state to saturation for a while, and this effect gets amplified in each amplification stage. Eventually, the final waveform results in a clipped sinusoidal, decreasing both the gain and quality of the sound.

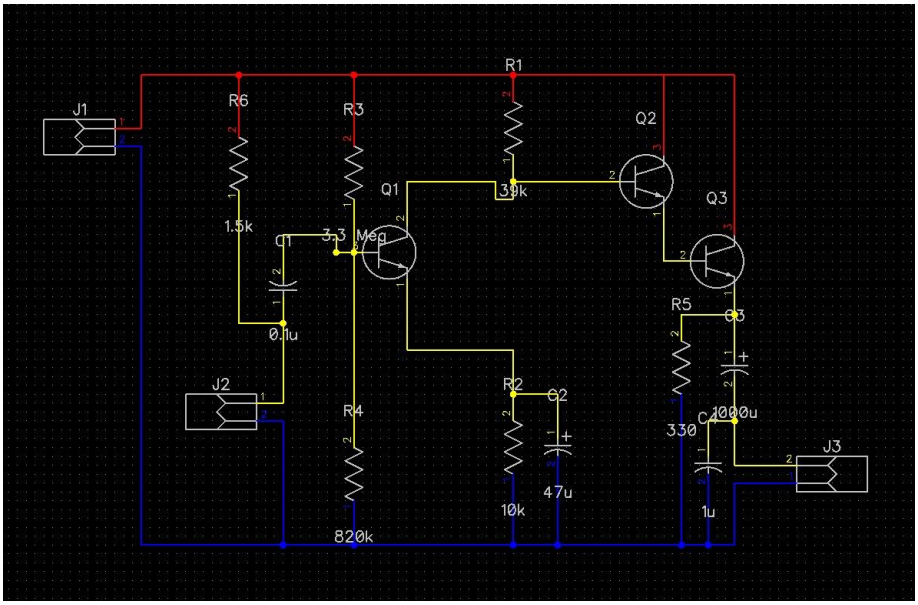


Figure 13: PCB Schematic

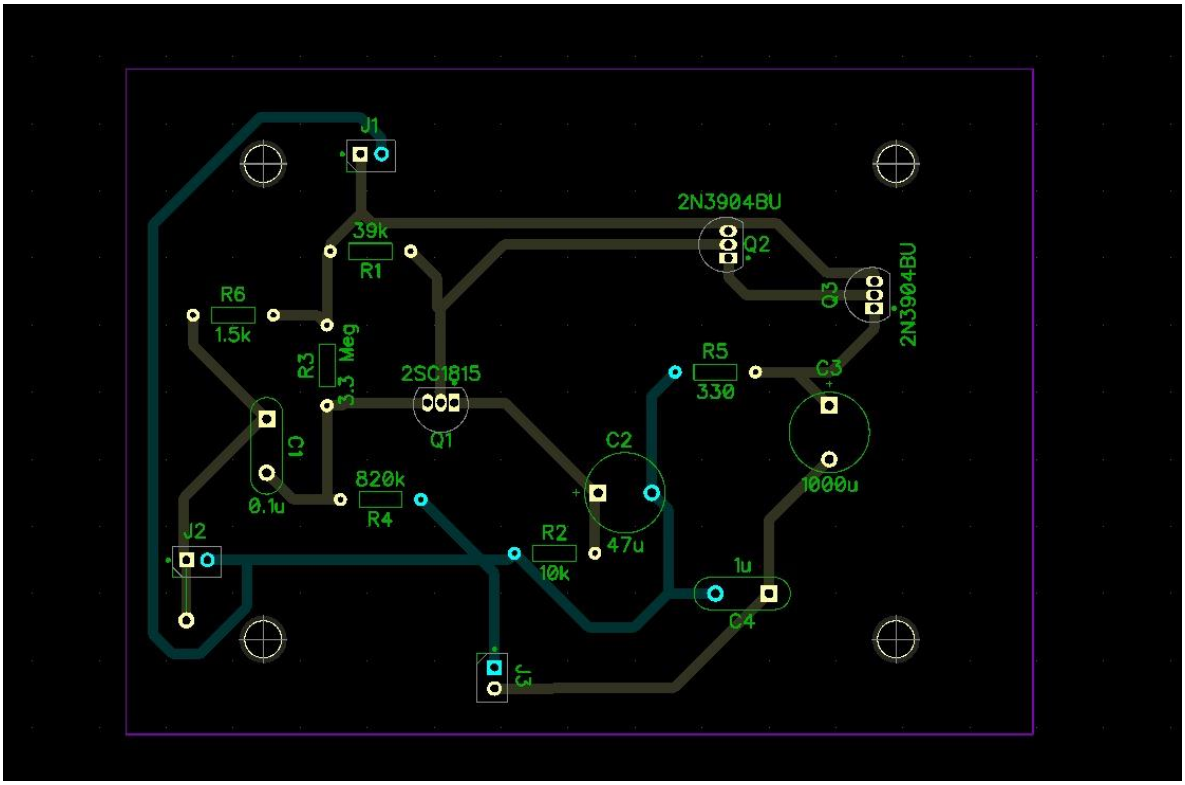


Figure 14: PCB Design

PCB is designed with DipTrace and printed in Bilkent Univrsity laboratory with the given design in Figure 14.

3. HARDWARE WORK

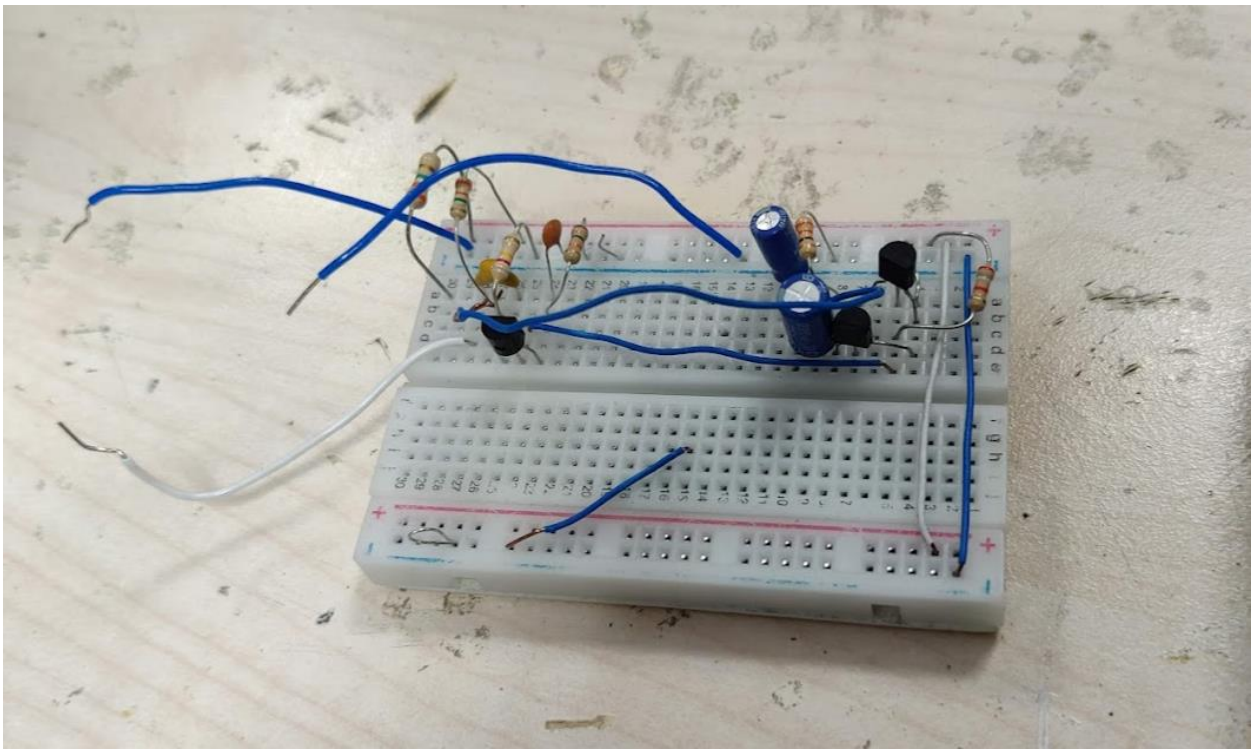


Figure 15: Circuit implementation breadboard

The breadboard is implemented according to Figure 2. It worked except for the tremendous amount of noise resulting from the breadboard's stray capacitances. The gain was similar to the PCB version but with more noise. We both tested the circuit with the aux output of the cellphone and the electret microphone, but the aux port had an output voltage greater than what we needed, and it was getting clipped and distorted more than a tolerable level.

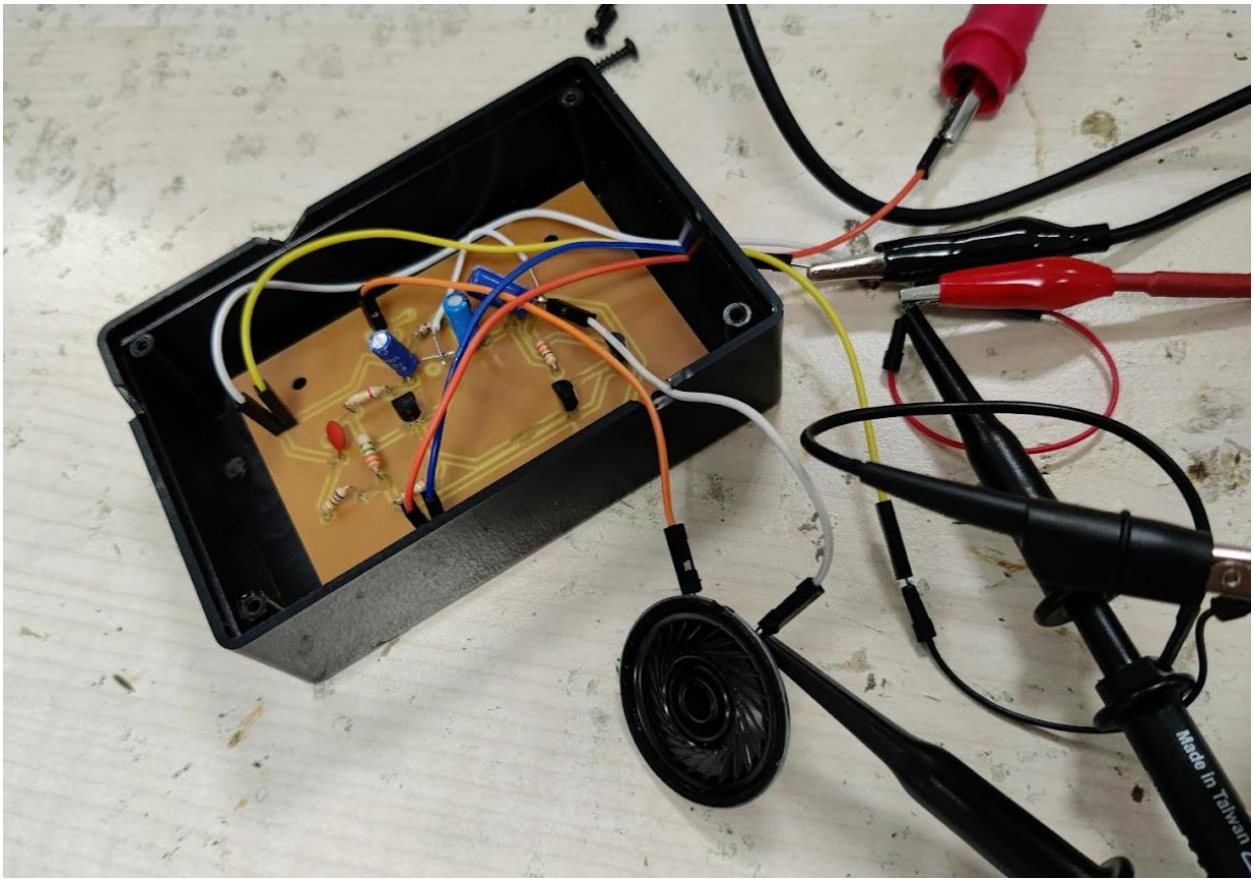


Figure 16: PCB implementation of the circuit

PCB design was successful in terms of sound clarity and gain. The gain was enough to drive the speaker. We ran tests with the function generator, and it had a problem. It couldn't output voltages small enough for us to observe nonclipped signals, and the output it had on lower voltage levels was noisy. So we sacrificed our gain and increased the input voltage enough to get a clear signal.

4. RESULTS AND ANALYSIS

Figure 17: Input signal used for the calculating gain

We used a 45 mV peak-to-peak signal as our input to run our tests. This was not the optimal input voltage to observe the entire gain, but the voltages lower than 45 mV resulted in a noisy input which led to noisy output. The absolute minimum output of the function generator was 10mv's. As expected, the gain dropped significantly as the input signal increased, so we stuck with 45 mV. Due to the 50Ω expected impedance, the value at the input terminals is double the entered value, i.e., 85.6 mV.

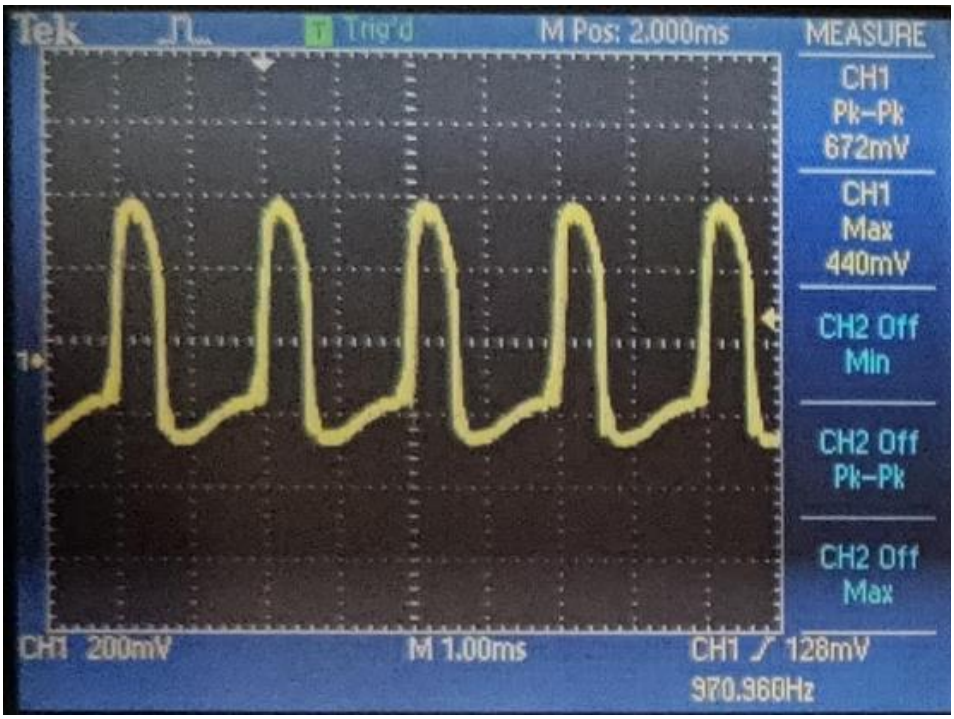


Figure 18: Output signal @ 500 Hz

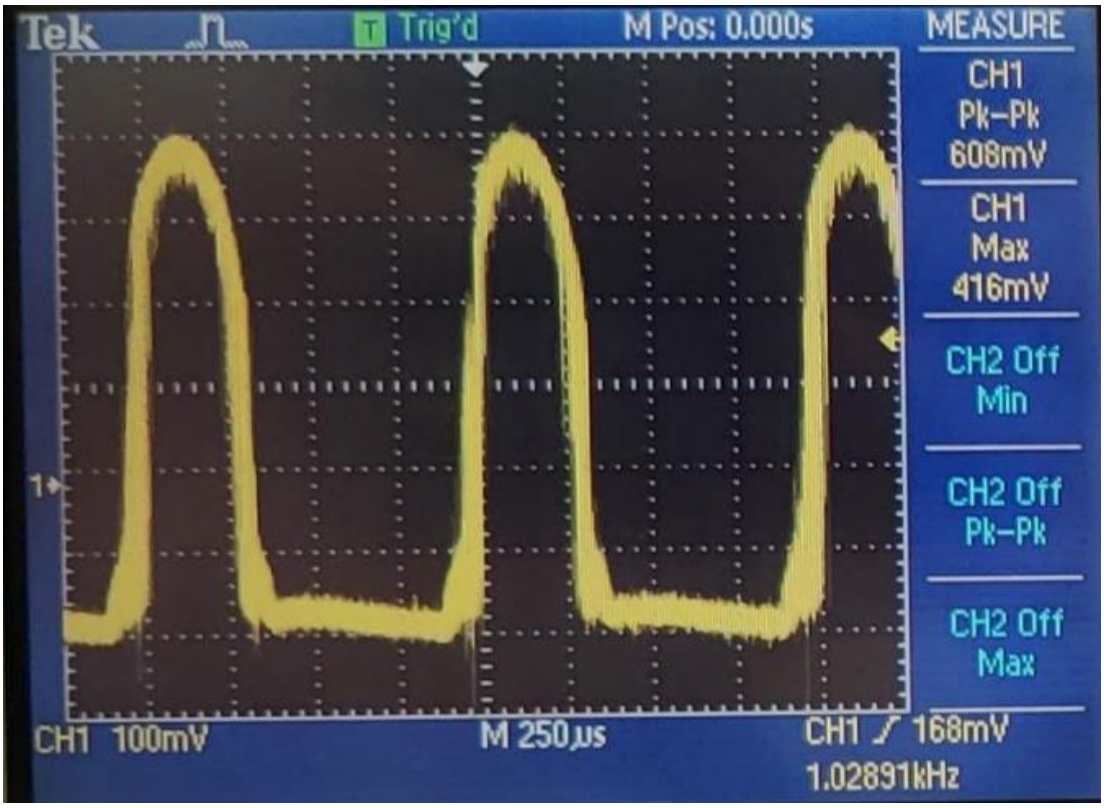


Figure 19: Output signal @ 1 kHz

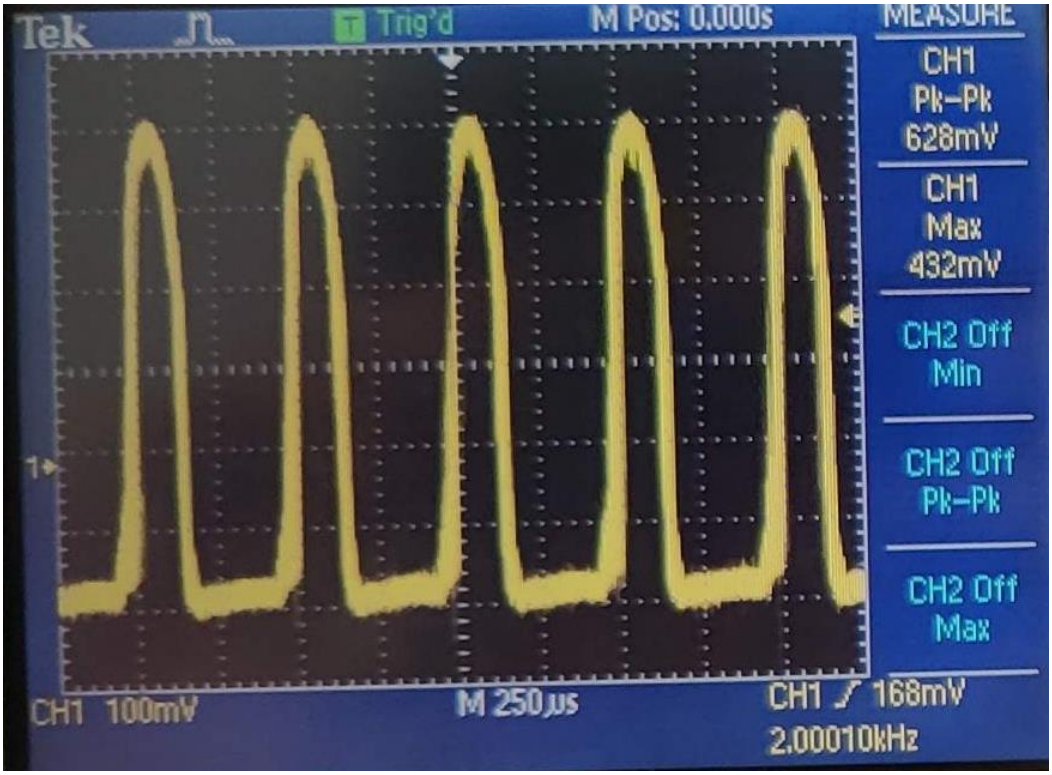


Figure 20: Output signal @ 2 kHz

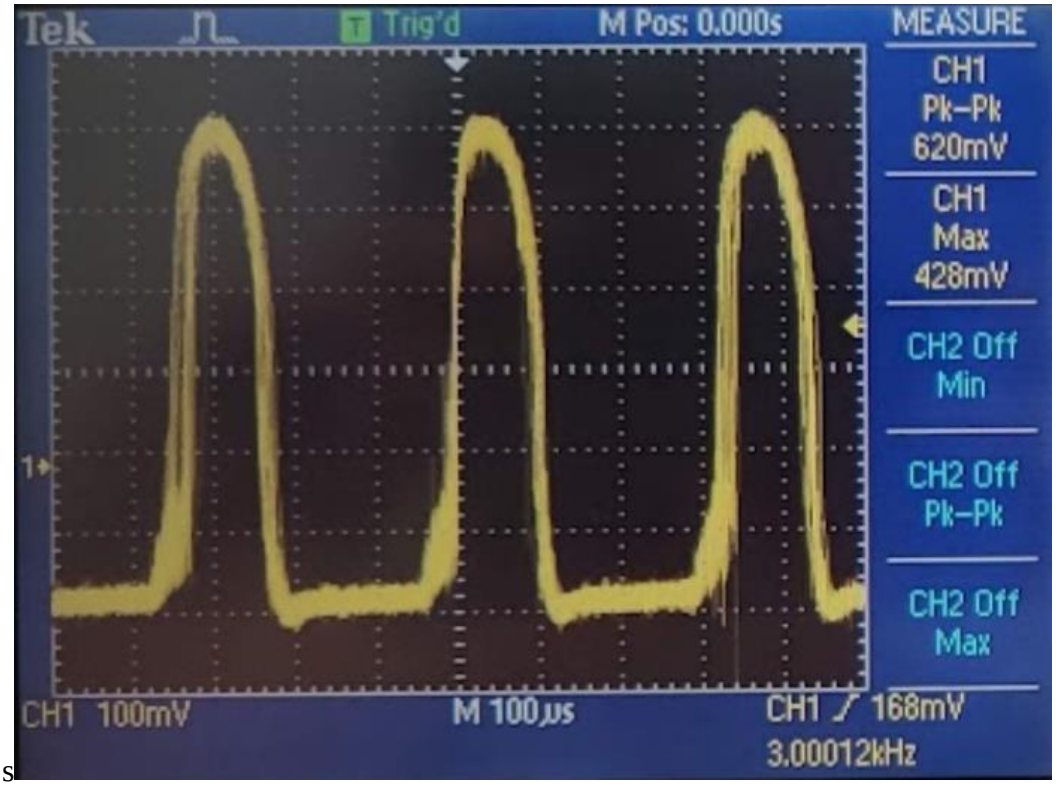


Figure 21: Output signal @ 3 kHz

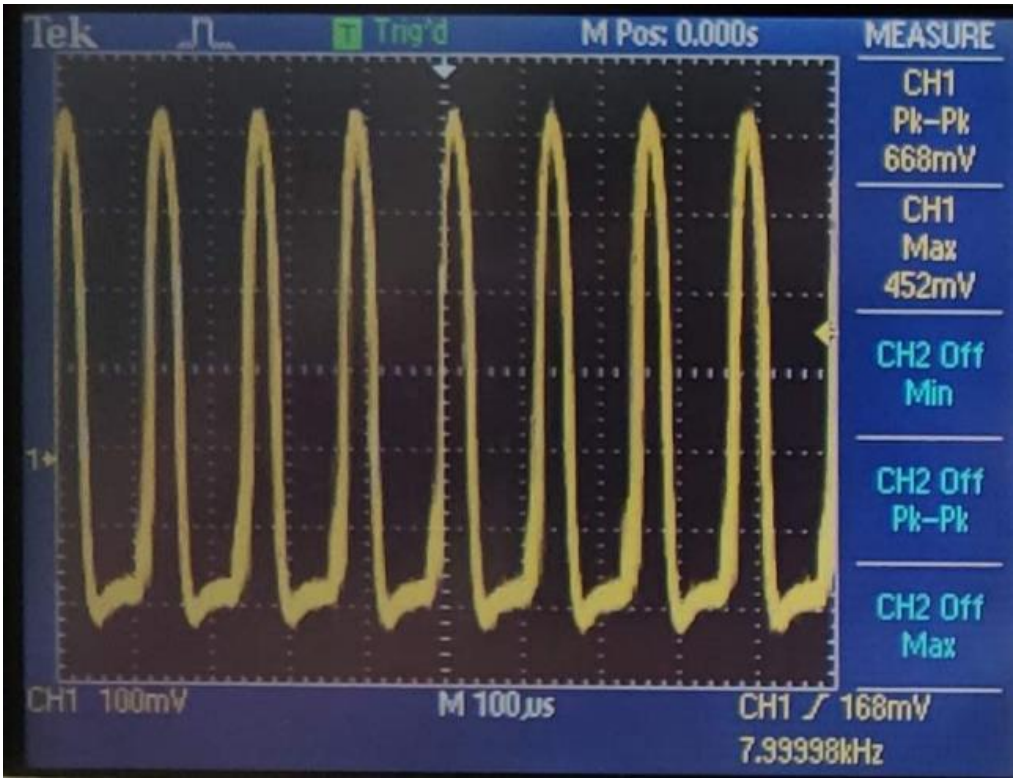


Figure 22: Output signal @ 8 kHz

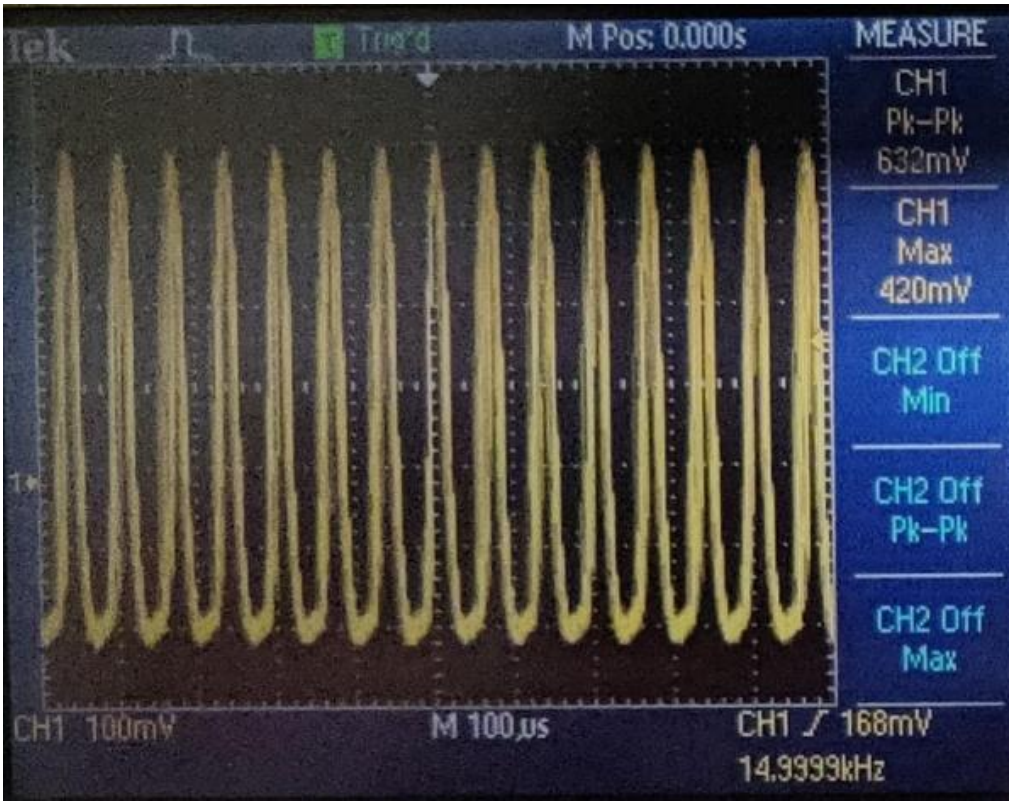


Figure 23: Output signal @ 15 kHz

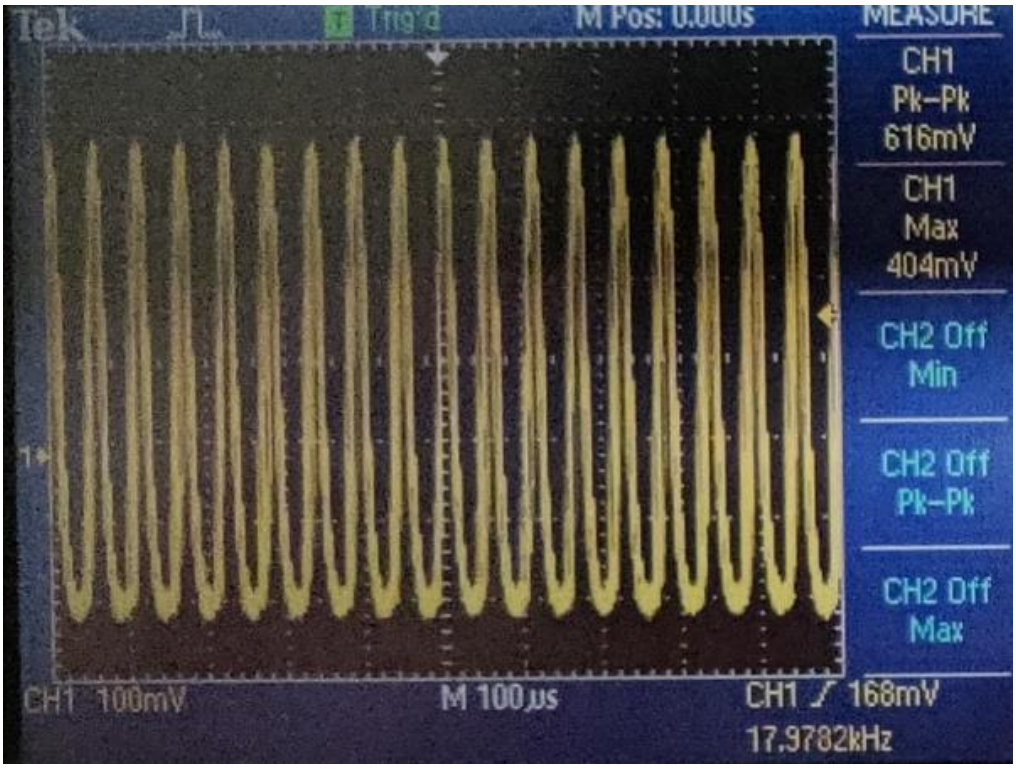


Figure 24: Output signal @ 18 kHz

Table 2: Frequency gain relation

Frequency (Hz)	Gain ($A_v = {}^{V_o}/_{V_i}$)
500	7.85
1000	7.10
2000	7.34
3000	7.24
8000	7.80
15000	7.38
18000	7.20

When Table 2 is inspected, it can be seen that if 500 Hz is neglected, the gain increases slightly towards the middle of the audible audio spectrum and decreases again. Even though the gain is much lower than the intended, it is expected from the tests that were run on LTSpice. The outputs in Figures 9 and 20 have nearly identical graphs regarding the maximum, minimum, and peak-to-peak values of the signals. The reason that 500 Hz data is neglected is explained in the following discussion.

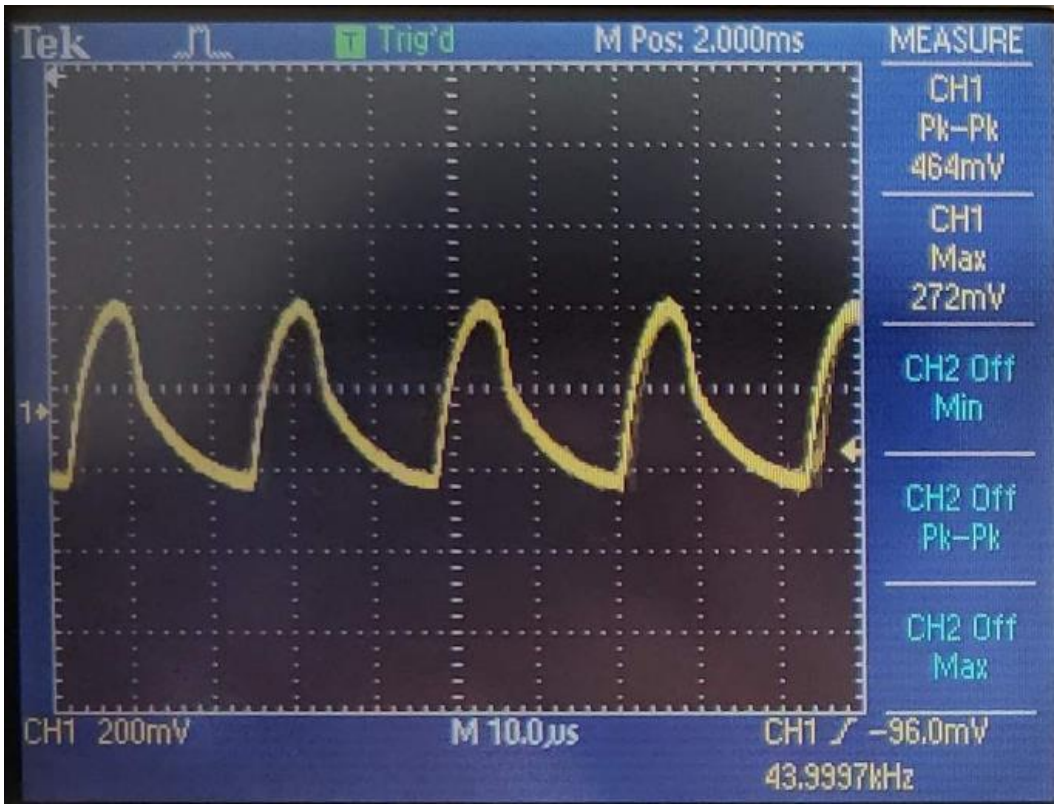


Figure 25: Higher 3db cut-off point @ 44 kHz

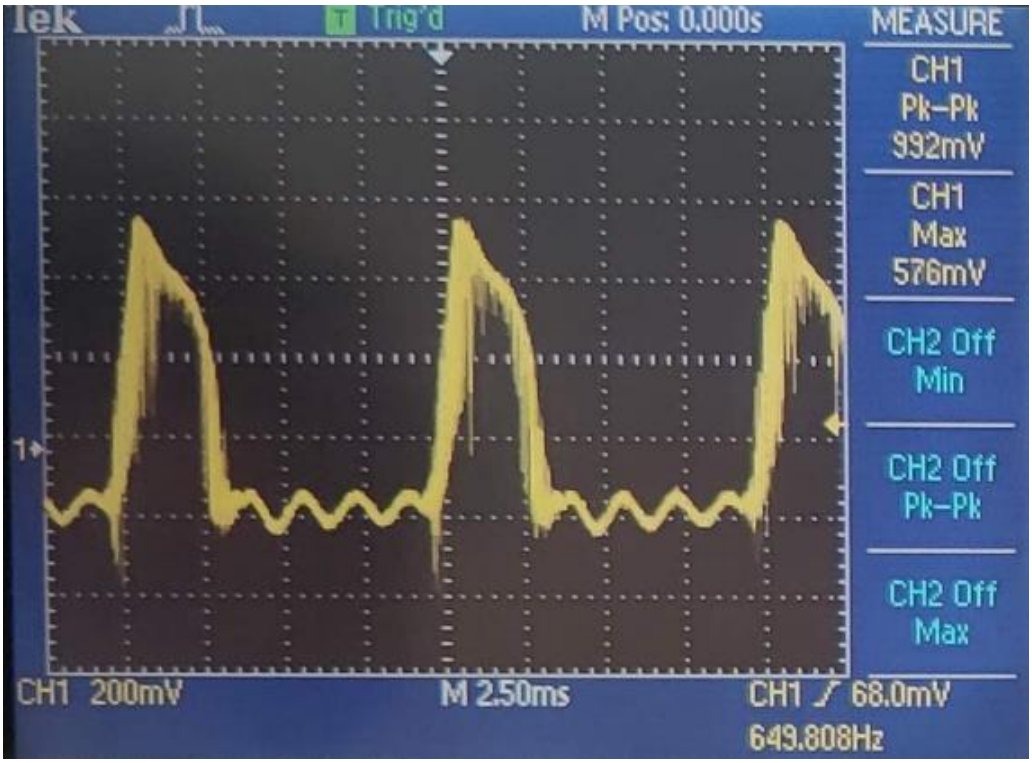


Figure 26: 100 Hz signal output

In Figure 25, the higher cut-off point of 44 kHz can be seen. The simulation calculated the cut-off point to be 66.1 kHz, but this is better for our use case. Even slight errors in the manufacture of the capacitors affect the cut-off points by a considerable amount which is the case in this circuit. The capacitors were measured before the soldering though their values were not recorded, the values changed up to $\pm 15\%$. The cut-off point is calculated by solving the following equation for V_x.

$$20 \log \left({}^{V_o}/_{V_i} \right) = 20 \log(7.45) = 17.6$$

7.6 is an approximate value for the passband gain found using Table 2.

$$17.6 - 3 = 20 \log \left({}^{V_o}/_{85.6} \right)$$

$$V_o \cong 460 \text{ mV}$$

The cut-off point is when the output peak to peak voltage is 460 mV which is satisfied in Figure 23.

In Figure 26, no cut-off point can be observed even though it was observed in the LTSpice simulation. As the input frequency decreases, the gain and distortion increase in the circuit and this increase can be observed until the minimum frequency the signal generator can output; because of that, the lower cut-off point cannot be determined. At 100 Hz, gain increases to 11.6. The reason for this increase is that the harmonics and the effects become prominent at frequencies below 600 Hz. This is the reason that we have neglected the gain at 500 Hz at Table 2.

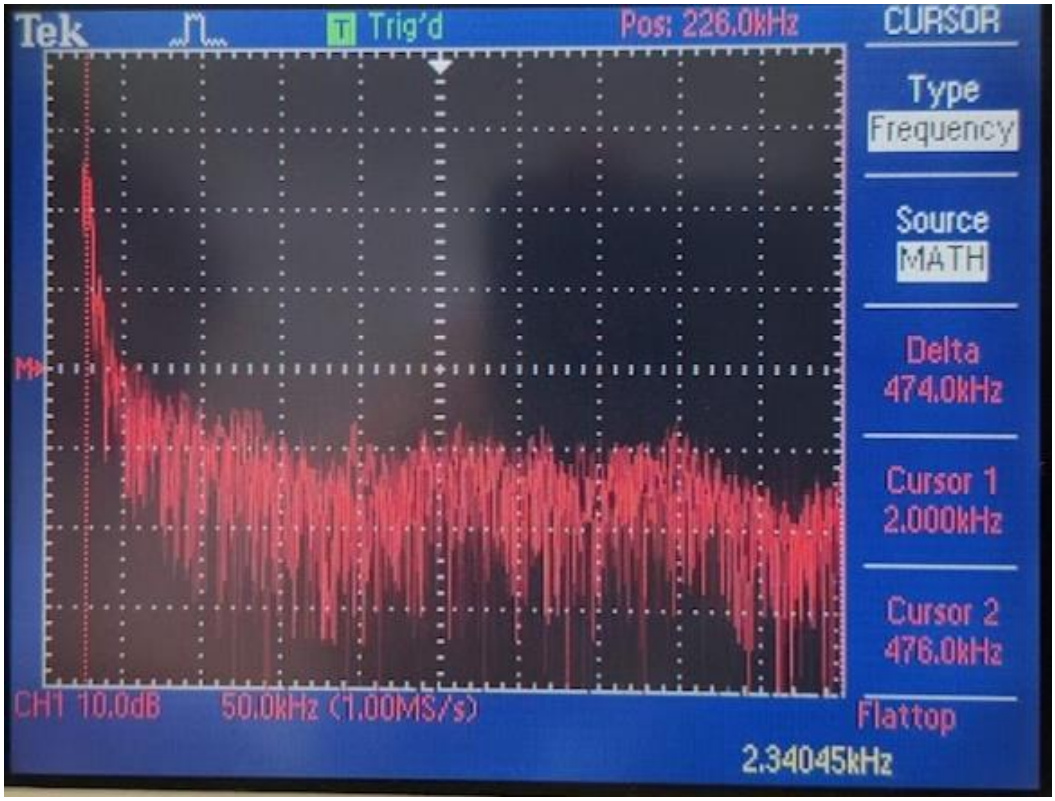


Figure 27: FFT analysis of the signal @ 2 kHz

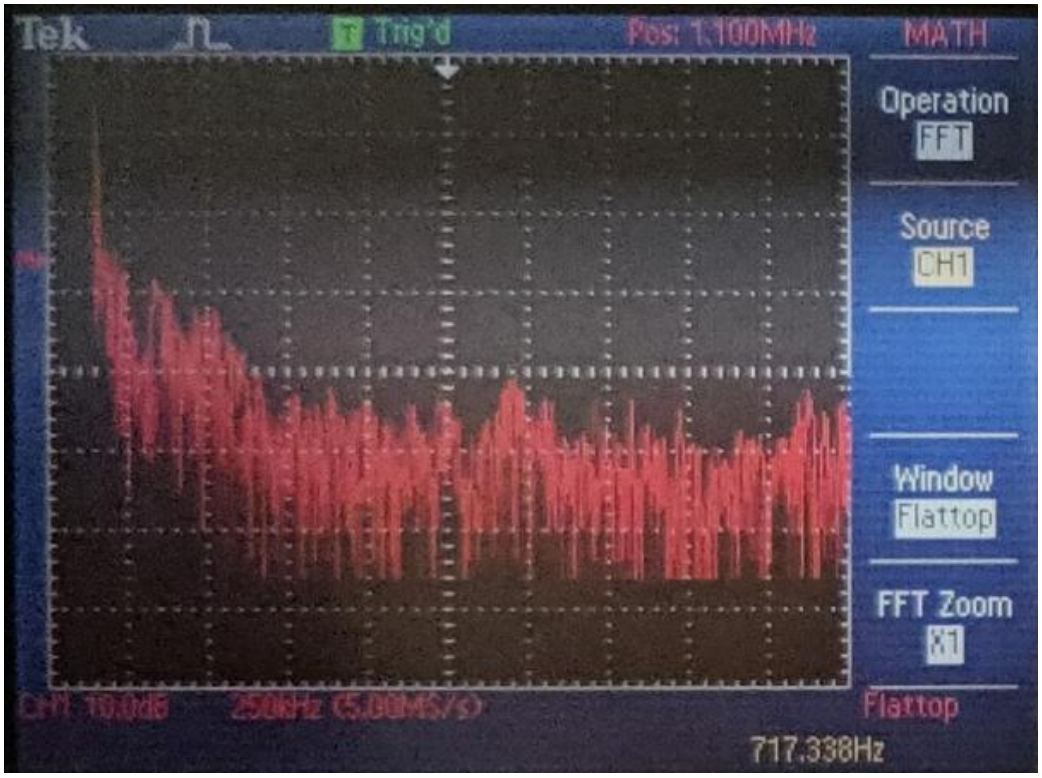


Figure 28: FFT analysis of the signal @ 500 Hz

In Figure 27, the FFT analysis of the output signal at 2 kHz can be seen. The cursor points at 2 kHz and the signals with other frequencies are attenuated relatively fast compared to that of the 500 Hz signal in Figure 28. In Figure 28, it can be seen that harmonics are present with a greater amplitude which gets further increased in lower frequencies. The harmonics both strengthen the signal and distort it. This is the reason for increased amplitude and corrupted waveform. Harmonics are usually the result of the non-linearity of the circuit elements, and non-linear elements in this circuit are the BJT transistors. As the low-frequency signals have more harmonics in the passband, low-frequency signals have more distorted waveform. A 2 kHz sine wave has 22 harmonics in the passband, whereas a 100 Hz sine wave has 440 harmonics.

5. CONCLUSION

The PCB circuit had a notable deviation from the simulation on the lower frequency spectrum. Apart from that, the circuit acted as expected. It is worth mentioning that the system's output is nearly the same as the simulation output in Figure 9 for the same input. When both the simulation and PCB have inputs of 45 mV peak and 2 kHz frequency, they both produce nearly identical results for the mid-band. The PCB had 628 mV and 432 mV for peak-to-peak and maximum voltage levels, whereas simulation had 613 mV and 429 mV for peak-to-peak and maximum voltage levels. Errors percentages are +2.5% and +0.70% respectively. These error levels are well below the expected errors for an amplifier design.

The Q point calculation for the Darlington pair also proved to be precise when the simulation was done and I_{B2Q} and V_{C2Q}values are checked.

The higher cut-off point could have been better chosen, but it differs when implemented in the actual circuit. The calculated cut-off, the simulated cut-off, the cut-off on the breadboard, and the cut-off on the PCB were all different from each other. So the best practice for finding the correct higher cut-off point by trial and error, but the result cuts the high-frequency noise, so it is enough for this application.

The deformation of low-frequency inputs can be restored by applying another non-linear delay element that would counter the effect of the amplifier on higher frequency harmonics.

Designing amplifiers are not a one-step job. They require debugging and tweaking the values of the components, as every system has unique defects that computers cannot predict. Even though a computer can design an amplifier, applying it to real life and making it work as intended usually requires expertise.

Working on this project helped me better understand the nature of amplifiers and gave me a lot of insight into Darlington pair transistor amplifiers. Also, debugging the circuit and tackling different problems was informative and fun in its own way. Seeing my prototype work and results being parallel to the simulated and calculated values was invaluable for me.

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