

Piyush Mishra

piymis.com
piymis6@gmail.com | +91 9911669538

EDUCATION

DELHI TECHNOLOGICAL UNIVERSITY

B.TECH IN ELECTRONICS & COMMUNICATIONS
May 2015 | Delhi, India
Aggregate: 73.4%

DAV PUBLIC SCHOOL AISSCE, CBSE

March 2011 | Delhi, India
Aggregate: 88.2%
AISSE, CBSE
March 2009 | Delhi, India
Aggregate: 85.8%

SKILLS

LANGUAGES

Proficient:
Python • C • C++ • Javascript
Java • Shell Script • HTML • CSS
Familiar:
Perl • VHDL • SQL • Assembly

FRAMEWORKS

Django • Flask • Bootstrap
React • Tkinter

TOOLS

Git • Jenkins • Jira
NPM

LINKS

Github:// [piymis](#)
LinkedIn:// [piymis](#)

PROJECTS

AI chatbot
Reddit bot
Terminal text editor
URL shortener
Shell utility scripts

EXPERIENCE

AMADEUS | SENIOR SOFTWARE ENGINEER

July 2015 – Present | Bangalore, India & Nice, France

- Developing REST APIs to handle shopping, booking & after-sales operation of Hotel IT platform for Premier Inn. Languages: Python
- Developed backend components for rail webservices distribution platform handling booking & ticketing functionalities. Languages: Python & C++
- Developed web application, REST API & python library for managing of passenger record data. Framework: Django. Languages: Python
- Developed tool to migrate API changes for SOAP based test scenarios. Languages: Python & Perl
- Developed command line interface for using internal logging facility & issue tracking tools. Languages: Python
- Acted as production load coordinator across global regression teams for Rail Business Unit.
- Mentoring and grooming of team-members and interns.

MTS INDIA | INTERN

May 2013 – Aug 2013 | Delhi, India

- Developed command line interface for internal issue tracking system. Language: Python

BHARAT ELECTRONICS LIMITED | INTERN

Jan 2013 – May 2013 | Ghaziabad, India

- Design, simulation & testing of electronic FPGA systems. Language: VHDL & C.

RESEARCH

I2C BUS PROTOCOL DESIGN AND SIMULATION

Sep 2013 – Dec 2013

Implemented I2C bus protocol clocked at 100 KHz on Spartan-3E FPGA board.

REVERSIBLE LOGIC GATES

Feb 2014 – May 2014

Implemented and simulated the design of reversible combinational circuits using CMOS transmission gates in VHDL.

WORKSHOPS

AGILE ASIA

Bangalore, India

Behavior driven development using Java & Python

TEXAS INSTRUMENTS

New Delhi, India

BeagleBone Black development using cloud9 IDE

AWARDS

2018	Top 10	Futurize hackathon. Amadeus Labs
2017	Top 4	Department Innovation. Amadeus Labs
2016	Twice	Recognised for work. Amadeus Labs
2013	Top 5	Electronic Voting Machine, Troika IEEE
2011	Top 0.2%	IIT-JEE & AIEEE 2011