End of exam

Visvesvaraya National Institute of Technology, Nagpur Department of Electronics and Communication Engineering	*Mid Semester Examination (2023 – 24)*
Sub: (ECL216) Digital Circuits and Hardware Design	Time: 1 Hour and 30 Minutes **Max. Marks: 30**

Important Instructions:

1. Questions carry marks as indicated in ***bold and italics.*** Use of non-programmable calculator is allowed.
2. Assume suitable data, constants if required. (Specify it before using in the answer).
3. CO refers to Course Outcome Covered in the respective question.

		Marks
Que 1:	Find the output Y of the circuit as shown in figure 1 and implemented it using NAND gates only. **(CO1, CO2)**	*(05)*

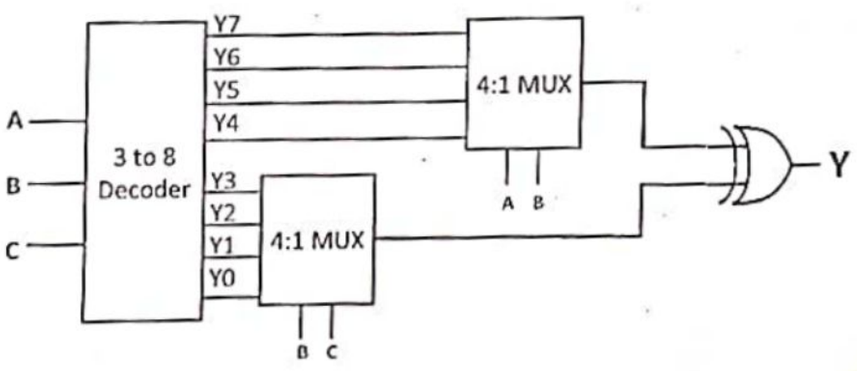


Figure 1: Figure for question 1.

		Marks
Que 2:	The five variable function f is given in terms of minterms as follows:- $f(A, B, C, D, E) = \sum m(0,2,3,8,10,11,12,14,15,17,19,20,31)$. Using the Quine Mccluskey method minimize the function in the sum of products (SOP) form. Also, give the realization of the minimized function using basic gates only. Show all steps and all connections properly. **(CO1, CO2)**	*(10)*

Que 3: For the multiple code convertor (MCC) black box shown in figure 2, the inputs are $I_3I_2I_1I_0$ and the mode selector bits are M_1M_0. The working of the black box is as follows:-

Sr. No.	Mode Control bits (M_1M_0)	Working Mode
1	00	Binary to Gray Code Convertor
2	01	Gray to Binary Code Convertor
3	10	Binary to Excess-3 Code convertor
4	11	Block all above three options and make the output "Valid/Invalid Output" bit as 1(high).

Design this multi code convertor (MCC) black box to convert the 4-bit input to corresponding code. To implement the circuit use basic gates only. Use of any other devices is not permitted. For $M_1M_0 = (11)_B$ only the "Valid/Invalid Output" bit is 1 (1 high) for all remaining combinations it is 0 (Low). Show all the steps properly in the designing. **Hint:** I_3 is MSB; M_1 is MSB, Design the circuit as per the table indicated above.

(CO1, CO2)

Mark

(15)

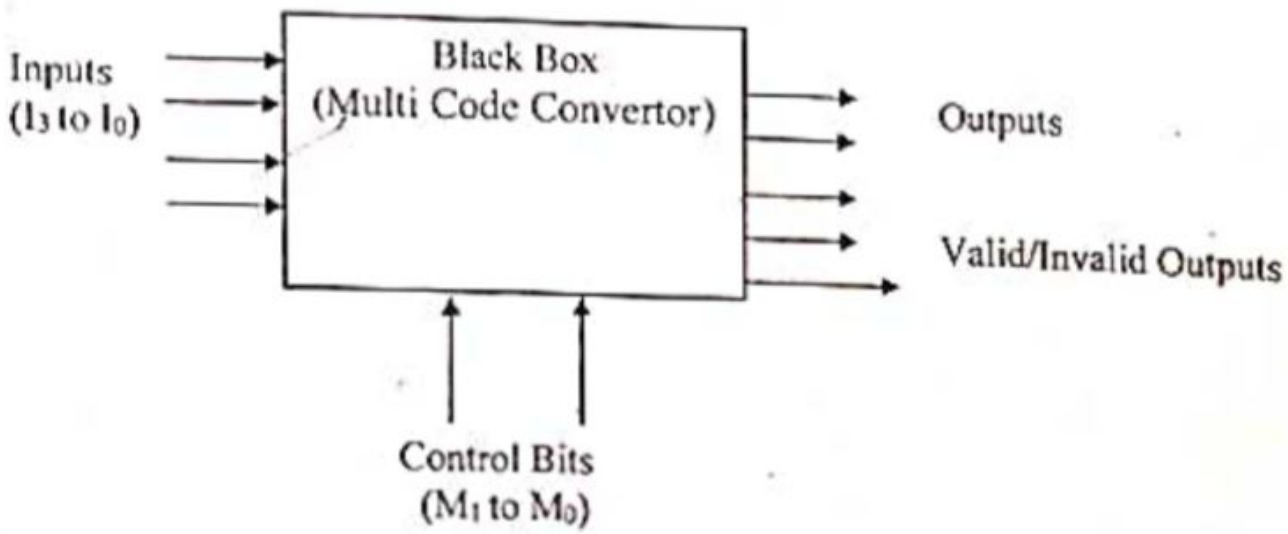


Figure 2: Figure for Question 3.

BT22ECE034

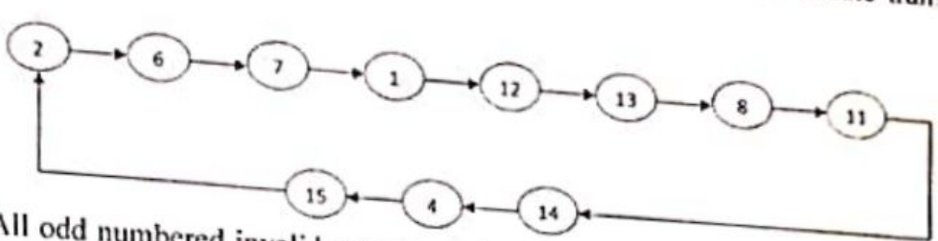
Visvesvaraya National Institute of Technology, Nagpur

Department of Electronics and Communication Engineering

End Semester Examination (2023 – 2024)

Sub: (ECL216) Digital Circuits and Hardware Design | **Time:** 3.00 Hrs | **Max. Marks:** 50

1. Use decimal numbers (default) for calculations
2. Numbers (Bold and Italics) on right hand side indicates marks. [CO] indicates COs.
3. ***Assume suitable data if necessary and specify it in your design at the beginning.***
4. Default number system used in questions is decimal number system unless specified otherwise.

Q. 1	Find a minimum sum-of-products expression for the following function: f(A, B, C, D, E) = $\sum$m (0, 1, 3, 8, 9, 13, 14, 15, 16, 17, 19, 24, 25, 27, 31) using Quine Mc-cluskey method. Obtain all possible minimal expressions.	[CO1, CO2] ***(10M)***
Q. 2	Design a FSM to detect the sequence **1010** in an incoming bit stream. When the sequence is detected, the FSM produces an output logic high else the output always remains active low. FSM designing steps are to be followed with memory element designing using D flip flops. Show all steps properly. Overlapping of sequence is permitted.	[CO2, CO3] ***(10M)***
Q. 3	Design a synchronous counter using T flip flops which has the state transitions as given below.  All odd numbered invalid states must jump to state 6 while all even number invalid states must jump to state 11. Draw the full sate diagram and design the circuit with proper details.	[CO1, CO2, CO3] ***(10M)***
Q. 4	a) Write Verilog code for 4:1 MUX using a) Behavioural and b) Gate level modelling. b) Write Verilog code for the function f(P, Q, R, S) = Σm(0,2,4,6,7,8,10,12,13,15) using Dataflow modelling.	[CO3, CO5] ***(6M)*** [CO3, CO5] ***(4M)***
Q. 5	Write Verilog code 8-bit adder which adds $A_0A_1A_2A_3A_4A_5A_6A_7$ with $B_0B_1B_2B_3B_4B_5B_6B_7$ Use Full adder as instantiation component using gate level modelling.	[CO4, CO5] ***(10M)***

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