Department of Electronics and Communication Engineering, VNIT Nagpur

Subject: Digital Circuits and Hardware Design (ECL 216)

Assignment No.1

Cos Mapped: CO1

Questions on number system (conversion type):

1. Convert the following Octal numbers to binary

23	76	55	765	765	65	32	453	321	321	11	67	123
54	65	66	342	342	12	76	123	156	156	232	232	240

2. Convert the following floating Octal numbers to binary

34.56	23.54	10.43	76.33	657.444	12.34	34.43	77.4	132.4	1233.33	22.46	22.22	67.34
11.25	11.23	55.22	343.22	234.54	40.36	24.43	74.4	152.4	1243.33	25.46	122.22	467.34

3. Convert the following Hexadecimal numbers to binary

A759	976	329	D43	9965	3AD4	543	956	9B7	3456	AB54	FE52	12DC
32C	997	876	9CC5	9345	9D6	759	932	87A	4222	932	349	A76

4. Convert the following floating Hexadecimal numbers to binary

23.54	90.43	2A.22	7A.33	234.54	34.43	95.22	9C.23	9BB.33	23F.54	8D.34	9AB.D
22.22	76.33	CD.43	234.54	91.23	34.B3	9D.22	9233.33	95.23	54.C3	5D.82	9BC.33

5. Convert the following Decimal numbers to binary

239	96	55	765	765	65	32	453	321	58321	811	9867	123
754	65	66	342	342	12849	76	183	156	9156	232	2328	240

6. Convert the following floating Decimal numbers to binary

34.56	23.54	18.43	76.33	659.444	12.34	34.43	77.4	932.4	1833.33	22.46	822.22	697.34
11.25	11.23	55.22	343.22	234.54	40.36	24.43	74.4	159.4	1983.33	25.46	122.22	467.34

7. Convert the following binary numbers to decimal:

101001001	11001001	1001001111	101001	101010101
10101001	11000001	1100111	1111	11001001
1111001	110011	110000001	110011	1111111001
11001001	1101	110010011111	1001001	11001001
101101	110011	101001001	100100100	1000010
11001001	11101001	10101001	1000010	11001001
1111	1001	1111001	11001001	1101101001
110011	1000010	11001001	1001001111	111001
1001001	11001001	111101	1100111	110100101010

8. Convert the following floating binary numbers to decimal:

111.01101	11101.01	1111.11	1001.1	1101011001.01101
11111.01	111111.1	11101.0001	1111.1111	1101110001.01101
11001.001	11001.00001	11.101001	100101010.111	1000111001.01101

9. Convert the following binary numbers to octal:

1011010	11001001	110010011111	111001	11111111
1011111	1000010	101001001	110100101010	101010101
1010101001	110011	101001001	110010	11001001
100110101	1101	10101001	110010	1001111001
10010001	11101001	1111001	110010	11111001
1001001111	1001	1010101001	110001	1101001

1100111	1000010	11010000111010	1000010	100001110
101010101	11001001	110101	11001001	1101111
11001001	1001001111	11001001	1001001111	1101111
1111111001	1100111	1101101001	1100111	1001101111

10. Convert the following floating binary numbers to octal:

1101.0011	11001.001	111101101.01	1010010.01	1010101101.0111
1111.1111	100001.11	1101010.1101	1100111101.001	110011101.1001
100101010.111	10100100.111	1101101.001	1011101001.001	1011011101.0111
11001.001	1010111101.0101	11001.0101	111100111101.11	111100101.1001

11. Convert the following binary numbers to hexadecimal**:**

111001	11011001	11001111	10010111	111101111001
101001	11001001	101010101	1101101001	11111110110101
1111001	110101	1000010	1111100111	110010011111
1111001	110010	101001001	1101101001	10001101010
111001	11001001	1100101101	1111111001	110101101010
101101	11001001	1010100111	11001000001	110110001010
111101	11001001	1010010101	1101101001	110100101010
1111001	11001001	10100111001	1010101010101	11010000111010
10101001	101001001	1101101010	1010101001	11010100110
11001001	1000010	1111111001	110010011111	11010110110

12. Convert the following floating binary numbers to hexadecimal**:**

11001.001	110011110.00001	11010010101.11	1111100110.1101	10101010101.1001
101011001.111	1101001010.11	11010000111.1101	11011010010.001	101010111010.11
10111111.0011	11010010101.1101	100101010.1101	111111100.1011	111110000011.101

13. Convert the following decimal numbers to any base:

93	86	543	956	75	759	932	932	42	329	543	543	9345
84	72	997	876	87	349	976	976	39	956	997	3456	4222
86	932	876	9965	35	976	329	3456	45695	9965	2351468	548623216	12546897945

14. Convert the following floating decimal numbers to any base:

23.54	91.23	76.69	569.26	91.23	34.96	81.23	932.4	76.33	91.29	76.33
34.43	90.43	34.43	234.54	90.43	92.34	90.53	8856.33	56262.336	8569.264	92346.55
22.22	95.55	52.22	456.59	95.22	42.4	25.22	14233.33	458951.1265	32478465.25	1223.486

Theory Questions:

1. Explain how BCD addition is carried out?
2. How can the XOR operation be expressed using other operators?
3. Compare and contrast the AND gate and the NOR gate.
4. What is meant by overflow? Is it a software problem or a hardware problem?
5. Distinguish between l's and 2's complements.
6. Distinguish between 9's and l0's complements.
7. How do you add two decimal numbers in the BCD form if the sum is greater than 9?
8. Define odd and even parity check codes.
9. Write a short note on "weighted and non-weighted codes".
10. What is a Gray code? Why is it important?
11. What is a Hamming code and how is it used?
12. Design AND, OR, NOT, EX-OR, EX-NOR gates using universal gates.
13. Draw the internal IC structure and pin diagram of AND Gate, OR Gate,.
14. Draw the internal IC structure and pin diagram of NOR Gate, NOT Gate

15. Draw the internal IC structure and pin diagram of NAND Gate, EX-OR Gate and EX-NOR Gate.
16. Discuss the pin diagram, logical gate structure and Boolean expression of universal gates.
17. What are the types of gates? Differentiate between basic gates and derived gates?
18. Write detailed description about SN7401 IC.
19. What is difference between logic gates and integrated circuits?
20. Explain the significance of MC, 74, HC, 04 and N from the series device number MC74HC04N.
21. Write down briefly on which technology the following logic family works :
    (a) 7400; (b) 74L00; (c) 74H00; (d) 74LS00; (e) 74LS02; (f) 74LS08
22. If a 3-input NOR gate has eight input possibilities, how many of those possibilities will result in a HIGH output?
23. If a signal passing through a gate is inhibited by sending a LOW into one of the inputs, and the output is HIGH, the gate is _____.
24. When used with an IC, what does the term "QUAD" indicate?
25. The output of an OR gate with three inputs, A, B, and C, is LOW when _____.
26. Name the gate for which the output will be a LOW for any case when one or more inputs are zero.
27. Draw OR, AND and NOT gate using Diode wired AND logic.
28. Draw OR, AND and NOT gate using Diode wired OR logic.
29. Draw OR, AND and NOT gate using Transistor.
30. Draw AND, NOR, XOR and XNOR using Diode.
31. Draw NAND, NOR, XOR and XNOR using Transistor.
32. Why is AND gate equivalent of positive logic OR gate in negative logic?
33. Explain the significance of DeMorgan's theorem.
34. Explain the principle of duality.
35. Implement AB + C'D' with only three NAND gates. Draw logic diagram also. Assume inverted input is available.
36. Build the logic circuit whose output expression is Y = A . B . C + A . B . C.
37. Build the logic circuit whose output expression is Y = (A + B + C) . (A + B +C).
38. Fill in the blanks of the statements below concerning the following logic families:
    Standard TTL (74XXLL), Low Power TTL (74LXX), Low Power Schottky TTL (74LSXX), Schottky TTL (74SXX), Emitter Coupled Logic (ECL), CMOS logic
    a. Among the TTL families, ---------- family requires considerably less power than the standard TTL and also has comparable propagation delay.
    b. Only the ---------- family can operate over a wide range of power supply voltages.
39. Define noise margin, fan in and fan out. State the noise margin for TTL, DTL, CMOS, ECL. When does the noise margin allow digital circuits to function properly?
40. Explain associative, cumulative , distributive properties of Boolean Algebra with example. Also, state the absorption law of Boolean Algebra.
41. What are the methods adopted to reduce the Boolean function? Explain each of them.
42. Define duality property. Find the complement of the functions F1 = x'yz' + x'y'z and F2= x(y'z' + yz).
43. State the limitations of karnaugh map.
44. What are called don't care conditions? Define prime implicants, essential prime implicants, non-essential implicants.
45. What are basic logic gates? Explain them with the truth table.
46. Which gates are called as the universal gates? What is its advantage?
47. Classify the logic family by operation.
48. Mention the classification of Saturated bipolar logic families.
49. Mention different IC packages available.
50. Explain in detail the following characteristics of digital IC's.

(a) Fan out; (b) Fan in; (c) Power dissipation; (d) Propagation delay; (e) Noise Margin; (f) Operation temperature; (g) Power supply requirements

51. List and explain the types of TTL logics. Why totem pole outputs cannot be connected together?
52. Explain TTL, DTL, ECL and CMOS. Give advantage and disadvantage of each.
53. Implement the Boolean Expression for EX-OR gate using NAND Gates.

Basic Level Questions:

1. Name six types of gates. Draw their logic diagrams and give truth tables.
2. Give the three representations of a NOT gate and define in words what NOT means.
3. Give the three representations of an AND gate and define in words what AND means.
4. Give the three representations of an OR gate and define in words what OR means.
5. Give the three representations of an XOR gate and define in words what XOR means.
6. Give the three representations of a NAND gate and define in words what NAND means.
7. Give the three representations of a NOR gate and define in words what NOR means.
8. Draw and label the symbol for a three input AND gate, then show its behavior with a truth table.
9. Draw and label the symbol for a three-input OR gate, then show its behavior with a truth table.
10. Draw a circuit diagram corresponding to the following Boolean expression: (A+B)(B+C)
11. Draw a circuit diagram corresponding to the following Boolean expression: (AB+C)D
12. Draw a circuit diagram corresponding to the following Boolean expression: A'B+(B+C)'
13. Draw a circuit diagram corresponding to the following Boolean expression. (AB)'+(CD)'
14. Show the behavior of the circuit as shown in Fig. 1 in truth table format:
15. Show the behavior of the circuit as shown in Fig. 2 in truth table format:
16. Show the behavior of the circuit as shown in Fig. 3 in truth table format:
17. Show the behavior of the circuit as shown in Fig. 4 in truth table format:
18. Derive truth table for the following Boolean function. F(x,y,z) = (x+y')'(y'+z)
19. A logic family has threshold voltage of 2 volts, minimum guaranteed output high voltage V_{OH}=4 volts, minimum accepted input high voltage V_{IH}=3 volts, maximum guaranteed output low voltage V_{OL}=1 volts, and maximum accepted input low voltage V_{IL}=1.5 volts. Find out the noise margin.
20. For a TTL gate, match the following:
    a) IOHmax=-0.4 mA; (b) IOLmax=8 mA; (c) IIHmax=20 μA; (d) IILmax=-0.1 mA
21. State De Morgan's theorem. Solve the following. Y = [((AB)'C)" D]' [((AB)'C)" D]'
22. Show that (X + Y' + XY)(X + Y')(X'Y) = 0
23. Prove that ABC + ABC' + AB'C + A'BC = AB + AC + BC
24. Convert the given expression in canonical SOP form Y = AC +AB+BC.
25. Find the minterms of the logical expression Y = A'B'C' + A'B'C + A'BC + ACC'
26. Write the max term corresponding to the logical expression.

    Y = (A + B + C')(A + B' + C')(A' + B' + C)

Moderate level Questions:

1. Find out the product of sums of given function of Boolean variables X,Y and Z is expressed in terms of the min-terms as F(X,Y,Z)=$\sum m(1,2,5,6,7)$.
2. Given the two binary numbers X=1010100 and Y=1000011, perform the subtraction
   (a) X-Y and ; (b) Y-X using 1's complements.
3. What logic functions are performed by the circuit as shown in Fig. 5 ?
4. Output of the circuit as shown in Fig. 6 will be.
5. For the circuit shown in Fig. 7 for AB=00, AB=01, C<S values respectively are
6. The circuit shown in the Fig. 8 is equivalent to?
7. The black box in the Fig. 9 consists of a minimum complexity circuit that uses only AND,OR and NOT gates. The function f (x,y,z) = 1 whenever x , y are different and 0 otherwise. In addition the 3 inputs x,y,z are never all the same value. Write the equation lead to the correct design for the minimum complexity circuit?
8. What is the minimum number of 2 input NAND gates required to implement the function. F = (x'+y') (z+w) Elaborate your answer.

9. Identify the logic function performed by the circuit shown in the Fig. 10.
10. Figure 11 shows the internal schematic of a TTL AND-OR-Invert (AOI) gate. For the inputs shown in this figure, the output Y is
11. Identify the type of logic gate shown in Fig. 12, and explain why it has the name it:
12. Find the IC number and type of IC's shown in Fig. 22 and 23?what is the significance of A,B and Y?
13. Identify the type of logic gate shown in Fig. 13, and explain why it has the name it:
14. Identify the type of logic gate shown in Fig. 14, and explain why it has the name it:
15. Crude logic gates circuits may be constructed out of nothing but diodes and resistors. Take for example the logic gate circuit given in Fig. 15:
16. Crude logic gates circuits may be constructed out of nothing but diodes and resistors. Take for example this logic gate circuit given in Fig. 16:
17. Simplify the POS Boolean expression below, providing a result in SOP form.

$$Out= (A+B+C+\overline{D})(A+B+\overline{C}+D)(A+\overline{B}+C+\overline{D})(A+\overline{B}+\overline{C}+D)$$
$$(\overline{A}+\overline{B}+\overline{C}+D)(\overline{A}+B+C+\overline{D})(\overline{A}+B+\overline{C}+D)$$

18. The four variable function f is given in terms of min-terms as f(A,B,C,D)=$\sum m(2,3,8,10,11,12,14,15)$. Using the K-map minimize the function in the sum of products form. Also, give the realization using only two input NAND gates.
19. Given the Boolean function, is there variables R,S and T as F=R'ST'+RS'T+RST.
    a. Express F in the minimum sum of products form.
    b. Express F in the minimum products of sum form.
    c. Assuming that both true and complement forms of the input variables are available, draw the circuit to implement F using the minimum number of 2 input NAND gate only.
20. The K-map for the Boolean function is shown in the figure. State the number of essential prime implicants for this function shown in K-map 1.
21. Determine the dual form for the identity, AB+A'C+BC=AB+A'C.
22. Find out the Boolean expression for the truth table.
23. Draw the circuit using only 2 input NAND gate for the Boolean Function Y=AB+CD. Also determine the minimum number of gates required.
24. Minimize the following Boolean Function.

    Y=A'B'C'D+A'BCD'+AB'C'D+ABC'D'

25. Determine the prime implicants for f(X, Y, Z)= $\sum(2,3,4,5)$.
26. Determine the essential prime implicants and prime implicants for the function.

    f(w,x,y,z)=wy +xy + $\overline{w}$xyz + $\overline{w}$ $\bar{x}$y + xz + $\bar{x}$ $\bar{y}$ $\bar{z}$.
27. Determine the minimum number of NAND gate required to implement the function

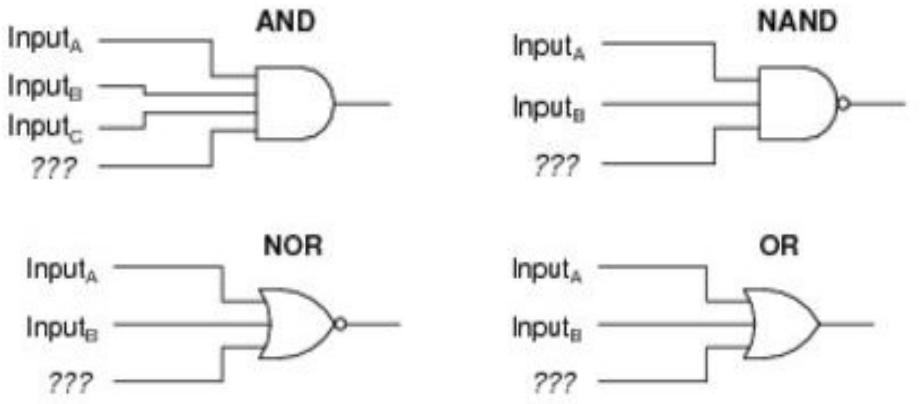
    F=($\bar{X}$+$\bar{Y}$)(Z+W)
28. For the logic circuit shown in Fig. 17, determine the output Y.
29. Find output F for the circuit shown in Fig. 18.
30. The output of the logic gate shown in Fig. 19
31. For the logic circuit shown in Fig. 20, the simplified Boolean expression for the output Y will be
32. For the logic circuit shown in Fig. 21, determine the required input combination (A,B,C) to make output X=1.

High Level Questions:

1. One way to think of the basic logic gate types (all but the XOR and XNOR gates) is to consider what single input state guarantees a certain output state. For example, we could describe the function of an OR gate as such: *Any low input guarantees a low output*
   Identify what type of gate is represented by each of the following phrases:
   - Any low input guarantees a high output.
   - Any high input guarantees a low output.

- Any high input guarantees a high output.
- Any difference in the inputs guarantees a high output.
- Any difference in the inputs guarantees a low output.

2. A different way to view the functions of two-input logic gates is to think of them in terms of *signal controllers*, where the status of one input affects how the other input's signal passes through to the output. The generic schematic diagram for this format is as shown in Fig. 24:
3. Identify the types of logic gates which do the following (there is more than one type of gate for each of the following rules!):
   (a) B = A when Control is high; (b) B = A when Control is low; (c) B = [~A] when Control is high
   (d) B = [~A] when Control is low
   Also, explain how an understanding of this can be helpful in troubleshooting faulted logic gates
4. Suppose you needed a two-input AND gate, but happened to have an unused 3-input AND gate in one of the integrated circuits ("chips") already in the system you were building. Of course, you could just add another IC containing 2-input AND gates, but it seems an extra burden in cost and complexity to waste the 3-input gate already there. Explain what you would need to do with the third input terminal on the gate shown in Fig. 25 in order to use it as a 2-input AND gate:
5. Now, explain what to do with each of the following gates' third inputs, in order to use each of them as 2-input gates:



Note: Figures are given on Page-7 and Page-8 (Fig. 1 to Fig. 25)

Figures:

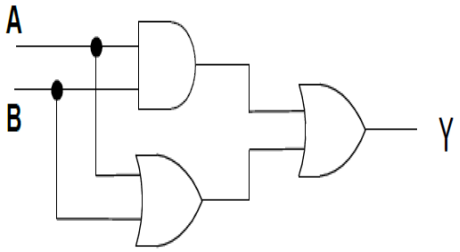


Fig.1

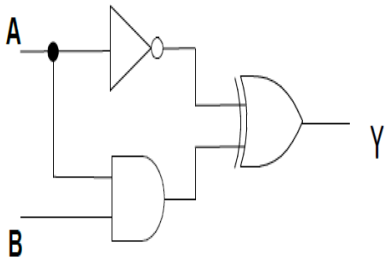


Fig. 2

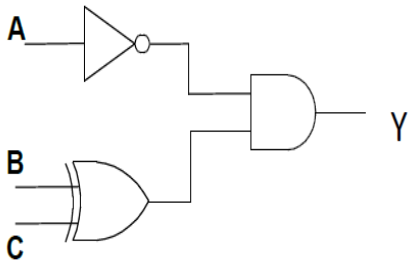


Fig. 3

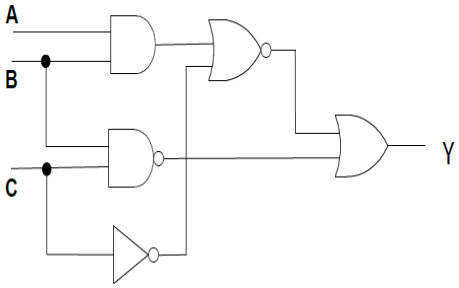


Fig.4

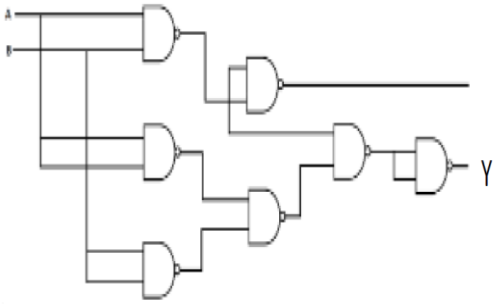


Fig. 5

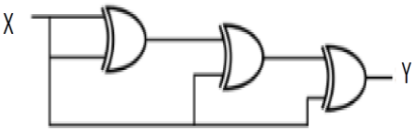


Fig. 6

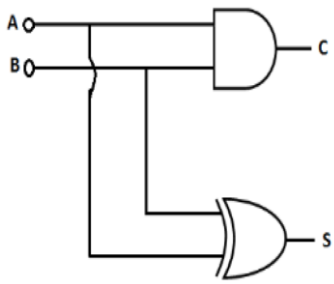


Fig.7

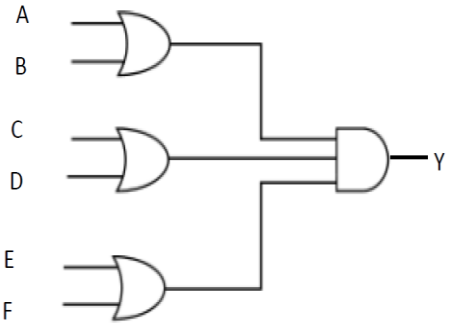


Fig. 8

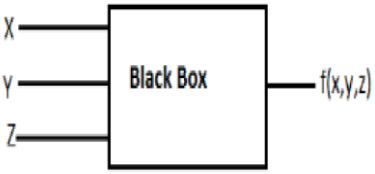


Fig. 9

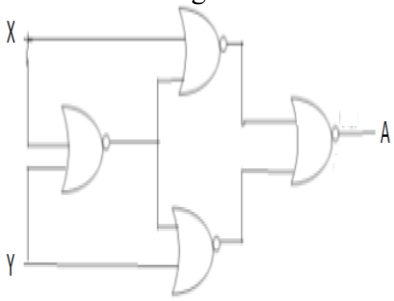


Fig.10

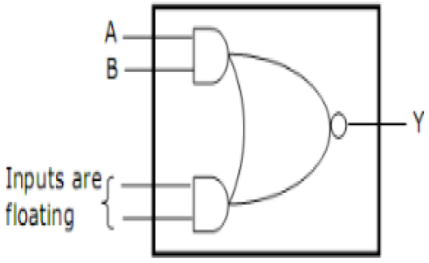


Fig. 11

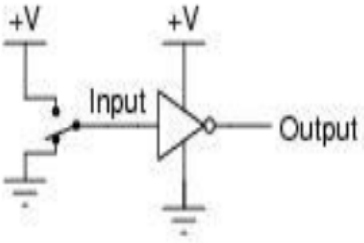


Fig. 12

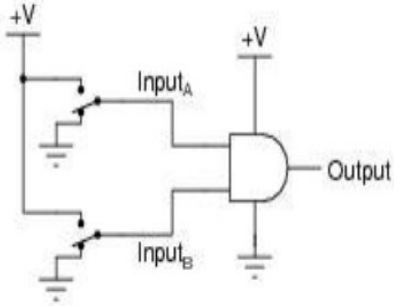


Fig.13

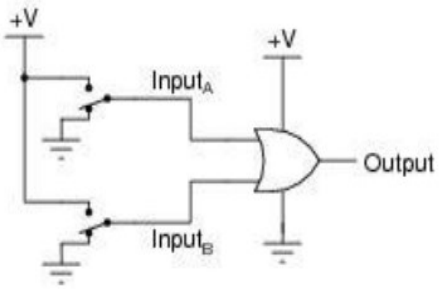


Fig. 14

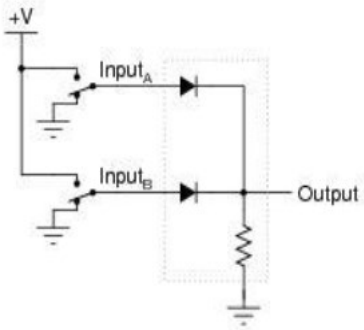


Fig. 15

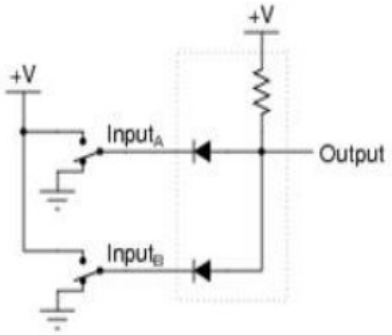


Fig.16

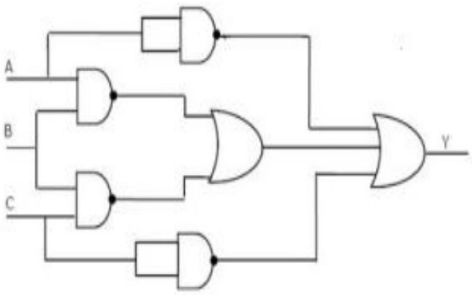


Fig. 17

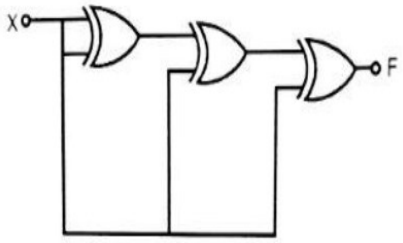


Fig. 18

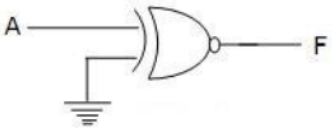


Fig.19

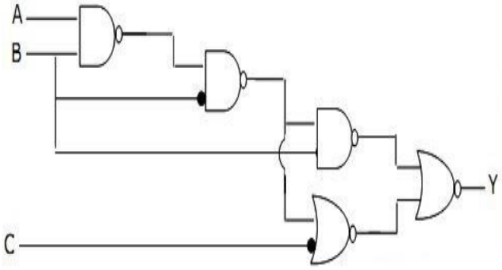


Fig. 20

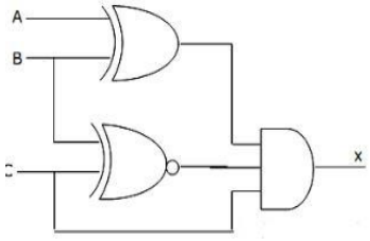


Fig. 21

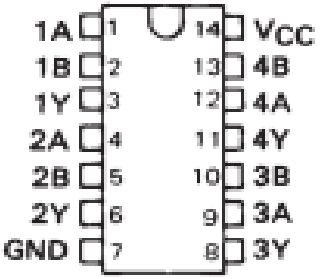


Fig.22

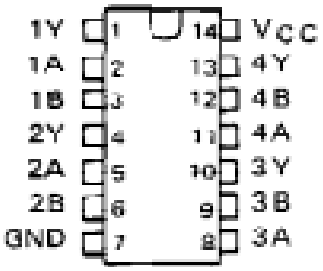


Fig. 23

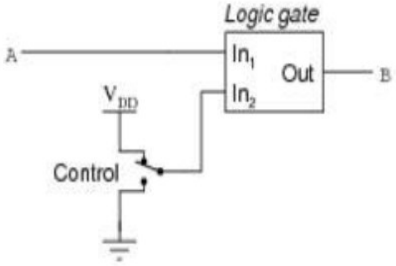


Fig.24

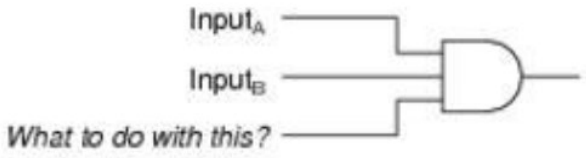


Fig. 25

K-map: 1

CD \ AB	00	01	11	10
00	1	1	0	1
01	0	0	0	1
11	1	0	0	0
10	1	0	0	1

Truth table-1

A	B	C	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0