

Combinational Circuits

Basic level Questions.

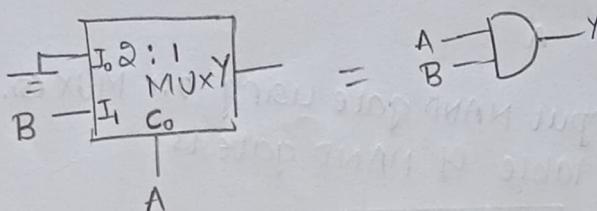
1. Design 2 input AND gate using only 2:1 MUX (s).

Truth table for AND gate:

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

output is '0'
when A=0output is 'B'
when A=1.

So, here A acts as control input



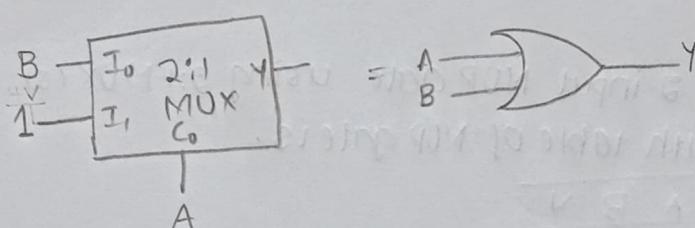
2. Design 2 input OR gate using 2:1 MUX (s).

Truth table of OR gate is:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

output is 'B'
when A=0output is '1'
when A=1

Input 'A' acts as control input.



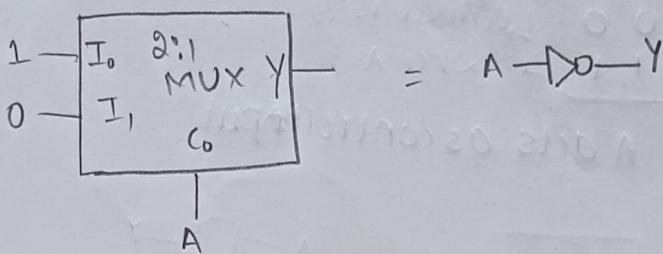
3. Design 2 input NOT gate using only 2:1 MUX (s).

Truth table of NOT gate is

A	Y
0	1
1	0

→ output is 1, when A=0
→ output is 0, when A=1

Input 'A' acts as control input.



4. Design 2 input NAND gate using 2:1 MUX (s).

Truth table of NAND gate is

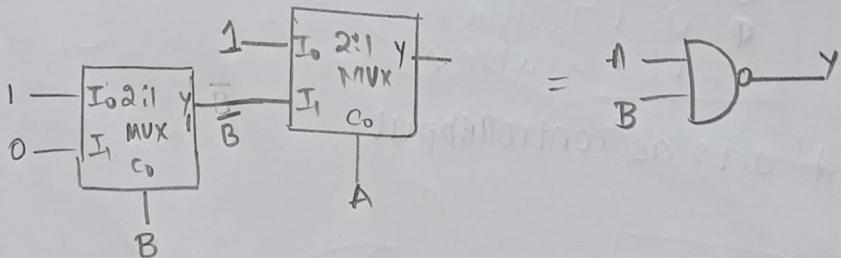
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

→ output = 1, when A=0

→ output = \bar{B} , when A=1

To get \bar{B} , we use NOT gate with the help of 2:1 MUX

Input 'A' acts as control input.



5. Design 2 input NOR gate using 2:1 MUX (s).

Truth table of NOR gate is.

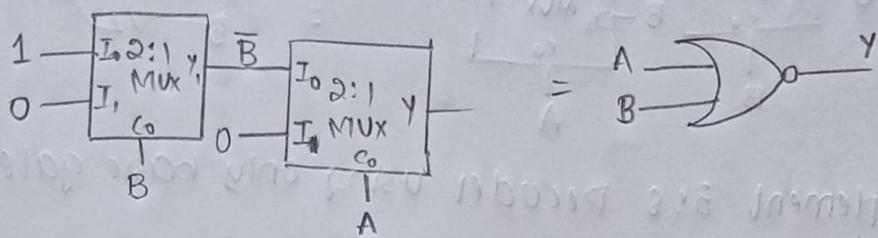
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

→ output is \bar{B} , when A=0

→ output = 0, when A=1

Input 'A' acts as control input.

We implement \bar{B} using one more 2:1 MUX, taking 'B' as control input.



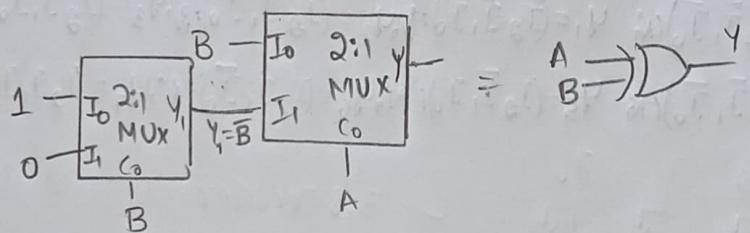
6. Design a 2 input XOR gate using only 2:1 MUX(s).

Truth table of XOR gate is:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

→ output = B, when A=0
→ output = \bar{B} , when A=1

To implement \bar{B} we use 1 2:1 MUX and for other MUX we take A as control input.



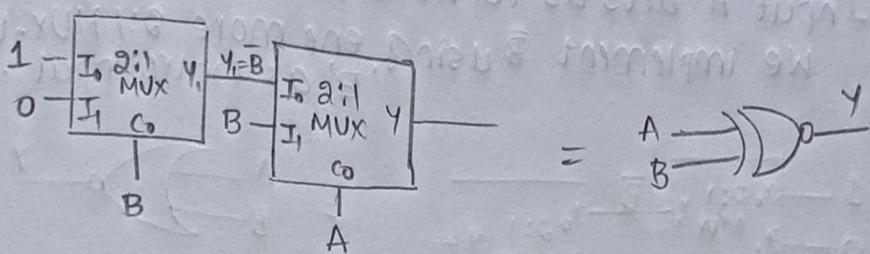
7. Design a 2 input XNOR gate using only 2:1 MUX (s).

Truth table of XNOR gate is

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

→ output = \bar{B} , when A=0
→ output = B, when A=1.

we take B as controller (control input) to implement \bar{B} . And input be 'A' as acts as control input for 2nd MUX.

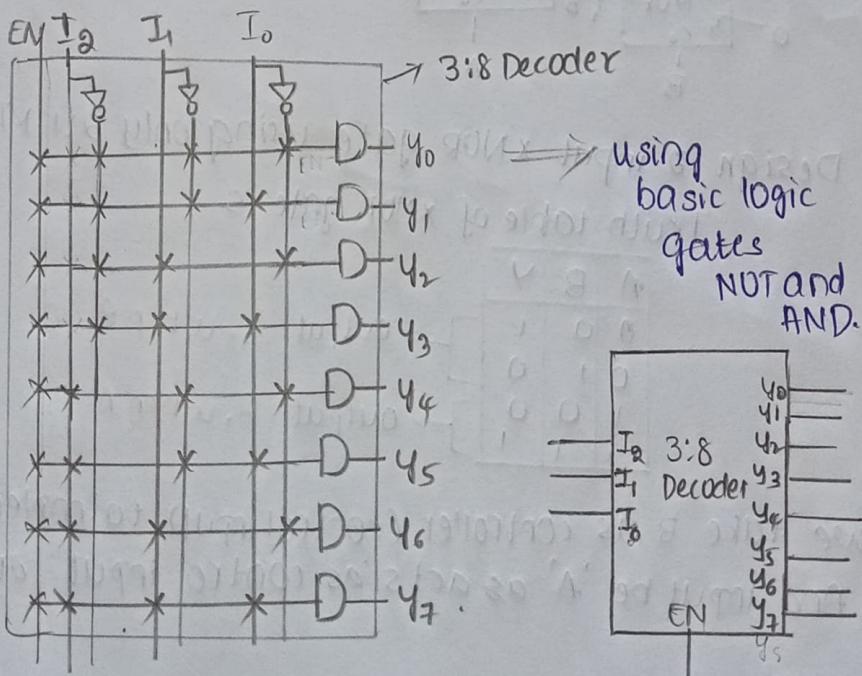


8. Implement 3:8 Decoder using only basic gates.

EN	I ₂	I ₁	I ₀	Y ₇	Y ₆	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁	Y ₀
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0
0	X	X	X	X	X	X	X	X	X	X	X

$$Y_0 = (\bar{I}_2 \bar{I}_1 \bar{I}_0)_{EN}, Y_1 = (\bar{I}_2 \bar{I}_1 I_0)_{EN}, Y_2 = (\bar{I}_2 I_1 \bar{I}_0)_{EN}, Y_3 = (I_2 \bar{I}_1 \bar{I}_0)_{EN}$$

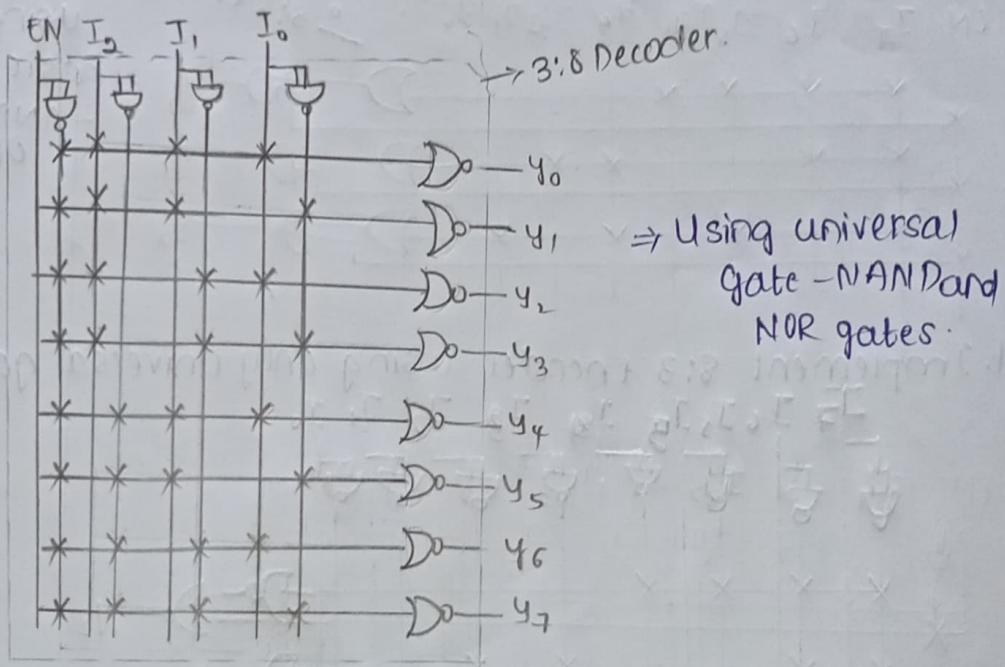
$$Y_4 = (I_2 \bar{I}_1 I_0)_{EN}, Y_5 = (I_2 \bar{I}_1 I_0)_{EN}, Y_6 = (I_2 I_1 \bar{I}_0)_{EN}, Y_7 = (I_2 I_1 I_0)_{EN}$$



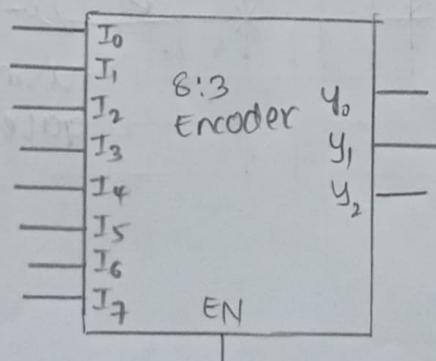
9. Implement 3:8 Decoder using only universal gates.

I_2	I_1	I_0	y_7	y_6	y_5	y_4	y_3	y_2	y_1	y_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

$$\begin{aligned}
 y_0 &= (\bar{I}_2, \bar{I}_1, \bar{I}_0) \text{EN} & y_1 &= (\bar{I}_2, \bar{I}_1, I_0) \text{EN} & y_2 &= (I_2, \bar{I}_1, \bar{I}_0) \text{EN} & y_3 &= (I_2, I_1, \bar{I}_0) \text{EN} \\
 y_4 &= (I_2, \bar{I}_1, I_0) \text{EN} & y_5 &= (I_2, \bar{I}_1, I_0) \text{EN} & y_6 &= (I_2, I_1, \bar{I}_0) \text{EN} & y_7 &= (I_2, I_1, I_0) \text{EN}
 \end{aligned}$$



10. Implement 8:3 Encoder using only basic gates.

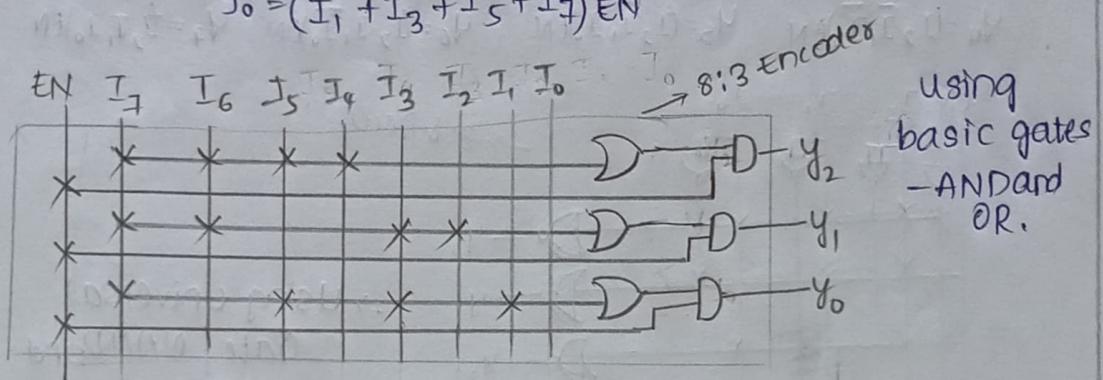


EN	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	y_2	y_1	y_0
1	0	0	0	0	0	0	0	1	0	0	0
1	0	0	0	0	0	0	1	0	0	0	1
1	0	0	0	0	0	1	0	0	0	1	0
1	0	0	0	0	1	0	0	0	0	1	1
1	0	0	0	1	0	0	0	0	1	0	0
1	0	0	1	0	0	0	0	0	1	0	1
1	0	1	0	0	0	0	0	0	1	1	0
1	1	0	0	0	0	0	0	0	1	1	1
0	x	x	x	x	x	x	x	x	x	x	x

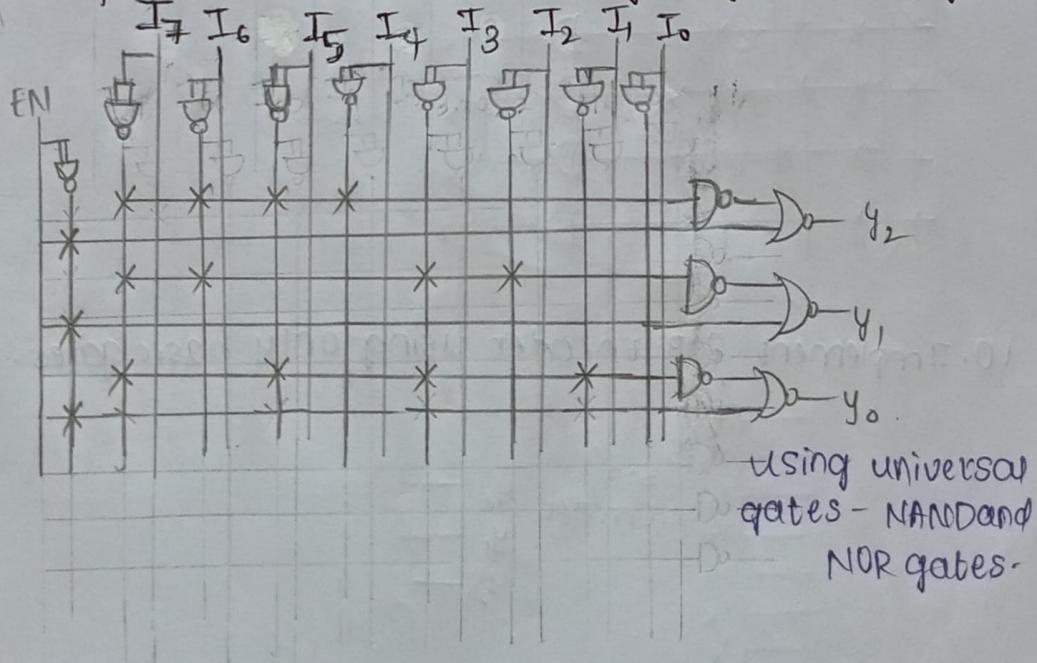
$$y_2 = (I_4 + I_5 + I_6 + I_7) EN$$

$$y_1 = (I_2 + I_3 + I_6 + I_7) EN$$

$$y_0 = (I_1 + I_3 + I_5 + I_7) EN$$

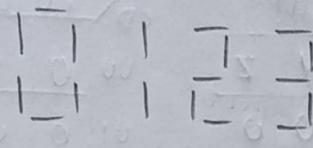


II. Implement 8:3 Encoder using only universal gates.



12. Design a circuit for displaying 0 to 3 on 7 segment display.

$$\begin{array}{c} a \\ f \mid b \\ e \mid c \\ d \end{array}$$



A	B	a	b	c	d	e	f	g
0	0	1	1	1	1	1	0	
0	1	0	1	1	0	0	0	
1	0	1	1	0	1	1	0	1
1	1	1	1	1	1	0	0	1

$$\begin{array}{c} a \\ A \\ B \\ 0 \\ 0 \\ 1 \\ 0 \end{array}$$

$$\begin{array}{c} e \\ A \\ B \\ 0 \\ 0 \\ 1 \\ 0 \end{array}$$

$$e = \bar{B}$$

$$\begin{array}{c} b \\ A \\ B \\ 0 \\ 0 \\ 1 \\ 0 \end{array}$$

$$\begin{array}{c} f \\ A \\ B \\ 0 \\ 0 \\ 1 \\ 0 \end{array}$$

$$f = \bar{A}\bar{B}$$

$$\begin{array}{c} c \\ A \\ B \\ 0 \\ 0 \\ 1 \\ 0 \end{array}$$

$$\begin{array}{c} g \\ A \\ B \\ 0 \\ 0 \\ 1 \\ 0 \end{array}$$

$$g = A$$

$$\begin{array}{c} d \\ A \\ B \\ 0 \\ 0 \\ 1 \\ 0 \end{array}$$

$$d = A + \bar{B}$$

$$a = A + \bar{B}$$

$$e = \bar{B}$$

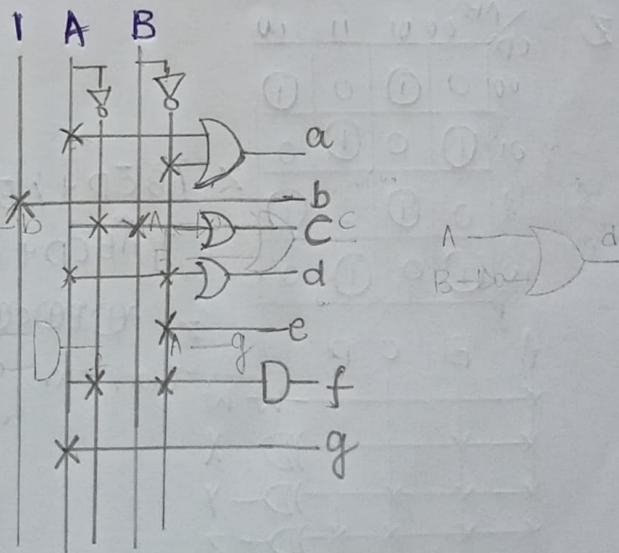
$$b = 1$$

$$f = \bar{A}\bar{B}$$

$$c = \bar{A} + B$$

$$g = A$$

$$d = A + \bar{B}$$



13. Design a circuit for converting Gray to Binary code.

Gray Code (Input)				Binary code (Output)			
A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
1	0	0	0	1	1	1	1
1	0	0	1	1	1	1	0
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	0	0	1	1	1
1	1	1	1	0	1	0	0

CD \ AB	00	01	11	10	W
00	0	0	1	1	
01	0	0	1	1	
11	0	0	1	1	
10	0	0	1	1	

$$W = A$$

CD \ AB	00	01	11	10	X
00	0	1	0	1	
01	0	1	0	1	
11	0	1	0	1	
10	0	1	0	1	

$$X = \bar{A}B + A\bar{B} = A \oplus B$$

CD \ AB	00	01	11	10	Y
00	0	1	0	1	
01	0	1	0	1	
11	1	0	1	0	
10	1	0	1	0	

$$Y = \bar{A}\bar{B}C + \bar{A}B\bar{C} + ABC + A\bar{B}\bar{C}$$

$$Y = A \oplus B \oplus C$$

$$Z = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}B\bar{C}D + ABC\bar{D} + A\bar{B}CD + A\bar{B}CD + A\bar{B}CD + A\bar{B}CD.$$

$$Z = A \oplus B \oplus C \oplus D$$

CD \ AB	00	01	11	10
00	0	1	0	1
01	1	0	1	0
11	0	1	0	1
10	1	0	1	0

→ Black box.

A	B	C	D	W	X	Y	Z
*	*	*	*	1	0	0	0
*	*	*	*	1	0	0	1
*	*	*	*	1	0	1	1
*	*	*	*	1	1	0	1

14. Design a circuit for converting Binary to Gray code.

Binary code (Input)				Gray code (Output)			
A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	1	0	0

AB	CD	Z
00	00	000
00	01	000
01	11	111
11	00	000
10	10	111

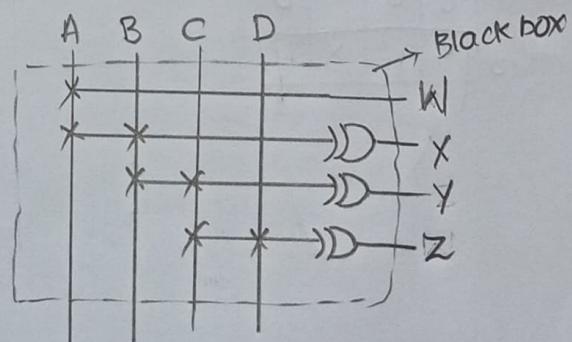
$$Z = \overline{C}D + C\overline{D} = C \oplus D$$

AB	CD	W
00	00	0011
00	01	0011
01	11	0011
11	00	0011
10	10	0011

AB	CD	X
00	00	0101
00	01	0101
01	11	0101
11	00	0101
10	10	0101

AB	CD	Y
00	00	0110
00	01	1110
01	11	1110
11	00	1110
10	10	1110

$$Y = B\overline{C} + \overline{B}C = B \oplus C$$



15. Design a circuit for converting Excess-3 to Binary code.

Excess-3 (Input)				Binary code (Output)			
W	X	Y	Z	A	B	C	D
0	0	0	0	X	X	X	X
0	0	0	1	X	X	X	X
0	0	1	0	X	X	X	X
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

W	X	A			
Y	Z	00	01	11	10
0	0	X	0	1	0
0	1	X	0	X	0
1	0	0	0	X	1
1	1	X	0	X	0
0	0	X	0	X	0

$$A = WX + WYZ$$

W	X	B			
Y	Z	00	01	11	10
0	0	X	0	0	1
0	1	X	0	X	1
1	0	0	1	X	0
1	1	X	0	X	1
0	0	X	0	X	1

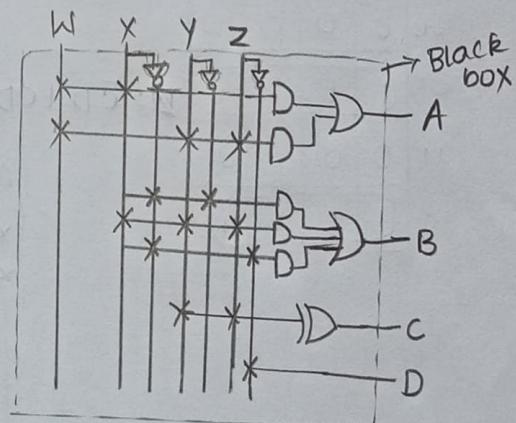
$$B = \bar{X}\bar{Y} + XY + \bar{X}\bar{Z}$$

W	X	C			
Y	Z	00	01	11	10
0	0	X	0	0	0
0	1	X	1	X	1
1	0	0	0	X	0
1	1	X	1	X	1
0	0	X	1	X	1

$$C = \bar{Y}Z + \bar{Z}Y + Y \oplus Z$$

W	X	D			
Y	Z	00	01	11	10
0	0	X	1	1	1
0	1	X	0	X	0
1	0	0	0	X	0
1	1	X	1	X	1
0	0	X	1	X	1

$$D = \bar{Z}$$



16. Design a circuit for converting Binary code to Excess-3.

Binary code (Input)				Excess-3 Output				
A	B	C	D	W	X	Y	Z	V
0	0	0	0	0	0	1	1	1
0	0	0	1	0	1	0	0	1
0	0	1	0	0	1	0	1	1
0	0	1	1	0	1	0	0	1
0	1	0	0	0	1	1	0	1
0	1	0	1	1	0	0	0	1
0	1	1	0	1	0	0	1	1
0	1	1	1	1	0	1	0	1
1	0	0	0	1	0	1	1	1
1	0	0	1	1	1	0	0	1
1	0	1	0	1	1	0	1	1
1	0	1	1	1	1	1	0	1
1	1	0	0	1	1	1	1	1
1	1	0	1	X	X	X	X	0
1	1	1	0	X	X	X	X	0
1	1	1	1	X	X	X	X	0

AB	CD	W
00	00 01 11 10	0 0 1 1
01	00 01 11 10	0 1 X 1
11	00 01 11 10	0 1 X 1
10	00 01 11 10	1 X 1

$$W = A + BD + BC$$

$$W = A + B(C+D)$$

AB	CD	X
00	00 01 11 10	0 1 1 0
01	00 01 11 10	1 0 X 1
11	00 01 11 10	1 0 X 1
10	00 01 11 10	1 0 X 1

$$X = B\bar{C}\bar{D} + \bar{B}D$$

$$+ \bar{B}C$$

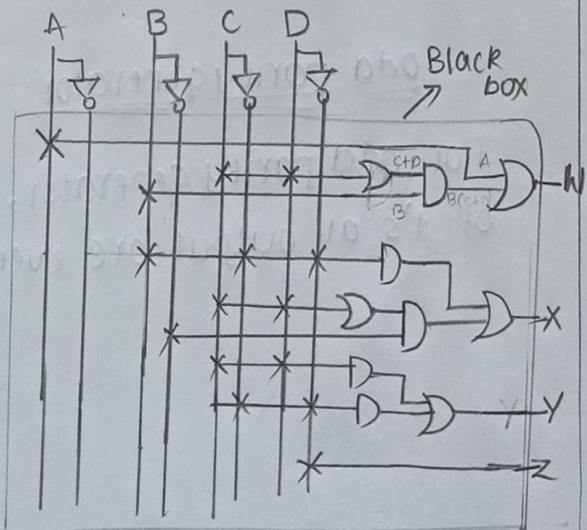
$$X = B\bar{C}\bar{D} + \bar{B}(C+D)$$

AB	CD	Y
00	00 01 11 10	1 1 1 1
01	00 01 11 10	0 0 X 0
11	00 01 11 10	1 1 X 1
10	00 01 11 10	0 0 X 0

$$Y = \bar{C}\bar{D} + CD$$

CD	AB	Z
00	00 01 11 10	
01	00 01 11 10	
11	00 01 11 10	
10	00 01 11 10	

$$Z = \bar{D}$$



17. Design a parity generator circuit using any gate(s).

Even parity generator:-

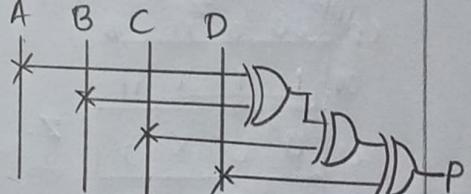
For even parity generator, output=1, when number of 1's at input are odd.

A	B	C	D	O/P - P
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

AB		CD	P
00	01	11	10
0	0	0	0
0	1	0	1
1	0	0	1
1	1	0	0
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	1

$$\begin{aligned}
 P = & \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \\
 & \bar{A}B\bar{C}\bar{D} + \bar{A}BC\bar{D} + \\
 & A\bar{B}\bar{C}D + ABC\bar{D} + \\
 & A\bar{B}\bar{C}\bar{D} + A\bar{B}CD
 \end{aligned}$$

$$P = A \oplus B \oplus C \oplus D.$$



Odd parity generator:-

For odd parity generator, output=1, when number of 1's at output are even.

A	B	C	D	P
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

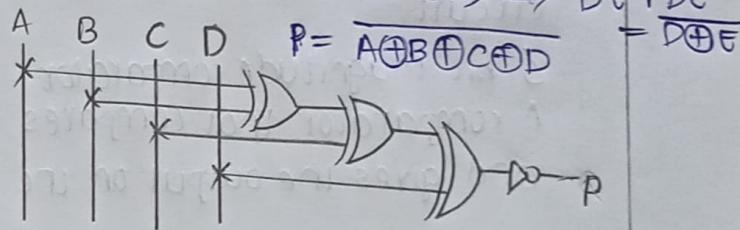
AB	CD	P
00	00	1
00	01	0
00	11	1
00	10	0
01	00	0
01	01	1
01	10	0
01	11	1
10	00	0
10	01	1
10	10	0
10	11	1
11	00	1
11	01	0
11	10	1
11	11	0

$$P = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}\bar{C}D + \bar{ABC}\bar{D}$$

$$+ A\bar{B}\bar{C}\bar{D} + ABCD + A\bar{B}\bar{C}\bar{D} + A\bar{B}C\bar{D}$$

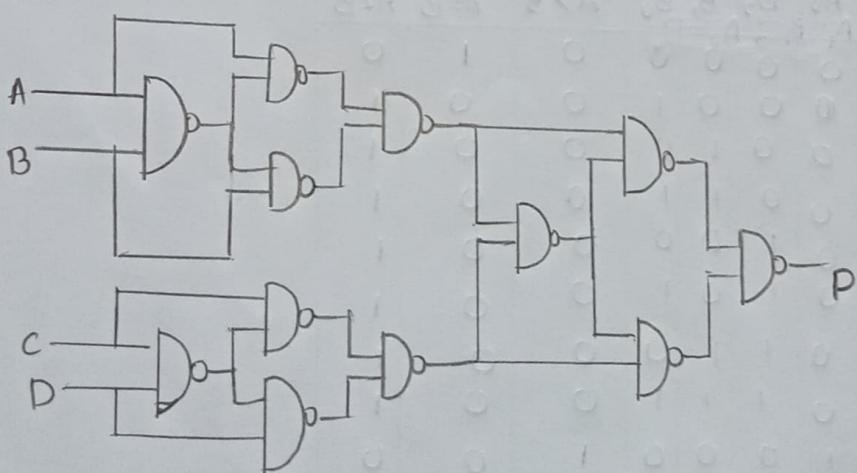
$$P = (\bar{A}\bar{B} + AB)(\bar{C}\bar{D} + CD) + (\bar{A}\bar{B} + A\bar{B})(\bar{C}D + C\bar{D})$$

$$P = (A \oplus B)(C \oplus D) + (A \oplus B)(C \oplus D) \Rightarrow \overline{DE} + DE = \overline{D \oplus E}$$

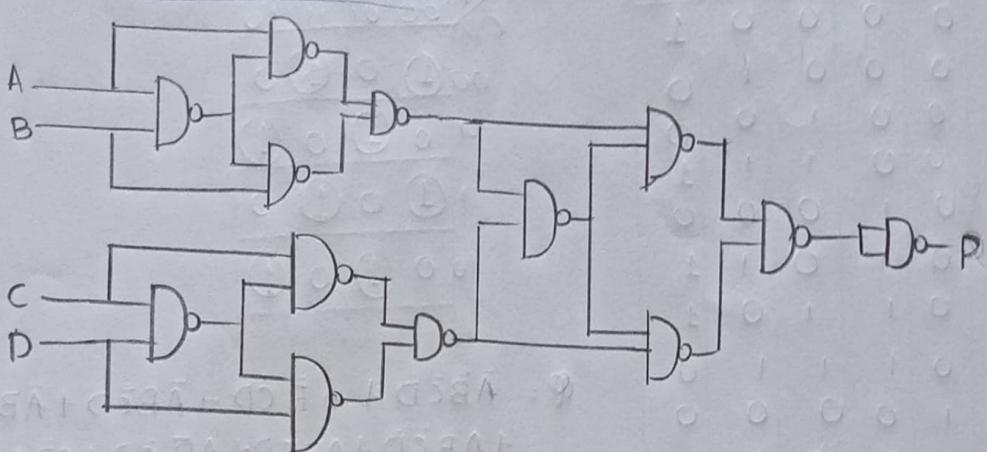


18. Design a parity generator circuit using only universal gates.

Even parity generator



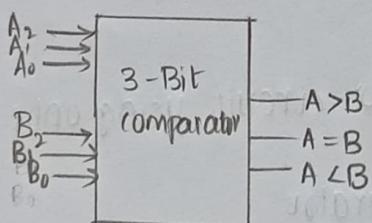
odd parity generator



19. Design a 3-bit Magnitude comparator combinational circuit.

3-bit Magnitude comparator:

A comparator that compares 2 binary numbers of 3bit and gives the output on the basis of magnitude.



$A_2 = B_2$	A_1	A_0	B_2	B_1	B_0	$A > B$	$A = B$	$A < B$
0	0	0	0	0	0	0	1	0
1	0	0	0	0	1	0	0	1
2	0	0	0	1	0	0	0	1
3	0	0	0	1	1	0	0	1
4	0	0	0	1	0	0	0	1
5	0	0	0	1	0	0	0	1
6	0	0	0	1	1	0	0	1
7	0	0	0	1	1	0	0	1
8	0	0	1	0	0	1	0	0
9	0	0	1	0	0	0	1	0
10	0	0	1	0	1	0	0	1
11	0	0	1	0	1	0	0	1

	A ₂	A ₁	A ₀	B ₂	B ₁	B ₀	G	E	L
12	0	0	1	1	0	0	0	0	1
13	0	0	1	1	0	1	0	0	1
14	0	0	1	1	1	0	0	0	1
15	0	0	1	1	1	0	0	0	1
16	0	1	0	0	0	0	1	0	1
17	0	1	0	0	0	1	1	0	0
18	0	1	0	0	1	0	0	1	0
19	0	1	0	0	1	1	0	0	1
20	0	1	0	1	0	0	0	0	1
21	0	1	0	1	0	1	0	0	1
22	0	1	0	1	1	0	0	0	1
23	0	1	0	1	1	1	0	0	1
24	0	1	1	0	0	0	1	0	0
25	0	1	1	0	0	1	1	0	0
26	0	1	1	0	1	0	1	0	0
27	0	1	1	0	1	1	0	1	0
28	0	1	1	1	0	0	0	0	1
29	0	1	1	1	0	1	0	0	1
30	0	1	1	1	1	0	0	0	1
31	0	1	1	1	1	1	0	0	1
32	1	0	0	0	0	0	1	0	0
33	1	0	0	0	0	1	1	0	0
34	1	0	0	0	1	0	1	0	0
35	1	0	0	0	1	1	1	0	0
36	1	0	0	1	0	0	0	1	0
37	1	0	0	1	0	1	0	0	1
38	1	0	0	1	1	0	0	0	1
39	1	0	0	1	1	1	0	0	1
40	1	0	1	0	0	0	1	0	0
41	1	0	1	0	0	1	1	0	0
42	1	0	1	0	Φ	0	1	0	0
43	1	0	1	0	1	1	1	0	0
44	1	0	1	1	0	0	1	0	0
45	1	0	1	1	0	1	0	1	0
46	1	0	1	1	1	0	0	0	1
47	1	0	1	1	1	1	0	0	1

	A_2	A_1	A_0	B_2	B_1	B_0	G	E	L
48	1	1	0	0	0	0	1	0	0
49	1	1	0	0	0	1	1	0	0
50	1	1	0	0	1	0	1	0	0
51	1	1	0	0	1	1	1	0	0
52	1	1	0	1	0	0	1	0	0
53	1	1	0	1	0	1	1	0	0
54	1	1	0	1	0	1	1	0	0
55	1	1	0	1	1	1	0	0	1
56	1	1	1	0	0	0	1	0	0
57	1	1	1	0	0	1	1	0	0
58	1	1	1	0	1	0	1	0	0
59	1	1	1	0	1	1	1	0	0
60	1	1	1	1	0	0	1	0	0
61	1	1	1	1	0	1	1	0	0
62	1	1	1	1	1	0	1	0	0
63	1	1	1	1	1	1	0	1	0

Boolean expression -

$$\Rightarrow E = \bar{A}_1 \bar{A}_2 \bar{A}_0 \bar{B}_2 \bar{B}_1 \bar{B}_0 + \bar{A}_1 \bar{A}_2 A_0 \bar{B}_2 \bar{B}_1 B_0 + \\ + A_1 \bar{A}_2 A_0 \bar{B}_2 B_1 B_0 + A_1 \bar{A}_2 \bar{A}_0 \bar{B}_2 B_1 \bar{B}_0 + \\ + \bar{A}_1 A_2 \bar{A}_0 B_2 \bar{B}_1 \bar{B}_0 + \bar{A}_1 A_2 A_0 B_2 \bar{B}_1 B_0 + \\ + A_1 A_2 A_0 B_2 B_1 B_0 + A_1 A_2 \bar{A}_0 B_2 B_1 \bar{B}_0$$

$$\Rightarrow E = \bar{A}_1 \bar{A}_0 \bar{B}_1 \bar{B}_0 (A_2 B_2 + \bar{A}_2 \bar{B}_2)$$

$$+ \bar{A}_1 A_0 \bar{B}_1 B_0 (A_2 B_2 + \bar{A}_2 \bar{B}_2)$$

$$+ A_1 A_0 B_1 B_0 (A_2 B_2 + \bar{A}_2 \bar{B}_2)$$

$$+ A_1 \bar{A}_0 B_1 \bar{B}_0 (A_2 B_2 + \bar{A}_2 \bar{B}_2)$$

$$\Rightarrow E = (\bar{A}_2 \oplus B_2) [\bar{A}_1 \bar{B}_1, (\bar{A}_0 \bar{B}_0 + A_0 B_0)]$$

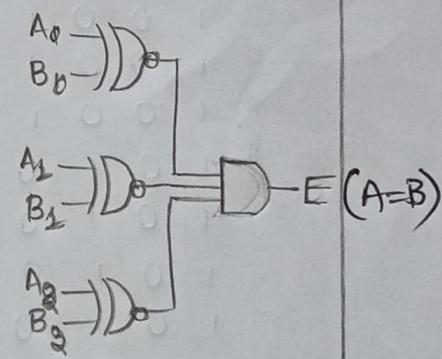
$$+ A_1 B_1 (A_0 \bar{B}_0 + A_0 B_0)]$$

$$\Rightarrow E = (\bar{A}_2 \oplus B_2) (A_0 \oplus B_0) [\bar{A}_1 \bar{B}_1, + A_1 B_1]$$

$$\Rightarrow E = (\bar{A}_2 \oplus B_2) (A_1 \oplus B_1) (A_0 \oplus B_0)$$

\bar{E}									
		\bar{A}_1							
		$A_0 B_2$	00	01	11	10			
$\bar{B}_1 B_0$	00	1	0	4	0	2	0	8	
\bar{A}_2	01	0	1	0	5	0	1	9	
	11	0	3	0	7	15	0	11	
	10	0	2	0	6	14	0	10	

\bar{E}									
		A_1							
		$A_0 B_2$	00	01	11	10			
$B_1 B_0$	00	0	16	0	20	0	28	0	24
01	0	17	0	21	0	29	0	25	
	11	0	19	0	23	0	31	0	27
	10	1	0	22	0	30	0	26	



E									
		A_1							
		$A_0 B_2$	00	01	11	10			
$B_1 B_0$	00	0	32	1	0	40	0	48	
01	0	33	0	37	1	41	0	49	
	11	0	35	0	39	0	47	0	43
	10	0	34	0	38	0	46	0	42

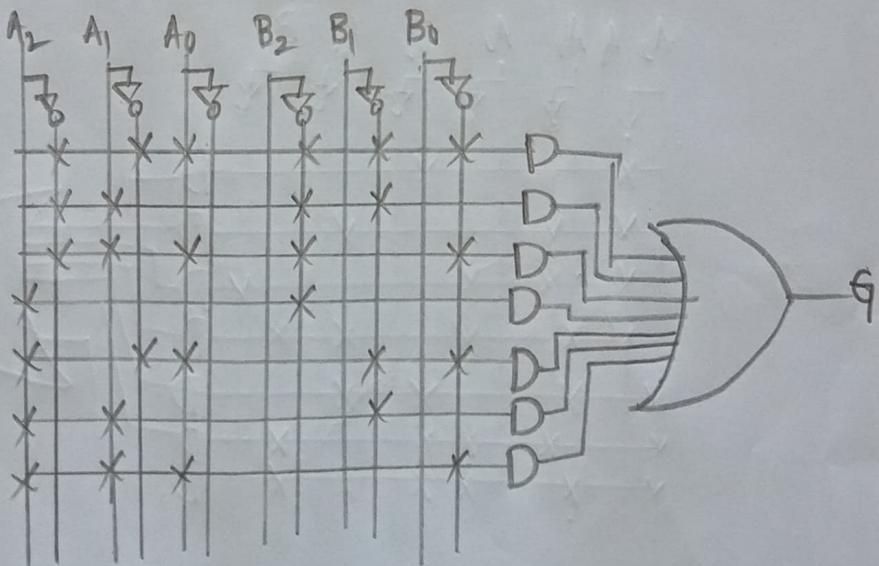
E									
		A_1							
		$A_0 B_2$	00	01	11	10			
$B_1 B_0$	00	0	48	0	52	0	60	0	56
01	0	49	0	53	0	61	0	57	
	11	0	51	0	55	0	63	0	59
	10	0	50	0	54	0	62	0	58

		\bar{A}_1						A_1					
		$B_1 B_2$	00	01	11	10			$B_1 B_2$	00	01	11	10
\bar{A}_2	$B_1 B_0$	00	0	0	0	1			00	1	0	0	1
	01	0	1	0	0	0			01	1	0	0	0
	11	0	0	1	0	0			11	0	1	0	0
	10	0	0	0	1	0			10	0	0	1	0
A_2		$B_1 B_2$	00	01	11	10			$B_1 B_2$	00	01	11	10
		00	1	32	0	36			00	1	32	1	60
		01	1	33	0	37			01	1	33	1	61
		11	1	35	0	39			11	1	35	0	63
		10	1	34	0	38			10	1	34	1	62

$$G = \bar{A}_1 \bar{A}_2 (A_0 \bar{B}_2 \bar{B}_1 \bar{B}_0) + A_1 \bar{A}_2 (\bar{B}_2 B_1 + A_0 \bar{B}_2 \bar{B}_0) \\ + A_2 \bar{A}_1 (\bar{B}_2 + A_0 \bar{B}_1 \bar{B}_0) + A_2 A_1 (\bar{B}_2 + \bar{B}_1 + A_0 \bar{B}_0)$$

$$G = \bar{A}_2 \bar{A}_1 A_0 \bar{B}_2 \bar{B}_1 \bar{B}_0 + \bar{A}_2 A_1 \bar{B}_2 \bar{B}_1 + \bar{A}_2 A_1 A_0 \bar{B}_2 \bar{B}_0 + A_2 \bar{A}_1 \bar{B}_2 \\ + A_2 \bar{A}_1 A_0 \bar{B}_1 \bar{B}_0 + \underbrace{A_2 A_1 \bar{B}_2 + A_2 A_1 \bar{B}_1 + A_2 A_1 A_0 \bar{B}_0}$$

$$G = \bar{A}_2 \bar{A}_1 A_0 \bar{B}_2 \bar{B}_1 \bar{B}_0 + \bar{A}_2 A_1 \bar{B}_2 \bar{B}_1 + \bar{A}_2 A_1 A_0 \bar{B}_2 \bar{B}_0 + A_2 \bar{B}_2 \\ + A_2 \bar{A}_1 A_0 \bar{B}_1 \bar{B}_0 + A_2 A_1 \bar{B}_1 + A_2 A_1 A_0 \bar{B}_0$$



		\bar{A}_1	L				
		$A_0 B_2$	00	01	11	10	
\bar{A}_2		$B_1 B_0$	00	0	1	1	0
01	00	1	1	1	0		
	01	1	1	1	0		
11	00	1	1	1	0		
	10	1	1	1	0		

		\bar{A}_1	L				
		$A_0 B_2$	00	01	11	10	
		$B_1 B_0$	00	0	1	1	0
01	00	1	1	1	0		
	01	1	1	1	0		
11	00	1	1	1	0		
	10	0	1	1	0		

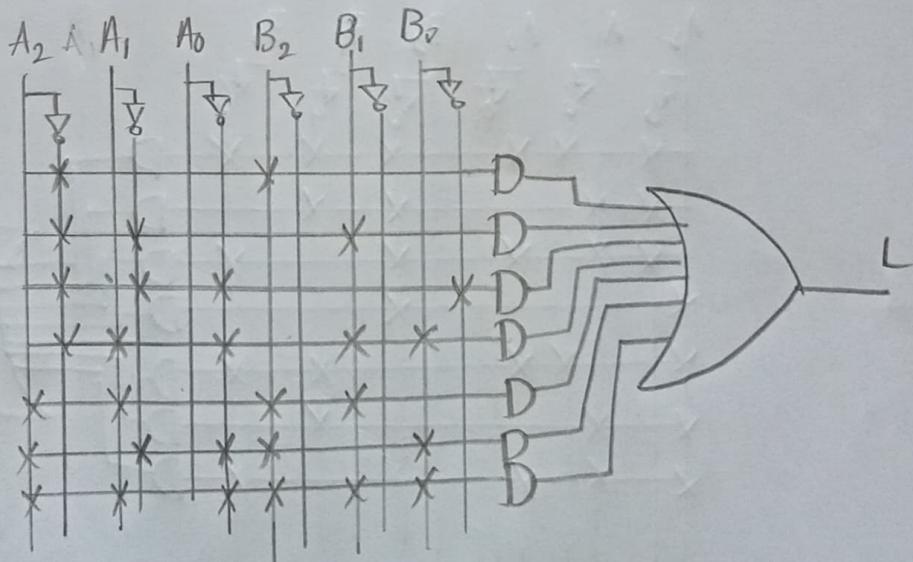
		\bar{A}_1	L				
		$A_0 B_2$	00	01	11	10	
A_2		$B_1 B_0$	00	0	0	0	0
01	00	0	1	0	0		
	01	0	1	1	0		
11	00	0	1	1	0		
	10	0	1	1	0		

		\bar{A}_1	L				
		$A_0 B_2$	00	01	11	10	
		$B_1 B_0$	00	0	0	0	0
01	00	0	0	0	0		
	01	0	0	0	0		
11	00	0	0	0	0		
	10	0	0	0	0		

$$\begin{aligned}
 L &= \bar{A}_2 \bar{A}_1 (B_2 + B_1 + \bar{A}_0 \bar{B}_0) + \bar{A}_2 A_1 (B_2 + \bar{A}_0 B_1 B_0) \\
 &\quad + A_2 \bar{A}_1 (B_2 B_1 + \bar{A}_0 B_2 B_0) + A_2 A_1 (\bar{A}_0 B_2 B_1 B_0)
 \end{aligned}$$

$$\begin{aligned}
 L &= \bar{A}_2 \bar{A}_1 B_2 + \bar{A}_2 \bar{A}_1 B_1 + \bar{A}_2 \bar{A}_1 \bar{A}_0 \bar{B}_0 + \bar{A}_2 A_1 B_2 + \bar{A}_2 A_1 \bar{A}_0 B_1 B_0 \\
 &\quad + A_2 A_1 B_2 B_1 + A_2 \bar{A}_1 \bar{A}_0 B_2 B_0 + A_2 A_1 \bar{A}_0 B_2 B_1 B_0
 \end{aligned}$$

$$\begin{aligned}
 L &= \bar{A}_2 B_2 + \bar{A}_2 \bar{A}_1 B_1 + \bar{A}_2 \bar{A}_1 \bar{A}_0 \bar{B}_0 + \bar{A}_2 A_1 \bar{A}_0 B_1 B_0 + A_2 A_1 B_2 B_1 \\
 &\quad + A_2 \bar{A}_1 \bar{A}_0 B_2 B_0 + A_2 A_1 \bar{A}_0 B_2 B_1 B_0
 \end{aligned}$$



$$20. F = \sum m(0, 6, 7, 9, 10, 15, 16, 24, 29, 30) + \sum d(1, 5, 11, 12, 25, 27)$$

		BC		DE	00	01	11	10
		00	01	DE	00	01	11	10
		1	0	d	12	0	8	
		d	d	0	13	1	9	
		0	1	d	15	1	11	
		0	1	1	16	0	10	

		BC		DE	00	01	11	10
		00	01	DE	00	01	11	10
		1	16	0	20	0	28	1
		0	17	0	21	1	29	d
		0	19	0	23	0	31	d
		0	18	0	22	1	30	26

ABC_{DE}
↓
MSB LSB

$$Y_1 = \bar{A} [\bar{B}\bar{C}\bar{D} + \bar{B}CE + \bar{BC}D + B\bar{C}\bar{D}\bar{E} + BDE + \bar{B}\bar{C}E + \bar{B}\bar{C}D]$$

$$Y_2 = A [\bar{C}\bar{D}\bar{E} + B\bar{D}E + \bar{B}\bar{C}E + BCP\bar{E})]$$

$$Y = Y_1 + Y_2 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CE + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D}\bar{E} + \bar{B}\bar{C}E + \bar{A}\bar{B}DE$$

$$21. F = \sum m(0, 1, 5, 9, 11, 12, 15, 19, 21, 25, 29, 31) + d(4, 7, 8, 20)$$

		BC		DE	00	01	11	10
		00	01	DE	00	01	11	10
		1	d	1	19	d		
		1	1	0	13	1	9	
		0	d	1	15	1	11	
		0	2	0	14	0	10	

		BC		DE	00	01	11	10
		00	01	DE	00	01	11	10
		0	16	d	14	0	20	24
		0	17	1	21	1	29	d
		1	19	0	23	1	31	0
		0	18	0	22	0	30	26

ABC_{PE}
↓
MSB LSB

$$Y_1 = \bar{A} (\bar{D}\bar{E} + \bar{B}\bar{D} + B\bar{C}E + CDE); Y_2 = A [\bar{B}\bar{C}\bar{D} + B\bar{D}E + \bar{B}\bar{C}DE + BCE]$$

$$Y = Y_1 + Y_2 = \bar{A}\bar{D}\bar{E} + \bar{A}\bar{B}\bar{D} + \bar{A}\bar{B}\bar{C}E + \bar{A}\bar{C}DE + A\bar{B}\bar{C}\bar{D} + AB\bar{D}E + A\bar{B}\bar{C}DE + ABCE$$

$$22. F = m(10, 11, 12, 18, 19, 24, 28, 29, 31) + \sum d(0, 1, 5, 9, 20, 21)$$

		BC		DE	00	01	11	10
		00	01	DE	00	01	11	10
		d	4	1				
		d	d	13	d	9		
		3	7	15	11			
		2	6	14	10			

		BC		DE	00	01	11	10
		00	01	DE	00	01	11	10
		d	20	1	12	1	24	
		17	2	1	25			
		1	19	23	31	27		
		1	18	22	30	26		

ABC_{DE}
↓
MSB LSB

$$Y_1 = \bar{A} [\bar{B}\bar{C}\bar{D} + \bar{B}\bar{D}\bar{E} + BC\bar{D}\bar{E} + B\bar{C}E + B\bar{C}\bar{D}]$$

$$Y = Y_1 + Y_2$$

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{D}\bar{E} + \bar{A}\bar{B}C\bar{D}\bar{E} + \bar{A}\bar{B}CE + \bar{A}\bar{B}\bar{C}D + AC\bar{D} + AB\bar{D}\bar{E} + ABCE + A\bar{B}\bar{C}D$$

$$23. F = \sum m(5, 6, 7, 8, 11, 12, 13, 15, 20, 21, 22, 23, 26, 27, 28, 29) + \sum d(0, 2, 4, 31).$$

	BC	00	01	11	10
DE					
00	d	d	1	1	
01	0	1	1	0	
11	0	1	1	1	1
10	d	1	0	0	0

	BC	00	01	11	10
DE					
00	0	16	26	1	24
01	0	17	27	1	25
11	0	18	28	1	27
10	0	19	22	0	30

ABCDE
↓
MSB ↓
LSB

$$Y_1 = \bar{A}(\bar{D}\bar{E} + \underline{\bar{C}\bar{D}} + \bar{B}\bar{E} + \bar{B}\bar{C} + \underline{B\bar{D}\bar{E} + \bar{C}\bar{E}}); Y_2 = A(\bar{B}\bar{C} + \underline{\bar{C}\bar{D}} + \underline{\bar{C}\bar{E}} + \bar{B}\bar{C}\bar{D})$$

$$Y = Y_1 + Y_2 \Rightarrow Y = \bar{A}\bar{D}\bar{E} + \underline{C\bar{D}} + \bar{A}\bar{B}\bar{E} + \bar{B}\bar{C} + \bar{A}\bar{B}\bar{D}\bar{E} + \bar{C}\bar{E} + \bar{A}\bar{B}\bar{C}\bar{D}$$

$$24. F = \sum m(0, 1, 5, 9, 22, 24, 26, 28, 31) + \sum d(10, 11, 13, 15, 17, 19)$$

	BC	00	01	11	10
DE					
00	1	0	0	0	8
01	1	1	d	1	1
11	0	0	d	1	1
10	0	0	0	d	10

	BC	00	01	11	10
DE					
00	0	16	0	1	28
01	d	17	0	0	25
11	d	18	0	1	27
10	0	19	1	0	29

$$Y_1 = \bar{A}(\bar{B}\bar{C}\bar{D} + \bar{D}\bar{E} + B\bar{E} + B\bar{C}\bar{D}); Y_2 = A(\bar{B}\bar{C}\bar{E} + B\bar{D}\bar{E} + B\bar{C}\bar{E} + BCDE + \bar{B}CD\bar{E})$$

$$Y = Y_1 + Y_2$$

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{D}\bar{E} + \bar{A}B\bar{E} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{E} + AB\bar{D}\bar{E} + AB\bar{C}\bar{E} + ABCDE + A\bar{B}\bar{C}\bar{D}\bar{E}$$

$$25. F = \sum m(0, 2, 4, 5, 8, 9, 10, 12, 15, 16, 18, 19, 21, 25, 26, 29, 31) + \sum d(1, 3, 6, 17, 20, 24, 27, 30)$$

$$+ \sum d(1, 3, 6, 17, 20, 24, 27, 30)$$

	BC	00	01	11	10
DE					
00	0	1	1	1	1
01	d	1	1	0	1
11	d	3	0	1	0
10	0	1	d	0	1

	BC	00	01	11	10
DE					
00	1	16	d	0	1
01	d	17	1	21	1
11	1	18	0	23	1
10	1	19	0	22	1

ABCDE
↑
MSB ↓
LSB

$$Y_1 = \bar{A}(\bar{D}\bar{E} + \underline{\bar{B}\bar{D}} + \bar{B}\bar{C} + \bar{C}\bar{E} + \bar{C}\bar{D} + \bar{B}\bar{E} + BCDE); Y_2 = \bar{C} + \underline{\bar{B}\bar{D}} + \bar{D}\bar{E} + BD$$

$$Y = Y_1 + Y_2$$

$$Y = \bar{A}\bar{D}\bar{E} + \bar{A}\bar{B}\bar{E} + \bar{B}\bar{D} + \bar{A}\bar{C}\bar{E} + \bar{A}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{E} + \bar{A}\bar{B}\bar{C}\bar{D}\bar{E} + \bar{A}\bar{C} + \bar{A}\bar{D}\bar{E} + \bar{A}\bar{B}\bar{D}$$

$$26. F = \sum m(0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 15, 16, 17, 19, 18, 20, 21, 31) + \sum d(22, 23, 25, 29)$$

		BC		DE			
		00	01	11	10	11	10
00		1	0	0	1	1	0
01		1	1	0	0	1	1
11		1	1	1	1	0	1
10		1	1	1	0	0	0

		BC		DE			
		00	01	11	10	11	10
00		1	0	0	0	0	0
01		1	1	d	d	d	d
11		1	1	d	1	0	1
10		1	1	d	0	0	0

$$Y_1 = \bar{A}(\bar{B} + \bar{C}\bar{D} + CDE)$$

$$Y_2 = A(\bar{B} + \bar{D}E + CE)$$

$$Y = Y_1 + Y_2 \Rightarrow Y = \bar{B} + \bar{A}\bar{C}\bar{D} + \bar{A}CDE + ACE + A\bar{D}E$$

$$27. F = \sum m(0, 2, 4, 5, 9, 11, 15, 16, 17, 19, 24, 25, 29, 31) + \sum d(1, 3, 7, 10, 21, 26, 28)$$

		BC		DE			
		00	01	11	10	11	10
00		1	1	12	8		
01		d	15	13	19		
11		d	d	15	11		
10		1	2	6	4	d	10

		BC		DE			
		00	01	11	10	11	10
00		1	16	10	d	14	
01		d	17	21	29	d	25
11		1	17	23	31	29	
10		18	22	30	d	26	

$$Y_1 = \bar{A}(\bar{B}\bar{D} + \bar{B}\bar{C} + DE + \bar{C}E + \bar{CD})$$

$$Y_2 = A(\bar{D}E + \bar{C}\bar{D} + B\bar{D} + B\bar{C}\bar{E} + BCE + \bar{B}\bar{C}E)$$

$$Y = \bar{A}\bar{B}\bar{D} + \bar{A}\bar{B}\bar{C} + \bar{A}DE + \bar{A}\bar{C}E + \bar{A}\bar{C}D + A\bar{D}E + A\bar{C}\bar{D} + AB\bar{D} + AB\bar{C}\bar{E} + ABCE + A\bar{B}CE$$

$$28. F = \sum m(0, 1, 5, 6, 7, 8, 9, 14, 15, 16, 18, 19, 24, 26, 28, 30) + \sum d(2, 3, 10, 11, 12, 21, 25)$$

$$+ \sum d(2, 3, 10, 11, 12, 21, 25)$$

		BC		DE			
		00	01	11	10	11	10
00		1	0	d	18		
01		1	1	5	13	19	
11		d	2	17	15	d	11
10		d	1	16	14	d	9

		BC		DE			
		00	01	11	10	11	10
00		1	16	20	18	24	
01		d	17	21	29	d	25
11		1	19	23	31	29	
10		18	22	30	11	26	

$$Y_1 = \bar{A}(C + D + \bar{B}E + \bar{B}\bar{E})$$

$$Y_2 = (\bar{C}\bar{E} + \bar{B}\bar{E} + B\bar{C}\bar{D} + \bar{B}\bar{C}D + BC\bar{D})$$

$$y = Y_1 + Y_2$$

$$Y = \bar{A}\bar{C} + \bar{A}D + \bar{A}\bar{B}E + \bar{B}\bar{E} + A\bar{C}\bar{E} + ABC\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D}$$

29. $F = \sum m(0, 1, 4, 5, 6, 7, 8, 9, 14, 15, 16, 17, 18, 19, 24, 25, 26, 27, 28, 29, 31) + \sum d(2, 3, 11, 12, 13, 21, 22, 23)$.

		BC		DE	
		00	01	11	10
		00	1 0	1 1	d ₁ 1
		01	1 1	d ₂ 1	1 1
		11	d ₃ 1	1 1	d ₄ 1
		10	d ₅ 1	1 1	1 0

		BC		DE	
		00	01	11	10
		1	"	28	24
		1	d ₁	1	11
		11	"	d	1
		10	d	1	1

ABCDE
↓
MSB USB

$$Y_1 = \bar{A}(\bar{B} + C + \bar{D} + E)$$

$$Y = Y_1 + Y_2$$

$$Y = \bar{A}\bar{B} + \bar{A}C\bar{T} + A\bar{D} + E + A\bar{C} + AB\bar{D} + A\bar{B}D.$$

30. $F = \sum m(1, 5, 9, 11, 15, 19, 21, 25, 29, 31) + \sum d(0, 10, 12, 14, 18, 20, 24, 26, 28)$

		BC		DE	
		00	01	11	10
		00	d	u	d ₁
		01	1	1	1
		11	3	1	1
		10	2	6	d ₂ d ₁₀

		BC		DE	
		00	01	11	10
		00	d ₁₁	d ₂₀	d ₁₆ d ₂₁
		01	"	1	1
		11	1	1	1
		10	d ₁	"	1

$$Y_1 = \bar{A}(\bar{B}\bar{C}\bar{D} + \bar{B}\bar{D}\bar{E} + B\bar{C}\bar{E} + B\bar{C}E + BD)$$

$$Y_2 = A(C\bar{B} + B\bar{D} + BC\bar{E} + \bar{B}\bar{C}D + B\bar{C}\bar{E})$$

$$Y = Y_1 + Y_2 \Rightarrow Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{D}\bar{E} + \bar{A}B\bar{C}\bar{E} + \bar{A}B\bar{C}E + \bar{A}BD + A\bar{C}\bar{D} + ABD + ABC\bar{E} + A\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{E}$$

Moderate level :-

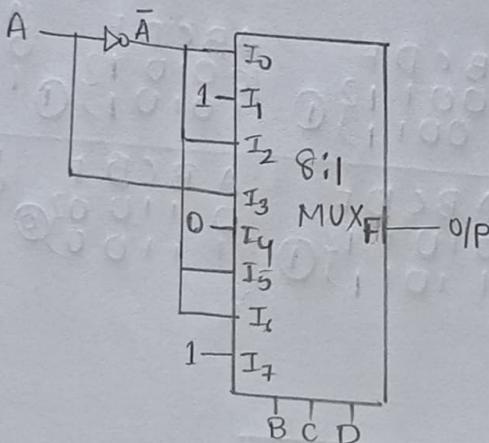
1. Implementation of 'n' variable functions using only MUX(s) with 'n-1' selection lines.

$$a. F = \sum m(0, 1, 5, 7, 9, 11, 15) + \sum d(2, 6).$$

$n=4$. $n-1=3$ selection lines

$B, C, D \rightarrow$ selection lines

A B C D o/p 0 0 0 0 1 1 0 0 0 0 } A	A B C D o/p 0 0 0 1 1 1 0 0 1 0 } ①	A B C D o/p 0 0 1 0 d 1 0 1 0 0 } A	A B C D o/p 0 0 1 1 0 1 0 1 1 1 } A
A B C D o/p 0 1 0 0 0 1 1 0 0 0 } ①	A B C D o/p 0 1 0 1 1 1 1 0 1 0 } A	A B C D o/p 0 1 1 0 d 1 1 1 0 0 } A	A B C D o/p 0 1 1 1 1 1 1 1 1 1 } ①

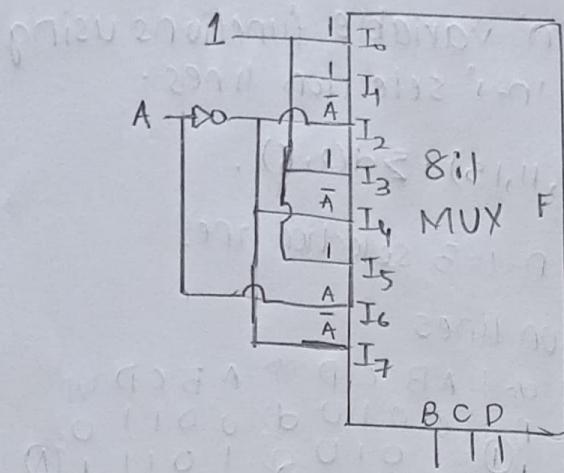


$$b) F = \sum m(0, 2, 5, 4, 7, 9, 11, 13, 14) + \sum d(1, 3, 8)$$

$n=4$

$n-1=3 \rightarrow$ Selection lines = B, C, D.

A B C D F 0 0 0 0 1 1 0 0 0 0 } A } ①	A B C D F 0 0 0 1 d 1 0 0 1 0 } ①	A B C D F 0 0 1 0 1 1 0 1 0 0 } A } ①	A B C D F 0 0 1 1 d 1 0 1 1 1 } ①
A B C D F 0 1 0 0 1 1 1 0 0 0 } A } ①	A B C D F 0 1 0 1 1 1 1 0 1 0 } ①	A B C D F 0 1 1 0 0 1 1 1 0 1 } A } ①	A B C D F 0 1 1 1 1 1 1 1 1 0 } A } ①



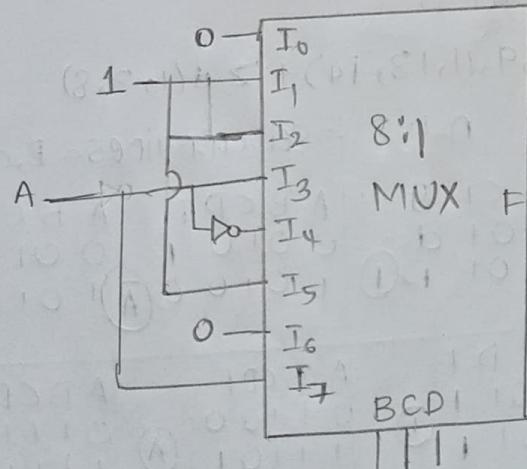
$$c) F = \sum m(1, 2, 4, 5, 9, 10, 13) + \sum d(11, 15)$$

$n=4$

$B, C, D = \text{selection lines } (n-1=3)$

A B C D F	A B C D F	A B C D F	A B C D F
0 0 0 0 0 0 0	0 0 0 1 1 2 ①	0 0 1 0 1 3 ①	0 0 1 1 0 0 2 ④
1 0 0 0 0 0 0	1 0 0 1 1 3 ①	1 0 1 0 1 ①	1 0 1 1 1 0 2 ④

A B C D F	A B C D F	A B C D F	A B C D F
0 1 0 0 1 ④	0 1 0 1 1 2 ①	0 0 1 1 0 0 2 ④	0 1 1 1 0 0 2 ④
1 1 0 0 0 0	1 1 0 1 1 ①	1 1 1 0 0 0	1 1 1 1 1 0 2 ④



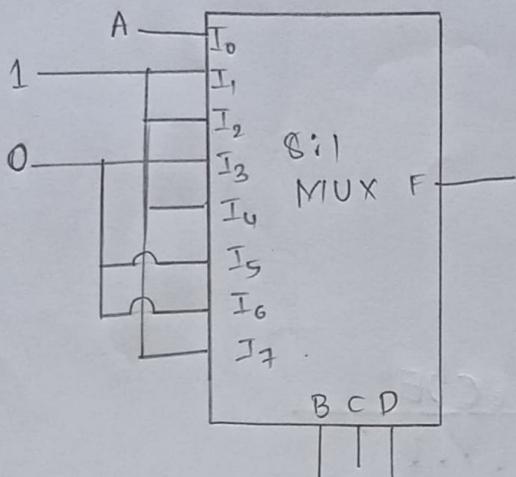
d) $F = \sum m(2, 4, 8, 12, 15) + \sum d(1, 7, 9, 10)$

$n=4$

B, C, D → Selection lines ($n-1=3$)

A B C D F	A B C D F	A B C D F	A B C D F
0 0 0 0 0 0 2	0 0 0 1 0 2	0 0 1 0 1 2	0 0 1 1 0 2
1 0 0 0 1 1 0	1 0 0 1 1 0 1	1 0 1 0 1 1 0	1 0 1 1 1 1 0

A B C D F	A B C D F	A B C D F	A B C D F
0 1 0 0 1 1 2	0 1 0 1 0 2	0 1 1 0 0 2	0 1 1 1 1 2
1 1 0 0 1 1 0	1 1 0 1 0 0	1 1 1 0 0 0	1 1 1 1 1 0



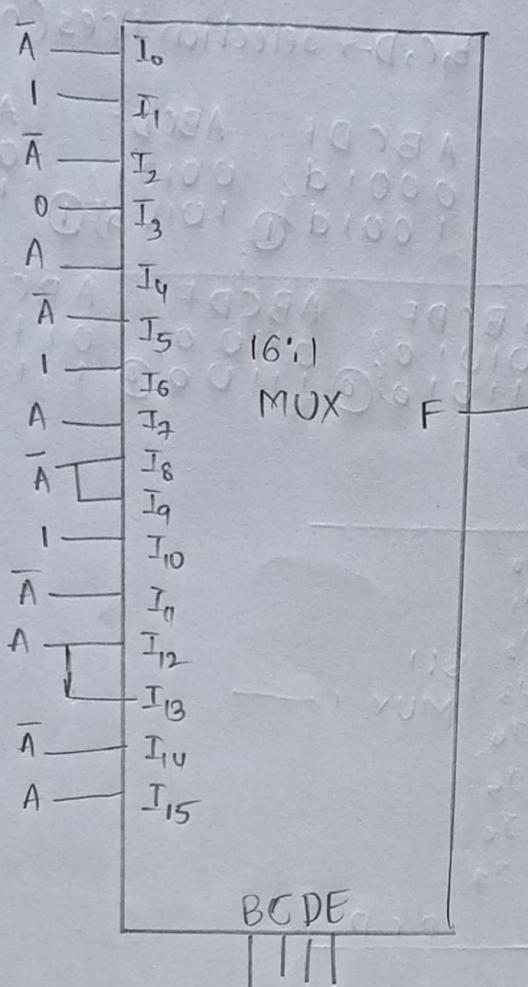
e) $F = \sum m(0, 2, 5, 8, 9, 11, 14, 17, 23, 26, 28, 29, 31)$

+ $\sum d(1, 6, 10, 20, 22)$

$n=5$ $n-1=4$ (B, C, D, E) - selection lines.

Decimal	A B C D E F	Dec A B C D E F	Dec A B C D E F
0	0 0 0 0 0 0	0 0 0 1 1 0 2	12 0 1 1 0 0 2
16	1 0 0 0 0 0	22 1 0 1 1 0 2	28 1 1 1 0 0 2
1	0 0 0 0 1 1 2	7 0 0 1 1 1 0 2	13 0 1 0 0 1 2
17	1 0 0 0 1 1 0	23 1 0 1 1 1 1 0	29 1 1 1 0 1 1 0
2	0 0 0 1 0 1 2	8 0 0 0 0 0 1 2	14 0 1 1 1 0 1 2
18	1 0 0 1 0 0 2	24 1 1 0 0 0 0 2	30 1 1 1 1 0 0 2
3	0 0 0 1 1 0 2	9 0 1 0 0 1 1 2	15 0 1 1 1 1 0 2
19	1 0 0 1 1 0 0	25 1 1 0 0 1 0 2	31 1 1 1 1 1 1 0
4	0 0 1 0 0 0 2	10 0 1 0 1 0 2	
20	1 0 1 0 0 0 2	26 1 1 0 1 0 1 2	
5	0 0 1 0 1 1 2	11 0 1 0 1 1 1 2	
21	1 0 1 0 1 0 2	27 1 1 0 1 1 0 2	

$$(0, 1, F, F, F)D3 + (2, 3, 8, 4, 6, 8)M3 = 7 \quad (b)$$



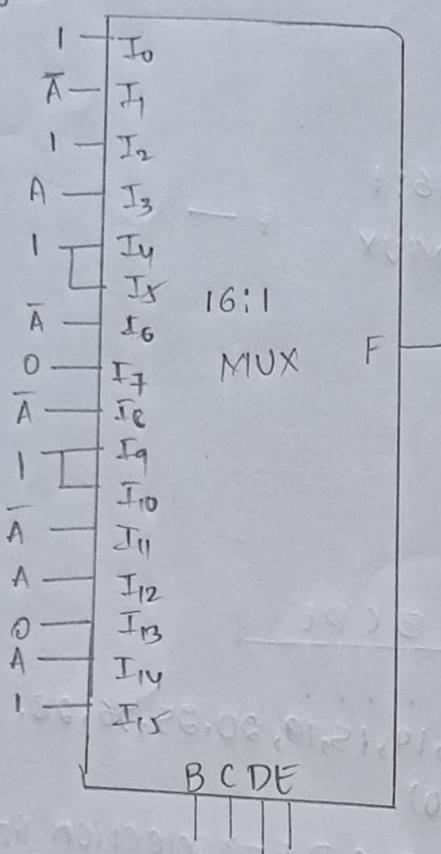
$$f) F = \sum m(0, 2, 4, 5, 6, 8, 9, 11, 15, 19, 21, 25, 26, 30) + \sum d(1, 10, 16, 18, 20, 28, 31).$$

$n=5$ $B, C, D, E \rightarrow$ selection lines ($n-1=4$)

DEC	A	B	C	D	E	F
0	0	0	0	0	0	1
16	0	0	0	0	d	1
1	0	0	0	1	d	2
17	1	0	0	1	0	A
2	0	0	1	0	1	2
18	1	0	0	1	d	1
3	0	0	0	1	0	2
19	1	0	0	1	1	A
4	0	0	1	0	1	1
20	1	0	1	0	d	1
5	0	0	1	0	1	1
21	1	0	1	0	1	1

Dec	A	B	C	D	E	F	Dec	A	B	C	D	E	F
6	0	0	1	1	0	1	12	0	1	1	0	0	2
22	1	0	1	1	0	0	28	1	1	1	0	d	1
7	0	0	1	1	1	0	13	0	1	1	0	1	0
23	1	0	1	1	1	0	29	1	1	1	0	1	0
8	0	1	0	0	0	1	14	0	1	1	1	0	0
24	1	1	0	0	0	1	30	1	1	1	1	0	1
9	0	1	0	0	1	1	15	0	1	1	1	1	1
25	1	1	0	0	1	1	31	1	1	1	1	d	1
10	0	1	0	1	0	1							
26	1	1	0	1	0	1							
11	0	1	0	1	1	1							
27	1	1	0	1	1	0							

$$\bar{A} = \overline{I_1} \oplus \bar{I_2}$$



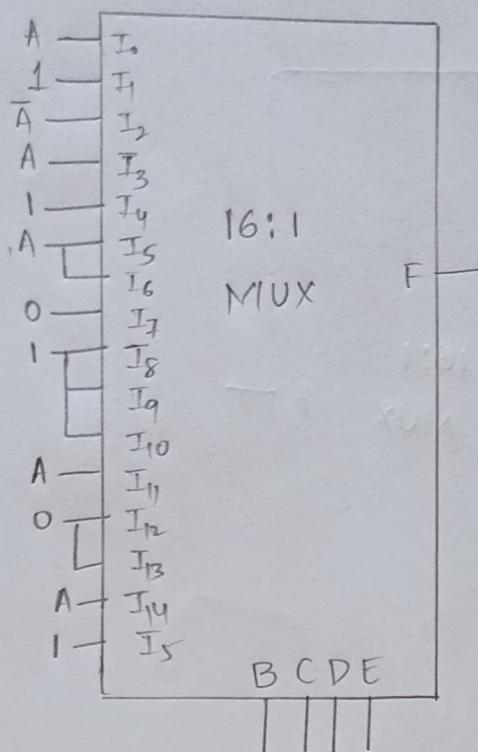
g) $F = \sum m(1, 2, 4, 8, 9, 10, 15, 16, 17, 19, 20, 25, 26, 27) + \sum d(21, 22, 24, 30, 31)$.

$n=5$

B, C, D, E = Selection lines ($5-1=4$)

Dec	A	B	C	D	E	F
0	0	0	0	0	0	02
1	1	0	0	0	1	A
2	0	0	0	1	1	
3	1	0	0	1	1	
4	0	0	1	0	1	
5	1	0	1	0	1	A
6	0	0	1	0	0	
7	1	0	1	0	0	A
8	0	0	1	1	0	
9	1	0	0	1	1	
10	0	0	1	1	1	
11	1	0	0	1	1	A
12	0	0	1	1	0	
13	1	0	0	1	0	
14	0	0	1	0	1	
15	1	0	0	0	1	
16	0	0	0	1	1	
17	1	0	0	0	1	
18	0	0	0	1	0	
19	1	0	0	0	1	
20	0	0	0	0	1	
21	1	0	0	0	0	
22	0	0	0	0	0	
23	1	0	0	0	0	
24	0	0	0	0	0	d
25	1	0	0	0	0	
26	1	0	0	0	1	
27	1	0	0	1	1	
28	1	0	0	0	0	
29	1	0	0	0	0	
30	0	0	0	0	1	
31	1	0	0	0	0	d

Dec	A	B	C	D	E	F
8	0	1	0	0	0	1
24	1	1	0	0	0	d
9	0	1	0	0	1	1
25	1	1	0	0	1	1
10	0	1	0	1	0	1
26	1	1	0	1	0	1
11	0	1	0	1	0	2
27	1	1	0	1	1	1
12	0	1	1	0	0	0
28	1	1	0	0	0	
13	0	1	1	0	1	0
29	1	1	0	1	0	
14	0	1	1	1	0	0
30	1	1	1	1	0	d
15	0	1	1	1	1	1
31	1	1	1	1	1	d

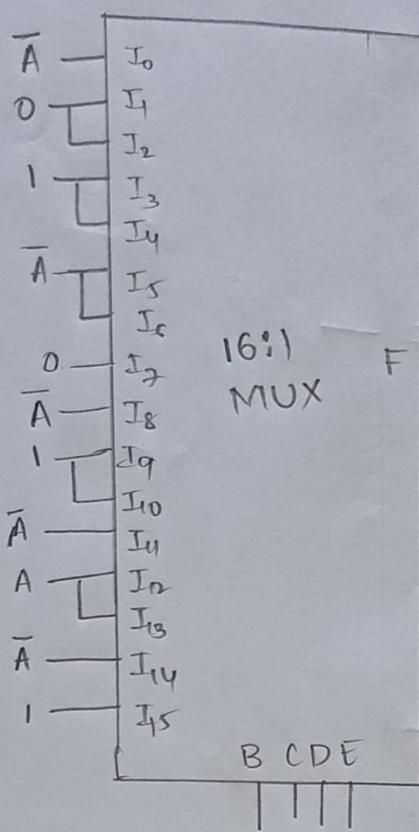


$$h) F = \sum m(3, 4, 5, 8, 9, 11, 14, 15, 19, 20, 25, 26, 28, 29, 31) + \sum d(0, 6, 10)$$

$n=5$ B, C, D, E \rightarrow selection lines ($5-1=4$)

Dec	A	B	C	D	E	F
0	0	0	0	0	0	d2
16	1	0	0	0	0	0
1	0	0	0	0	1	03
17	1	0	0	0	0	03
2	0	0	0	1	0	02
18	1	0	0	1	0	03
3	0	0	0	1	1	12
19	1	0	0	1	1	13
4	0	0	1	0	0	12
20	1	0	1	0	0	13
5	0	0	1	0	1	12
21	1	0	1	0	0	10
6	0	0	1	0	0	03
22	1	0	1	1	0	03
7	0	0	1	1	0	30
23	0	1	1	1	0	30

Dec	A	B	C	D	E	F
8	0	1	0	0	0	13
24	1	1	0	0	0	0
9	0	1	0	0	1	13
25	1	1	0	0	1	1
10	0	1	0	1	0	12
26	1	1	0	1	0	13
11	0	1	0	1	1	13
27	1	1	0	1	0	0
12	0	1	1	0	0	03
28	1	1	1	0	0	1
13	0	1	1	0	1	03
29	1	1	1	0	1	13
14	0	1	1	1	0	13
30	1	1	1	1	0	03
15	0	1	1	1	1	1
31	1	1	1	1	1	13



$$F = \sum m(0, 5, 7, 8, 10, 15, 16, 18, 19, 20, 25, 27, 29, 31)$$

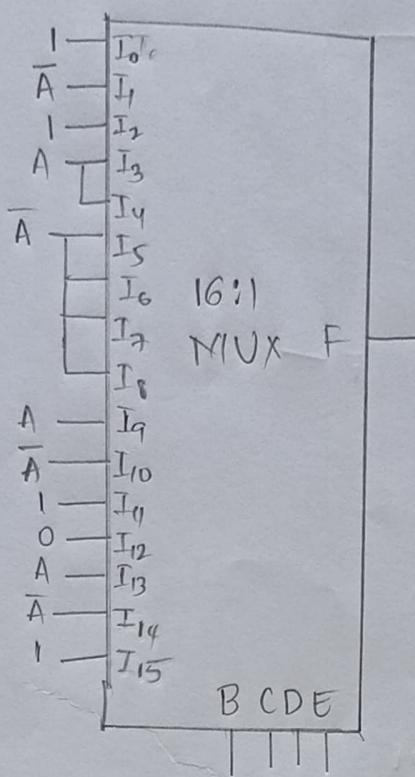
$$+ \sum d(1, 2, 6, 11, 14)$$

$n=5$

B, C, D, E \rightarrow selection lines ($n=4$)

Dec	A	B	C	D	E	F
0	0	0	0	0	0	1
16	1	0	0	0	0	1
1	0	0	0	0	1	$\overline{d_3A}$
17	1	0	0	0	1	$\overline{d_3A}$
2	0	0	0	1	0	$\overline{d_3A}$
18	1	0	0	1	0	1
3	0	0	0	1	0	$\overline{d_3A}$
19	1	0	0	1	1	$\overline{d_3A}$
4	0	0	1	0	0	$\overline{d_3A}$
20	1	0	1	0	0	1
5	0	0	1	0	1	$\overline{T_3A}$
11	1	0	1	0	1	$\overline{d_3A}$
6	0	0	1	1	0	$\overline{d_3A}$
22	1	0	1	1	0	$\overline{d_3A}$
7	0	0	1	1	1	$\overline{T_3A}$
23	1	0	1	1	1	$\overline{d_3A}$

Dec	A	B	C	D	E	F
8	0	1	0	0	0	1
24	1	1	0	0	0	0
9	0	1	0	0	1	0
25	1	1	0	0	1	1
10	0	1	0	1	0	1
26	1	1	0	1	0	0
11	0	1	0	1	1	$\overline{d_3A}$
27	1	1	0	1	1	1
12	0	1	1	0	0	$\overline{d_3A}$
28	1	1	1	0	0	0
13	0	1	1	0	1	$\overline{d_3A}$
29	1	1	1	0	1	1
14	0	1	1	1	0	$\overline{d_3A}$
30	1	1	1	1	0	$\overline{d_3A}$
15	0	1	1	1	1	$\overline{T_3A}$
31	1	1	1	1	1	1

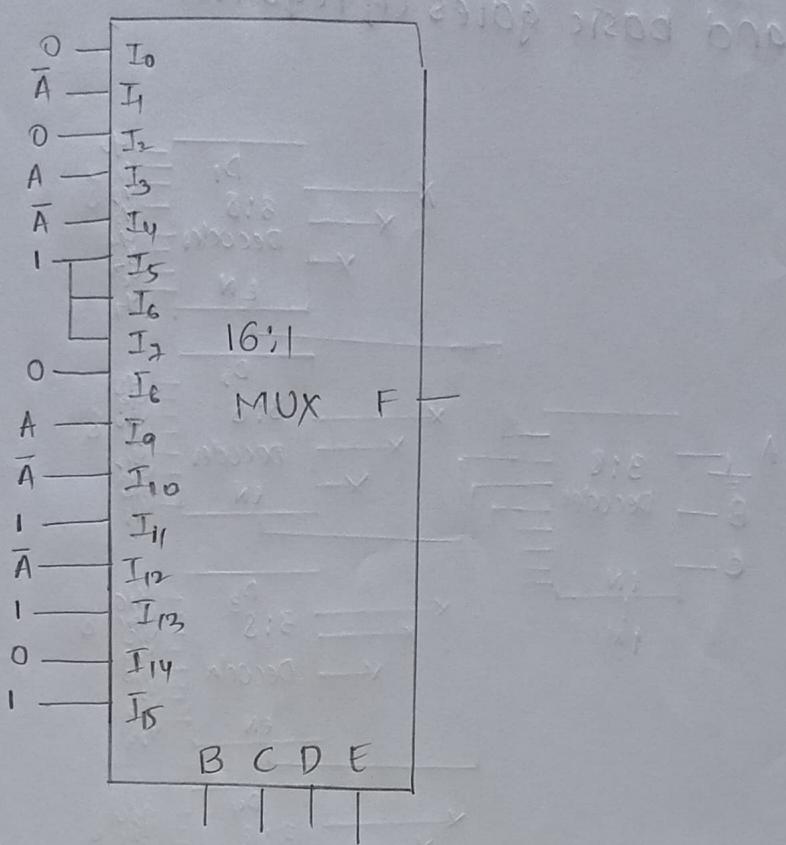


$$j) F = \sum m(1, 7, 10, 15, 19, 27, 29, 31) + \sum d(4, 5, 6, 11, 12, 13, 21, 22, 23, 25).$$

$n=5$ $B, C, D, E \rightarrow$ selection lines ($n-1=4$)

Dec	A	B	C	D	E	F
0	0	0	0	0	0	0
4	0	0	0	0	0	1
16	1	0	0	0	0	0
1	0	0	0	1	1	0
17	1	0	0	0	1	0
2	0	0	0	1	0	0
18	1	0	0	1	0	0
3	0	0	0	1	0	0
19	1	0	0	1	1	0
4	0	0	1	0	0	1
20	1	0	1	0	0	0
5	0	0	1	0	1	1
21	1	0	1	0	1	0
6	0	0	1	1	0	0
22	1	0	1	1	0	0
7	0	0	1	1	1	1
23	1	0	1	1	1	0

Dec	A	B	C	D	E	F
8	0	1	0	0	0	0
24	1	1	0	0	0	0
9	0	1	0	0	1	0
25	1	1	0	0	1	0
10	0	1	0	1	0	0
26	1	1	0	1	0	0
11	0	1	0	1	1	0
27	1	1	0	1	1	1
12	0	1	1	0	0	0
28	1	1	1	0	0	0
13	0	1	1	0	1	0
29	1	1	1	0	1	1
14	0	1	1	1	0	0
30	1	1	1	1	0	0
15	0	1	1	1	1	1
31	1	1	1	1	1	1



(0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0)

(1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0)

(0, 1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0)

(0, 0, 1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0)

(0, 0, 0, 1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0)

(0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0)

(0, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0)

(0, 0, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 0, 0, 0, 0)

(0, 0, 0, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 0, 0, 0)

(0, 0, 0, 0, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 0, 0)

(0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 0)

(0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0)

(0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 0, 0, 0, 0)

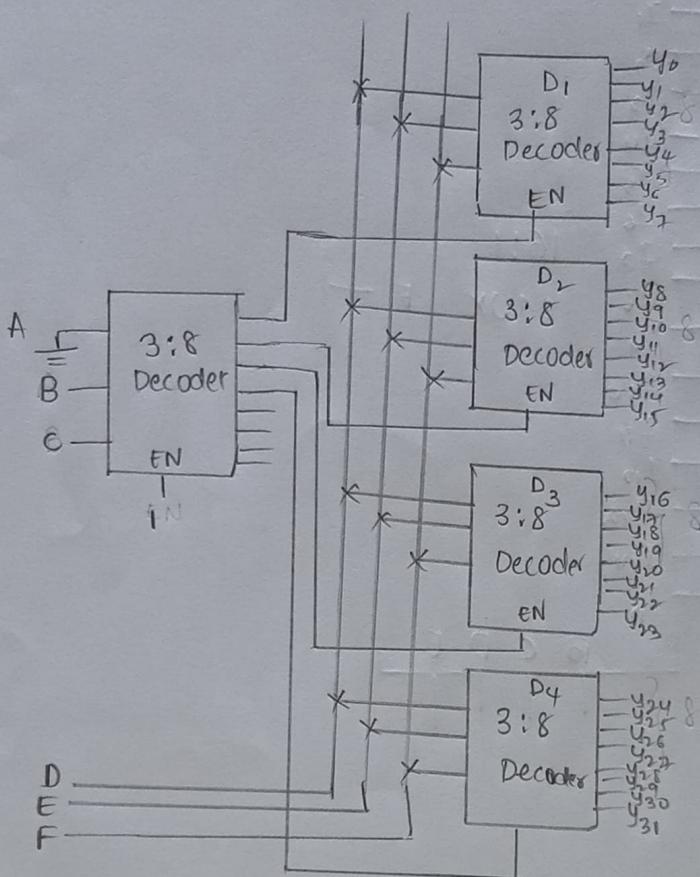
(0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 0, 0, 0)

(0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 0, 0)

(0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 0)

(0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1)

2. Implement 5:32 Decoder using only 3:8 Decodes and basic gates (if required).



A	B	C	$\rightarrow D_1$ is selected (D ₁ - Decoder is enabled)
0	0	0	$\rightarrow D_2$ is selected (D ₂ - Decoder is enabled)
0	0	1	$\rightarrow D_3$ is selected (D ₃ - Decoder is enabled)
0	1	0	$\rightarrow D_4$ is selected (D ₄ - Decoder is enabled)
0	1	1	

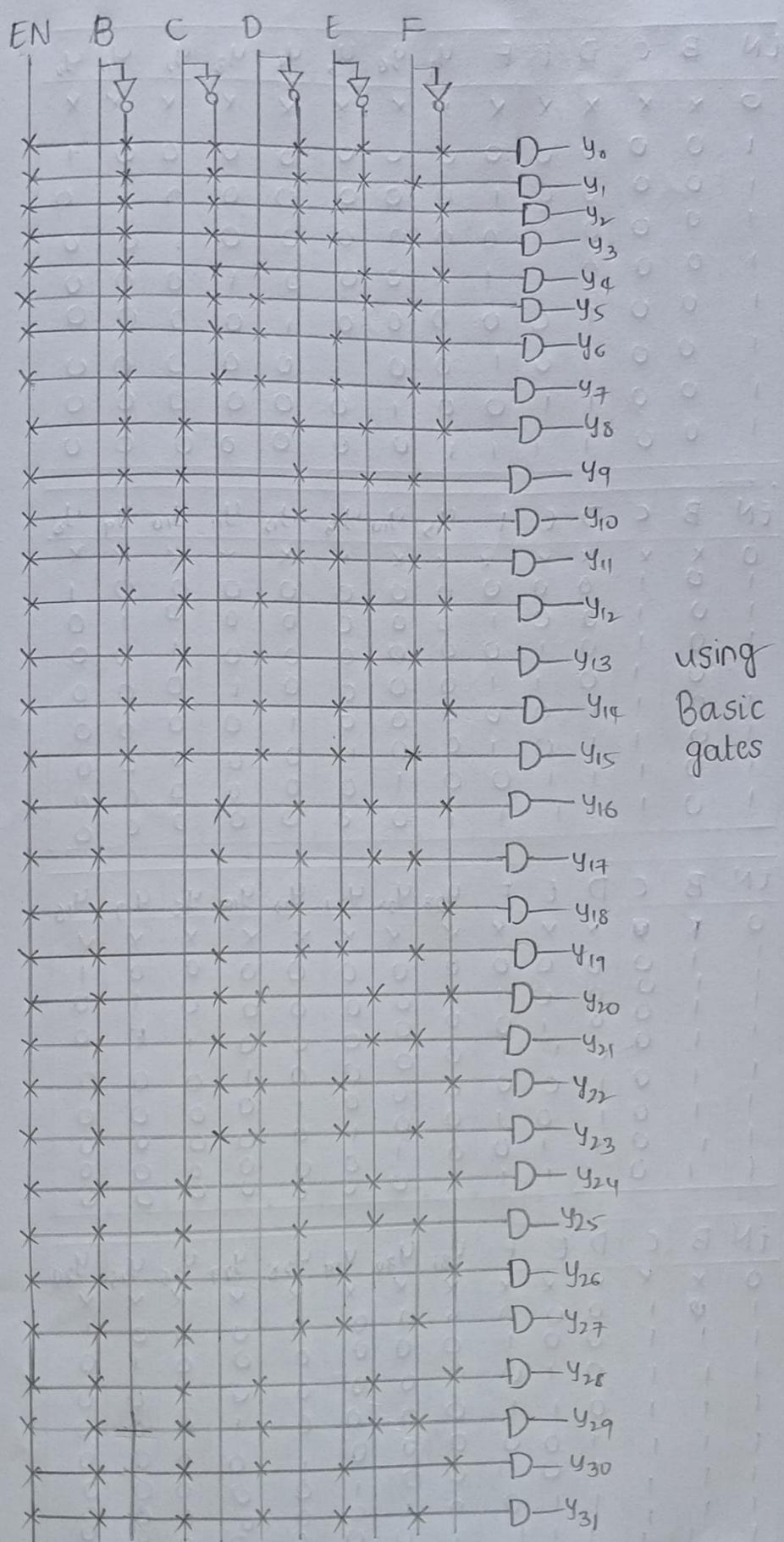
B, C, D, E, F \rightarrow Inputs - (5)

EN	B	C	D	E	F	y_7	y_6	y_5	y_4	y_3	y_2	y_1	y_0
0	x	x	x	x	x	x	x	x	x	x	x	x	x
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	0	1	0	0	0	0	0	0	0	1
1	0	0	0	1	0	0	0	0	0	0	1	0	0
1	0	0	0	1	1	0	0	0	0	0	1	0	0
1	0	0	1	0	0	0	0	0	0	1	0	0	0
1	0	0	1	0	1	0	0	0	0	1	0	0	0
1	0	0	1	0	1	0	0	0	1	0	0	0	0
1	0	0	1	1	0	0	1	0	0	0	0	0	0
1	0	0	1	1	1	1	0	0	0	0	0	0	0

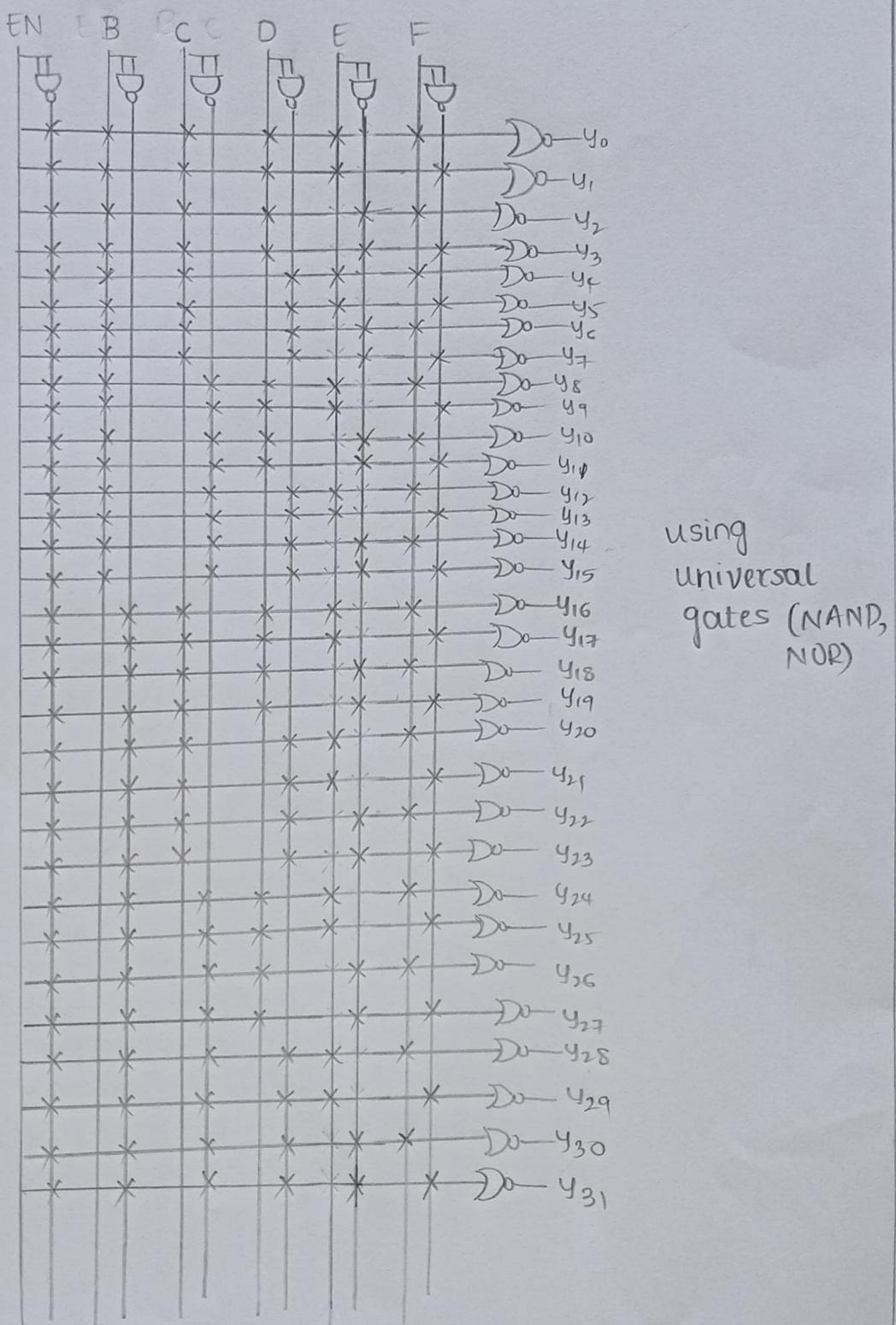
EN	B	C	D	E	F	y_{15}	y_{14}	y_{13}	y_{12}	y_{11}	y_{10}	y_9	y_8
0	x	x	x	x	x	x	x	x	x	x	x	x	x
1	0	1	0	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	0	1	1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	0	1	0	0	0
1	0	1	1	0	0	1	0	0	0	0	0	0	0
1	0	1	1	1	0	0	1	0	0	0	0	0	0
1	0	1	1	1	1	0	0	0	0	0	0	0	0

EN	B	C	D	E	F	y_{23}	y_{22}	y_{21}	y_{20}	y_{19}	y_8	y_{17}	y_{16}
0	x	x	x	x	x	x	x	x	x	x	x	x	x
1	1	0	0	0	0	0	0	0	0	0	0	0	1
1	1	0	0	0	0	1	0	0	0	0	0	0	1
1	1	0	0	0	1	0	0	0	0	0	0	1	0
1	1	0	0	1	1	0	0	0	0	0	1	0	0
1	1	0	1	0	0	0	0	0	0	0	1	0	0
1	1	0	1	0	1	0	0	0	1	0	0	0	0
1	1	0	1	1	0	0	0	0	1	0	0	0	0
1	1	0	1	1	1	0	0	0	0	1	0	0	0
1	1	0	1	1	1	1	0	0	0	0	0	0	0

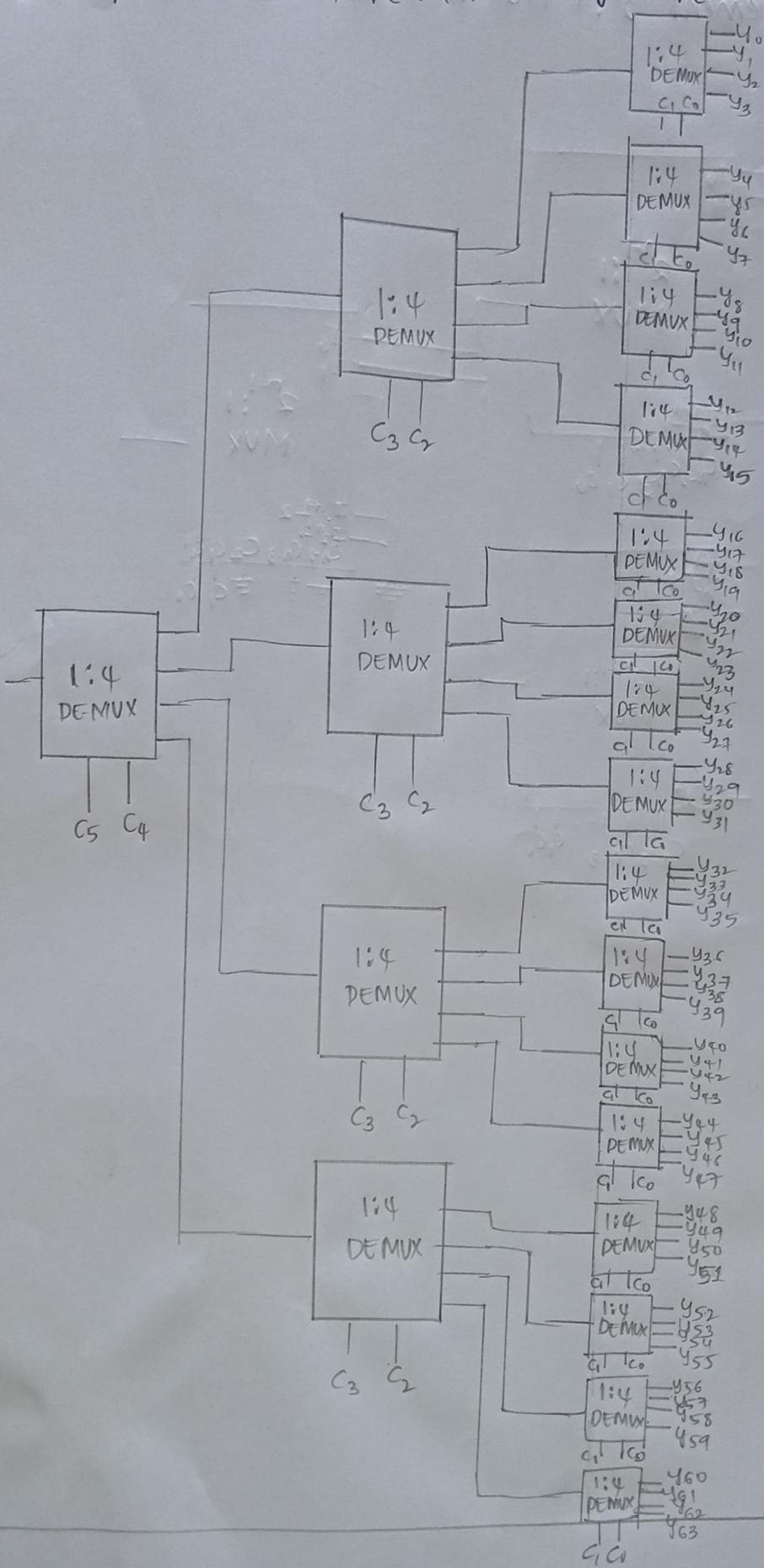
EN	B	C	D	E	F	y_{31}	y_{30}	y_{29}	y_{28}	y_{27}	y_{26}	y_{25}	y_{24}
0	x	x	x	x	x	x	x	x	x	x	x	x	x
1	1	0	0	0	0	0	0	0	0	0	0	0	1
1	1	1	0	0	1	0	0	0	0	0	0	1	0
1	1	1	0	1	0	0	0	0	0	0	1	0	0
1	1	1	0	1	1	0	0	0	0	0	1	0	0
1	1	1	1	0	0	0	0	0	0	1	0	0	0
1	1	1	1	0	0	1	0	0	0	0	0	0	0
1	1	1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	1	1	0	0	0	0	0	0	0



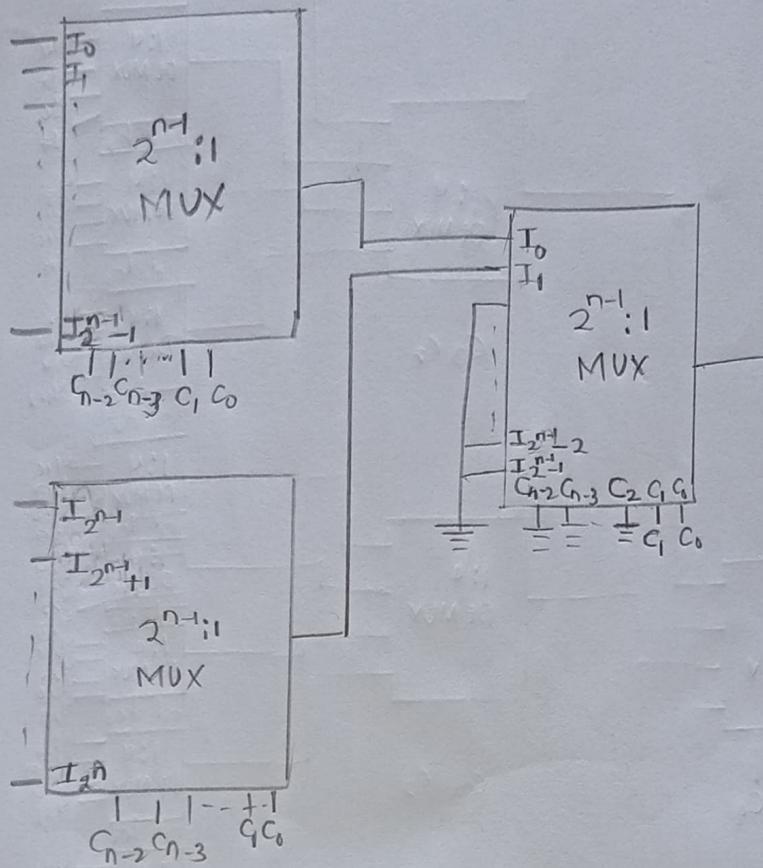
4. Implement 5:32 decoder using only 3:8 decoders and universal gates (if required).



6. Implement 1:64 De-MUX using 1:4 De-MUX only.



7. Implement $2^n:1$ MUX with $2^{n-1}:1$ MUX(s).



High level:-

1. 5 Questions $\rightarrow A \ B \ C \ D \ E \ D \ F \ M \ N \ S$
 marks $\rightarrow 30 \ 25 \ 20 \ 15 \ 10 \times \times \times \times$
 score greater than equal to 65y. \rightarrow pass

For the student to pass, any one of the following condition must be satisfied.

$$ABC\bar{D}\bar{E}=1$$

$$A\bar{B}CD\bar{E}=1$$

$$A\bar{B}\bar{C}DE=1$$

$$ABCDE=1$$

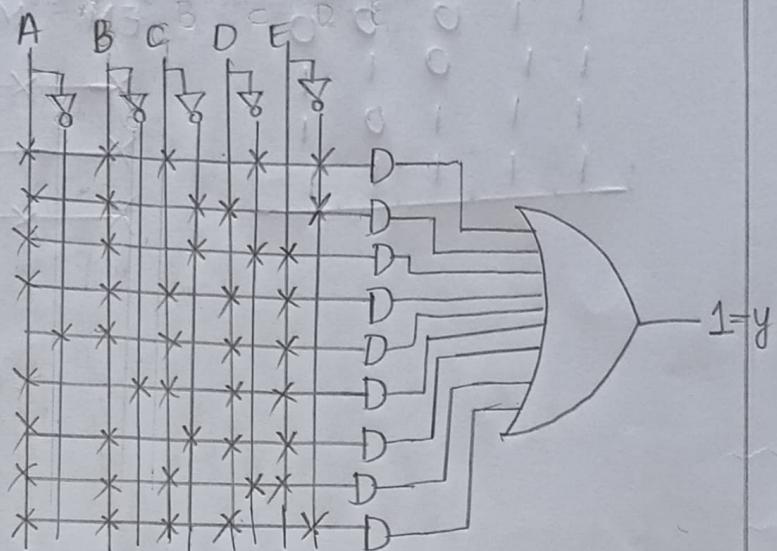
$$\bar{A}BCDE=1$$

$$A\bar{B}CDE=1$$

$$AB\bar{C}DE=1$$

$$AB\bar{C}\bar{D}E=1$$

$$ABC\bar{D}\bar{E}=1$$



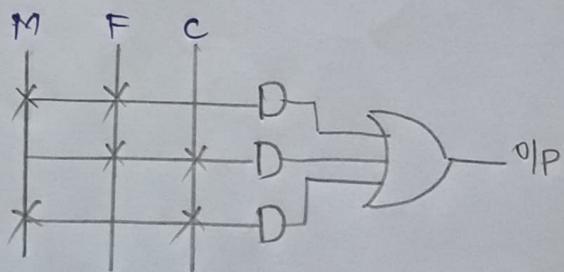
2.

M	F	C	O/P
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

I/P = 1 \rightarrow If member is present, else 0.
 O/P = 1 \rightarrow If locker is open, else 0.

C	MF			
	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$$O/P = MF + FC + MC$$



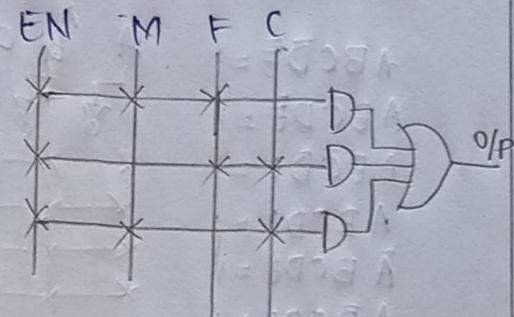
3.

$I/O = 1 \rightarrow$ If member is present, else 0
 $O/I = 1 \rightarrow$ If locker is open, else 0.

EN	M	F	C	O/I
0	X	X	X	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

MF	00	01	11	10
C	0,0	1,0	0,1	1,1
O/I	0,1,1,0	1,1,0,1	1,0,1,1	0,1,1,1

$$O/I = EN(MF + FC + MC)$$

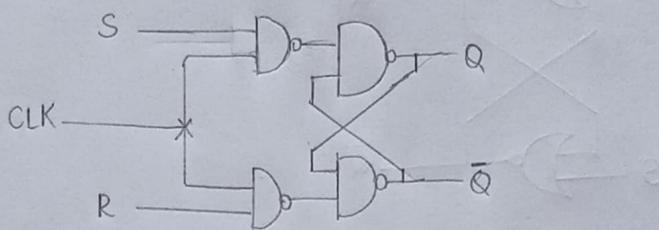


EN	M	F	C	O/I
0	0	0	0	0
0	1	0	0	0
0	0	1	0	0
0	0	0	1	1
1	0	0	0	0
1	1	0	0	0
1	0	1	0	0
1	1	1	0	1
1	1	1	1	1

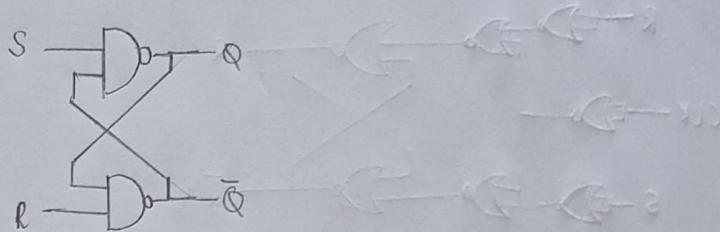
Sequential circuits

Basis level Questions:

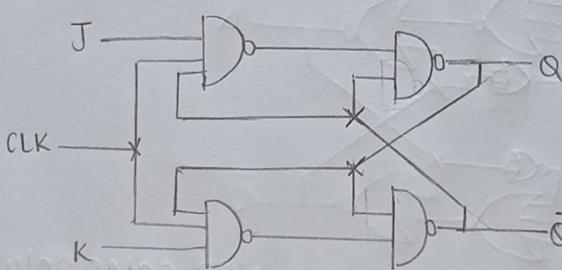
1. Implement SR flip flop using NAND gates only.



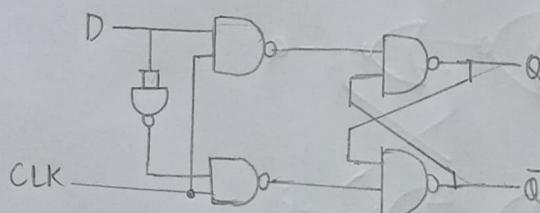
2. Implement SR latch using NAND gates only.



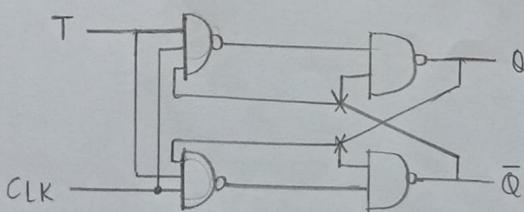
3. Implement JK flip flop using NAND gates only.



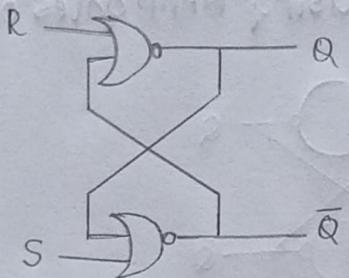
4. Implement D flip flop using NAND gates only.



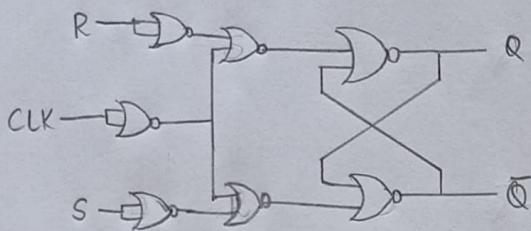
5. Implement T flip flop using NAND gates only.



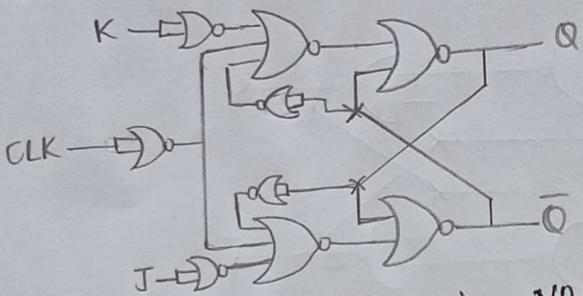
6. Implement SR latch using NOR gates only.



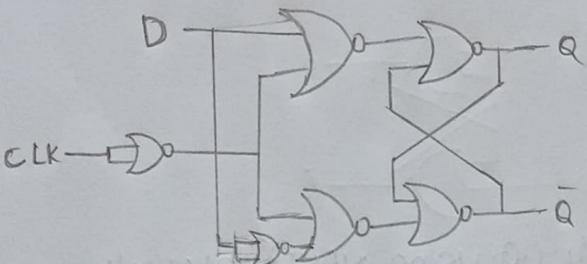
7. Implement SR flip flop using NOR gates only.



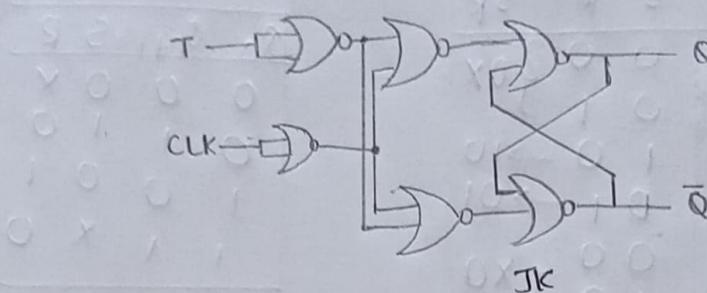
8. Implement JK flip flop using NOR gates only.



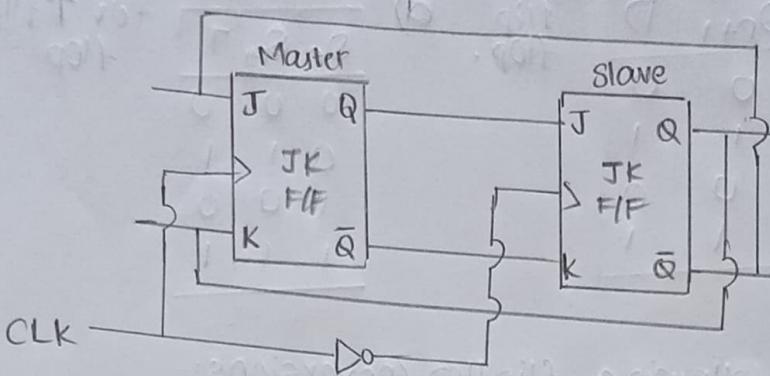
9. Implement D flip flop using NOR gates only.



10. Implement T flip flop using NOR gates only.



11. Implement master-slave flip flop.



12. Write the excitation tables of the following flip flops:-
 a) JK b) SR c) D d) T.

a)

Q_n	Q_{n+1}	J	K	J	K
0	0	0	0	0	X
0	0	0	1	0	X
0	1	1	0	1	X
0	1	1	1	X	1
1	0	0	1	X	1
1	0	1	1	X	1
1	1	0	0	X	0
1	1	1	0	X	0

Excitation table for JK flip flop.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

b)

Q_n	Q_{n+1}	S	R	SR
0	0	0	0	2'0X
0	0	0	1	
0	1	1	0	$\rightarrow 10$
1	0	0	1	$\rightarrow 01$
1	1	0	0	2'X0
1	1	1	0	

Excitation table
for SR flip flop

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

c)

Excitation table for D
flip flop.

Q_n	Q_{n+1}	D	flip flop.
0	0	0	
0	1	1	
1	0	0	
1	1	1	

d)

Excitation table
for T flip flop

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	0
1	1	1

13) Perform following flip flop conversions-

a) SR to D

D	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0

Expressing S and R in terms of D using K-maps.

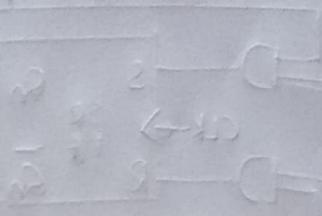
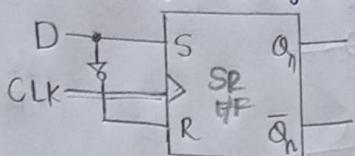
D	Q_n	S	
		0	1
0	0	0	0
1	1	1	X

D	Q_n	R	
		0	1
D	Q_n	R	
		0	1
0	0	X	1
1	0	0	0

$$S = D$$

$$R = \overline{D}$$

logic diagram



b. SR to JK

J	K	Q_n	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	1	*	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	*	0
1	1	0	1	1	0
1	1	1	0	0	1

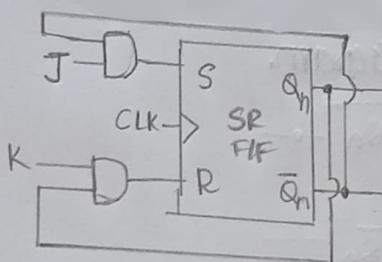
JK	S.			
	00	01	11	10
0	00	01	11	10
1	X	0	0	X

$S = \overline{Q_n} J$

JK	R			
	00	01	11	10
0	X	X	0	0
1	0	1	1	0

$R = \overline{Q_n} K$

logic diagram



c. SR to T

T	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	1	X	0
1	0	1	1	0
1	1	0	0	1

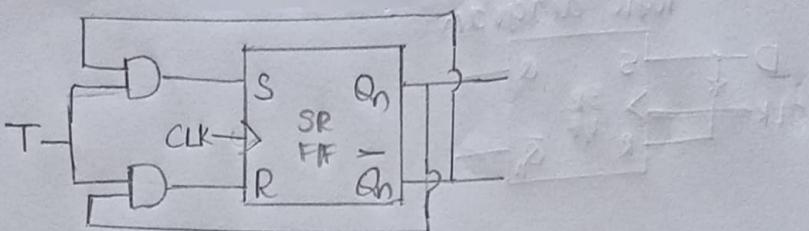
Q_n	S	
	0	1
0	0	1
1	X	0

$S = \overline{Q_n} T$

Q_n	R	
	0	1
0	X	0
1	0	1

$R = \overline{Q_n} T$

logic diagram



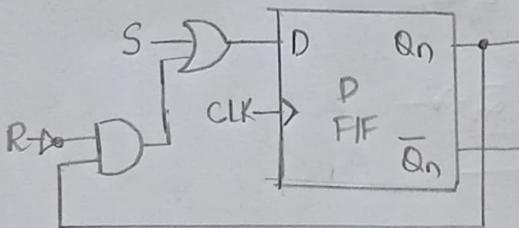
d. D to SR

S	R	Qn	Qn+1	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	X	X
1	1	Invalid	X	X
1	1	Invalid	X	X

Qn	SR	D
0	00	0
0	01	0
1	11	1
1	10	0

$$D = S + \bar{R} Q_n$$

logic diagram



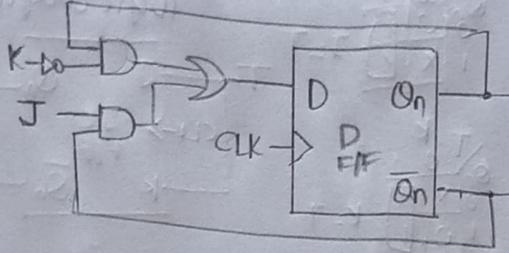
e. D to JK.

J	K	Qn	Qn+1	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

JK	D
00	0
01	1
10	1
11	0

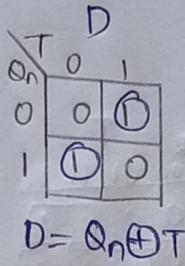
$$D = J\bar{Q}_n + Q_n K$$

logic diagram

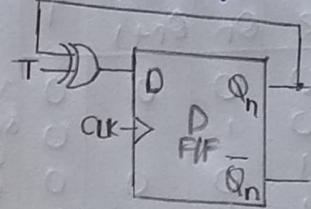


f) D to T

T	Q _n	Q _{n+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

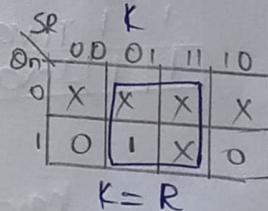
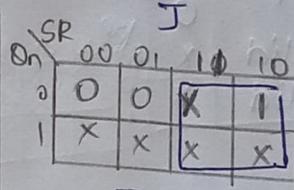


logic diagram

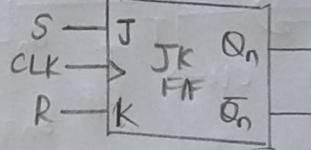


g) JK to SR

S	R	Q _n	Q _{n+1}	J	K
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	X	1
1	0	0	1	1	X
1	0	1	1	X	0
1	1	Invalid	X	X	
1	1	Invalid	X	X	

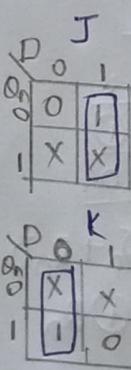


logic diagram



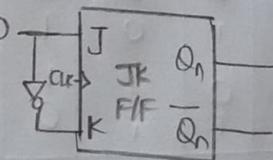
h) JK to D

D	Q _n	Q _{n+1}	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0



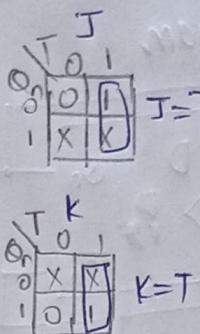
$K = \bar{D}$

logic diagram

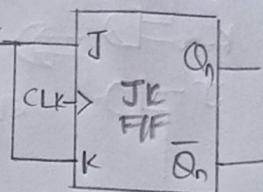


i) JK to T

T	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

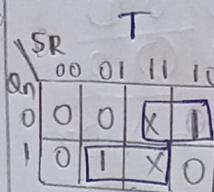


logic diagram



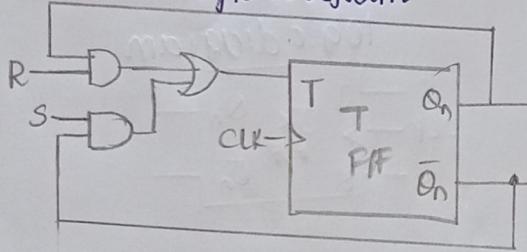
j) T to SR

S	R	Q_n	Q_{n+1}	T
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	Invalid	X	
1	1	Invalid	X	



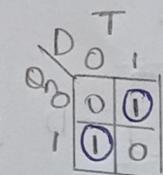
$$T = \bar{Q}_n S + Q_n R$$

logic diagram



k) T to D

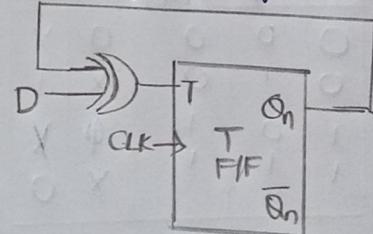
D	Q_n	Q_{n+1}	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0



$$T = D \bar{Q}_n + Q_n \bar{D}$$

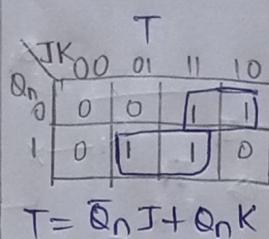
$$T = D \oplus Q_n$$

logic diagram

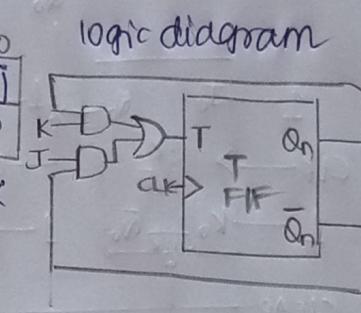


1. T to JK

J	K	On	OnH	T
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1



$$T = \bar{Q}_n J + Q_n K$$

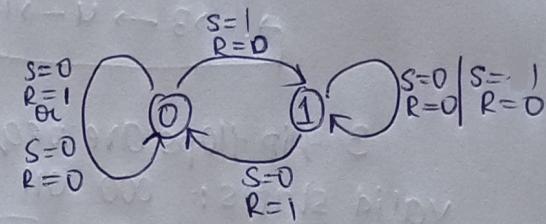


Moderate level Questions

1. Draw the state transition diagram of SR flip flop.

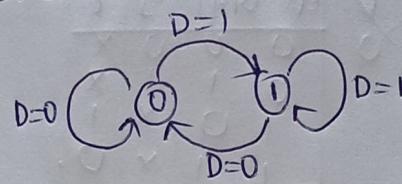
Truth table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	Invalid
1	1	1	Invalid



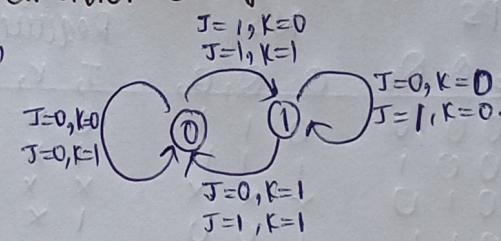
2. Draw the state transition diagram of D FF.

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1



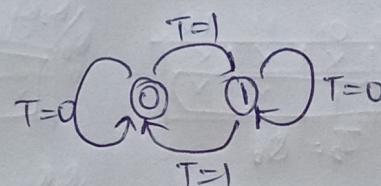
3. Draw the state transition diagram JK FF.

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

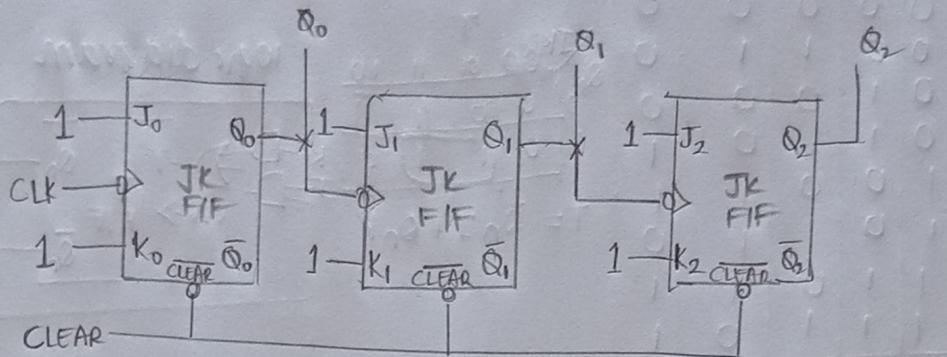


4. Draw the state transition diagram of T FF.

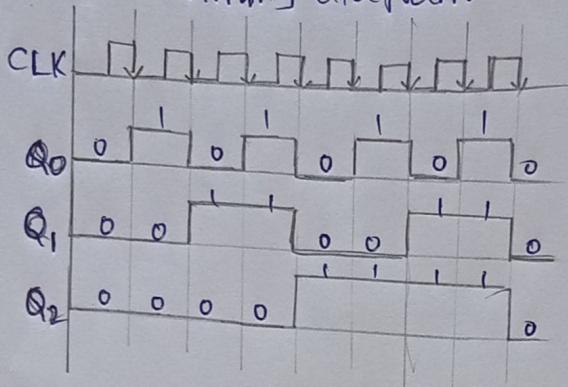
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0



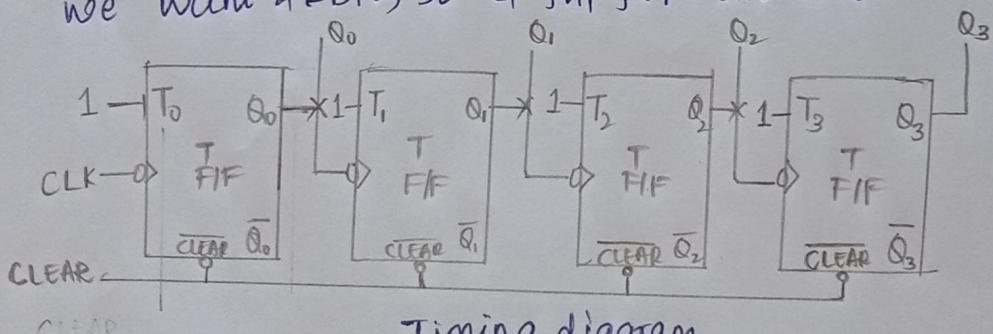
5. Design a 3-bit asynchronous up counter using JK flip flop.
we want 3-bit, so we use 3 flip flops.



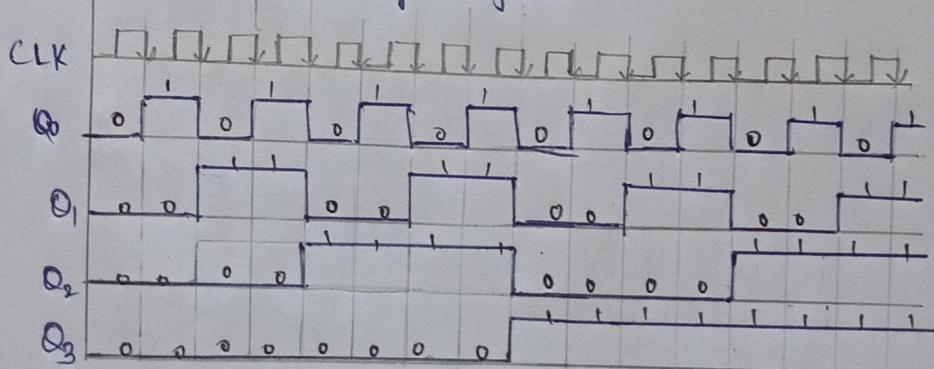
Timing diagram



6. Design 4-bit asynchronous up counter using T flip flop.
we want 4-bit, so 4 flip flops are used.



Timing diagram



7. Design a MOD-5 asynchronous counter using JK flip flop

MOD-5 :- It will have 5 values count

$(5)_D = (101)_2 \Rightarrow$ It is a 3 bit counter
count values for 3 bit are :-

000 001 010 011 100 101 110 111

↓ Invalid states.

Initial value = 000

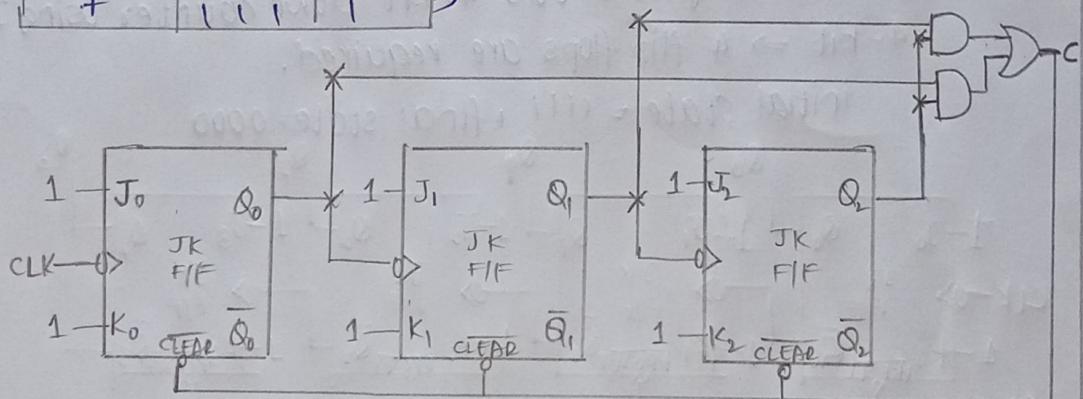
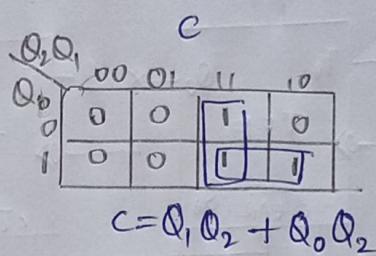
Final value = 100

∴ It is 3-bit counter \Rightarrow It will have 3 flip flops.

Truth table

Pulse Number	States $Q_2 Q_1 Q_0$	controller C
0	000	0
1	001	0
2	010	0
3	011	0
4	100	0
5	101	1
6	110	1
7	111	1

↓ Invalid states.



8. Design a MOD-6 asynchronous counter using T flip flop.

MOD-6 :- It will have 6 count values.

$(6)_D = (110)_2 \Rightarrow$ It is a 3-bit counter
count values of 3 bit are :-

000 001 010 011 100 101 110 111

↓ Invalid states

Initial value = 000

Final value = 101

∴ It is a 3-bit counter \Rightarrow 3 flip flops are required.

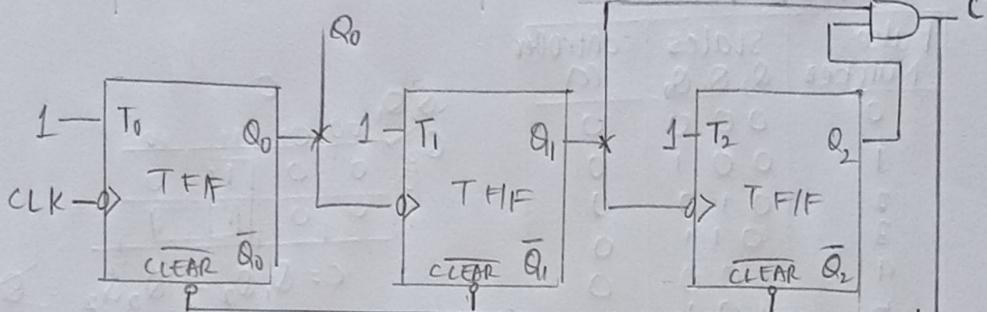
Truth table

Pulse number	$Q_2 Q_1 Q_0$	controlled (C)
0	0 0 0	0
1	0 0 1	0
2	0 1 0	0
3	0 1 1	0
4	1 0 0	0
5	1 0 1	0
6	1 1 0	1
7	1 1 1	1

$Q_2 Q_1$	00	01	11	10
Q_0	0	0	1	0
C	0	0	1	0

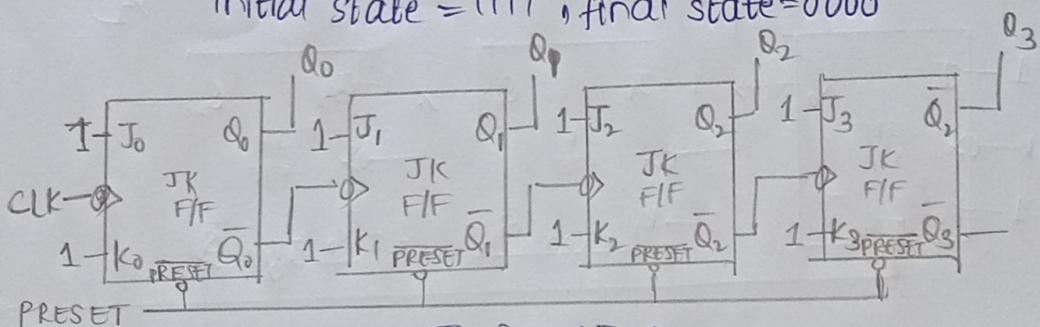
$$C = Q_1 Q_2$$

? Invalid states

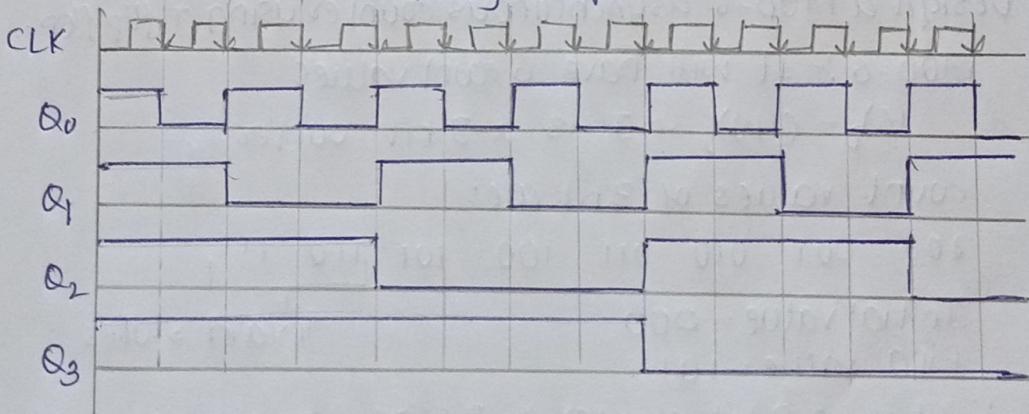


9. Design an asynchronous 4-bit down counter using JK flip-flop.
4-bit \Rightarrow 4 flip flops are required.

initial state = 1111, final state = 0000



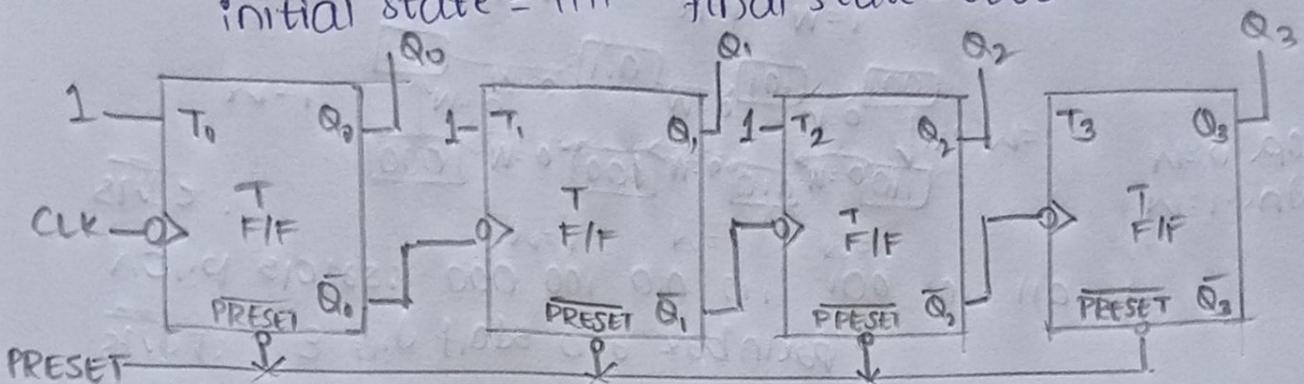
Timing diagram



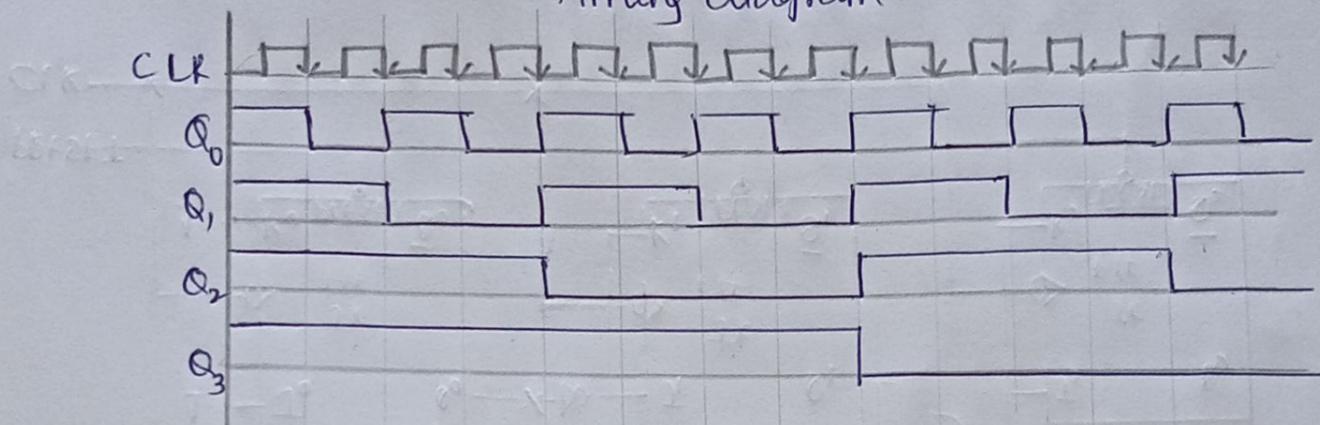
10. Design an asynchronous 4-bit down counter using T flip flop.

4 bit \Rightarrow 4 flip flops are required.

initial state = 1111 final state = 0000.

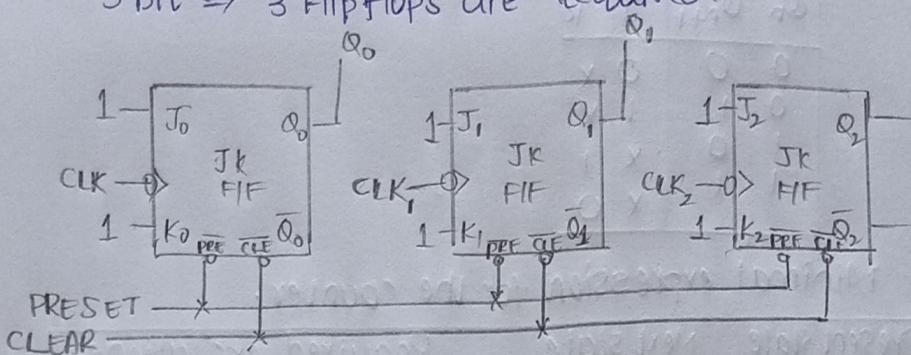


Timing diagram



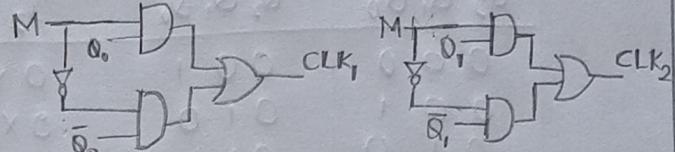
11. Design a 3-bit asynchronous up-down counter using JK flip flop.

3 bit \Rightarrow 3 Flip flops are required.



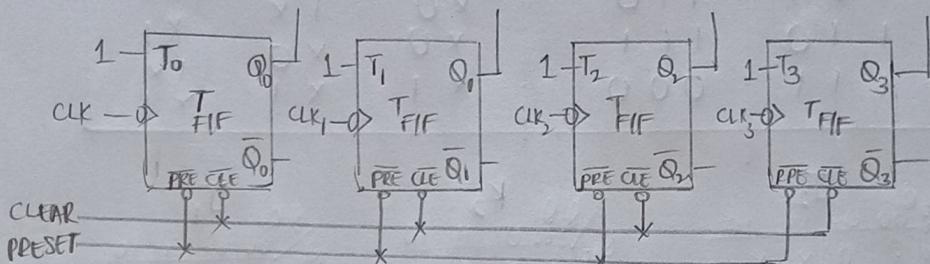
$M=1 \rightarrow$ upcounter

$M=0 \rightarrow$ downcounter



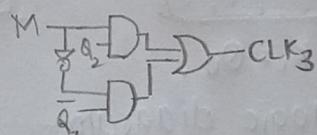
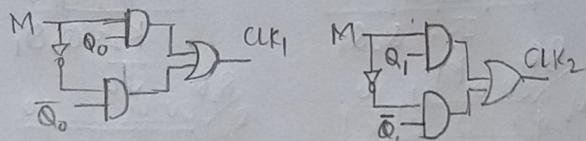
12. Design an asynchronous 4-bit up-down counter using T flip flop.

4 bit \Rightarrow 4 flip flops are required



$M=1 \rightarrow$ upcounter

$M=0 \rightarrow$ down counter

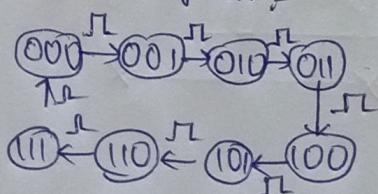


13. Design a synchronous 3-bit up counter using JK flip flop.

Step 1: 3 flip flops are required.

Valid states:- 000 001 010 011 100 101 110 111

Step 2: State diagram:-



Initial state=000

Final state=111

Step 3:- Excitation table of JK FF

Qn	Qn+1	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step 4:- Minimal expression for the counter.

Present state $Q_2\ Q_1\ Q_0$	Next state $Q_2\ Q_1\ Q_0$	Required excitations		
		$J_2\ K_2$	$J_1\ K_1$	$J_0\ K_0$
0 0 0	0 0 1	0 X	0 X	1 X
0 0 1	0 1 0	0 X	1 X	X 1
0 1 0	0 1 1	0 X	X 0	1 X
0 1 1	1 0 0	1 X	X 1	X 1
1 0 0	1 0 1	X 0	0 X	1 X
1 0 1	1 1 0	X 0	1 X	X 1
1 1 0	1 1 1	X 0	X 0	1 X
1 1 1	0 0 0	X 1	X 1	X 1

$Q_2\ Q_1\ Q_0$	J_2
0 0 0	0 0 X X
1 0 0	1 X X X

$$J_2 = Q_0 Q_1$$

$$K_1 = Q_0$$

$Q_2\ Q_1\ Q_0$	K_2
0 0 0	X X 0 0
1 0 0	X X 1 0

$$K_2 = Q_0 Q_1$$

$Q_2\ Q_1\ Q_0$	J_0
0 0 0	1 1 1 1

$$J_0 = 1$$

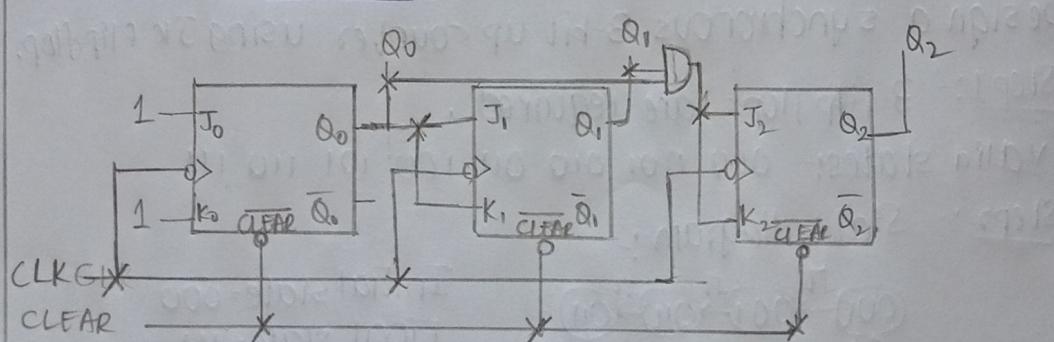
$Q_2\ Q_1\ Q_0$	J_1
0 0 0	0 0 X X 0
1 1 0	1 X X X 1

$$J_1 = Q_0$$

$Q_2\ Q_1\ Q_0$	K_0
0 0 0	X X X X

$$K_0 = 1$$

Step 5:- logic diagram

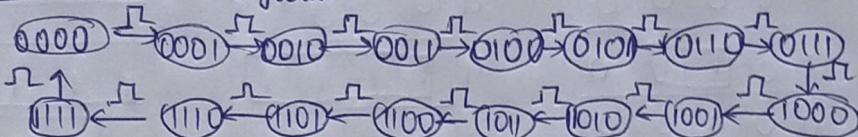


14. Design a synchronous 4-bit up counter using T flip flop.

Step 1: 4 flip flops are required.

Valid states:- 0000 0001 0010 0011 0100 0101 0110 0111
1000 1001 1010 1011 1100 1101 1110 1111

Step 2: State diagram:-



Initial state = 0000 ; Final state = 1111

Step 3: Excitation table of T flip flop:-

Q _n	Q _{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Step 4: Obtain the minimal expression for the counter.

PS Q ₃ Q ₂ Q ₁ Q ₀	NS Q ₃ Q ₂ Q ₁ Q ₀	Required excitations T ₃ T ₂ T ₁ T ₀
0 0 0 0	0 0 0 1	0 0 0 1
0 0 0 1	0 0 1 0	0 0 1 1
0 0 1 0	0 0 1 1	0 0 0 1
0 0 1 1	0 1 0 0	0 1 1 1
0 1 0 0	0 1 0 1	0 0 0 1
0 1 0 1	0 1 1 0	0 0 1 1
0 1 1 0	0 1 1 1	0 0 0 1
0 1 1 1	1 0 0 0	1 1 1 1
1 0 0 0	1 0 0 1	0 0 0 1
1 0 0 1	1 0 1 0	0 0 1 1
1 0 1 0	1 0 1 1	0 0 0 1
1 0 1 1	1 1 0 0	0 1 1 1
1 1 0 0	1 1 0 1	0 0 0 1
1 1 0 1	1 1 1 0	0 0 1 1
1 1 1 0	1 1 1 1	0 0 0 1
1 1 1 1	0 0 0 0	1 1 1 1

		T ₃				
		Q ₃ Q ₂	00	01	11	10
Q ₁ Q ₀		00	0	0	0	0
01		0	0	0	0	0
11		0	1	1	0	0
10		0	0	0	0	0

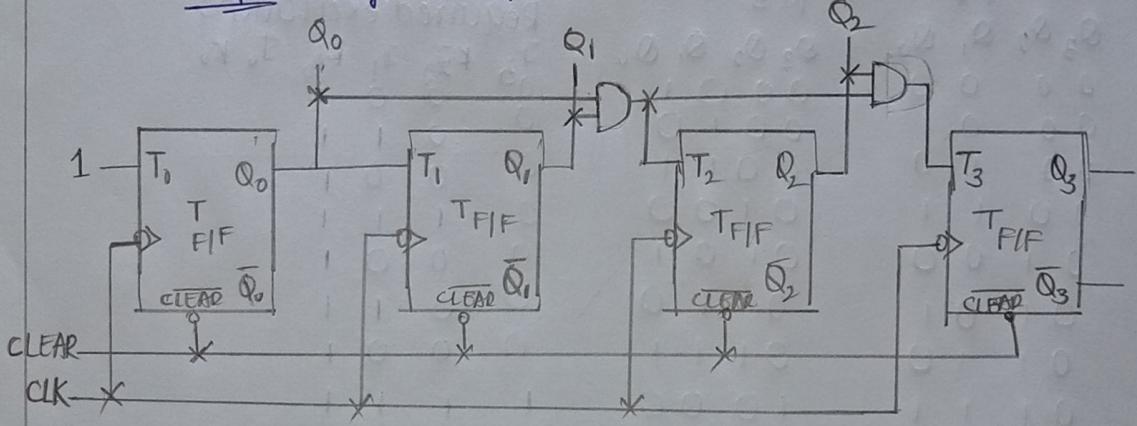
		T ₂				
		Q ₃ Q ₂	00	01	11	10
Q ₁ Q ₀		00	0	0	0	0
01		0	0	0	0	0
11		1	1	1	1	0
10		0	0	0	0	0

		T ₁				
		Q ₃ Q ₂	00	01	11	10
Q ₁ Q ₀		00	0	0	0	0
01		1	1	1	1	1
11		1	1	1	1	1
10		0	0	0	0	0

		T ₀				
		Q ₃ Q ₂	00	01	11	10
Q ₁ Q ₀		00	1	1	1	1
01		1	1	1	1	1
11		1	1	1	1	1
10		1	1	1	1	1

$$T_0 = 1$$

Step 5:- logic diagram



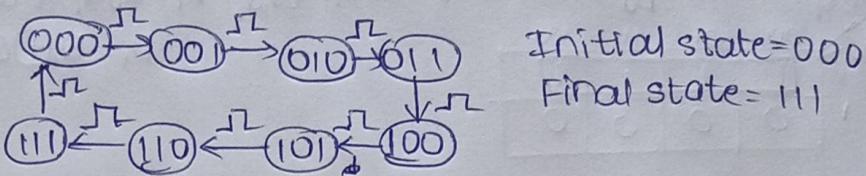
15. Design a synchronous 3-bit upcounter using D flipflop.

Step 1:- 3 flip flops are required.

Valid states are:-

000 001 010 011 100 101 110 111

Step 2:- State diagram:-



Step 3:- Excitation table of D flip flop:-

PS(Q_n)	NS(Q_{n+1})	D
0	0	0
0	1	1
1	0	0
1	1	1

Step 4:- Minimal expression for the counter.

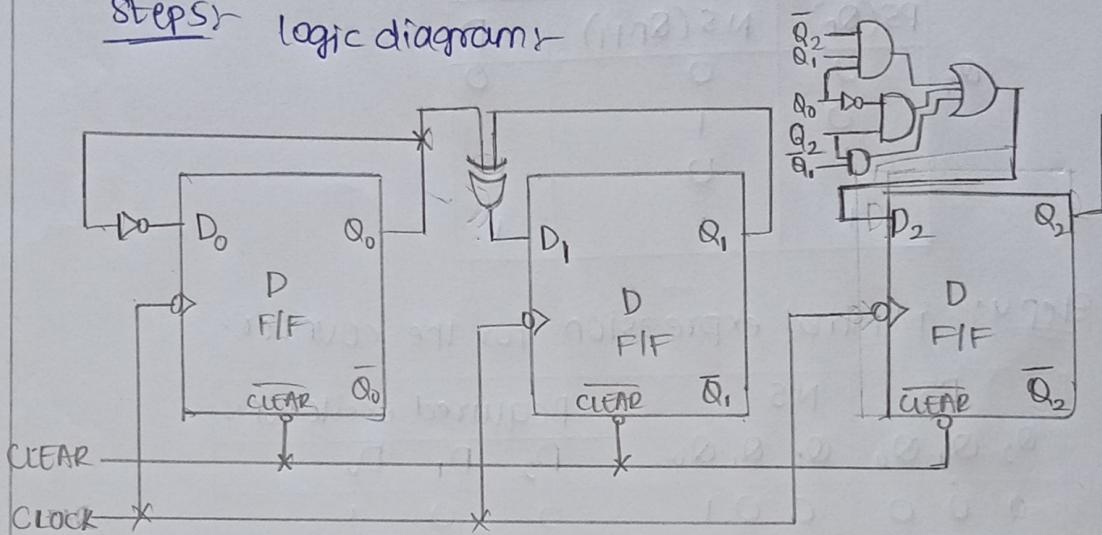
PS $Q_2\ Q_1\ Q_0$	NS $Q_2\ Q_1\ Q_0$	Required excitations		
		D_2	D_1	D_0
0 0 0	0 0 1	0	0	1
0 0 1	0 1 0	0	1	0
0 1 0	0 1 1	0	1	1
0 1 1	1 0 0	1	0	0
1 0 0	1 0 1	1	0	1
1 0 1	1 1 0	1	1	0
1 1 0	1 1 1	1	1	1
1 1 1	0 0 0	0	0	0

D_2	D_1
$Q_0 Q_1$	$Q_0 Q_1$
00 01 11 10	00 01 11 10
0 0 1 1	0 1 1 0
1 0 0 1	1 0 0 1

D_0	$D_2 = \bar{Q}_0 Q_2 + Q_2 \bar{Q}_1 + \bar{Q}_2 Q_1 Q_0$	$D_1 = Q_0 \bar{Q}_1 + \bar{Q}_0 Q_1$
$Q_0 Q_1$	$Q_0 Q_1$	$Q_1 \oplus Q_0$
00 01 11 10	00 01 11 10	00 01 11 10
1 1 1 1	0 0 0 0	0 0 0 0
0 0 0 0		

$$D_0 = \bar{Q}_0$$

Step 1:- logic diagram :-

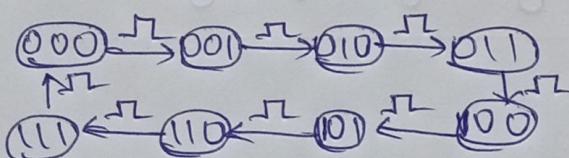


16. Design a synchronous 3-bit up counter using SR flip flop.

Step 1:- 3 Flip flops are required

Valid states :- 000 001 010 011 100 101 110 111

Step 2:- State diagram:-



initial state = 000
Final state = 111

Step 3:- Excitation table of SR flip flop.

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Step 4:- Minimal expressions for the counter.

PS	NS	Required excitations			
		S_2	R_2	S_1	R_1
0 0 0	0 0 1	0	X	0	X
0 0 1	0 1 0	0	X	1	0
0 1 0	0 1 1	0	X	X	0
0 1 1	1 0 0	1	0	0	1
1 0 0	1 0 1	X	0	0	X
1 0 1	1 1 0	X	0	1	0
1 1 0	1 1 1	X	0	X	1
1 1 1	0 0 0	0	1	0	1

$Q_2 Q_1$		S_2
Q_0	00 01 11 10	
0	0 0 X X	
1	0 1 0 X	

$$S_2 = \overline{Q}_2 Q_1 Q_0$$

$Q_2 Q_1$		S_1
Q_0	00 01 11 10	
0	0 0 X X	
1	1 0 0 1	

$$S_1 = \overline{Q}_1 Q_0$$

$Q_2 Q_1$		S_0
Q_0	00 01 11 10	
0	1 1 1 1	
1	0 0 0 0	

$$S_0 = \overline{Q}_0$$

$Q_2 Q_1$		R_2
Q_0	00 01 11 10	
0	X X 0 0	
1	X 0 1 0	

$$R_2 = Q_2 Q_1 Q_0$$

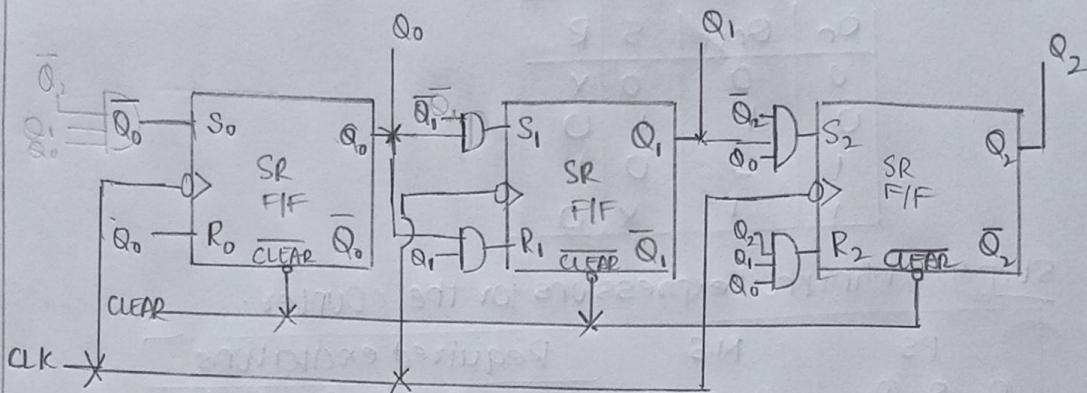
$Q_2 Q_1$		R_1
Q_0	00 01 11 10	
0	X 0 0 X	
1	0 1 1 0	

$$R_1 = Q_1 Q_0$$

$Q_2 Q_1$		R_0
Q_0	00 01 11 10	
0	0 0 0 0	
1	1 1 1 1	

$$R_0 = Q_0$$

Step 5: logic diagram

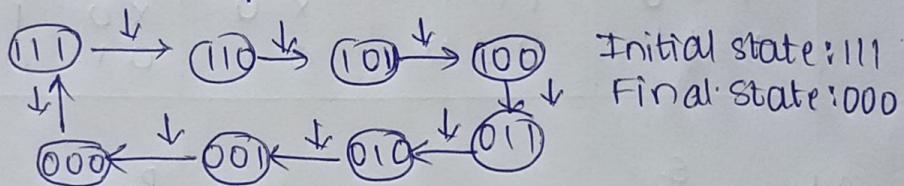


17. Design a synchronous 3-bit down counter using JK flip flop

Step 1: 3 flip flops are required.

Valid States:- 000 001 010 011 100 101 110 111

Step 2: State diagram



Step 3: Excitation table of JK flip flop.

Qn	Qn+1	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step 4: Minimal expressions for the counter.

PS	NS	Excitation required
Q ₂ Q ₁ Q ₀	Q ₂ Q ₁ Q ₀	J ₂ K ₂ J ₁ K ₁ J ₀ K ₀
1 1 1	1 1 0	X O X O X I
1 1 0	1 0 1	X O X I I X
1 0 1	1 0 0	X O O X X I
1 0 0	0 1 1	X O 1 X I X
0 1 1	0 1 0	O X X O X I
0 1 0	0 0 1	O X X I I X
0 0 1	0 0 0	O X O X X I
0 0 0	1 1 1	I X I X I X

Q_0, Q_1	J_2			
	00	01	11	10
0	1	0	X	X
1	0	0	X	X

$$J_2 = \overline{Q}_0 \overline{Q}_1$$

Q_0, Q_1	J_1			
	00	01	11	10
0	1	X	X	1
1	0	X	X	0

$$J_1 = \overline{Q}_0$$

Q_0, Q_1	J_0			
	00	01	11	10
0	1	1	1	1
1	X	X	X	X

$$J_0 = 1$$

Q_0, Q_1	K_2			
	00	01	11	10
0	X	X	0	1
1	X	X	0	0

$$K_2 = \overline{Q}_0 \overline{Q}_1$$

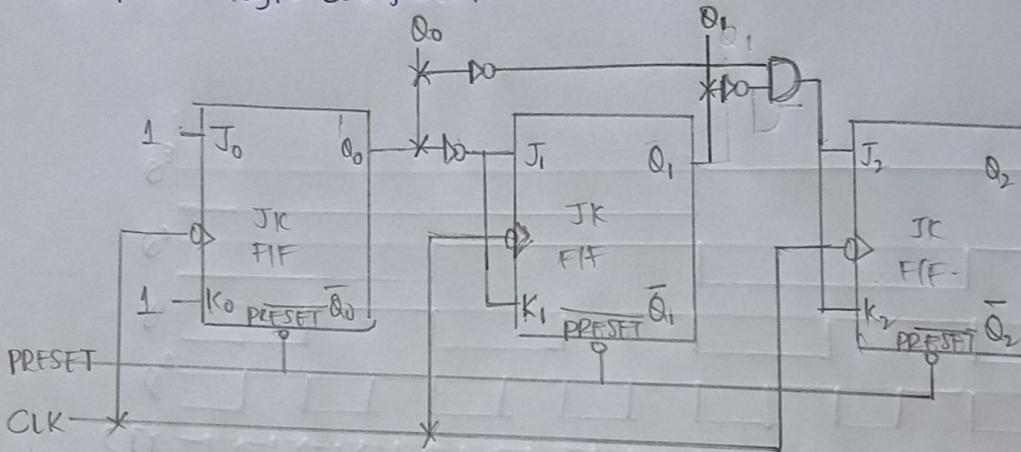
Q_0, Q_1	K_1			
	00	01	11	10
0	X	1	1	X
1	X	0	0	X

$$K_1 = \overline{Q}_0$$

Q_0, Q_1	K_0			
	00	01	11	10
0	X	X	X	X
1	1	1	1	1

$$K_0 = 1$$

Step 5:- logic diagram,

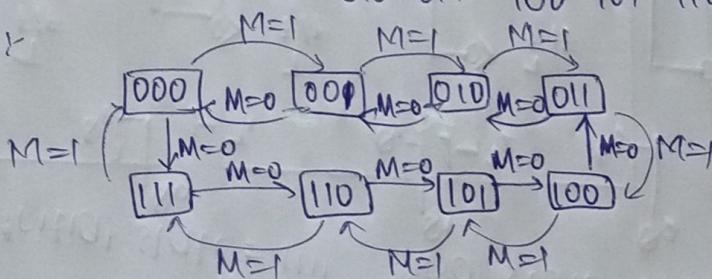


18. Design a synchronous 3-bit up down counter using JK flip flop

Step 1) 3 flip flops are required.

Valid states:- 000 001 010 011 100 101 110 111

Step 2)



$M=1 \rightarrow$ Upcounter
 $M=0 \rightarrow$ Downcounter

Step 3: Excitation table of JK FF

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

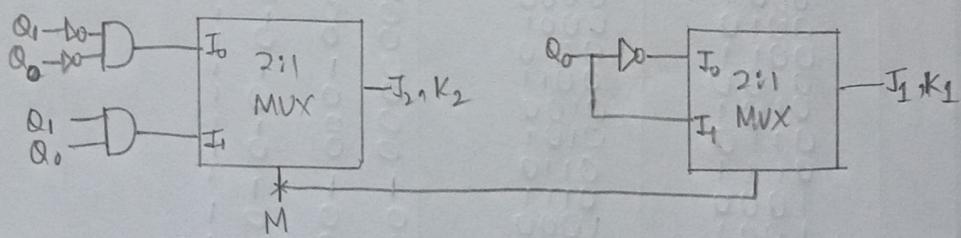
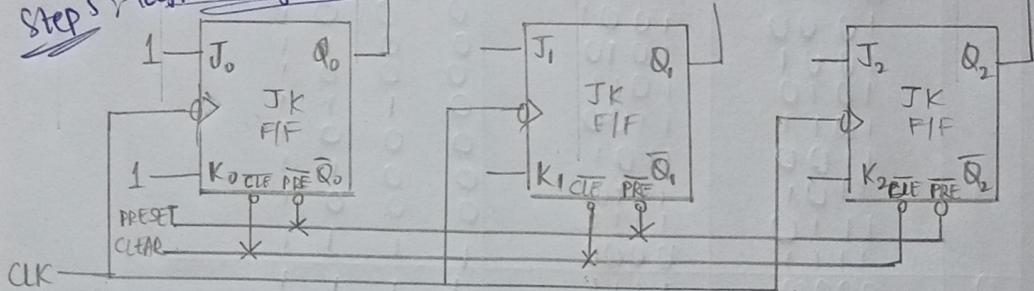
Step 4:

M	PS			NS			Required excitation					
	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0
1	0	0	0	0	0	1	0	X	0	X	0X	1X
1	0	0	1	0	1	0	0	X	0	X	1X	X1
1	0	1	0	0	1	1	0	X	0	X	X0	1X
1	0	1	1	1	0	0	1	X	1	X	X1	X1
1	1	0	0	1	0	1	X	0	X	0	0X	1X
1	1	0	1	1	1	0	X	0	1	X	1X	X1
1	1	1	0	1	1	1	X	0	X	0	X0	1X
1	1	1	1	0	0	0	X	1	X	1	X1	X1
0	0	0	0	1	1	1	1	X	1	X	1X	1X
0	0	0	1	0	0	0	0	X	0	X	0X	X1
0	0	1	0	0	0	1	0	X	0	X	X1	1X
0	0	1	1	0	1	0	0	1	0	1	X0	X1
0	1	0	0	0	1	1	X	1	1	X	1X	X1
0	1	0	0	1	1	1	X	1	0	1	0X	X1
0	1	0	1	0	0	0	X	0	0	X	X1	1X
0	1	1	0	1	0	1	X	0	1	X	0X	1X
0	1	1	1	0	1	0	X	0	0	X	X1	1X

up counter :- M=1 $J_2 = K_2 = Q_1 Q_0$; $J_1 = K_1 = Q_0$; $J_0 = K_0 = 1$

down counter - M=0 $J_2 = K_2 = \bar{Q}_1 \bar{Q}_0$; $J_1 = K_1 = \bar{Q}_0$; $J_0 = K_0 = 1$

Step 5: logic diagram

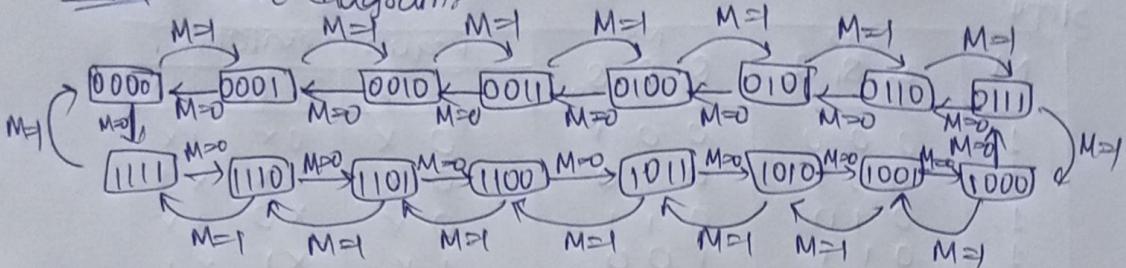


19. Design a synchronous 4 bit up-down counter using T flip flop.

Step 1: 4 flip flops are required

Valid states: 0000 0001 0010 0011 0100 0101 0110 0111
1000 1001 1010 1011 1100 1101 1110 1111

Step 2: State diagram



Step 3: Excitation table for T flip flop.

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Step 4:

M	PS			NS			Required excitations			
	$Q_3 Q_2 Q_1 Q_0$			$Q_3 Q_2 Q_1 Q_0$			T_3	T_2	T_1	T_0
1	0000			0001			0	0	0	1
	0001			0010			0	0	1	1
	0010			0011			0	0	0	1
	0011			0100			0	1	1	1
	0100			0101			0	0	0	1
	0101			0110			0	0	1	1
	0110			0111			0	0	0	1
	0111			1000			1	1	1	1
	1000			1001			0	0	0	1
	1001			1010			0	0	1	1
	1010			1011			0	0	0	1
	1011			1100			0	1	1	1
	1100			1101			0	0	0	1
	1101			1110			0	0	0	1
	1110			1111			0	0	0	1
	1111			0000			1	1	1	1
0	0000			1111			1	1	1	1
	0001			0000			0	0	0	1
	0010			0001			0	0	0	1
	0011			0010			0	0	0	1
	0100			0011			0	1	1	1
	0101			0100			0	0	0	1
	0110			0101			0	0	1	1
	0111			0110			0	0	0	1
	1000			0111			1	1	1	1
	1001			1000			0	0	0	1
	1010			1001			0	0	1	1
	1011			1010			0	0	0	1
	1100			1011			0	1	0	1
	1101			1100			0	0	0	1
	1110			1101			0	0	0	1
	1111			1110			0	0	0	1

		T ₃				
		Q ₃ Q ₂	00	01	11	10
Q ₁ Q ₀		00	0	0	0	0
01		0	0	0	0	0
11		0	1	1	0	0
10		0	0	0	0	0

$T_3 = Q_2 Q_1 Q_0$

		T ₂				
		Q ₃ Q ₂	00	01	11	10
Q ₁ Q ₀		00	0	0	0	0
01		0	0	0	0	0
11		1	1	1	1	0
10		0	0	0	0	0

$T_2 = Q_1 Q_0$

		T ₁				
		Q ₃ Q ₂	00	01	11	10
Q ₁ Q ₀		00	0	0	0	0
01		1	1	1	1	0
11		1	1	1	1	0
10		0	0	0	0	0

$T_1 = Q_0$

		T ₀				
		Q ₃ Q ₂	00	01	11	10
Q ₁ Q ₀		00	1	1	1	1
01		1	1	1	1	0
11		1	1	1	1	0
10		1	1	1	1	0

$T_0 = 1$

		T ₃				
		Q ₃ Q ₂	00	01	11	10
Q ₁ Q ₀		00	1	0	0	1
01		0	0	0	0	0
11		0	0	0	0	0
10		0	0	0	0	0

$T_3 = \bar{Q}_2 \bar{Q}_1 Q_0$

		T ₂				
		Q ₃ Q ₂	00	01	11	10
Q ₁ Q ₀		00	1	1	1	1
01		0	0	0	0	0
11		0	0	0	0	0
10		0	0	0	0	0

$T_2 = Q_1 \bar{Q}_0$

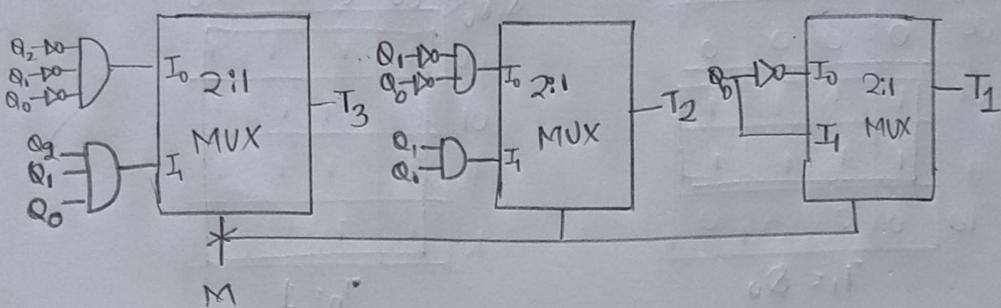
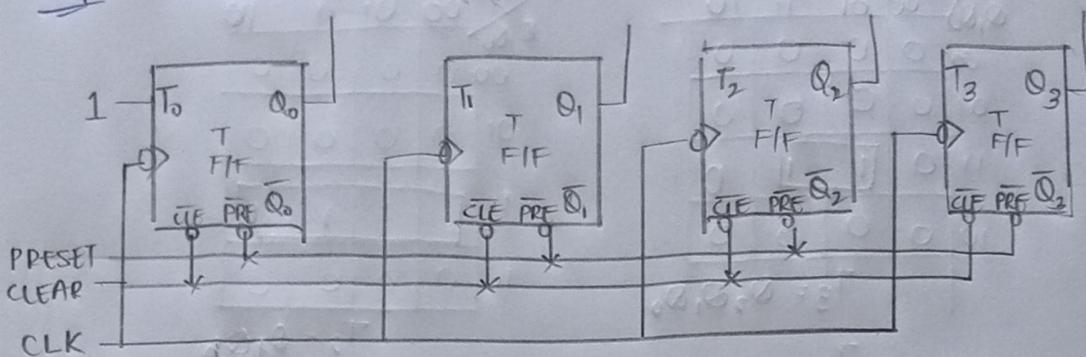
		T ₁				
		Q ₃ Q ₂	00	01	11	10
Q ₁ Q ₀		00	1	1	1	1
01		1	1	1	1	0
11		0	0	0	0	0
10		1	1	1	1	0

$T_1 = \bar{Q}_0$

		T ₀				
		Q ₃ Q ₂	00	01	11	10
Q ₁ Q ₀		00	1	1	1	1
01		1	1	1	1	0
11		1	1	1	1	0
10		1	1	1	1	0

$T_0 = 1$

Step 1: Logic diagram



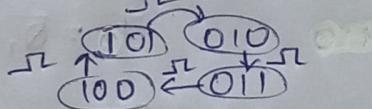
Ques. Design MOD-4 synchronous counter using JK flip flop starting from count '2'.

Step 1: $(4)_D = (100)_2 \Rightarrow 3$ flip flops are required.

Valid states:- 010 011 100 101

Invalid states:- 000 001 110 111

Step 2: State diagram



Initial state:- 010

Final state:- 101.

Step 3: Excitation table of JK flip flop.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step 4:- Minimal expressions for the counter.

PS	NS	Required excitations	C
$Q_2\ Q_1\ Q_0$	$Q_2\ Q_1\ Q_0$	$J_2\ K_2\ J_1\ K_1\ J_0\ K_0$	
0 0 0	X X X	X X X X X X	1
0 0 1	X X X	X X X X X X	1
0 1 0	0 1 1	0 X X 0 1 X 0	0
0 1 1	1 0 0	1 X X 1 X 1 0	0
1 0 0	1 0 1	X 0 0 X 1 X 0	0
1 0 1	0 1 0	X 1 1 X X 1	0
1 1 0	X X X	X X X X X X	1
1 1 1	X X X	X X X X X X	1

J_2

$Q_2\ Q_1$	00	01	11	10
0	X	0	X	X
1	X	1	X	X

$J_2 = Q_0$

J_1

$Q_2\ Q_1$	00	01	11	10
0	X	X	X	0
1	X	X	X	1

$J_1 = Q_0$

J_0

$Q_2\ Q_1$	00	01	11	10
0	X	1	X	1
1	X	X	X	X

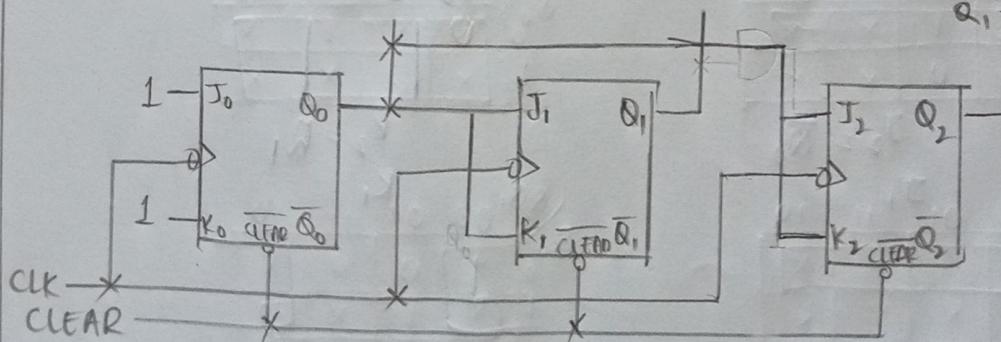
$J_0 = 1$

C

$Q_2\ Q_1\ C$	00	01	11	10
0	0	0	1	0
1	1	0	1	0

$$C = Q_2 Q_1 + \bar{Q}_2 \bar{Q}_1$$

$$Q_2 \rightarrow D_0 - C$$

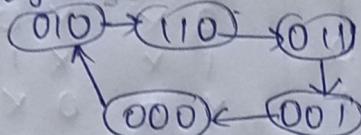


Q. Design a synchronous counter to generate arbitrary count sequence 2, 6, 3, 1, 0, 2, 6, 3, 1, ... using JK FF.

3 flip flops are required.

Valid states: - 010, 110, 011, 001, 000

State diagram:



Excitation table of JK FF

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Minimal expressions for the counters:

PS	NS	Excitation required
$Q_2 Q_1 Q_0$	$Q_2 Q_1 Q_0$	$J_2 \ K_2 \ J_1 \ K_1 \ J_0 \ K_0$
0 0 0	0 1 0	x 0 x 1 x 0 0
0 0 1	0 0 0	0 x 0 x x 1 0
0 1 0	1 1 0	1 x x 0 0 x 0
0 1 1	0 0 1	0 x x 1 x 0 0
1 0 0	x x x	x x x x x x 1
1 0 1	x x x	x x x x x x 1
1 1 0	0 1 1	x 1 x 0 1 x 0
1 1 1	x x x	x x x x x x 1

$Q_2 Q_1$	J_2
0 0	0 1
0 1	x x

$$J_2 = \bar{Q}_0$$

$Q_2 Q_1$	J_1
0 0	x x x x
0 1	x x x x

$$J_1 = \bar{Q}_0$$

$Q_2 Q_1$	K_2
0 0	x 1
0 1	x x

$$K_2 = Q_1$$

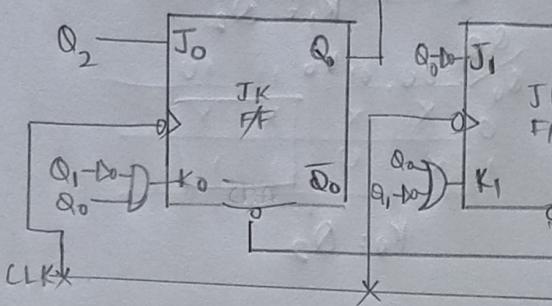
$Q_2 Q_1$	K_1
0 0	x 0
0 1	1 x

$$K_1 = Q_0 + \bar{Q}_1$$

		J ₀			
		00	01	11	10
Q ₂ , Q ₁	00	X	0	1	X
	1	X	X	X	X

$$J_0 = Q_2$$

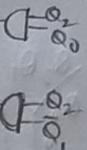
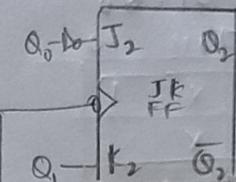
logic diagram:



		K ₀			
		00	01	11	10
Q ₂ , Q ₁	00	0	X	X	X
	1	1	1	0	X

$$K_0 = \bar{Q}_1 Q_0$$

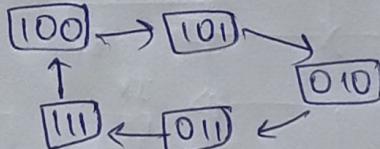
$$C = Q_2 Q_0 + Q_2 \bar{Q}_0$$



22. Design a synchronous counter to generate arbitrary count sequence 4, 5, 2, 3, 7, 4, 5, 2, ... using JKFF.
- 3 flip flops are required

Valid states: 100 101 010 011 111

state diagram:



Excitation table:

Q _n	Q _{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Minimal expressions for the counter:

PS	NS	Required excitation				C
		J ₂	K ₂	J ₁	K ₁	
0 0 0	X X X	X	X	X X	X X	1
0 0 1	X X X	X	X	X X	X X	1
0 1 0	0 1 1	0	X	X 0	1 X	0
0 1 1	1 1 1	1	X	X 0	X 0	0
1 0 0	1 0 1	X 0	0 X	1 X	0	0
1 0 1	0 1 0	X	1	1 X	X 1	0
1 1 0	X X X	X	X	X X	X X	1
1 1 1	1 0 0	X 0	X 1	X 1	X 1	0

$Q_2 Q_1$	00	01	J ₂	K ₂	10
Q ₂	X	0	X	X	00
Q ₁	0				
	X	1	X	X	

$$J_2 = Q_0$$

$Q_2 Q_1$	00	01	J ₁	K ₁	10
Q ₂	X	X	X	0	
Q ₁	0				
	X	X	X	1	

$$J_1 = Q_0$$

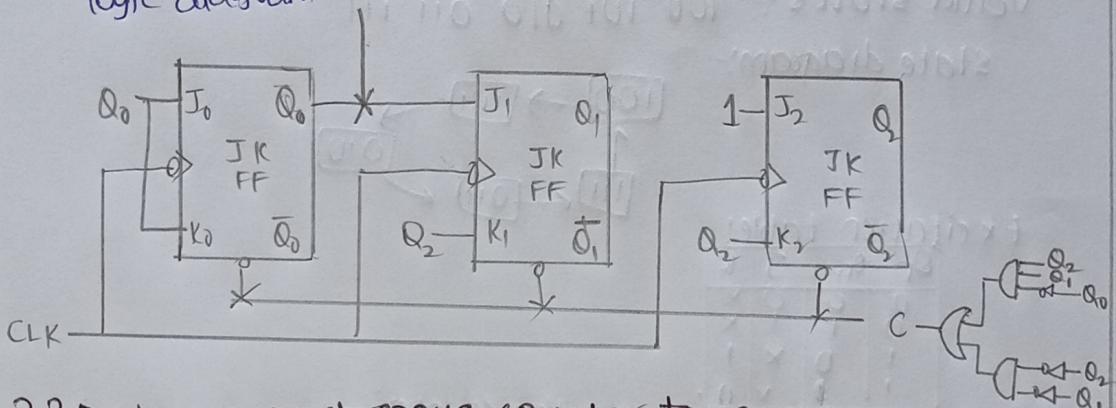
$Q_2 Q_1$	00	01	J ₀	K ₀	10
Q ₂	X	1	X	1	
Q ₁	0				
	X	X	X	X	

$$J_0 = 1$$

$Q_2 Q_1$	00	01	C	11	10
Q ₂	1	0	1	0	
Q ₁	1	0	0	0	

$$C = \overline{Q}_2 \overline{Q}_1 + Q_2 Q_1 \overline{Q}_0$$

logic diagram

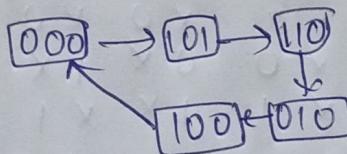


23. Design a synchronous counter to generate arbitrary count sequence 0, 5, 6, 2, 4, 0, 5, 6, ... using JK FF.

3 Flip flops are required,

Valid states → 000 101 110 010 100

State diagram



Excitation table

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Minimal expressions for the counter:

PS $Q_2 Q_1 Q_0$	NSR $Q_2' Q_1' Q_0'$	$J_2 \ K_2 \ J_1 \ K_1 \ J_0 \ K_0$	C
0 0 0	1 0 1	1 X 0 X 1 X 0	0
0 0 1	X X X	X X X X X X	1
0 1 0	1 0 0	1 X X X X X	0
0 1 1	X X X	X X X X X X	1
1 0 0	0 0 0	X 1 0 X 0 X	0
1 0 1	1 1 0	X 0 1 X X 1	0
1 1 0	0 1 0	X 1 X 0 0 X	0
1 1 1	X X X	X X X X X X	1

Q_2	J_2			
Q_0	00	01	11	10
0	T	1	X	X
1	X	X	X	X

$$J_2 = 1$$

Q_2	J_1			
Q_0	00	01	11	10
0	0	X	X	0
1	X	X	X	1

$$J_1 = Q_0$$

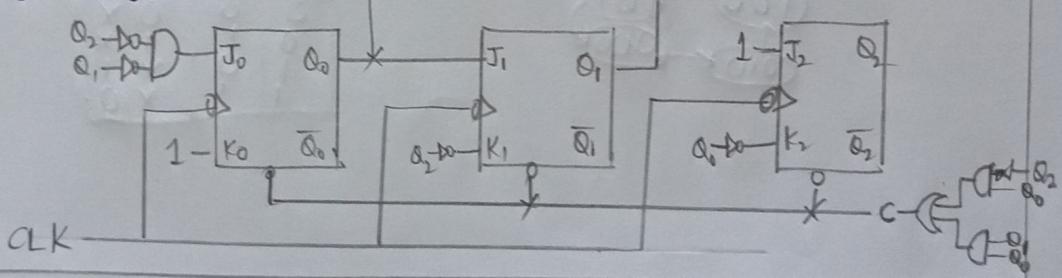
Q_2	J_0			
Q_0	00	01	11	10
0	1	0	0	0
1	X	X	X	X

$$J_0 = \bar{Q}_2 \bar{Q}_1$$

Q_2	C			
Q_0	00	01	11	10
0	0	0	0	0
1	1	1	1	0

$$C = \bar{Q}_2 Q_0 + Q_1 Q_0$$

Logic diagram

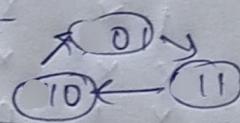


24. Design a synchronous counter to generate arbitrary count sequence 1, 3, 2, 1, 3, 2, ... using JK FF.

2 Flip flops are required.

Valid states: 01 10 11

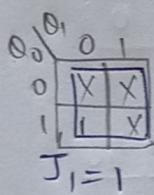
State diagram:



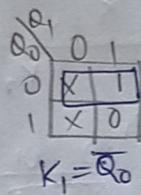
Excitation

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

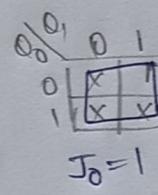
PS	NS	Excitation				c
$Q_1 Q_0$	$Q_1 Q_0$	J_1	K_1	J_0	K_0	
00	XX	X	X	XX	X	1
01	11	1	X	X	0	0
10	01	X	1	1	X	0
11	10	X	0	X	1	0



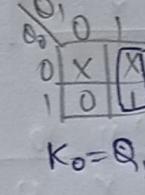
$$J_1 = 1$$



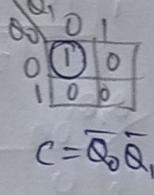
$$K_1 = \bar{Q}_0$$



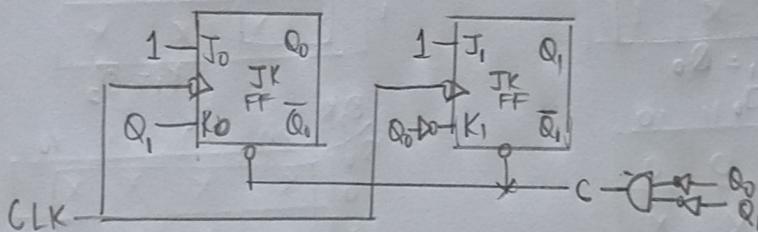
$$J_0 = 1$$



$$K_0 = Q_1$$



$$C = \bar{Q}_0 \bar{Q}_1$$

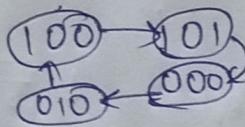


25. Design a synchronous counter to generate arbitrary count sequence 4, 5, 0, 2, 4, 5, 0, ... using JK FF.

3 Flip flops are required.

Valid state:- 100 101 000 010

State diagram:



Excitation table-

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Minimal expressions for the counter!-

PS	NS	excitation					C
$Q_2\ Q_1\ Q_0$	$Q_2\ Q_1\ Q_0$	$J_2\ K_2$	$J_1\ K_1$	$J_0\ K_0$	$I\ C$		C
0 0 0	0 1 0	0 X	1 X	0 X			0
0 0 1	X X X	X X	X X	X X			1
0 1 0	1 0 0	1 X	X 1	0 X			0
0 1 1	X X X	X X	X X	X X			1
1 0 0	1 0 1	X 0	0 X	1 X			0
1 0 1	0 0 0	X 1	0 X	X 1			0
1 1 0	X X X	X X	X X	X X			1
1 1 1	X X X	X X	X X	X X			1

$Q_2\ Q_1\ Q_0$	00	01	11	10
0	0	1	X	X
1	X	X	X	X

$$J_2 = Q_1$$

$Q_2\ Q_1\ Q_0$	00	01	11	10
0	X	X	X	0
1	X	X	X	1

$$K_2 = Q_0$$

$Q_2\ Q_1\ Q_0$	00	01	11	10
0	1	X	X	0
1	X	X	X	0

$$J_1 = \bar{Q}_2$$

$Q_2\ Q_1\ Q_0$	00	01	11	10
0	X	1	X	X
1	X	X	X	X

$$K_1 = 1$$

$Q_2\ Q_1\ Q_0$	00	01	11	10
0	0	0	X	1
1	X	X	X	X

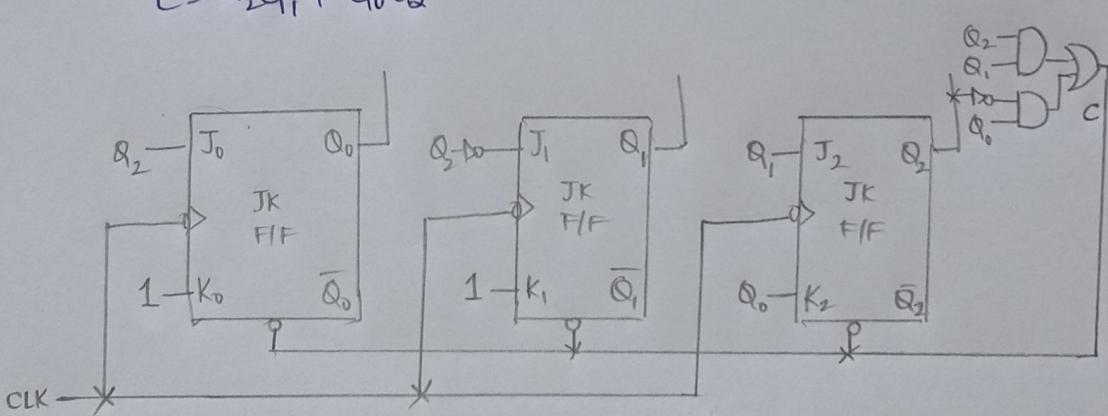
$$J_0 = Q_2$$

$Q_2\ Q_1\ Q_0$	00	01	11	10
0	X	X	X	X
1	X	X	X	1

$$K_0 = 1$$

$Q_2\ Q_1\ Q_0$	00	01	11	10
0	0	0	1	0
1	1	1	1	0

$$C = Q_2 Q_1 + Q_0 \bar{Q}_2$$



High level Questions:

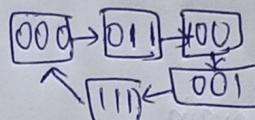
- i. Design a synchronous counter which regenerates the count pattern shown below.

$$[0 \rightarrow 3 \rightarrow 4 \rightarrow 1 \rightarrow 7]$$

3 flip flops are required.

Valid states:- 000 011 100 001 111

State diagram:-



Excitation table:- (I am using JK FF)

Q_0	Q_{nt1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Obtaining minimal expressions:-

PS	NS	Required excitation	C
$Q_2 Q_1 Q_0$	$Q_2 Q_1 Q_0$	$J_2 K_2 J_1 K_1 J_0 K_0$	
000	011	0 X 1 X 1 X	0
001	111	1 X 1 X X 0	0
010	X X X	X X X X X X	1
011	100	1 X X 1 X 1	0
100	001	X 1 0 X 1 X	0
101	X X X	X X X X X X	1
110	X X X	X X X X X X	1
111	000	X 1 X 1 X 1	0

Q_2	Q_1	Q_0	00	01	11	10
0	0	0	0	X	X	X
1	1	1	1	X	X	X

$$J_2 = Q_0$$

Q_2	Q_1	Q_0	00	01	11	10
0	0	0	X	X	X	1
1	1	1	X	X	1	X

$$K_2 = 1$$

Q_2	Q_1	Q_0	00	01	11	10
0	0	0	1	X	X	0
1	1	1	1	X	X	X

$$J_1 = Q_2$$

Q_2	Q_1	Q_0	00	01	11	10
0	0	0	X	X	X	X
1	1	1	X	X	X	X

$$K_1 = 1$$

Q_2	Q_1	Q_0	00	01	11	10
0	0	0	1	X	X	1
1	1	1	X	X	X	X

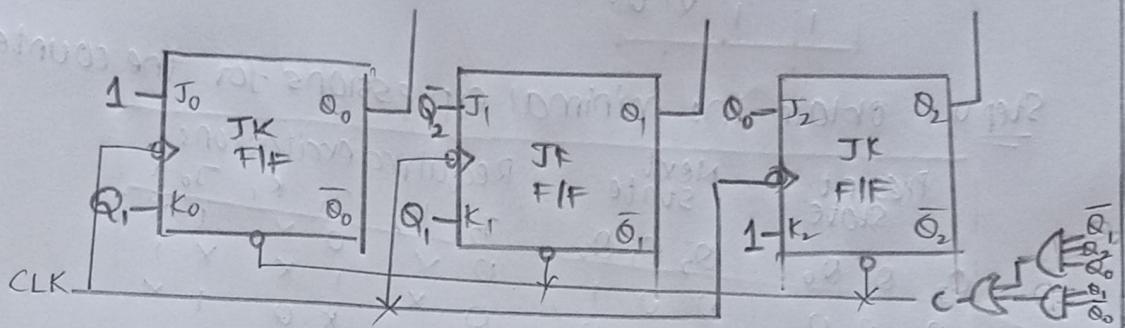
$$J_0 = 1$$

Q_2	Q_1	Q_0	00	01	11	10
0	0	0	X	X	X	X
1	1	1	0	1	1	X

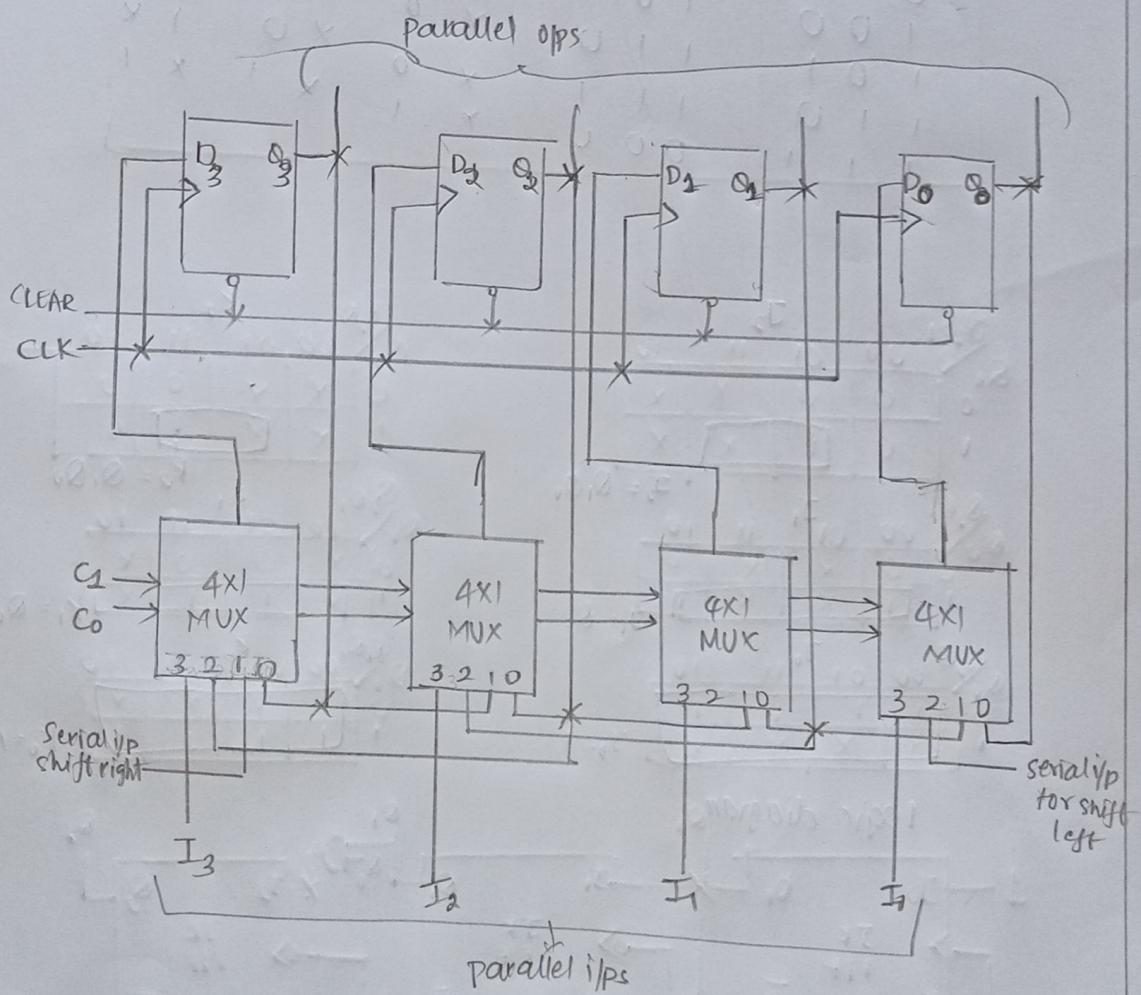
$$K_0 = Q_1$$

	00	01	11	10
0	0	1	1	0
1	0	0	0	1

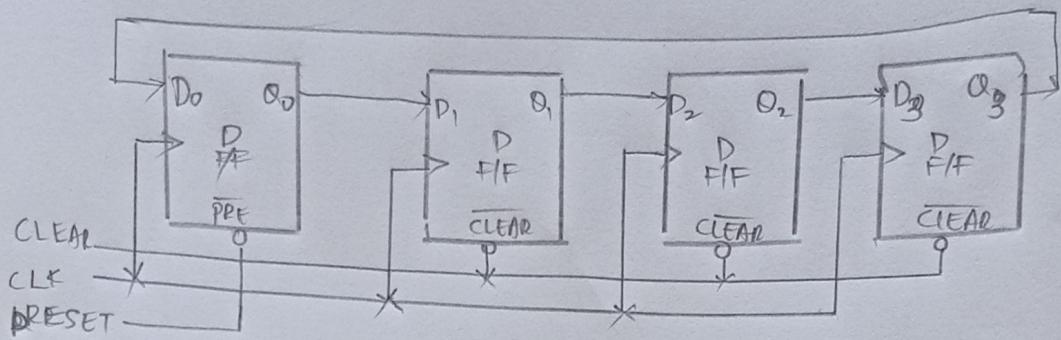
$$C = Q_1 \bar{Q}_0 + Q_2 \bar{Q}_1 Q_0$$



2. Design a 4-bit universal shift register using multiplexers



3. Design a 4-bit counter using D flip flop.



4. Design a 4-bit johnson counter using DFIF.

