**Visvesvaraya National Institute of Technology Nagpur**
**Department of Electronics and Communication Engineering**
**Mid-Semester Examination, Odd Session 2024-25**
**V Semester B. Tech. ECE**

**Course:** Computer Architecture and Organization | **Course Code:** CSL311 {Elective}
**Slot:** A | **Date of Exam:** 26-09-2024
**Max. Marks:** 30 | **Time:** 10:00 - 11:30 am

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**Instructions**:

- All questions are compulsory. **There is a choice in Question 3.**
- Assume suitable data wherever required
- Draw neat labelled diagrams wherever suitable

| Ques. No. | Question | Marks | CO |
|---|---|---|---|
| Q.1(a) | State the significance of memory hierarchy in computer architecture.<br>Imagine you are storing a video game application in your computer and you want to play it. With this assumption, answer the following questions:<br>i. In which type of memory does the bootable information reside and why?<br>ii. Which memory component contains the video game application and why?<br>iii. Once you click on the video game to start the application, where will it be loaded and why? | [2M]<br>[3M] | CO1<br>CO2 |
| Q.1(b) | Justify the significance of functional units of a digital computer with a neat sketch. Elaborate the components of the I/O unit and processor unit in detail. | [3M]<br>[3M] | CO1<br>CO2 |
| Q. 2 | List and explain the steps involved in the execution of a complete instruction cycle. Illustrate the execution of the following instruction<br>JUMP LABEL where LABEL = current_address + 30 | [3M]<br>[2M] | CO3 |
| Q. 3 | Assume that only the following two instructions are available to transfer data between the memory and general-purpose registers $R_i$<br>LOAD LOC, Ri<br>*and*<br>STORE Ri, LOC<br>Give a short sequence of machine instructions considering the following task: "Add the contents of memory location A to those of location B, and place the answer in location C."<br>Do not destroy the contents of either locations A or B. | [5M] | CO2 |

**OR**

Q. 4 A company is developing an embedded system for real-time signal processing. The system uses a 32-bit processor with 4 KB of cache memory, divided into 64-byte blocks. The processor runs a loop-based algorithm to process a large array of signal samples stored in main memory. The array is 64 KB in size, and each element is 4 bytes. — 04 — CO3

The algorithm processes the array using the following loop:

```
for (int i = 0; i < N; i++) {
        result[i] = signal[i] + signal[i + 1];
}
```

The company notices that despite having cache memory, the algorithm suffers from frequent cache misses, leading to performance bottlenecks.

In the context of the given loop and hardware setup, answer the following:

i. How and where does spatial locality occur in this code?

ii. How and where does temporal locality occur in this code?

Q. 5 Explain the correlation between cache hit rate and virtual memory in a computer system. Address the following points: — 06 — CO3

i. How does a high cache hit rate affect the performance of a system using virtual memory?

ii. What are the performance implications when the cache frequently misses in a virtual memory system?

Q. 6 Consider the given code segment in a typical 5-stage pipelined processing system involving the stages IF, ID, EX, MEM, WB: — 05 — CO5

```
LOAD R1, 0(R2);
ADD R3, R1, R4;
SUB R5, R3, R6;
```

i. Identify the type(s) of data hazard(s) present in the given code.

ii. Explain the cause of the identified hazard(s) with reference to the specific instructions involved.

iii. Suggest technique(s) to mitigate the identified hazard(s) in a pipelined processor.

Q. 7 Consider a process with 3-page frames and the following sequence of page references: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5 — 05 — CO3 CO5

i. Calculate the number of page faults using First-In-First-Out page replacement policy.

ii. Calculate the number of page faults using Least Recently Used page replacement policy.

iii. Explain which policy performs better than the other in this case & why?

Q. 8 What is the significance of cache-mapping techniques? Analyse the key differences between direct-mapped and set-associative cache organizations on the basis of block placement, conflict misses, need for block replacement policy. — 05 — CO4 CO5

**OR**

Q. 9 A multimedia company is developing a high-definition video streaming app, transferring large video files between the disk drive and main memory. Initially using CPU-controlled I/O, they face slow transfer rates and high CPU utilization. Analyse how DMA could improve data transfer rates and compare it with CPU-controlled I/O. Justify why DMA is particularly beneficial for high-speed peripherals like disk drives in video streaming applications. — 05 — CO4 CO5

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**OR**

**Q. 3** State the significance of using addressing modes in a computer system? Examine the four instructions given below and answer the respective questions for each: [2M] [3M] CO2

i) **LOAD A, 50**

Identify the addressing mode and explain how the operand is accessed?

ii) **ADD R1, #20**

Identify the addressing mode and describe what the operand represents in this context?

iii) **STORE R3, 100(R4)**

Identify the addressing mode. Explain how the effective address is calculated.

**Q.4(a)** Explain why computers use binary number systems instead of decimal systems. [2M] CO2

Illustrate with the help of a suitable example, how the range of representable values in 4-bit signed representation differs to that in 4-bit unsigned representation? [3M]

**Q.4(b)** Represent the following decimal values as signed 7-bit number using sign-magnitude and signed 1's complement formats. [4M] CO2

Provide detailed calculations and summarize your answers in the following tabulated format in the answer book:

| | Decimal Values | Sign-magnitude | Signed 1's complement |
|---|---|---|---|
| (i) | +23 | | |
| (ii) | -23 | | |

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