gatecse-2014-set1 digital-logic normal multiplexer min-sum-of-products-form

Answer key

6.22.9 Min Sum of Products Form: GATE CSE 2014 Set 1 | Question: 7

Consider the following Boolean expression for F:

$F(P,Q,R,S) = PQ + \bar{P}QR + \bar{P}Q\bar{R}S$

The minimal sum—of—products form of F is

A. $PQ + QR + QS$
B. $P + Q + R + S$
C. $\bar{P} + \bar{Q} + \bar{R} + \bar{S}$
D. $\bar{P}R + \bar{R}\bar{P}S + P$

gatecse-2014-set1 digital-logic normal min-sum-of-products-form

Answer key

6.22.10 Min Sum of Products Form: GATE CSE 2014 Set 3 | Question: 7

Consider the following minterm expression for F:

$$F(P,Q,R,S) = \sum 0,2,5,7,8,10,13,15$$

The minterms 2, 7, 8 and 13 are 'do not care' terms. The minimal sum-of-products form for F is

A. $Q\bar{S} + \bar{Q}S$
B. $\bar{Q}\bar{S} + QS$
C. $\bar{Q}\bar{R}\bar{S} + \bar{Q}R\bar{S} + Q\bar{R}S + QRS$
D. $\bar{P}\bar{Q}\bar{S} + \bar{P}QS + PQS + P\bar{Q}\bar{S}$

gatecse-2014-set3 digital-logic min-sum-of-products-form normal

Answer key

6.22.11 Min Sum of Products Form: GATE CSE 2018 | Question: 49

Consider the minterm list form of a Boolean function F given below.

$$F(P,Q,R,S) = \Sigma m(0,2,5,7,9,11) + d(3,8,10,12,14)$$

Here, m denotes a minterm and d denotes a don't care term. The number of essential prime implicants of the function F is ___

gatecse-2018 digital-logic min-sum-of-products-form numerical-answers 2-marks

Answer key

6.22.12 Min Sum of Products Form: GATE CSE 2021 Set 2 | Question: 52

Consider a Boolean function $f(w,x,y,z)$ such that

$$\begin{aligned} f(w,0,0,z) &= 1 \\ f(1,x,1,z) &= x+z \\ f(w,1,y,z) &= wz+y \end{aligned}$$

The number of literals in the minimal sum-of-products expression of f is _____

gatecse-2021-set2 digital-logic boolean-algebra min-sum-of-products-form numerical-answers 2-marks

Answer key

6.22.13 Min Sum of Products Form: GATE CSE 2024 | Set 1 | Question: 37

Consider a Boolean expression given by $\mathrm{F(X, Y, Z)} = \sum(3,5,6,7)$.
Which of the following statements is/are CORRECT?

A. $\mathrm{F(X, Y, Z)} = \Pi(0,1,2,4)$
B. $\mathrm{F(X, Y, Z)}$=X Y+Y Z+X Z

C. $\mathrm{F(X, Y, Z)}$ is independent of input Y

D. $\mathrm{F(X, Y, Z)}$ is independent of input X

gatecse2024-set1 multiple-selects digital-logic min-sum-of-products-form

Answer key

6.22.14 Min Sum of Products Form: GATE IT 2008 | Question: 8

Consider the following Boolean function of four variables

$f(A, B, C, D) = \Sigma(2, 3, 6, 7, 8, 9, 10, 11, 12, 13)$

The function is

A. independent of one variable
B. independent of two variables
C. independent of three variable
D. dependent on all the variables

gateit-2008 digital-logic normal min-sum-of-products-form

Answer key

6.23 Multiplexer (14)

6.23.1 Multiplexer: GATE CSE 1990 | Question: 5-b

Show with the help of a block diagram how the Boolean function :

$f = AB + BC + CA$

can be realised using only a $4:1$ multiplexer.

gate1990 descriptive digital-logic combinational-circuit multiplexer

Answer key

6.23.2 Multiplexer: GATE CSE 1998 | Question: 1.14

A multiplexer with a $4 - bit$ data select input is a

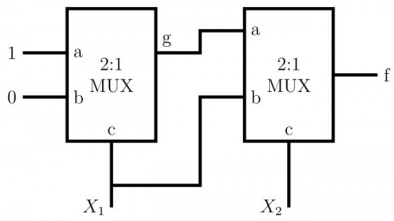
A. $4:1$ multiplexer
B. $2:1$ multiplexer
C. $16:1$ multiplexer
D. $8:1$ multiplexer

gate1998 digital-logic multiplexer easy

Answer key

6.23.3 Multiplexer: GATE CSE 2001 | Question: 2.11

Consider the circuit shown below. The output of a $2:1$ MUX is given by the function $(ac' + bc)$.



Which of the following is true?

A. $f = X_1' + X_2$
B. $f = X_1'X_2 + X_1X_2'$
C. $f = X_1X_2 + X_1'X_2'$
D. $f = X_1 + X_2'$

gatecse-2001 digital-logic normal multiplexer

Answer key

6.23.4 Multiplexer: GATE CSE 2004 | Question: 60

Consider a multiplexer with X and Y as data inputs and Z the as the control input. $Z = 0$ selects input X, and $Z = 1$ selects input Y. What are the connections required to realize the 2-variable Boolean function $f = T + R$, without using any additional hardware?

A. R to $\mathrm{X}, 1$ to Y, T to Z
B. T to X, R to Y, T to Z
C. T to X, R to $\mathrm{Y}, 0$ to Z
D. R to $\mathrm{X}, 0$ to Y, T to Z

gatecse-2004 digital-logic normal multiplexer

Answer key

6.23.5 Multiplexer: GATE CSE 2007 | Question: 34

Suppose only one multiplexer and one inverter are allowed to be used to implement any Boolean function of n variables. What is the minimum size of the multiplexer needed?

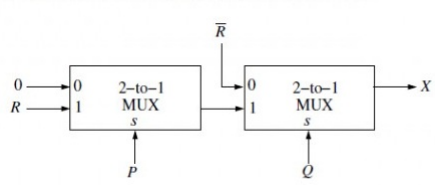
A. 2^n line to 1 line
B. 2^{n+1} line to 1line
C. 2^{n-1} line to 1line
D. 2^{n-2} line to 1line

gatecse-2007 digital-logic normal multiplexer

Answer key

6.23.6 Multiplexer: GATE CSE 2016 Set 1 | Question: 30

Consider the two cascade 2 to 1 multiplexers as shown in the figure .



The minimal sum of products form of the output X is

A. $\overline{P}\,\overline{Q}+PQR$
B. $\overline{P}\,Q+QR$
C. $PQ+\overline{P}\,\overline{Q}R$
D. $\overline{Q}\,\overline{R}+PQR$

gatecse-2016-set1 digital-logic multiplexer normal

Answer key

6.23.7 Multiplexer: GATE CSE 2020 | Question: 19

A multiplexer is placed between a group of 32 registers and an accumulator to regulate data movement such that at any given point in time the content of only one register will move to the accumulator. The number of select lines needed for the multiplexer is _____.

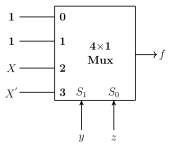
gatecse-2020 numerical-answers digital-logic multiplexer 1-mark

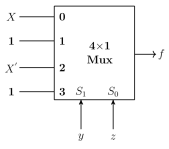
Answer key

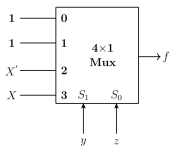
6.23.8 Multiplexer: GATE CSE 2021 Set 2 | Question: 5

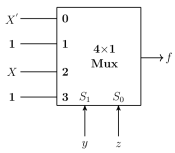
Which one of the following circuits implements the Boolean function given below?

$f(x,y,z)=m_0+m_1+m_3+m_4+m_5+m_6$, where m_i is the i^{th} minterm.

A.


B.


C.


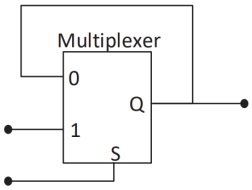
D.


gatecse-2021-set2 digital-logic combinational-circuit multiplexer 1-mark

Answer key

6.23.9 Multiplexer: GATE CSE 2023 | Question: 11

The output of a 2-input multiplexer is connected back to one of its inputs as shown in the figure.



Match the functional equivalence of this circuit to one of the following options.

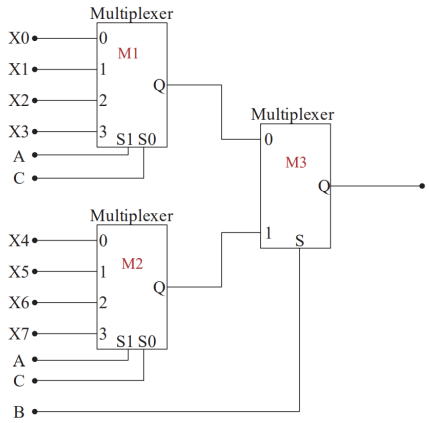
A. D Flip-flop B. D Latch C. Half-adder D. Demultiplexer

gatecse-2023 digital-logic combinational-circuit multiplexer 1-mark

Answer key

6.23.10 Multiplexer: GATE CSE 2023 | Question: 34

A Boolean digital circuit is composed using two 4-input multiplexers $(\mathrm{M1}\text{ and }\mathrm{M2})$ and one 2-input multiplexer $(\mathrm{M3})$ as shown in the figure. $\mathrm{X0}$-$\mathrm{X7}$ are the inputs of the multiplexers $\mathrm{M1}\text{ and }\mathrm{M2}$ and could be connected to either 0 or 1. The select lines of the multiplexers are connected to Boolean variables $\mathrm{A}, \mathrm{B}\text{ and }\mathrm{C}$ as shown.



Which one of the following set of values of $(\mathrm{X0}, \mathrm{X1}, \mathrm{X2}, \mathrm{X3}, \mathrm{X4}, \mathrm{X5}, \mathrm{X6}, \mathrm{X7})$ will realise the Boolean function $\overline{\mathrm{A}} + \overline{\mathrm{A}} \cdot \overline{\mathrm{C}} + \mathrm{A} \cdot \overline{\mathrm{B}} \cdot \mathrm{C}$?

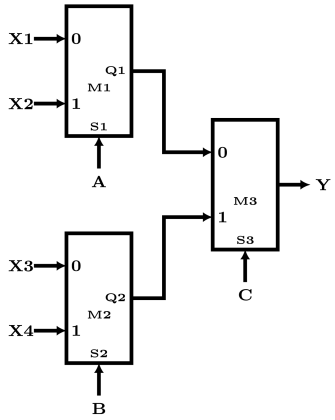
A. $(1,1,0,0,1,1,1,0)$
B. $(1,1,0,0,1,1,0,1)$
C. $(1,1,0,1,1,1,0,0)$
D. $(0,0,1,1,0,1,1,1)$

gatecse-2023 digital-logic combinational-circuit multiplexer 2-marks

Answer key

6.23.11 Multiplexer: GATE CSE 2024 | Set 1 | Question: 54

Consider a digital logic circuit consisting of three 2-to-1 multiplexers $\mathrm{M1}, \mathrm{M2}$, and $\mathrm{M3}$ as shown below. $\mathrm{X1}$ and $\mathrm{X2}$ are inputs of $\mathrm{M1}$. $\mathrm{X3}$ and $\mathrm{X4}$ are inputs of $\mathrm{M2}$. A, B, and C are select lines of $\mathrm{M1}, \mathrm{M2}$, and $\mathrm{M3}$, respectively.



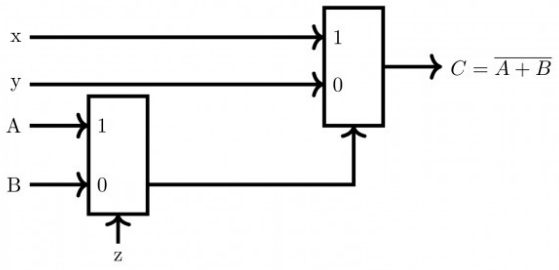
For an instance of inputs $\mathbf{X1 = 1, X2 = 1, X3 = 0}$, and $\mathbf{X4 = 0}$, the number of combinations of $\mathrm{A, B, C}$ that give the output $\mathbf{Y = 1}$ is _____.

gatecse2024-set1 numerical-answers digital-logic multiplexer

Answer key

6.23.12 Multiplexer: GATE IT 2005 | Question: 48

The circuit shown below implements a 2-input NOR gate using two $2 - 4$ MUX (control signal 1 selects the upper input). What are the values of signals x, y and z?



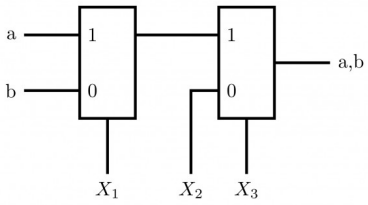
A. $1, 0, B$ B. $1, 0, A$ C. $0, 1, B$ D. $0, 1, A$

gateit-2005 digital-logic normal multiplexer

Answer key

6.23.13 Multiplexer: GATE IT 2007 | Question: 8

The following circuit implements a two-input AND gate using two $2 - 1$ multiplexers.



What are the values of X_1, X_2, X_3?

A. $X_1 = b, X_2 = 0, X_3 = a$
B. $X_1 = b, X_2 = 1, X_3 = b$
C. $X_1 = a, X_2 = b, X_3 = 1$
D. $X_1 = a, X_2 = 0, X_3 = b$

gateit-2007 digital-logic normal multiplexer

Answer key

6.23.14 Multiplexer: GATE1992-04-b

A priority encoder accepts three input signals $(\mathrm{A}, \mathrm{B} \text{ and } \mathrm{C})$ and produces a two-bit output (X_1, X_0) corresponding to the highest priority active input signal. Assume A has the highest priority followed by B and C has the lowest priority. If none of the inputs are active the output should be 00, design the priority encoder using $4:1$ multiplexers as the main components.

gate1992 digital-logic combinational-circuit multiplexer descriptive

Answer key

6.24 Number Representation (57)

6.24.1 Number Representation: GATE CSE 1988 | Question: 2-vi

Define the value of r in the following: $\sqrt{(41)_r} = (7)_{10}$

gate1988 digital-logic normal number-representation descriptive

Answer key

6.24.2 Number Representation: GATE CSE 1990 | Question: 1-viii

The condition for overflow in the addition of two $2's$ complement numbers in terms of the carry generated by the two most significant bits is _____.

gate1990 digital-logic number-representation fill-in-the-blanks

Answer key

6.24.3 Number Representation: GATE CSE 1991 | Question: 01-iii

Consider the number given by the decimal expression:

$$16^3 * 9 + 16^2 * 7 + 16 * 5 + 3$$

The number of $1's$ in the unsigned binary representation of the number is _____

gate1991 digital-logic number-representation normal numerical-answers

Answer key

6.24.4 Number Representation: GATE CSE 1991 | Question: 01-v

When two 4-bit numbers $A = a_3a_2a_1a_0$ and $B = b_3b_2b_1b_0$ are multiplied, the bit c_1 of the product C is given by _____

gate1991 digital-logic normal number-representation fill-in-the-blanks

Answer key

6.24.5 Number Representation: GATE CSE 1992 | Question: 4-a

Consider addition in two's complement arithmetic. A carry from the most significant bit does not always correspond to an overflow. Explain what is the condition for overflow in two's complement arithmetic.

gate1992 digital-logic normal number-representation descriptive

Answer key

6.24.6 Number Representation: GATE CSE 1993 | Question: 6.5

Convert the following numbers in the given bases into their equivalents in the desired bases:

A. $(110.101)_2 = (x)_{10}$
B. $(1118)_{10} = (y)_H$

gate1993 digital-logic number-representation normal descriptive

Answer key

6.24.7 Number Representation: GATE CSE 1994 | Question: 2.7

Consider n-bit (including sign bit) $2's$ complement representation of integer numbers. The range of integer values, N, that can be represented is _____ $\leq N \leq$_____ .

gate1994 digital-logic number-representation easy fill-in-the-blanks

Answer key

6.24.8 Number Representation: GATE CSE 1995 | Question: 18

The following is an incomplete Pascal function to convert a given decimal integer (in the range -8 to $+7$) into a binary integer in 2's complement representation. Determine the expressions A, B, C that complete program.

```
function TWOSCOMP (N:integer):integer;
  var
  REM, EXPONENT:integer;
  BINARY :integer;
  begin
    if(N>=-8) and (N<=+7) then
    begin
      if N<0 then
        N:=A;
      BINARY:=0;
      EXPONENT:=1;
      while N<>0 do
      begin
        REM:=N mod 2;
        BINARY:=BINARY + B*EXPONENT;
        EXPONENT:=EXPONENT*10;
        N:=C
      end
      TWOSCOMP:=BINARY
    end
  end;
```

gate1995 digital-logic number-representation normal descriptive

Answer key

6.24.9 Number Representation: GATE CSE 1995 | Question: 2.12, ISRO2015-9

The number of 1's in the binary representation of $(3 * 4096 + 15 * 256 + 5 * 16 + 3)$ are:

A. 8 B. 9 C. 10 D. 12

gate1995 digital-logic number-representation normal isro2015

Answer key

6.24.10 Number Representation: GATE CSE 1996 | Question: 1.25

Consider the following floating-point number representation.

31 24	23 0
Exponent	Mantissa

The exponent is in $2's$ complement representation and the mantissa is in the sign-magnitude representation. The range of the magnitude of the normalized numbers in this representation is

A. 0 to 1 B. 0.5 to 1 C. 2^{-23} to 0.5 D. 0.5 to $\left(1 - 2^{-23}\right)$

gate1996 digital-logic number-representation normal

Answer key

6.24.11 Number Representation: GATE CSE 1997 | Question: 5.4

Given $\sqrt{(224)_r} = (13)_r$.
The value of the radix r is:

A. 10 B. 8 C. 5 D. 6

gate1997 digital-logic number-representation normal

Answer key

6.24.12 Number Representation: GATE CSE 1998 | Question: 1.17

The octal representation of an integer is $(342)_8$. If this were to be treated as an eight-bit integer in an 8085 based computer, its decimal equivalent is

A. 226 B. -98 C. 76 D. -30

gate1998 digital-logic number-representation normal

Answer key

6.24.13 Number Representation: GATE CSE 1998 | Question: 2.20

Suppose the domain set of an attribute consists of signed four digit numbers. What is the percentage of reduction in storage space of this attribute if it is stored as an integer rather than in character form?

A. 80% B. 20% C. 60% D. 40%

gate1998 digital-logic number-representation normal

Answer key

6.24.14 Number Representation: GATE CSE 1999 | Question: 2.17

Zero has two representations in

A. Sign-magnitude
B. $2's$ complement
C. $1's$ complement
D. None of the above

gate1999 digital-logic number-representation easy multiple-selects

Answer key

6.24.15 Number Representation: GATE CSE 2000 | Question: 1.6

The number 43 in $2's$ complement representation is

A. 01010101 B. 11010101 C. 00101011 D. 10101011

gatecse-2000 digital-logic number-representation easy

Answer key

6.24.16 Number Representation: GATE CSE 2000 | Question: 2.14

Consider the values of $A = 2.0 \times 10^{30}, B = -2.0 \times 10^{30}, C = 1.0$, and the sequence

```
X:= A + B        Y:= A + C
X:= X + C        Y:= Y + B
```

executed on a computer where floating point numbers are represented with 32 bits. The values for X and Y will be

A. $X = 1.0, Y = 1.0$
B. $X = 1.0, Y = 0.0$
C. $X = 0.0, Y = 1.0$
D. $X = 0.0, Y = 0.0$

gatecse-2000 digital-logic number-representation normal

Answer key

6.24.17 Number Representation: GATE CSE 2001 | Question: 2.10

The $2's$ complement representation of (-539)$_{10}$ in hexadecimal is

A. ABE B. DBC C. $DE5$ D. $9E7$

gatecse-2001 digital-logic number-representation easy

Answer key

6.24.18 Number Representation: GATE CSE 2002 | Question: 1.14

The decimal value 0.25

A. is equivalent to the binary value 0.1
B. is equivalent to the binary value 0.01
C. is equivalent to the binary value 0.00111
D. cannot be represented precisely in binary

gatecse-2002 digital-logic number-representation easy

Answer key

6.24.19 Number Representation: GATE CSE 2002 | Question: 1.15

The $2's$ complement representation of the decimal value -15 is

A. 1111 B. 11111 C. 111111 D. 10001

gatecse-2002 digital-logic number-representation easy

Answer key

6.24.20 Number Representation: GATE CSE 2002 | Question: 1.16

Sign extension is a step in

A. floating point multiplication
B. signed 16 bit integer addition
C. arithmetic left shift
D. converting a signed integer from one size to another

gatecse-2002 digital-logic easy number-representation

Answer key

6.24.21 Number Representation: GATE CSE 2002 | Question: 1.21

In $2's$ complement addition, overflow

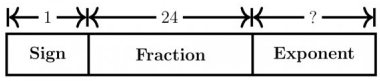
A. is flagged whenever there is carry from sign bit addition
B. cannot occur when a positive value is added to a negative value
C. is flagged when the carries from sign bit and previous bit match
D. None of the above

gatecse-2002 digital-logic number-representation normal

Answer key

6.24.22 Number Representation: GATE CSE 2002 | Question: 9

Consider the following 32-bit floating-point representation scheme as shown in the format below. A value is specified by 3 fields, a one bit sign field (with 0 for positive and 1 for negative values), a 24 bit fraction field (with the binary point is at the left end of the fraction bits), and a 7 bit exponent field (in excess-64 signed integer representation, with 16 is the base of exponentiation). The sign bit is the most significant bit.



A. It is required to represent the decimal value -7.5 as a normalized floating point number in the given format. Derive the values of the various fields. Express your final answer in the hexadecimal.
B. What is the largest value that can be represented using this format? Express your answer as the nearest power of 10.

gatecse-2002 digital-logic number-representation normal descriptive

Answer key

6.24.23 Number Representation: GATE CSE 2003 | Question: 9

Assuming all numbers are in $2's$ complement representation, which of the following numbers is divisible by 11111011?

A. 11100111 B. 11100100 C. 11010111 D. 11011011

gatecse-2003 digital-logic number-representation normal

Answer key

6.24.24 Number Representation: GATE CSE 2004 | Question: 19

If 73_x (in base-x number system) is equal to 54_y (in base y-number system), the possible values of x and y are

A. $8, 16$ B. $10, 12$ C. $9, 13$ D. $8, 11$

gatecse-2004 digital-logic number-representation easy

Answer key

6.24.25 Number Representation: GATE CSE 2004 | Question: 28

What is the result of evaluating the following two expressions using three-digit floating point arithmetic with rounding?

$(113. + -111.) + 7.51$

$113. + (-111. + 7.51)$

A. 9.51 and 10.0 respectively B. 10.0 and 9.51 respectively

C. 9.51 and 9.51 respectively D. 10.0 and 10.0 respectively

gatecse-2004 digital-logic number-representation normal

Answer key

6.24.26 Number Representation: GATE CSE 2004 | Question: 66

Let $A = 11111010$ and $B = 00001010$ be two $8 - bit$ $2's$ complement numbers. Their product in $2's$ complement is

A. 11000100 B. 10011100 C. 10100101 D. 11010101

gatecse-2004 digital-logic number-representation easy

Answer key

6.24.27 Number Representation: GATE CSE 2005 | Question: 16, ISRO2009-18, ISRO2015-2

The range of integers that can be represented by an n bit $2's$ complement number system is:

A. -2^{n-1} to $(2^{n-1} - 1)$ B. $-(2^{n-1} - 1)$ to $(2^{n-1} - 1)$

C. -2^{n-1} to 2^{n-1} D. $-(2^{n-1} + 1)$ to $(2^{n-1} - 1)$

gatecse-2005 digital-logic number-representation easy isro2009 isro2015

Answer key

6.24.28 Number Representation: GATE CSE 2005 | Question: 17

The hexadecimal representation of $(657)_8$ is:

A. $1AF$ B. $D78$ C. $D71$ D. $32F$

gatecse-2005 digital-logic number-representation easy

Answer key

6.24.29 Number Representation: GATE CSE 2006 | Question: 39

We consider the addition of two $2's$ complement numbers $b_{n-1}b_{n-2}\ldots b_0$ and $a_{n-1}a_{n-2}\ldots a_0$. A binary adder for adding unsigned binary numbers is used to add the two numbers. The sum is denoted by $c_{n-1}c_{n-2}\ldots c_0$ and the carry-out by c_{out}. Which one of the following options correctly identifies the overflow condition?

A. $c_{out}\left(\overline{a_{n-1}\oplus b_{n-1}}\right)$
B. $a_{n-1}b_{n-1}\overline{c_{n-1}}+\overline{a_{n-1}}\,\overline{b_{n-1}}c_{n-1}$
C. $c_{out}\oplus c_{n-1}$
D. $a_{n-1}\oplus b_{n-1}\oplus c_{n-1}$

gatecse-2006 digital-logic number-representation normal

Answer key

6.24.30 Number Representation: GATE CSE 2006 | Question: 40

Consider numbers represented in 4-bit Gray code. Let $h_3h_2h_1h_0$ be the Gray code representation of a number n and let $g_3g_2g_1g_0$ be the Gray code of $(n+1)(modulo 16)$ value of the number. Which one of the following functions is correct?

A. $g_0(h_3h_2h_1h_0)=\sum(1,2,3,6,10,13,14,15)$
B. $g_1(h_3h_2h_1h_0)=\sum(4,9,10,11,12,13,14,15)$
C. $g_2(h_3h_2h_1h_0)=\sum(2,4,5,6,7,12,13,15)$
D. $g_3(h_3h_2h_1h_0)=\sum(0,1,6,7,10,11,12,13)$

gatecse-2006 digital-logic number-representation binary-codes normal

Answer key

6.24.31 Number Representation: GATE CSE 2008 | Question: 6

Let r denote number system radix. The only value(s) of r that satisfy the equation $\sqrt{121_r}=11_r$ is/are

A. decimal 10
B. decimal 11
C. decimal 10 and 11
D. any value >2

gatecse-2008 digital-logic number-representation normal

Answer key

6.24.32 Number Representation: GATE CSE 2009 | Question: 5, ISRO2017-57

$(1217)_8$ is equivalent to

A. $(1217)_{16}$
B. $(028F)_{16}$
C. $(2297)_{10}$
D. $(0B17)_{16}$

gatecse-2009 digital-logic number-representation isro2017

Answer key

6.24.33 Number Representation: GATE CSE 2010 | Question: 8

P is a 16-bit signed integer. The 2's complement representation of P is $(F87B)_{16}$. The 2's complement representation of $8\times P$ is

A. $(C3D8)_{16}$
B. $(187B)_{16}$
C. $(F878)_{16}$
D. $(987B)_{16}$

gatecse-2010 digital-logic number-representation normal

Answer key

6.24.34 Number Representation: GATE CSE 2013 | Question: 4

The smallest integer that can be represented by an 8-bit number in $2's$ complement form is

A. -256
B. -128
C. -127
D. 0

gatecse-2013 digital-logic number-representation easy

Answer key

6.24.35 Number Representation: GATE CSE 2014 Set 1 | Question: 8

The base (or radix) of the number system such that the following equation holds is_____.

$\frac{312}{20} = 13.1$

gatecse-2014-set1 digital-logic number-representation numerical-answers normal

Answer key

6.24.36 Number Representation: GATE CSE 2014 Set 2 | Question: 8

Consider the equation $(123)_5 = (x8)_y$ with x and y as unknown. The number of possible solutions is _____ .

gatecse-2014-set2 digital-logic number-representation numerical-answers normal

Answer key

6.24.37 Number Representation: GATE CSE 2015 Set 3 | Question: 35

Consider the equation $(43)_x = (y3)_8$ where x and y are unknown. The number of possible solutions is _____

gatecse-2015-set3 digital-logic number-representation normal numerical-answers

Answer key

6.24.38 Number Representation: GATE CSE 2016 Set 1 | Question: 07

The 16-bit $2's$ complement representation of an integer is $1111 \quad 1111 \quad 1111 \quad 0101;$ its decimal representation is _____

gatecse-2016-set1 digital-logic number-representation normal numerical-answers

Answer key

6.24.39 Number Representation: GATE CSE 2016 Set 2 | Question: 09

Let X be the number of distinct 16-bit integers in $2's$ complement representation. Let Y be the number of distinct 16-bit integers in sign magnitude representation Then $X - Y$ is_____.

gatecse-2016-set2 digital-logic number-representation normal numerical-answers

Answer key

6.24.40 Number Representation: GATE CSE 2017 Set 1 | Question: 9

When two 8-bit numbers $A_7 \cdots A_0$ and $B_7 \cdots B_0$ in 2's complement representation (with A_0 and B_0 as the least significant bits) are added using a **ripple-carry adder,** the sum bits obtained are $S_7 \cdots S_0$ and the carry bits are $C_7 \cdots C_0$. An overflow is said to have occurred if

A. the carry bit C_7 is 1
B. all the carry bits $(C_7, \cdots, C_0)$ are 1
C. $\left(A_7 \cdot B_7 \cdot \overline{S_7} + \overline{A_7} \cdot \overline{B_7} \cdot S_7\right)$ is 1
D. $\left(A_0 \cdot B_0 \cdot \overline{S_0} + \overline{A_0} \cdot \overline{B_0} \cdot S_0\right)$ is 1

gatecse-2017-set1 digital-logic number-representation

Answer key

6.24.41 Number Representation: GATE CSE 2017 Set 2 | Question: 1

The representation of the value of a 16-bit unsigned integer X in hexadecimal number system is BCA9. The representation of the value of X in octal number system is

A. 571244 B. 736251 C. 571247 D. 136251

gatecse-2017-set2 digital-logic number-representation

Answer key

6.24.42 Number Representation: GATE CSE 2019 | Question: 22

Two numbers are chosen independently and uniformly at random from the set $\{1, 2, \ldots, 13\}$. The probability (rounded off to 3 decimal places) that their 4-bit (unsigned) binary representations have the same most significant bit is _____.

gatecse-2019 numerical-answers digital-logic number-representation probability 1-mark

Answer key

6.24.43 Number Representation: GATE CSE 2019 | Question: 4

In 16-bit 2's complement representation, the decimal number -28 is:

A. $1111\ 1111\ 0001\ 1100$
B. $0000\ 0000\ 1110\ 0100$
C. $1111\ 1111\ 1110\ 0100$
D. $1000\ 0000\ 1110\ 0100$

gatecse-2019 digital-logic number-representation 1-mark

Answer key

6.24.44 Number Representation: GATE CSE 2019 | Question: 8

Consider $Z = X - Y$ where X, Y and Z are all in sign-magnitude form. X and Y are each represented in n bits. To avoid overflow, the representation of Z would require a minimum of:

A. n bits B. $n - 1$ bits C. $n + 1$ bits D. $n + 2$ bits

gatecse-2019 digital-logic number-representation 1-mark

Answer key

6.24.45 Number Representation: GATE CSE 2021 Set 1 | Question: 6

Let the representation of a number in base 3 be 210. What is the hexadecimal representation of the number?

A. 15 B. 21 C. $\mathrm{D2}$ D. 528

gatecse-2021-set1 digital-logic number-representation normal 1-mark

Answer key

6.24.46 Number Representation: GATE CSE 2021 Set 2 | Question: 18

If x and y are two decimal digits and $(0.1101)_2 = (0.8xy5)_{10}$, the decimal value of $x + y$ is _____

gatecse-2021-set2 numerical-answers digital-logic number-representation 1-mark

Answer key

6.24.47 Number Representation: GATE CSE 2021 Set 2 | Question: 44

If the numerical value of a 2-byte unsigned integer on a little endian computer is 255 more than that on a big endian computer, which of the following choices represent(s) the unsigned integer on a little endian computer?

A. $0\mathrm{x}6665$ B. $0\mathrm{x}0001$ C. $0\mathrm{x}4243$ D. $0\mathrm{x}0100$

gatecse-2021-set2 multiple-selects digital-logic number-representation little-endian-big-endian 2-marks

Answer key

6.24.48 Number Representation: GATE CSE 2022 | Question: 8

Let $\mathrm{R1}$ and $\mathrm{R2}$ be two $4-\mathrm{bit}$ registers that store numbers in 2's complement form. For the operation $\mathrm{R1}+\mathrm{R2}$, which one of the following values of $\mathrm{R1}$ and $\mathrm{R2}$ gives an arithmetic overflow?

A. $\mathrm{R1}=1011$ and $\mathrm{R2}=1110$
B. $\mathrm{R1}=1100$ and $\mathrm{R2}=1010$
C. $\mathrm{R1}=0011$ and $\mathrm{R2}=0100$
D. $\mathrm{R1}=1001$ and $\mathrm{R2}=1111$

gatecse-2022 digital-logic number-representation 1-mark

Answer key

6.24.49 Number Representation: GATE CSE 2023 | Question: 22

A particular number is written as 132 in radix-4 representation. The same number in radix-5 representation is _____.

gatecse-2023 digital-logic number-representation numerical-answers 1-mark

Answer key

6.24.50 Number Representation: GATE CSE 2024 | Set 1 | Question: 3

Consider a system that uses 5 bits for representing signed integers in 2 's complement format. In this system, two integers A and B are represented as A=01010 and B=11010. Which one of the following operations will result in either an arithmetic overflow or an arithmetic underflow?

A. $A+B$
B. $A-B$
C. $B-A$
D. $2*B$

gatecse2024-set1 digital-logic number-representation

Answer key

6.24.51 Number Representation: GATE CSE 2024 | Set 2 | Question: 39

Which of the following is/are EQUAL to 224 in radix - 5 (*i.e.*, base - 5) notation?

A. 64 in radix -10
B. 100 in radix -8
C. 50 in radix -16
D. 121 in radix -7

gatecse2024-set2 digital-logic number-representation multiple-selects

Answer key

6.24.52 Number Representation: GATE IT 2004 | Question: 42

Using a $4-bit\ 2's$ complement arithmetic, which of the following additions will result in an overflow?

i. $1100+1100$
ii. $0011+0111$
iii. $1111+0111$

A. i only
B. ii only
C. iii only
D. i and iii only

gateit-2004 digital-logic number-representation normal

Answer key

6.24.53 Number Representation: GATE IT 2004 | Question: 43

The number $(123456)_8$ is equivalent to

A. $(\mathrm{A72E})_{16}$ and $(22130232)_4$
B. $(\mathrm{A72E})_{16}$ and $(22131122)_4$
C. $(\mathrm{A73E})_{16}$ and $(22130232)_4$
D. $(\mathrm{A62E})_{16}$ and $(22120232)_4$

gateit-2004 digital-logic number-representation normal

Answer key

6.24.54 Number Representation: GATE IT 2005 | Question: 47

$(34.4)_8 \times (23.4)_8$ evaluates to

A. $(1053.6)_8$ B. $(1053.2)_8$ C. $(1024.2)_8$ D. None of these

gateit-2005 digital-logic number-representation normal

Answer key

6.24.55 Number Representation: GATE IT 2006 | Question: 7, ISRO2009-41

The addition of $4-bit$, two's complement, binary numbers 1101 and 0100 results in

A. 0001 and an overflow
B. 1001 and no overflow
C. 0001 and no overflow
D. 1001 and an overflow

gateit-2006 digital-logic number-representation normal isro2009

Answer key

6.24.56 Number Representation: GATE IT 2007 | Question: 42

$(C012.25)_H - (10111001110.101)_B =$

A. $(135103.412)_o$
B. $(564411.412)_o$
C. $(564411.205)_o$
D. $(135103.205)_o$

gateit-2007 digital-logic number-representation normal

Answer key

6.24.57 Number Representation: GATE IT 2008 | Question: 15

A processor that has the carry, overflow and sign flag bits as part of its program status word (PSW) performs addition of the following two $2's$ complement numbers 01001101 and 11101001. After the execution of this addition operation, the status of the carry, overflow and sign flags, respectively will be:

A. $1,1,0$ B. $1,0,0$ C. $0,1,0$ D. $1,0,1$

gateit-2008 digital-logic number-representation normal

Answer key

6.25 Prime Implicants (2)

6.25.1 Prime Implicants: GATE CSE 1997 | Question: 5.1

Let $f(x,y,z) = \bar{x} + \bar{y}x + xz$ be a switching function. Which one of the following is valid?

A. $\bar{y}x$ is a prime implicant of f
B. xz is a minterm of f
C. xz is an implicant of f
D. y is a prime implicant of f

gate1997 digital-logic normal prime-implicants

Answer key

6.25.2 Prime Implicants: GATE CSE 2004 | Question: 59

Which are the essential prime implicants of the following Boolean function?

$f(a,b,c) = a'c + ac' + b'c$

A. $a'c$ and ac' B. $a'c$ and $b'c$ C. $a'c$ only. D. ac' and bc'

gatecse-2004 digital-logic normal prime-implicants

Answer key

6.26 ROM (4)

6.26.1 ROM: GATE CSE 1993 | Question: 6.6

A ROM is used to store the Truth table for binary multiple units that will multiply two 4-bit numbers. The size of the ROM (number of words $\times$ number of bits) that is required to accommodate the Truth table is M words $\times$ N bits. Write the values of M and N.

gate1993 digital-logic normal rom descriptive

Answer key

6.26.2 ROM: GATE CSE 1996 | Question: 1.21

A ROM is used to store the table for multiplication of two 8-bit unsigned integers. The size of ROM required is

A. 256×16
B. $64K \times 8$
C. $4K \times 16$
D. $64K \times 16$

gate1996 digital-logic normal rom

Answer key

6.26.3 ROM: GATE CSE 2012 | Question: 19

The amount of ROM needed to implement a 4-bit multiplier is

A. 64 bits
B. 128 bits
C. 1 Kbits
D. 2 Kbits

gatecse-2012 digital-logic normal rom

Answer key

6.26.4 ROM: GATE IT 2004 | Question: 10

What is the minimum size of ROM required to store the complete truth table of an $8 - bit \times 8 - bit$ multiplier?

A. $32K \times 16$ bits
B. $64K \times 16$ bits
C. $16K \times 32$ bits
D. $64K \times 32$ bits

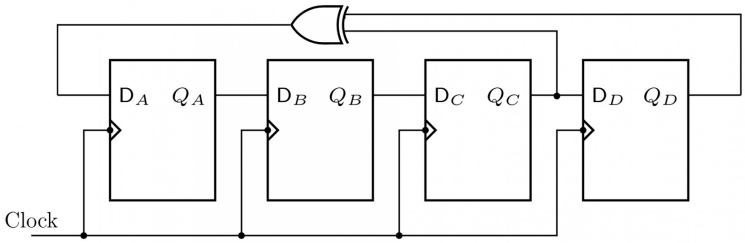
gateit-2004 digital-logic normal rom

Answer key

6.27 Shift Registers (2)

6.27.1 Shift Registers: GATE CSE 1987 | Question: 13-a

The below figure shows four D-type flip-flops connected as a shift register using a XOR gate. The initial state and three subsequent states for three clock pulses are also given.



State	Q_A	Q_B	Q_C	Q_D
Initial	1	1	1	1
After the first clock	0	1	1	1
After the second clock	0	0	1	1
After the third clock	0	0	0	1

The state $Q_AQ_BQ_CQ_D$ after the fourth clock pulse is

A. 0000
B. 1111
C. 1001
D. 1000

gate1987 digital-logic circuit-output sequential-circuit digital-counter shift-registers

Answer key

6.27.2 Shift Registers: GATE CSE 1991 | Question: 06,a

Using D flip-flop gates, design a parallel-in/serial-out shift register that shifts data from left to right with the following input lines:

i. Clock CLK
ii. Three parallel data inputs A, B, C
iii. Serial input S
iv. Control input $\mathrm{LOAD}/\overline{\mathrm{SHIFT}}$.

gate1991 digital-logic difficult sequential-circuit flip-flop shift-registers descriptive

Answer key

6.28 Static Hazard (1)

6.28.1 Static Hazard: GATE CSE 2006 | Question: 38

Consider a Boolean function $f(w, x, y, z)$. Suppose that exactly one of its inputs is allowed to change at a time. If the function happens to be true for two input vectors $i_1 = \langle w_1, x_1, y_1, z_1 \rangle$ and $i_2 = \langle w_2, x_2, y_2, z_2 \rangle$, we would like the function to remain true as the input changes from i_1 to i_2 (i_1 and i_2 differ in exactly one bit position) without becoming false momentarily. Let $f(w, x, y, z) = \sum(5, 7, 11, 12, 13, 15)$. Which of the following cube covers of f will ensure that the required property is satisfied?

A. $\overline{w}xz, wx\overline{y}, x\overline{y}z, xyz, wyz$
B. $wxy, \overline{w}xz, wyz$
C. $wx\overline{yz}, xz, w\overline{x}yz$
D. $wx\overline{y}, wyz, wxz, \overline{w}xz, x\overline{y}z, xyz$

gatecse-2006 digital-logic min-sum-of-products-form difficult static-hazard

Answer key

6.29 Synchronous Asynchronous Circuits (4)

6.29.1 Synchronous Asynchronous Circuits: GATE CSE 1991 | Question: 03-ii

Advantage of synchronous sequential circuits over asynchronous ones is:

A. faster operation
B. ease of avoiding problems due to hazards
C. lower hardware requirement
D. better noise immunity
E. none of the above

gate1991 digital-logic normal sequential-circuit synchronous-asynchronous-circuits multiple-selects

Answer key

6.29.2 Synchronous Asynchronous Circuits: GATE CSE 1998 | Question: 16

Design a synchronous counter to go through the following states:

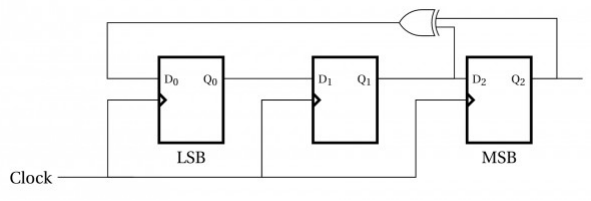
$$1, 4, 2, 3, 1, 4, 2, 3, 1, 4 \ldots$$

gate1998 digital-logic normal descriptive synchronous-asynchronous-circuits

Answer key

6.29.3 Synchronous Asynchronous Circuits: GATE CSE 2001 | Question: 2.12

Consider the circuit given below with initial state $Q_0 = 1, Q_1 = Q_2 = 0$. The state of the circuit is given by the value $4Q_2 + 2Q_1 + Q_0$



Which one of the following is correct state sequence of the circuit?

A. $1,3,4,6,7,5,2$
B. $1,2,5,3,7,6,4$
C. $1,2,7,3,5,6,4$
D. $1,6,5,7,2,3,4$

gatecse-2001 digital-logic normal synchronous-asynchronous-circuits

Answer key

6.29.4 Synchronous Asynchronous Circuits: GATE CSE 2003 | Question: 44

A 1-input, 2-output synchronous sequential circuit behaves as follows:

Let z_k, n_k denote the number of $0's$ and $1's$ respectively in initial k bits of the input $(z_k + n_k = k)$. The circuit outputs 00 until one of the following conditions holds.

- $z_k - n_k = 2$. In this case, the output at the k-th and all subsequent clock ticks is 10.
- $n_k - z_k = 2$. In this case, the output at the *k*-th and all subsequent clock ticks is 01.

What is the minimum number of states required in the state transition graph of the above circuit?

A. 5
B. 6
C. 7
D. 8

gatecse-2003 digital-logic synchronous-asynchronous-circuits normal

Answer key

Answer Keys

6.1.1	N/A	6.1.2	N/A	6.1.3	B	6.1.4	B	6.1.5	A
6.1.6	B	6.1.7	19.2	6.1.8	B	6.1.9	-1	6.2.1	B
6.2.2	C	6.3.1	D	6.3.2	C	6.3.3	N/A	6.3.4	N/A
6.3.5	N/A	6.3.6	D	6.3.7	N/A	6.3.8	A	6.3.9	B
6.3.10	D	6.3.11	C	6.3.12	D	6.3.13	C	6.3.14	C
6.3.15	D	6.3.16	D	6.3.17	D	6.3.18	A	6.3.19	A
6.3.20	D	6.3.21	D	6.3.22	D	6.3.23	1	6.3.24	A
6.3.25	C	6.3.26	C	6.3.27	D	6.3.28	B	6.3.29	B;C;D
6.3.30	B;C	6.3.31	B	6.3.32	C	6.4.1	N/A	6.4.2	A
6.4.3	B	6.4.4	A	6.4.5	C	6.4.6	B	6.5.1	A
6.5.2	A	6.5.3	C	6.5.4	A	6.5.5	3	6.5.6	A
6.5.7	3	6.5.8	B	6.5.9	C;D	6.6.1	A	6.6.2	B
6.7.1	B	6.7.2	N/A	6.7.3	C	6.7.4	N/A	6.7.5	N/A
6.7.6	A;C	6.7.7	B	6.7.8	B	6.7.9	B	6.7.10	011
6.7.11	D	6.7.12	C	6.7.13	N/A	6.7.14	N/A	6.7.15	B
6.7.16	B	6.7.17	A	6.7.18	A	6.7.19	A	6.7.20	D
6.7.21	A	6.7.22	A	6.7.23	D	6.7.24	A	6.7.25	C
6.7.26	C	6.7.27	C	6.7.28	A	6.7.29	A	6.7.30	B
6.7.31	D	6.7.32	B	6.7.33	C	6.7.34	C	6.7.35	X