# COL215 LAB REPORT 7

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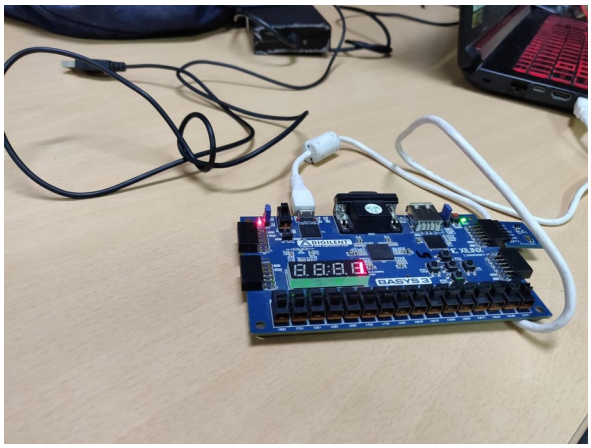
In this Lab we have extended lab 6 to create a rightness sensing circuit.
We have added 2 more components and remaining are extended from lab 6 . The two new components made are explained below:

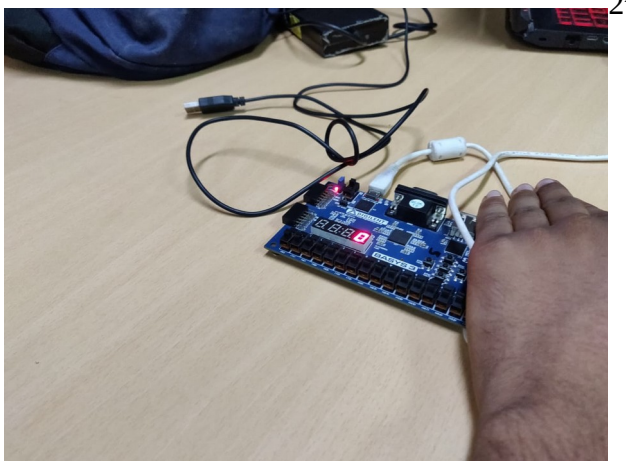
1MHz Clock :Takes as input the actual clock, of 100MHz frequency. It keeps a variable count which is incremented with every clock rising edge. When the count reaches 50, the output clock is flipped. That's how a frequency of 1 MHz is obtained.

Communication Module : It takes 2 clock as input with frequency 1Hz and 1MHz. The 1Hz clock acts as the enable signal. Thus with every rising edge of the enable signal, the count signal starts counting, incrementing its value at every positive edge of the 1MHz clock, and the CS signal is set to 0. Also, the slk signal fed into the Pmod is made equal to the 1MHz clock. When the count values reach 3,4,5 and 6, then the output four bits signal are modified, one bit at a time. These will be fed into the PWM and display later. When the count reaches 15, it is reset to 0, as the CS signal is reset to 1.

Test Case:
Some test cases-
1st test case: normal room light.



2nd test case: covered fully (No light)



3rd test case: Illuminated with phone torch