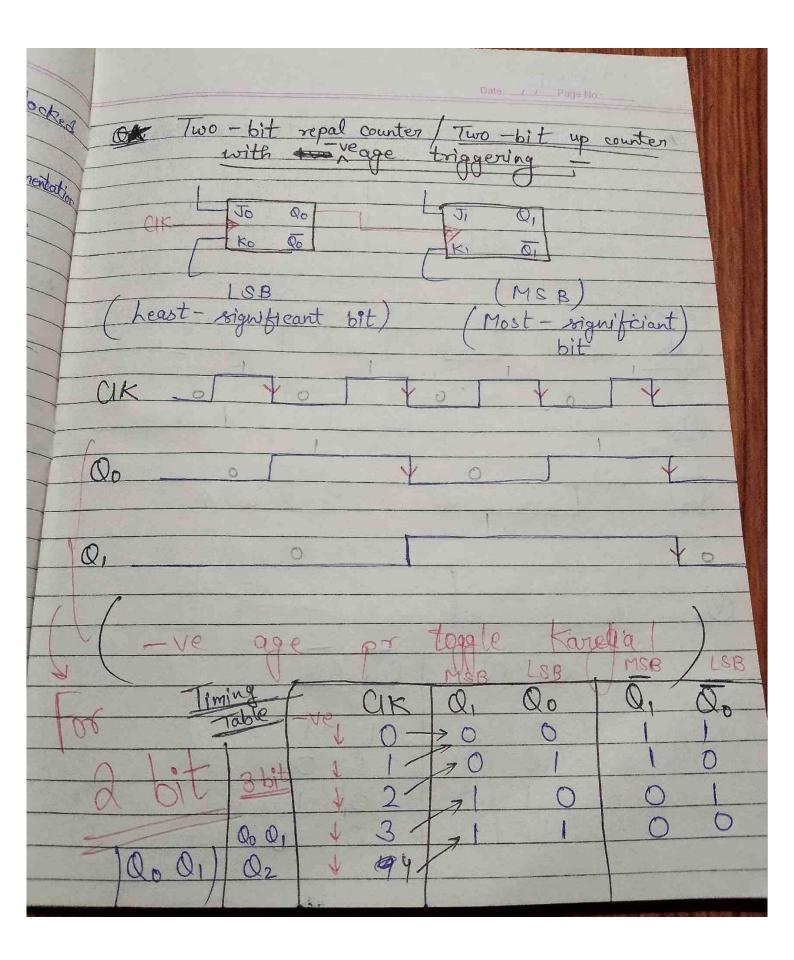
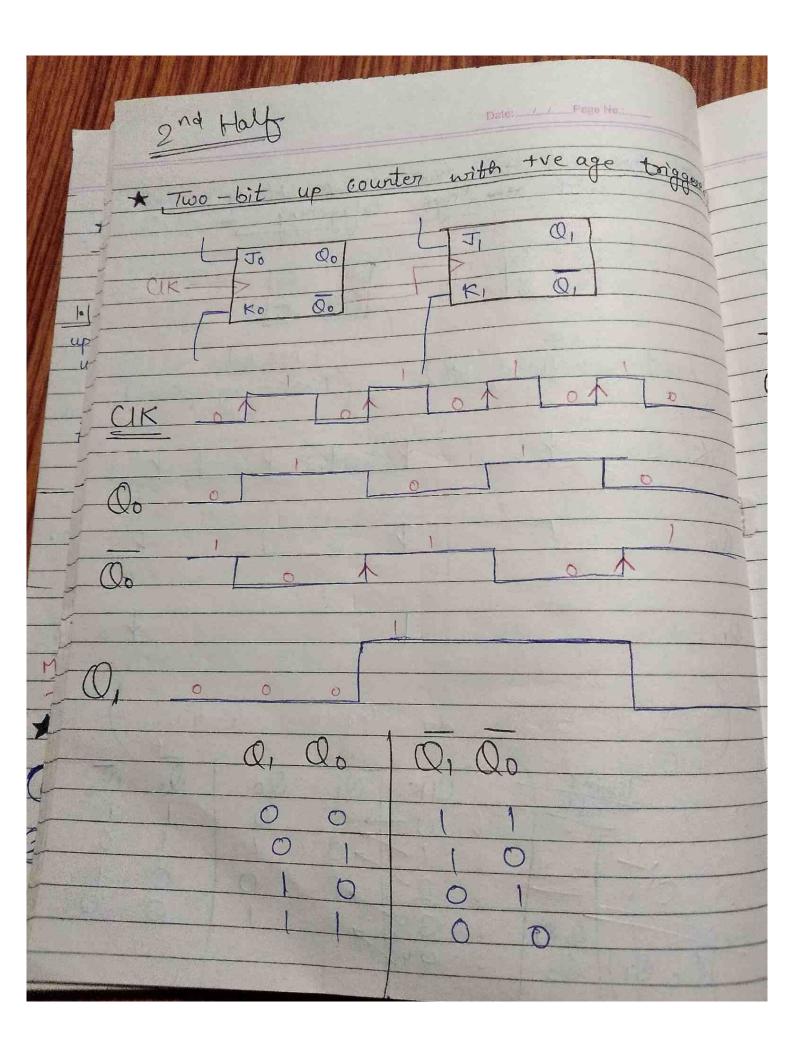


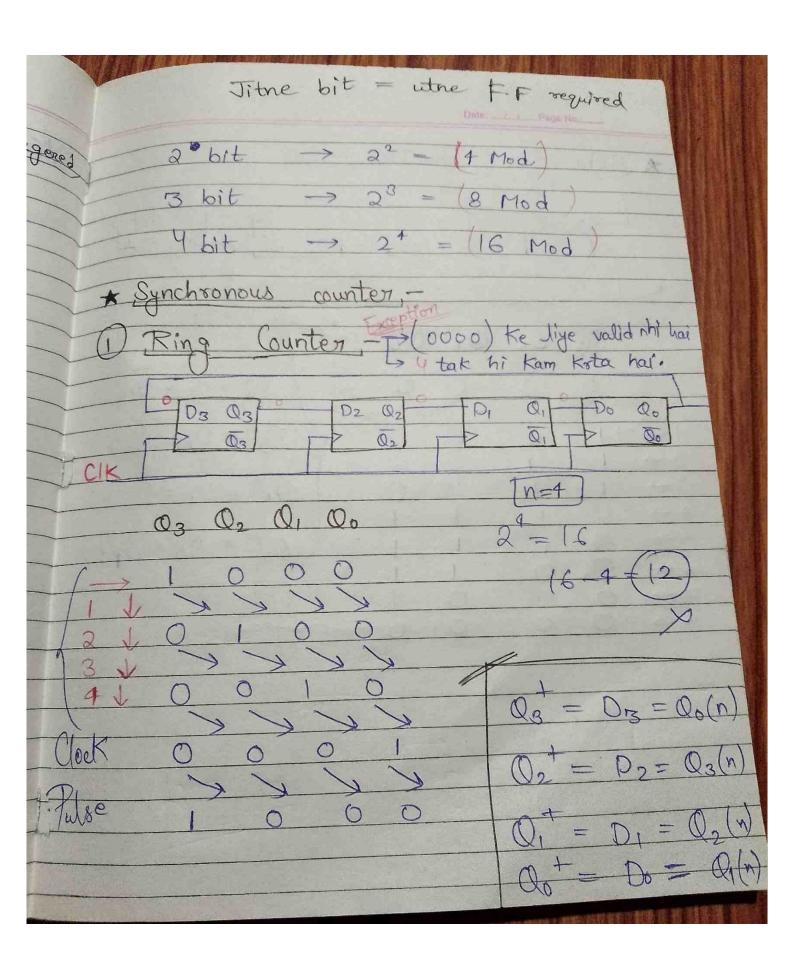
3

(+ve age Trigged) (-ve Trigged)  (2) AU F.F are not clocked simultaneously.  (3) Design an implementation is very simple for more to state.  (4) Low speed	simultaneously.
* Asynchronous counter-  reple / updown counter-	Tumping allowed which has
$\begin{array}{c} 0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow \dots & \text{Up} \\ \text{(ounter)} \\ \hline \\ 1 \qquad 3 \rightarrow 2 \rightarrow 1 \rightarrow 0 \qquad \text{down} \\ \hline \\ \text{counter)} \end{array}$	MI* Table (For 2/8/4)  * IMP Table (bit)  +ve -ve
Same > down +ve ->	Q(n) Q(n) down
Opposite charge > UP - Ve	Up down

4

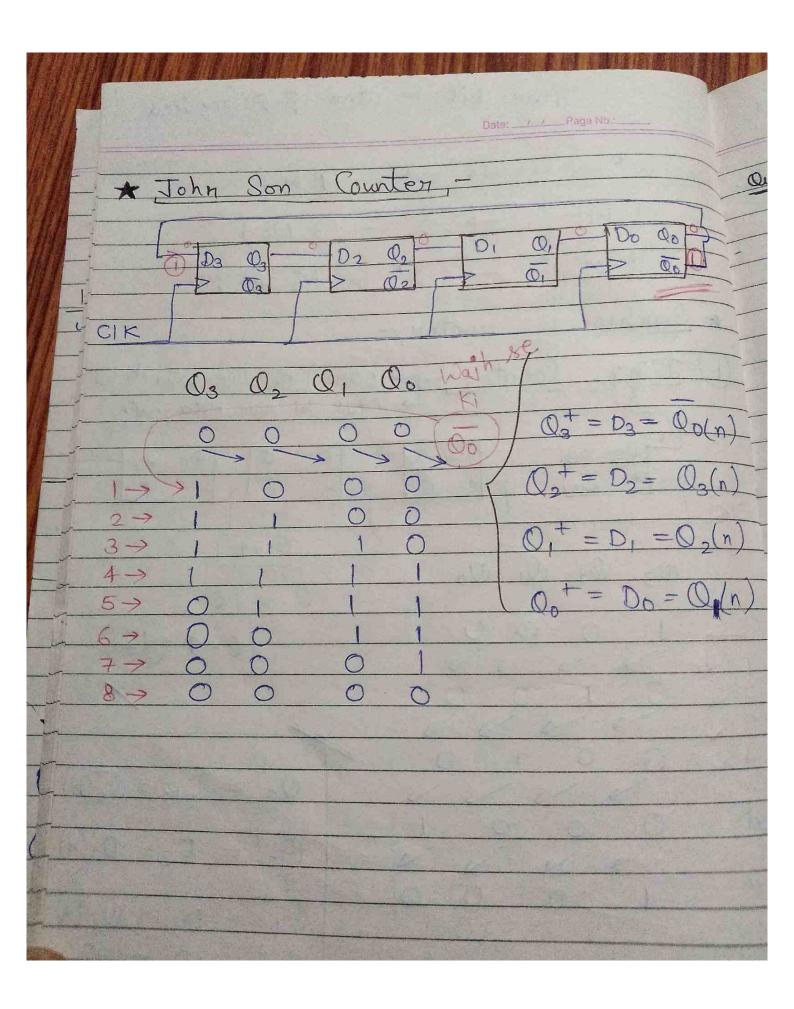


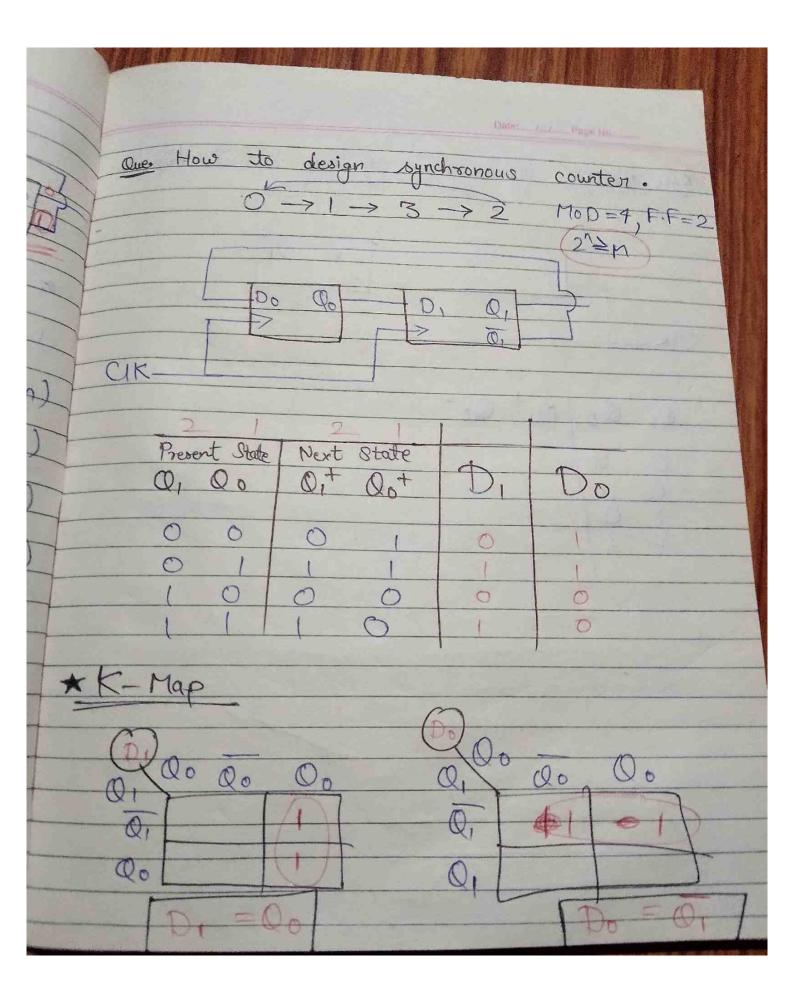


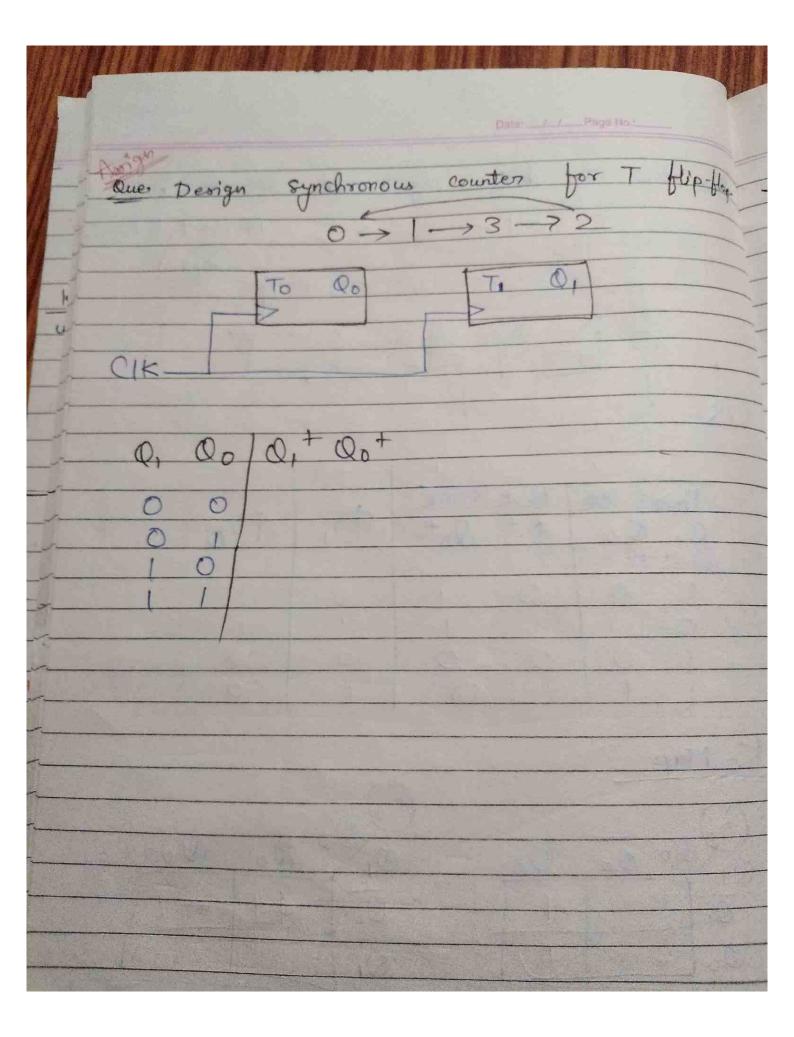


7

Piyush







	own counter > (7->6-)  Oute (ultringinti)	
#3-bit synchr. counter with JK F.F,-		
3 bit down 3 bit up counter counter  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	7 → 6 → 5 → 4 → 3 → 2 → 1 → 0  111  110  100  100  011  010  001	

