AMAN SHARMA

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INDIAN INSTITUTE OF INFORMATION TECHNOLOGY DESIGN & MANUFACTURING (IIITD&M) KANCHEEPURAM, CHENNAI - 600127

EDUCATION

Program	Name of the Institution	CGPA	Year of Completion
B. Tech. Computer Engineering + M. Tech. Computer Engineering	IIITDM Kancheepuram Chennai	9.17	2024
XII	Subodh Public School Jaipur	9	2019
X	Subodh Public School Jaipur	10	2017

SKILLS

- **Computer Engineering Fundamentals, Databases, OOPS**
- **Proficient in C++, Python**
- **Backend Programming in Python: Django and Flask**
- **REST APIs, Django Rest Framework**
- **Data Analysis, Understanding of Machine Learning / Deep Learning concepts**
- **Python ML platforms and libraries: Pandas, Numpy, Scikit-learn, Keras**
- **Computer Architecture**
- **Familiarity with cloud services**

PROJECTS

- **Shelf Reflection (Web App, Python):**

  A platform that allows users to create a personal profile, where they can login and share information about themselves and their reading preferences. Users can also create posts about the books they read, including reviews and recommendations. Backend created with Django and PostgresSQL database (live on Render cloud application) for handling user data and providing services. Django templating and Bootstrap used for frontend. The web app is hosted with Render cloud application. See project

- **Retinal OCT Image Classification Based on Convolutional Neural Networks (Deep Learning, Python):**

  Multi-class classification: AMD, DME, or NO Disease. Used VGG-16 Conv Net with ReLU activation function, softmax at output layer, Dropout and early stopping for regularization, Mini batches of size 16 and adam

optimization. The performance has been evaluated according to different metrics, which are precision, recall, f1-score, accuracy.

- **DNA Sequencing (HPC, C++):**
  Parallelized classification task for DNA Sequencing. Treating DNA Sequence as language break it down to k-mers and then apply count vectorizer (NLP). Perform Bayes' Classification on the feature vectors thus obtained. The classification task is parallelized using OpenMP, MPI and CUDA in C++. See project
- **VLIW Processor (Computer Architecture, Python, Verilog):**
  Designed a VLIW processor using functional units (Carry look ahead adder, Wallace tree multiplier, Double precision floating point adder and multiplier, and logic unit) implemented with Verilog HDL. Verification performed using a compiler written in Python that handles dependency checks, instruction scheduling and parallel dispatch. See project
- **More Projects on Github:** /sage-arts

HANDLES

- **Github:** /sage-arts
- **Leetcode:** /etgulli
- **Codechef:** /gashbell