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## **REPORT ON “Design NOR gate using AND gate”**

**SUBMITTED BY –**

<b>Sr. No.</b>	<b>Name of Student</b>	<b>Roll No.</b>
1	Piyush Sachin Lohar.	33
2	Aditya Vikram Pawal.	31
3	Raj Chandrakant Dewarde.	28
4	Gautam Vishal Chavare.	78

**UNDER THE GUIDANCE OF**

**Ms. S. S. Koli**



**DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING  
SANJAY GHODAWAT INSTITUTE, ATIGRE ACADEMIC  
YEAR: 2025-26**



## **Certificate**

This is to certify that the Micro project work entitled

**“Design NOR gate using AND gate and study the feature of logic family”**

Has been successfully completed by

**In fulfillment for the  
Diploma in Computer Science &Engineering  
Maharashtra State Board of Technical Education**

**During the academic year 2025-26 under the guidance of**

**Ms. S. S. Koli**

**Project Guide**

**Mr. S.V. Chavan**

**H.O.D**

**Dr. V. V. Giri**

**Principal**





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## Abstract

This project demonstrates the implementation of an AND gate using only NOR gates, showcasing the principle of universal gates in digital electronics. Since NOR gates can be combined to realize any logical operation, this design highlights their versatility in logic circuit construction. The project explains how input inversion and logical operations can be achieved with NOR configurations to obtain the functionality of an AND gate. It provides a practical understanding of digital logic design, Boolean algebra, and gate-level realization. The implementation not only emphasizes cost-effective circuit design but also enhances conceptual clarity for students in digital electronics.

### Key Points:

- NOR gate is a universal gate.
- AND gate is realized by interconnecting NOR gates.
- Demonstrates Boolean algebra simplification.
- Helps in understanding practical logic circuit design.
- Useful for low-cost hardware implementation and academic learning.



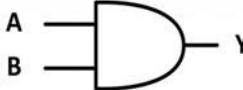
## Introduction

In digital electronics, logic gates are the basic building blocks used to design complex circuits. Among these, the AND gate is widely used for performing logical multiplication of binary inputs. However, using universal gates like NOR and NAND, we can design any other gate or logic function. The NOR gate is called a universal gate because it can implement NOT, OR, AND, and even more complex functions.

This project focuses on designing and implementing an AND gate using only NOR gates. The purpose is to understand gate-level realizations, apply Boolean algebra simplifications, and gain practical experience in logic design. By converting AND logic into a NOR-only configuration, students learn the importance of universality, cost-effectiveness, and flexibility in circuit design.



## AND gate:-

Symbol:	Equation	Truth Table																		
	$Y = A \cdot B$	<table border="1"> <thead> <tr> <th colspan="2">Inputs</th> <th>Output</th> </tr> <tr> <th>A</th> <th>B</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	Inputs		Output	A	B	Y	0	0	0	0	1	0	1	0	0	1	1	1
Inputs		Output																		
A	B	Y																		
0	0	0																		
0	1	0																		
1	0	0																		
1	1	1																		

## Datasheet:

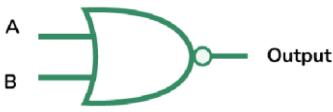
		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	6.5	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current $V_I < 0$		-50	mA
$I_{OK}$	Output clamp current $V_O < 0$		-50	mA
$I_O$	Continuous output current		$\pm 50$	mA
	Continuous current through $V_{CC}$ or GND		$\pm 100$	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>		227	$^{\circ}\text{C}/\text{W}$
$T_{stg}$	Storage temperature range	-65	150	$^{\circ}\text{C}$

## Description:-

- An AND gate is a digital logic gate with two or more inputs and one output that performs logical conjunction.
- The output of an AND gate is true only when all of the inputs are true.
- If one or more of an AND gate's inputs are false, then the output of the AND gate is false.
- The output of an AND gate is only HIGH (1) when all of its inputs are HIGH. If any of the inputs are LOW (0), then the output of the AND gate is also LOW (0).



## NOR gate

Symbol:	Equation	Truth Table															
	$Y = \overline{A+B}$	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>Output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	A	B	Output	0	0	1	1	0	0	0	1	0	1	1	0
A	B	Output															
0	0	1															
1	0	0															
0	1	0															
1	1	0															

## Datasheet:-

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_{IH}$	$V_{CC} = 2\text{ V}$	1.5		V
	$V_{CC} = 3\text{ V}$	2.1		
	$V_{CC} = 5.5\text{ V}$	3.85		
$V_{IL}$	$V_{CC} = 2\text{ V}$	0.5		V
	$V_{CC} = 3\text{ V}$	0.9		
	$V_{CC} = 5.5\text{ V}$	1.65		
$V_I$	Input voltage	0	5.5	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	$V_{CC} = 2\text{ V}$	-50		$\mu\text{A}$
	$V_{CC} = 3.3\text{ V} \pm 0.3$	-4		mA
	$V_{CC} = 5\text{ V} \pm 0.5$	-8		
$I_{OL}$	$V_{CC} = 2\text{ V}$	50		$\mu\text{A}$
	$V_{CC} = 3.3\text{ V} \pm 0.3$	4		mA
	$V_{CC} = 5\text{ V} \pm 0.5$	8		
$\Delta t/\Delta v$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	100		ns/V
	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	20		
$T_A$	Operating free-air temperature	-55	125	$^{\circ}\text{C}$

## Description:-

- ◆ The NOR gate is a combination of the or gate and not gate.
- ◆ A NOR gate is a digital logic gate that performs a logical NOR (NOT-OR) operation on its inputs.
- ◆ It outputs 1 when all inputs are 0; otherwise, it outputs 0.
- ◆ The NOR gate is also known as the Negated OR gate.



## Features of logic Circuits

**Supply voltage requirement:** It is defined as the minimum and maximum voltage required for proper operation of logic circuit.

**Power Dissipation:** This is the power supplied required to operate the gate. It is expressed in milli-watt (mW) and represents actual power dissipated in the gate. It is the number that represents power delivered to gate from the power supply. The total power dissipated in the digital system is sum of power dissipated in each digital IC.

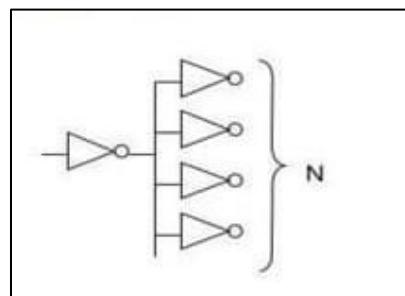
**Maximum clock frequency:** It is defined as the maximum frequency of input clock signal that the logic can process without error.

### Noise Margin:

- i) Noise: It is an unwanted disturbance present in input or output.
- ii) Noise Immunity: It is defined as the ability of logic circuit to tolerate the noise.

A Quantitative measure of noise immunity is called noise margin.

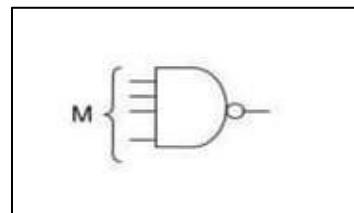
**Fan in:** This is the number of inputs of a logic gate. It is decided by the input current sinking capability of a logic gate.



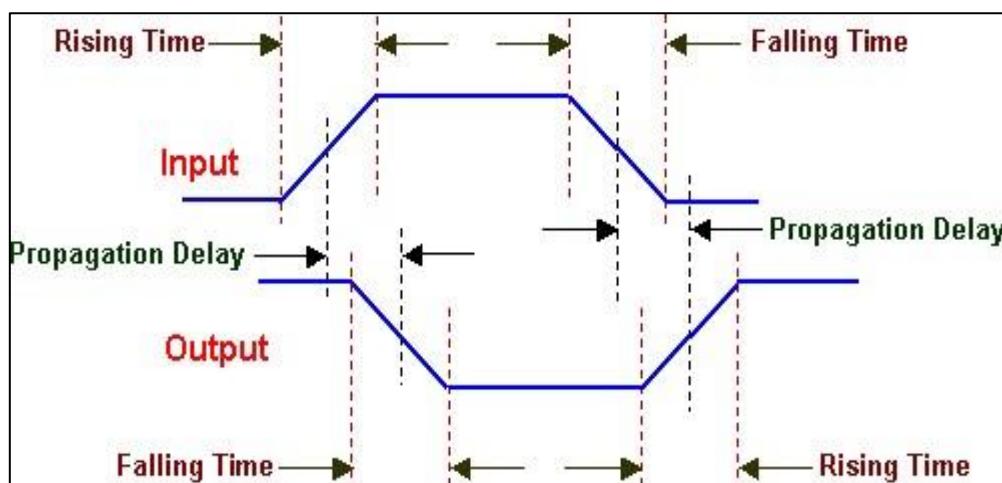
**Fan out:** It specifies the number of standard loads that the output of the gate can drive without affecting its normal operation. A standard load is usually defined as the amount of current needed by an input of another gate in the same family.



Sometimes, the term 'loading' is also used instead of 'fan out'. This term is derived from the fact that the output of the gate can supply a limited amount of current above which it ceases to operate properly and is said to be overloaded. The output of the gate is usually connected to the inputs of similar gates.



**Propagation delay:** The propagation delay is the time delay between the occurrence of change in the logical level at the input and before it is reflected at the output. It is the time delay between the specified voltage points on the input and output waveforms. Propagation delays are separately defined for LOW-to-HIGH and HIGH-to-LOW transitions at the output. In addition, we also define enable and disable time delays that occur during transition between the high-impedance state and defined logic LOW or HIGH states.





## Real-Time Application

Application: Security Access Control System

### Concept:

An AND gate ensures that both conditions must be true to activate an output. When built using NOR gates, it performs the same logic using only one universal gate type — which simplifies hardware design in some cases.

⚙️ Example: Door Lock System

Inputs:

A: Authorized keycard detection

B: Password verification

Output:

Y: Door unlock signal

Logic:

Door opens ( $Y = 1$ ) only when both the keycard ( $A = 1$ ) and password ( $B = 1$ ) are valid.

The AND logic ( $A \cdot B$ ) is created using NOR gates, which are universal and can form any logic function.

🔧 Practical Use:

Used in digital security systems, biometric authentication, and industrial control circuits where only NOR gates are available or preferred.

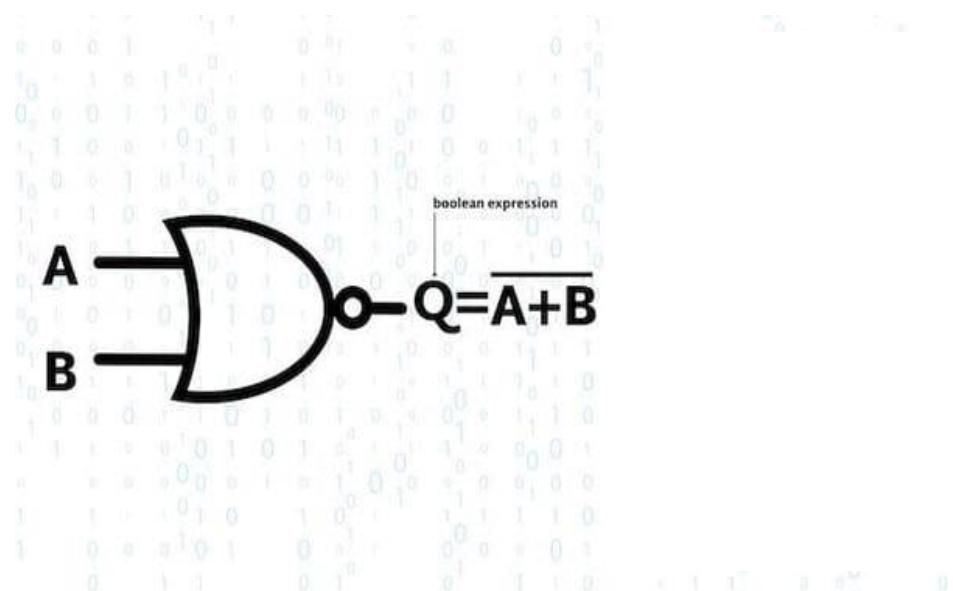


## Images

AND Gate:



NOR Gate:





## Conclusion

This project successfully demonstrates the design and implementation of an AND gate using only NOR gates, proving that the NOR gate is a universal gate. The work highlights the practical use of Boolean algebra and gate-level logic simplification. It also shows that complex digital circuits can be realized from a single type of gate, making designs more flexible, cost-effective, and reliable. Overall, this project enhances understanding of fundamental logic design principles and strengthens the concept of universality in digital electronics.

Furthermore, this work illustrates how real-time hardware limitations, such as restricted gate availability, can be overcome through logical transformations and proper design strategies. The exercise of building an AND gate from NOR gates provided valuable insights into digital logic, circuit minimization, and the foundational role of universal gates in modern electronics. Overall, this project demonstrates both the theoretical and practical significance of gate universality and strengthens the fundamental knowledge required for advanced studies in digital systems, computer architecture, and integrated circuit design.



## References

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- <https://www.tme.com/in/en/news/library-articles/page/51508/logic-gate-symbol-types-and-features/>