Mixer Notes

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1 High Level Design

For the mixer, we need:

- a large bandwidth (at least 200 MHz)
- low noise
- can be driven by a single ended source (for simplicity, I want to stick with single ended operation throughout the signal chain).

The LT5560 works for this application. It has:

- a large bandwidth (4 GHz)
- low noise (9.3 dB @ 900 MHz)
- can be driven by a single ended source

Design Notes:

- It seems like Automatic Frequency Control (AFC) is no longer used since crystals provide a very stable frequency, as seen on both wikipedia and this link: https://www.quora.com/What-is-frequency-drift-in-an-FM-receiver. Most LOs today use digitally synthesized signals connected to crystals. These are known as "frequency synthesizers" - they are able to generate many different stable frequencies using a single reference frequency from a crystal.
- PLLs also don't drift because any error is compensated for in the PLL.
- It seems like we can just use a PLL with a VCO built in. This seems like a good option: https://www.digikey.com/en/products/detail/analog-devices-inc/ADF4360-9BCPZRL7/2043337
- Actually, it seems like this is an integer-N PLL, but we need a fractional N PLL.
- Even if we find another PLL with an integrated VCO, it seems we'll still need an external loop filter, so might as well stick with the original with an external VCO

2 Detailed Design

- This seems like a really good PLL: https://www.digikey.com/en/products/detail/skyworks-solutions-inc/SI5351A-B-GTR/4069612. Unlike the previous one, it uses a crystal, so the frequency error is close to 0.
- However, it seems like it can only divide by multiples of 2, so it wouldn't work for our purposes since we need to change the LO frequency from 77 MHz to 98 MHz.
- This might be a better option: https://www.digikey.com/en/products/detail/analog-devices-inc/ADF4169CCPZ/5441070
- In a high-side mixer, the FM modulated signal will essentially be inverted. This is because $f_{IF} = \mid f_{RF} - f_{LO} \mid$, so if f_{RF} increases then f_{RF} becomes closer to f_{LO}, so f_{IF} decreases. This doesn't really matter (not completely sure about this), as long as we're aware that it's mirrored. https://www.edaboard.com/threads/high-side-injection-and-low-side-injection-in-mixer.125131/
- Let's use low-side mixing so that the signal is not inverted. This means that fLO = fRF - fIF = fRF - 10.7MHz.
- Does a clock generator work (square wave) or do I need a sine wave for the LO?
- There seems to be a variety of different opinions online. https://www.reddit.com/r/rfelectronics/comments/12wqxvw/rf_mixer_square_wave_lo/
- It seems like a square wave is practically hard to produce, but could be beneficial. Some people are also saying that the higher order harmonics could be aliased down to the IF, others are saying that a square wave is the ideal mixer input. For now, I'm going to go with a square wave.
- If we're using the ADF4169CCPZ above, we'll need to write to the registers to control the input, which means we'll need a microcontroller to do that.

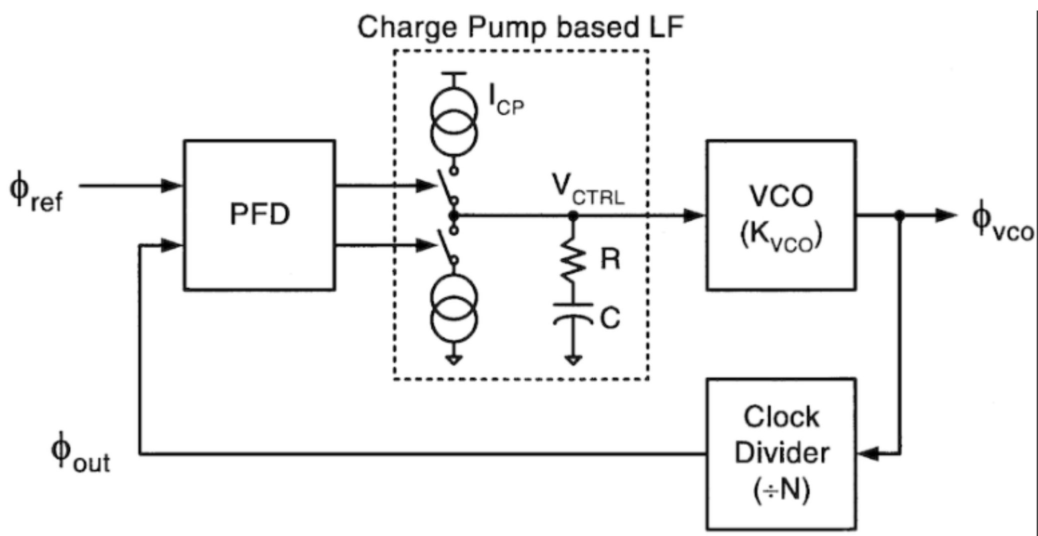
- It doesn't explicitly mention it, but looks like it uses I2C since it has a clock and data line. If not, we can just manually code the protocol instead of using an I2C library.

- We can use the same 0.1 uF cap we used as a blocking cap for the HF amp as a decoupling cap here since it has a very high self-resonant frequency of 6 GHz.

- The INT multiplier for the reference frequency is from 23 to 4095. If we want a LO signal of 77 MHz to 97 MHz, then we can potentially use a reference frequency around 1 MHz.

- Let's use this CMOS crystal oscillator: https://www.digikey.com/en/products/detail/analog-devices-inc-maxim-integrated/MAX7375AXR105-T/1520107

3 Understanding PLLs



- Assuming that the input is a square wave and the PFD is a digital circuit, a simple PFD can be implemented using an XOR gate that is high for the portion of time when the reference signal and the output signal are different. If the two signals are 1 degree out of phase, this will result in a pulse with a width of 1/180 the period of the signals.

- The charge pump performs integration, which can correct for both phase and freq. errors, since freq. is the derivative of phase.

- The charge pump for the ADF4169 outputs a current, which is converted to a voltage by the loop filter. https://electronics.stackexchange.com/questions/301056 filter-of-pll

- Since a LPF also performs integration, a charge pump can technically replace a LPF with a capacitor.

- This seems like a good VCO: `https://www.digikey.com/en/products/detail/analog-devices-inc-maxim-integrated/MAX2623EUA-T/1938007`

4 Loop Filter Design

- Following this link, second order loop filter design: `https://www.renesas.cn/cn/zh/document/apn/pll-loop-filter-design-and-fine-tuning`

- Desired loop bandwidth must satisfy Fpd/Fc ¿¿ 20, where Fpd is the freq. to the phase detector = the frequency of our ref signal, which is 1 MHz. This means that Fc ¡¡ 1 MHz/20 = 50 kHz. Let's set the loop bandwidth to 10 kHz.

- Rs = $\frac{2*pi*f_c*N}{/}I_{cp} * K_{Vco}$. N varies between 77 and 97 -¿ Let's choose 87 as the nominal value. According to the datasheet, it is best to start with 2.5 mA for the charge pump current. The VCO gain is given by 6.2 MHz/V. Therefore, $Rs = \frac{2*3.1415*10000*87}{2.5*10^-3*6.2*10^6}$ = 352.658709677 ohms.

- Cs = $\frac{alpha}{2*pi*f_c*R_c}$, where alpha is the ratio of the loop bandwidth to the zero frequency. It's recommended that alpha ¿ 3, so let's do alpha = 5. That gives $Cs = \frac{5}{2*3.1415*10000*352.6587}$ = 225.656757 nF.

- Cp = $\frac{Cs}{alpha*Beta}$, where beta is the ratio between pole freq. and bandwidth. It's recommended that beta ¿ 3, so let's choose beta = 5. That gives $Cp = \frac{225.656757*10^-9}{5*5}$ = 9.02627028 nF.

- The maximum phase margin is given by $arctan(\frac{b-1}{2*sqrt(b)})$, where $b = 1 + \frac{Cs}{Cp}$. In our case, $b = 1 + \frac{225.656757}{9.02627028} = 26$, so the phase margin = 67.80839366845 degrees $>$ 50 degrees $->$ the PLL is stable.

5 Mixer Input Impedance Matching

- For the mixer, the input impedance varies between approximately 28.5 + j to 28.5 + 1.4j for the frequencies of 88 MHz to 108 MHz based on this table.

- Since we're operating at a nominal frequency of 98 MHz, the input impedance = 28.5 + 1.12j. $Q = sqrt(\frac{Rs}{Rl} - 1) = sqrt(\frac{50}{28.5} - 1) = 0.86855395049$. $Xc = \frac{Rs}{Q} = \frac{50}{0.86855395049} = 57.5669478814$ ohms $= \frac{1}{2*pi*98M*C} => C = \frac{1}{2*pi*98M*57.5669478814} = 28.211154$ pF. $Xl = \frac{Rl}{Q} = \frac{28.5}{0.86855395049} = 32.8131602924$ ohms. $X_{ext} = X_l - X_int = 32.8131602924 - 1.12 = \frac{31.6931602924}{2} = 15.8465801462$ ohms per inductor $= 2*pi*98M*Lext => Lext = 25.7353221$nH.

nected from pins 3 and 4 to ground.

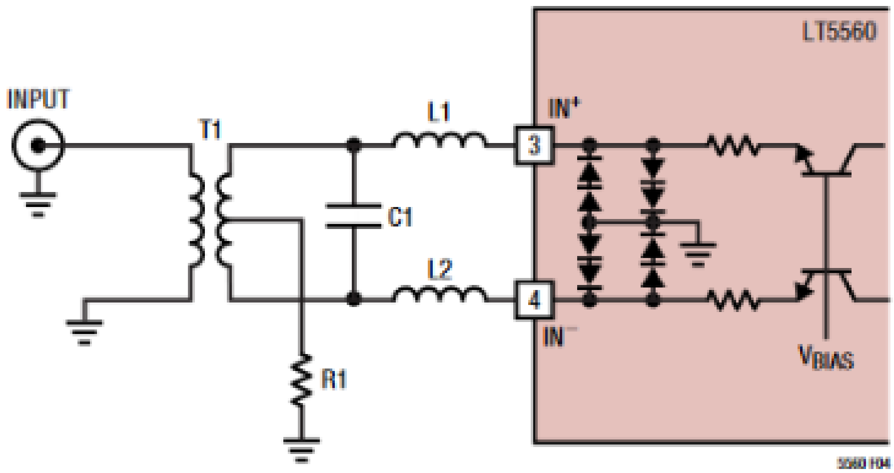


Figure 4. Input Port with Lowpass External Matching Topology

The lowpass impedance matching topology shown may be used to transform the differential input impedance at pins 3 and 4 to match that of the signal source. The differential input impedances for several frequencies are listed in Table 2.

Table 2. Input Signal Port Differential Impedance

FREQUENCY (MHz)	INPUT IMPEDANCE (Ω)	REFLECTION COEFFICIENT (Z_0 = 50Ω)	
		MAG	ANGLE (DEG.)
70	28.5 + j0.8	0.274	177
140	28.5 + j1.6	0.274	174
240	28.6 + j2.7	0.275	171
360	28.6 + j4.0	0.276	167
450	28.6 + j4.9	0.278	163
750	28.8 + j8.2	0.287	153
900	28.8 + j9.8	0.294	148
1500	29.1 + j16.3	0.328	138
1900	29.4 + j20.8	0.357	120
2150	29.6 + j23.6	0.376	114
2450	29.9 + j27.0	0.399	107
3600	31.7 + j42.1	0.499	86.2