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Total No. of Questions : 5 Total No. of Printed Pages : 2

EKS-174

B.E. V Sem. (CGPA) Electronics and Communication Engg. Examination 2017

COMPUTER ENGINEERING

Paper : EL-505

Time Allowed : Three Hours

Maximum Marks : 60

Note: Attempt all questions. All questions carry equal marks.

Q.1. a) What is instruction fetch, decoding and execution?
b) Explain various addressing modes.

OR

a) Explain the bus architecture of computer system.
b) What are instruction set design issues? Explain.

Q.2. a) Explain the control unit organisation.
b) What is Micro-instruction encoding?

OR

a) Explain the micro-programmed control organisation.
b) Differentiate between horizontal and vertical micro instructing.

Q.3. a) Define the essential differences between the following types of OS:
i) Batch
ii) Interactive
iii) Time-sharing
iv) Real-time

b) What do you understand by I/O bound jobs and CPU bound jobs?

OR

a) What types of services are provided by an operating system?
b) What is meant by non-preemptive scheduling? What are the factors that influence the selection of a scheduling technique?

Q.4. a) What do you understand by the following:
i) Process
ii) Process state
iii) Process control block
b) What is a Deadlock? How is such problem solved?

OR

a) Explain the dining philosopher problem with its solution.
b) Explain semaphores.

Q.5. a) Differentiate between logical and physical address space.
b) Explain contiguous and non-contiguous memory allocation.

OR

a) What is understood by page missing or segment missing fault?
b) What is best fit strategy? What is dynamic selection?

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Total No. of Questions : 5] [Total No. of Printed Pages : 3

EG-184

B.E. V Semester (CGPA) Elect. & Commun. Engg. Examination 2018

COMPUTER ENGINEERING

Paper - EL-505

Time Allowed : Three Hours] *[Maximum Marks : 60*

Note : Attempt all questions. All questions carry equal marks.

Q.1. a) Draw and explain flow chart of instruction cycle.

b) Draw the hardware implementation of the following Register transfer statement.

i) $x\bar{y} : A \leftarrow B$

ii) $xy + z : C \leftarrow D$

OR

c) Explain different types of instruction format.

d) What is bus organized computer? Draw multiple bus structure.

Q.2. a) Explain microinstruction format.

b) Discuss features of control memory.

OR

c) Draw and explain hardwired control unit.

d) Define horizontal and vertical microinstruction.

Q.3. a) What is meant by multiprocessor system?

b) What is an operating system.

OR

Describe I/O device organization.

Q.4. What is Deadlock? Explain dead lock prevention and dead lock Avoidance with the help of example.

OR

a) Draw and explain precedence graph.

b) Describe critical section problem.

Q.5. a) What is memory allocation? Explain the difference between contiguous and non contiguous allocation.

b) Discuss demand paging with the help of example.

OR

Explain the following terms (any three)

i) Cache memory

ii) Paging

iii) Thrashing

iv) Swapping

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Total No. of Questions : 6 Total No. of Printed Pages : 2

EC-158

B.E. V Sem. (CGPA) CSE Exam.-2012-13

COMPUTER ARCHITECTURE

Paper : CS-505

Time Allowed : Three Hours

Maximum Marks : 60

Note: Attempt all questions.

Q.1. Explain the following terms: 10

i) Cache memory.

ii) RISC.

iii) RAM.

iv) Multiprocessor.

v) Control memory.

Q.2. a) What is micro-operation 5

b) Define memory address register. 5

OR

Explain register transfer language. 10

P.T.O.

Q.3. Explain various branching technique used in microprommed control unit. 10

OR

a) What is microprogram sequencer? 5

b) What are the design considerations for microprom sequencer. 5

Q.4. Draw and explain Arithmetic logic unit design. 10

OR

Explain Multiplication and Division Algorithm. 10

Q.5. Define Data Communication. Explain the component of data communication. 10

OR

What is interrupt? Explain with it various types. 10

Q.6. What is memory? Explain different memory management technique. 10

OR

What are the memory performance parameters explain. 10

Total No. of Questions :6 Total No. of Printed Pages : 2

EH-65

B.E. V Sem (CGPA) CSE Exam. 2014

COMPUTER ARCHITECTURE

Paper : CS-505

Time Allowed : Three Hours

Maximum Marks : 60

Note:- Attempt all questions. All question carry equal marks.
10 marks each

Q.1. Explain the following terms:
- (i) ROM
- (ii) Address bus
- (iii) Micro-operation
- (iv) PROM
- (v) DMA controller

Q.2. Describe addressing mode with its types.

OR

Define instruction set. Explain design issue of instruction set.

Q.3. What do you understand by micro instruction? Explain with an example.

OR

Explain horizontal and vertical micro instruction in detail.

Q.4. Describe pipelining with its type.

OR

What is RISC? Explain the difference between RISC and CISC architecture.

Q.5. Write detail note on input-output organization with suitable diagram.

OR

What is I/O processor? Explain the basic features of I/O processor.

Q.6. Draw and explain structure of multi processor.

OR

What is associative memory? Explain memory hierarchy with suitable diagram.

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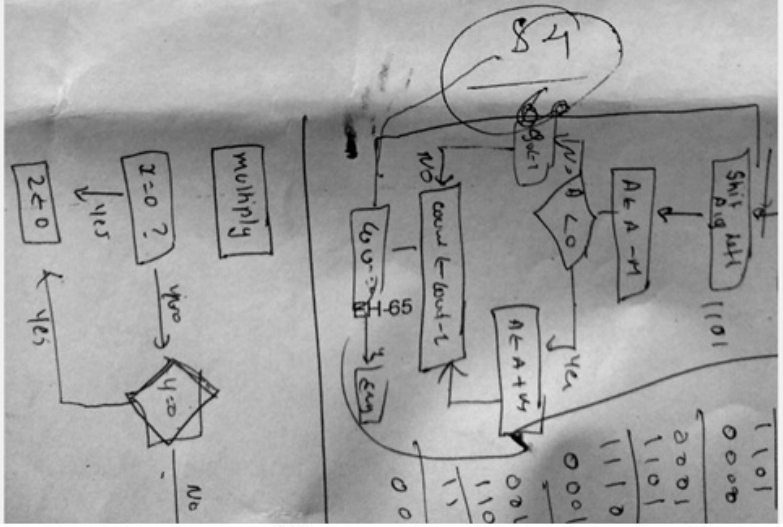

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EI-68

B.E. (Vth Sem.) (CGPA) CSE Examination-2015

COMPUTER ARCHITECTURE

Paper : CS-505

Time Allowed : Three Hours
Maximum Marks : 60

Note : Attempt one question from each units.
Each units carry equal marks.

Q.I (a) What are the different registers in CPU ? What are its functions ? 6

(b) What are the different types of buses ? Explain the differences between address bus and the data bus ? 6

or

(a) What are the different addressing modes ? Explain each one of them. 6

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(3)

Unit-IV

Q.IV (a) What is a program interrupt ? Explain the program flow of control without and with interrupts with the help of diagram. 6

(b) What is the role of a priority interrupt ? Explain. 6

or

(a) Draw block diagram of computer with I/O processor and explain how data transfer is achieved between them. 6

(b) Write a brief notes on different modes of data communications. 6

Unit-V

Q.V (a) What is meant by inclusion, coherence and locality in a memory hierarchy ? 6

(b) What is memory interleaving ? How is it different from cache memory ? 6

or

(a) How memory decoder is used to connect CPU with RAM ? 6

(b) Explain direct mapping and set associative mapping in associative memory 6

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(d) Draw the generic instruction format and explain each field. 6

Unit-II

Q.II Explain the terms— 12

(a) Micro operation

(b) Microinstructions

(c) Control memory

or

(a) What an shift micro operations ? Explain in details. 6

(b) Write a brief notes on microinstruction formats. 6

Unit-III

Q.III (a) How is multiplication of floating point numbers achieved ? Explain using flow chart. 6

(b) What are the factors limiting the degree of super scalar design ? 6

or

(a) Discuss the various performance issues in pipelining. 6

(d) What is the purpose of prefetch buffers in instruction pipelining. 6

Total No. of Questions : 5 Total No. of Printed Pages : 3

EK-213

B.E. (Vth Sem.) (CGPA) C.S.E. Exam.-2016

COMPUTER ARCHITECTURE

Paper - CS-505

Time Allowed : Three Hours
Maximum Marks : 60

Note : Attempt all questions.
All questions carry equal marks.

Unit-I

Q.I (a) What are the different addressing modes ? Explain each one of them. 6

(b) Explain architecture of computer organization with neat & clean diagram. 6

or

(a) Differentiate memory address register and data register. Also explain program counter briefly.

(b) Explain instruction set design issue in detail.

Unit-II

Q.II (a) Write a brief notes on micro-instruction formata. 6

(b) Explain micro program sequencer and control memory in detail. 6

or

(a) Differentiate hardwired control and micro programmed control organization briefly.

(b) What is instruction sequencing and instruction interpretation.

Unit-III

Q.III (a) Differentiate RISC and CISC architecture. 6

(b) Explain branch handling techniques. 6

or

(a) Describe Instruction Pipelining briefly.

(b) Discuss the various performance issues in pipelining.

Unit-IV

Q.IV (a) Explain I/O interfacing standards. 6

(b) What is DMA ? Explain with diagram. 6

Contd. .....

or

(a) What is data communication ? Describe the process of sender to receiver.

(b) Differentiate program interrupt and priority interrupt briefly.

Unit-V

Q.V (a) What is memory interleaving ? How is it different from cache memory ? 6

(b) Explain memory allocation and management policies. 6

or

(a) Explain basic concepts of multiprocessing. Also describe multiprogramming.

(b) Differentiate virtual and associative memory briefly.

Total No. of Questions : 5 Total No. of Printed Pages : 2

EKS-213

B.E. V Sem. (CGPA) CSE Exam. 2017

COMPUTER ARCHITECTURE

Paper : CS-505

Time Allowed : Three Hours

Maximum Marks : 60

Note: Attempt all questions.

Unit - I

Q.1. a) What are the different types of buses? Explain the differences between address bus and the data bus. 6

b) Explain program counter and accumulator. 6

OR

a) Explain instructions Fetching, Decoding and Execution. 6

b) What are the different registers in CPU? What are its functions? 6

Unit - II

Q.2. a) Write a brief notes on microinstruction formats. 6

b) Explain microinstruction encoding briefly. 6

OR

a) Explain control memory and instruction interpretation. 6

b) What are shift micro operations? Explain in detail. 6

Unit - III

Q.3. a) Explain addition of floating point numbers using flow chart. 6

b) What is the purpose of prefetch buffers in instruction pipelining? 6

OR

a) Describe division algorithm of floating point numbers. 6

b) Discuss the various performance issues in pipelining. 6

Unit - IV

Q.4. a) What is input-output addressing? 6

b) What is an program interrupt? Differentiate it with priority interrupt. 6

OR

a) Write a brief notes on different modes of data communications. 6

b) Draw block diagram of computer with I/O processor and explain how data transfer is achieved between them. 6

Unit - V

Q.5. a) Explain direct mapping and set associative mapping in associative memory. 6

b) Explain locality of reference in memory Hierarchy. 6

OR

Explain : 12

a) Memory Hierarchy

b) RAM and ROM

c) Virtual memory

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