**Lab 4- Hierarchy Design**

* **64 x 8-bit Static RAM (sixtyFour\_by\_four\_SRAM)**
  + **64 x 4-bit Static RAM (sixtyFour\_by\_four\_SRAM)**
    - **([1])** 3-to-8 decoder with output enable (provided) (three\_to\_eight\_decoder)
    - 8 x 4-bit Static RAM (provided) (eight\_by\_four\_sram)
      * 3-to-8 decoder with output enable (provided) (three\_to\_eight\_decoder)
      * n-bit tri-state buffer (lab3) (nbit\_tri\_buff.vhd)
        + Tri-state buffer (lab3) (tri\_buff.vhd)
      * **m x n-bit Static RAM cell array (m\_by\_n\_sram\_array)**
        + **Static RAM Cell (staticRAM\_cell.vhd)**

**D-latch (dLatch.vhd)**

Not gate (lab1) (Inverter\_VHDL.vhd)

2- input And (lab1) (TwoInputAND\_VHDL.vhd)

**2-input NOR (TwoInputNOR\_VHDL.vhd)**

Tri-state buffer (lab2) (tri\_buff.vhd)

2- input And (lab1) (TwoInputAND\_VHDL.vhd)

* **([2])8 x n-bit Register File (eight\_by\_nbit\_regFile.vhd**
  + **n-bit RFC register (nbit\_RFC\_reg.vhd)**
    - **Register File Cell (RFC) (reg\_fileCell.vhd)**
      * 2-input mux (lab1) (TwoInputMultiplexor\_VHDL.vhd)
      * D flip-flop (lab3) (dFlipFlop.vhd)
      * Tri-state buffer (lab3) (tri\_buff.vhd)
* **([4)] TDM (time division multiplex) display circuit (TDM\_dis.vhd)**
  + T flip-flop (provided lab3) (T\_flipflop.vhd)
  + N-bit tristate buffer (lab3) (nbit\_tri\_buff.vhd)
    - Tri-state buffer (lab3) (tri\_buff.vhd)
  + **([3]) 16 x 7-bit seven-segment decoder ROM (sixteen\_by\_sevenbit \_sevSegDis\_decROM)**